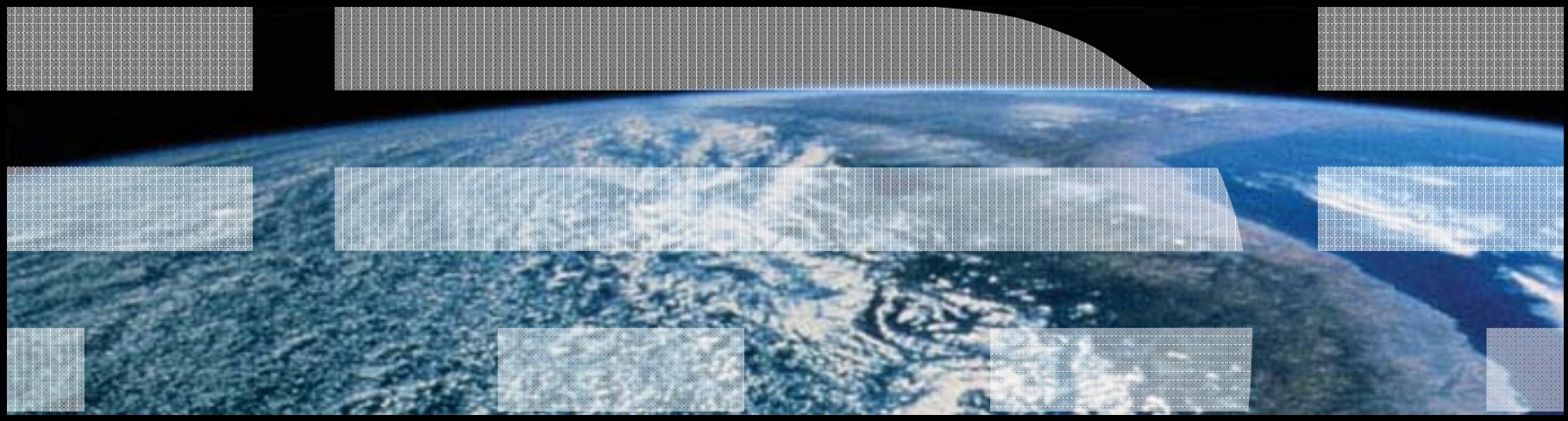

Evolution and Expansion of SOI in VLSI Technologies: Planar to 3D

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Evolution and Expansion of SOI in VLSI Technologies: Planar to 3D

I. **SOI History and Advantages**
   - High Performance Logic Applications
   - Embedded Memories
   - Analog Mixed-Signal Applications

II. **Fully Depleted Devices**
   - Fundamentals
   - FDSOI
   - FinFETs

III. **Business Considerations**

The Marketplace is Expanding

250nm 180nm 130nm 90nm 65nm 45nm 32nm 22nm 14nm

IBM High-End Servers →

Desktop Class Processors & Printers →

Games →

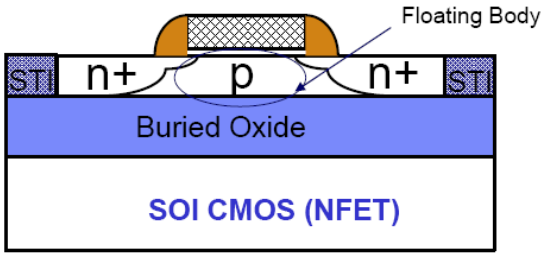
Communications & Storage →

Other Consumer →

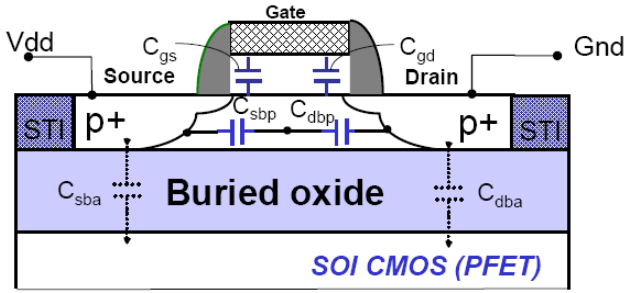
SOI can help take solutions well into the future

SOI Value Adders

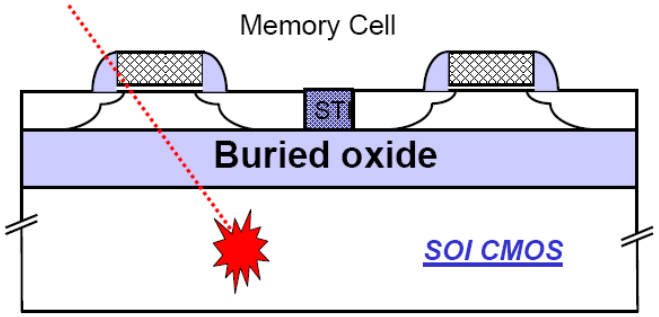
- Superior Isolation
  - **No Well Taps required**
  - **Smaller circuit foot-print**
  - **Latch-up free operation**



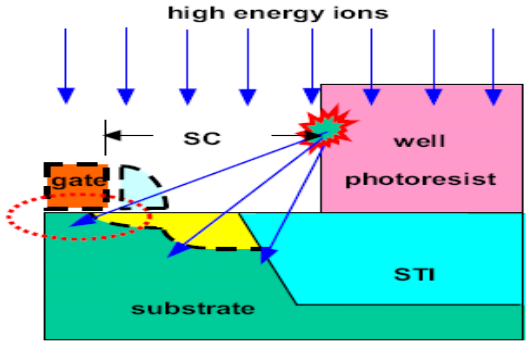
- High Speed Switching
  - **2X lower junction perimeter capacitance**
  - **Improved Short-Channel Effects**



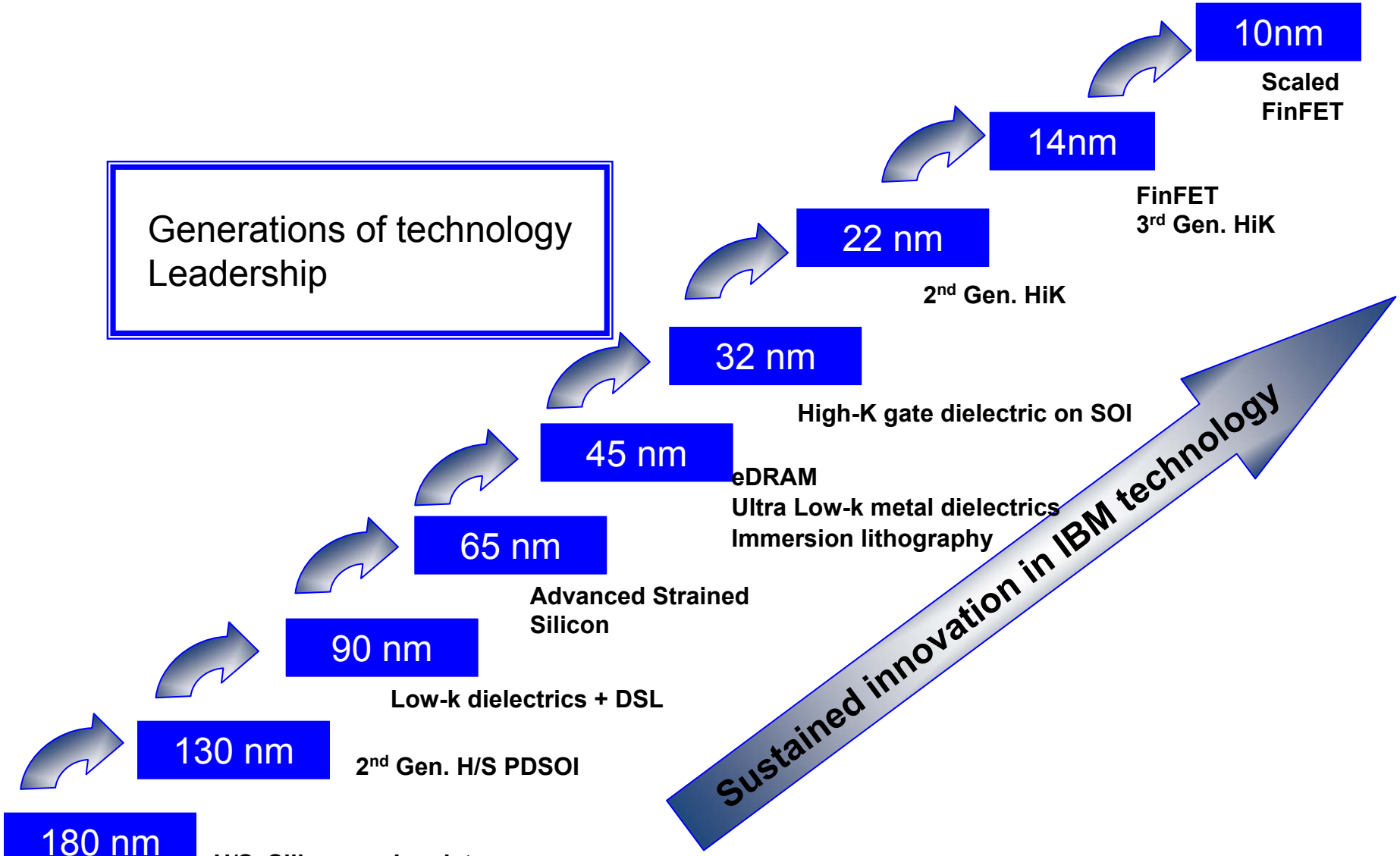
- Less susceptibility to soft errors
  - **SER reduced by 5-7X**
  - **Low power high reliability**



- Reduced Variation within Die
  - **Short-channel Vt roll-off suppression**
  - **Less variation in Vt vs Lgate.**
  - **No Well-Proximity Effects (no deep wells in SOI)**



IBM SOI Technology Roadmap



SOI-enabled Revolution in Computing Systems

Watson meets Jeopardy!

Beats two human competitors on the popular U.S. quiz show "Jeopardy!" in a three-day showdown .

What's in Watson?

Watson is powered by 10 racks of IBM POWER 750 systems

Processor Based on **45 nm SOI Technology with embedded DRAM (eDRAM) memory**

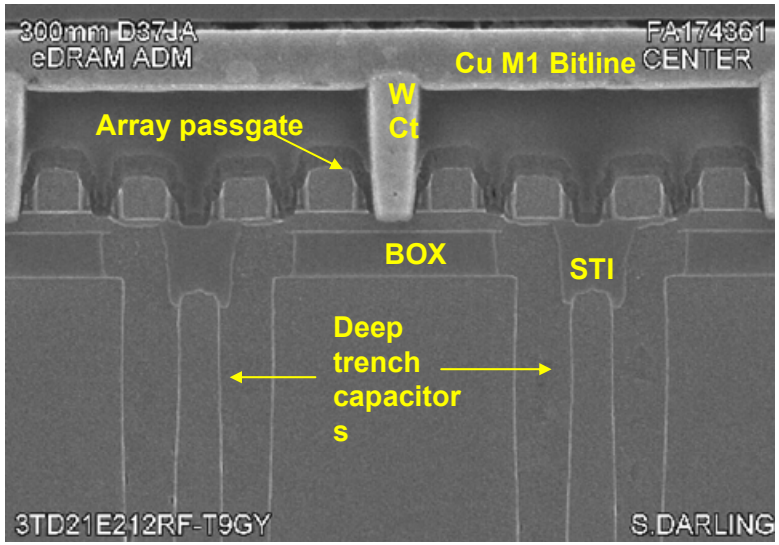
Watson can operate at 80 teraflops per second – 80 trillion operations per second

IBM, Nuance to Tune Watson for Use in Health Care & Other Applications

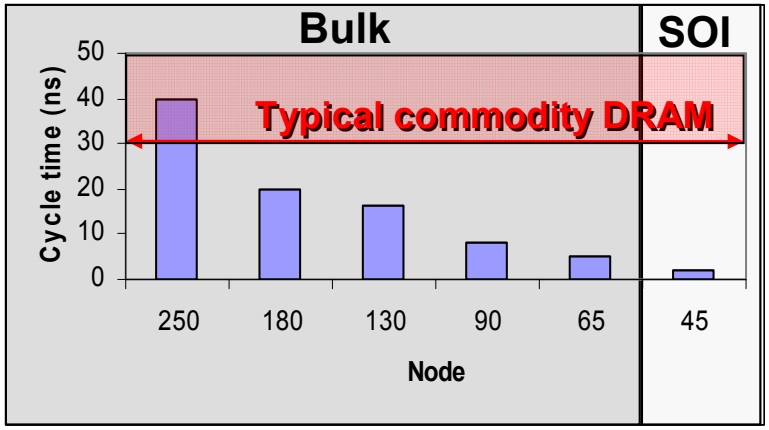
Integrating DRAM and Logic

Innovations to Obtain High Performance Systems

- **Technology:**
  - Use SOI buried oxide to simplify process & reduce parasitics
  - Scale the pass transistor for higher performance



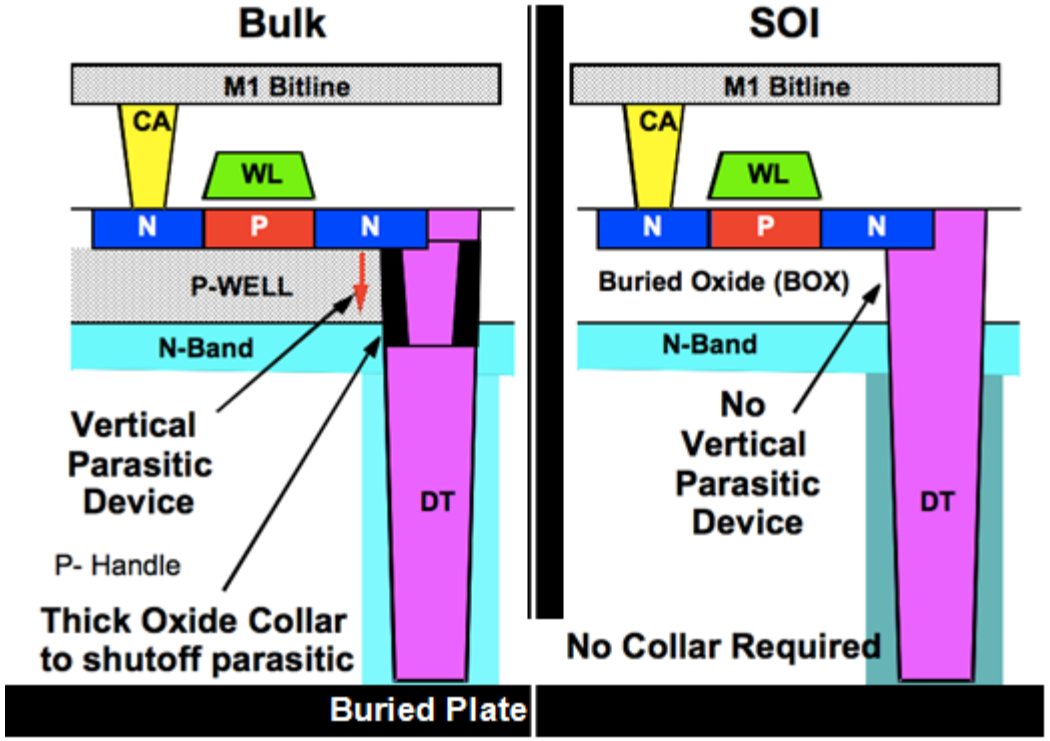
- **Design:**
  - Address retention through concurrent refresh
  - Innovative direct sense architecture for performance



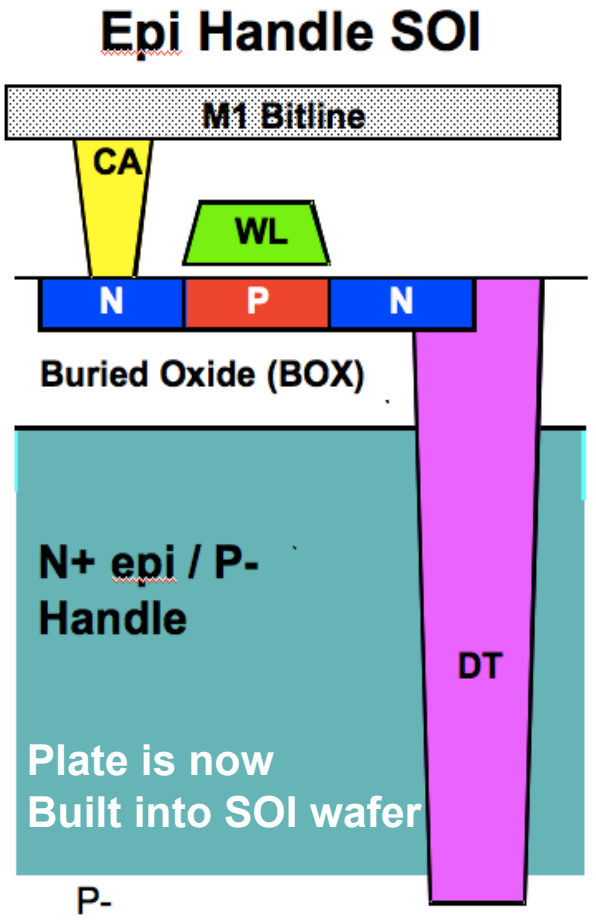
How SOI Facilitates eDRAM

Process Simplification: ~10-15% Adder

Collar process elimination

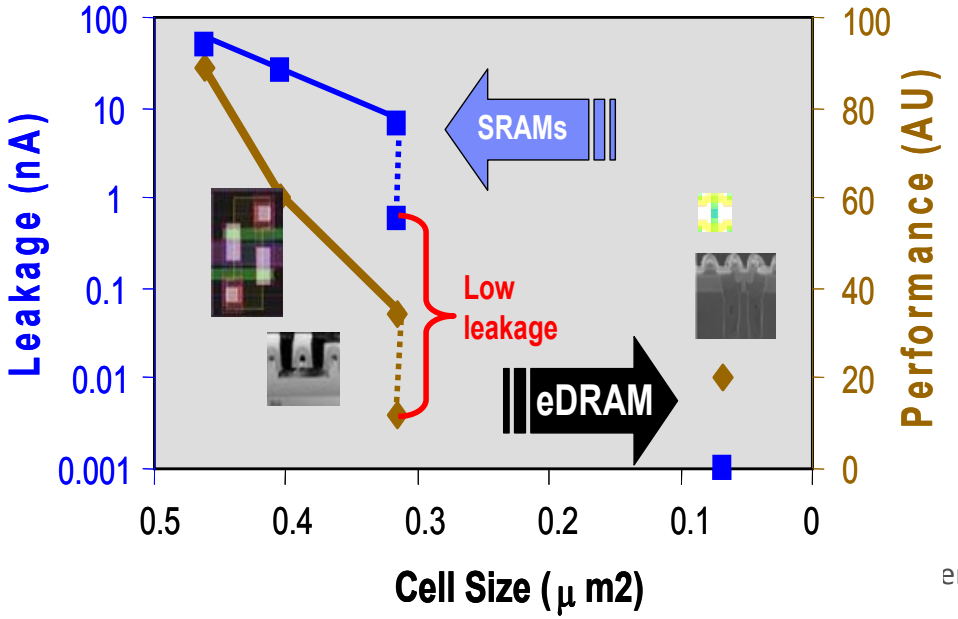


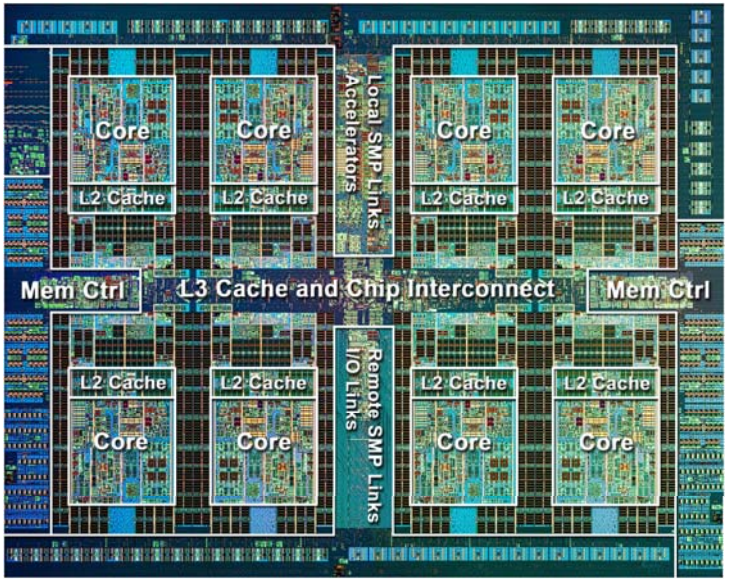
Buried Plate process elimination



Integrated Embedded Memory Solutions

- Memory is 50-70% of the die – key to optimizing performance
- High Performance eDRAM delivers 3X more memory at same die size & power
  - 3X density benefit vs SRAM
  - > 5X standby power benefit
  - > 1000X SER benefit
- Compact decoupling cap for noise reduction and I/O is a great bonus!



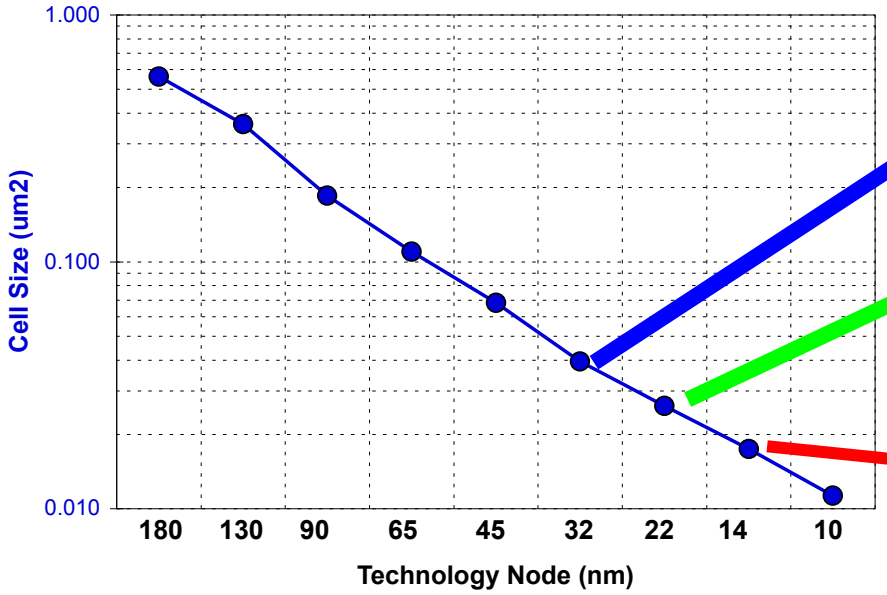


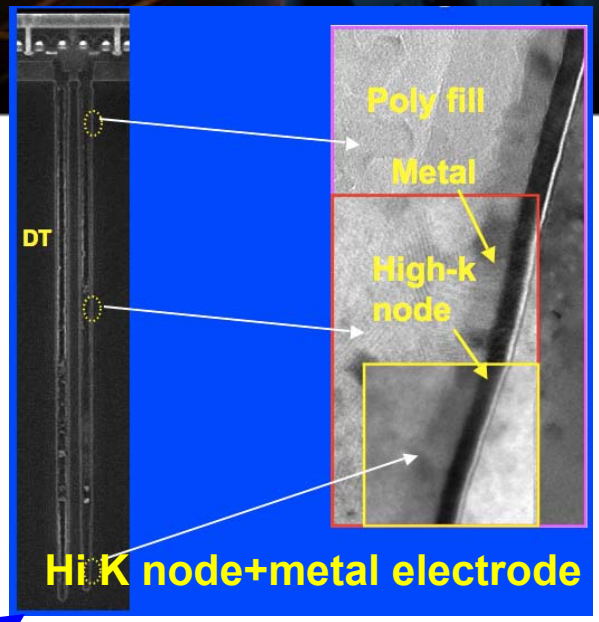
Power 7+ Process Chip

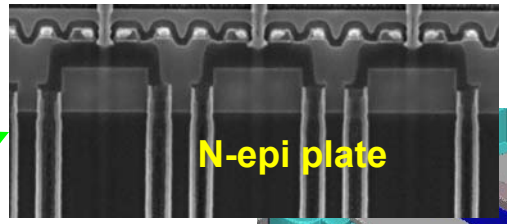
- 567mm2 32nm SOI eDRAM technology
- Eight processor cores
- 80MB on chip eDRAM shared L3
- Equivalent function of 5.4B transistors due to eDRAM efficiency

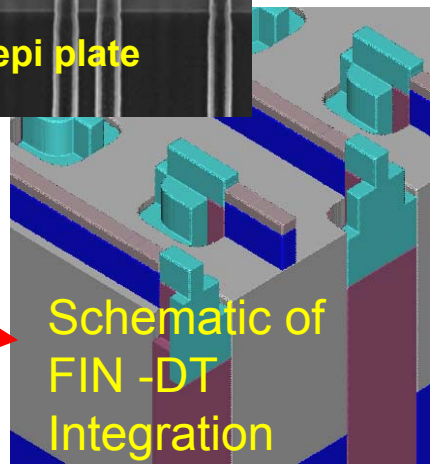
eDRAM Scalability

- eDRAM continues to scale with Logic
- Innovations enabling continued scaling include:
  - High-k Trench capacitor
  - N-epi plate
  - FinFET transfer device
- Scaling increases leverage over SRAM
  - Trend expected to continue to foreseeable future









More than Moore PDSOI

- **SOI is a Value-Add to mature CMOS base Technologies**
  - **Integration of wide variety of applications readily enabled**
    - **High-Voltage: (dielectric isolation eliminates latch-up and leakage)**
    - **High performance analog: (Complementary Bipolar with low Ccs and dielectric isolation)**
    - **RF – intrinsically low isolation capacitances and Low harmonic distortion with appropriate substrate design/engineering**
    - **High reliability applications (greatly reduced soft error rates)**
  - **Superior Isolation**
    - **High resistivity substrates**
      - Enables high Q passives with low loss
      - Low Harmonic distortion from coupling between adjacent devices
      - Reduced coupling from substrate noise
    - **Very High-temperature Operation**
      - No long-range carrier collection to swamp devices with thermally-generated leakages
      - No Latch-up concerns
    - **Easy support for Positive AND Negative Voltages on die**

RF SOI for Smartphone Applications

IBM technologies

Power control
RF CMOS

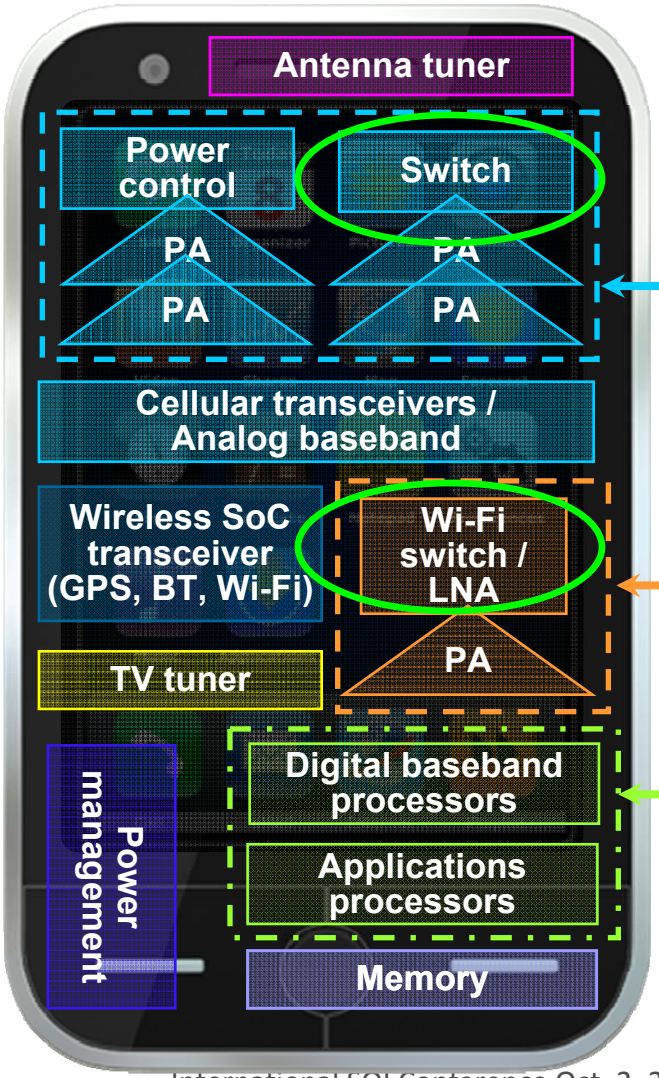
Cellular power amps
RF SOI, SiGe, RF CMOS*

Cellular transceivers
RF CMOS, SiGe

Wireless SoC transceiver (GPS, Bluetooth, Wi-Fi)
RF CMOS, CMOS

TV tuner
SiGe, RF CMOS

Power management
HV CMOS



Antenna tuners
RF SOI, RF MEMS*

Single-pole/multi-throw switch
*RF SOI**

Cellular front-end module integration opportunities
RF SOI

Wi-Fi RF switch, LNA
*RF SOI**

Wi-Fi front-end module integration opportunities
SiGe

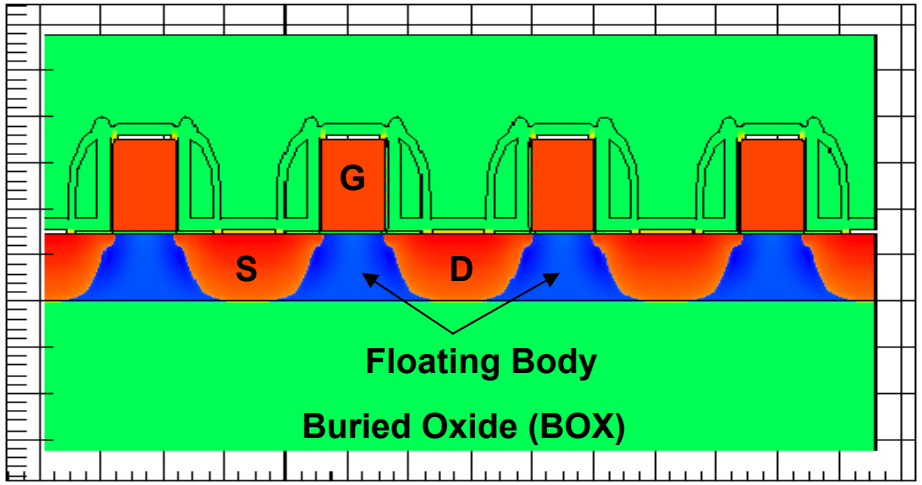
Wi-Fi power amps
SiGe

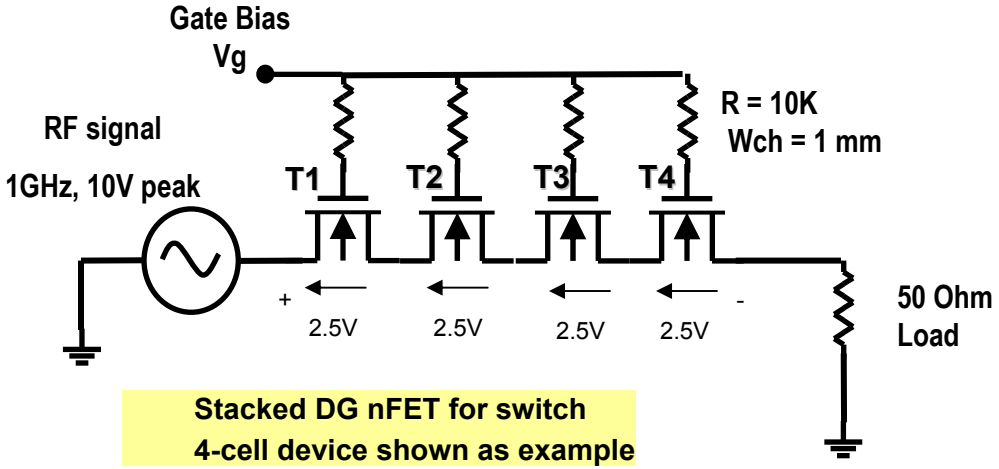
Processor integration opportunities

Application processors
Technology Development Alliance/ Common Platform technology

IBM CSOI7RF Technology for Switches

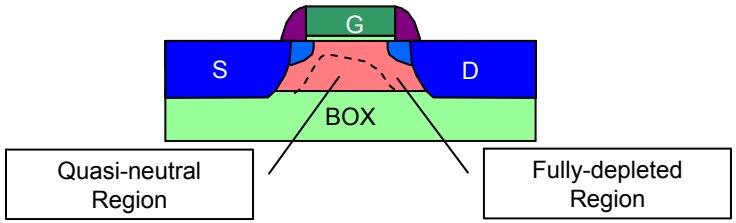
- Leverage IBM's proven expertise in SOI of 6 generations (180-32nm)
- Based on 180-nm Lithography
  - Combination of SOI server technology and CMRF7SF BEOL
- Custom SOI wafer with high resistivity substrate and thick BOX
  - High switch isolation
- Technology Features
  - 2.5V (std) and 1.5V (opt) FETs
  - MIMcap and High-Value serpentine resistor
  - SOI PSP models for accurate analog modeling
  - ESD protection diodes





Stacked DG nFET for switch
4-cell device shown as example

Partially Depleted SOI



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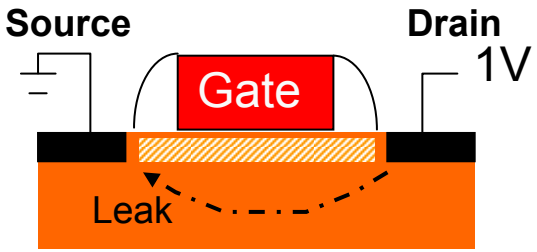
   - FDSOI
   - FinFETs

III. **Business Considerations**

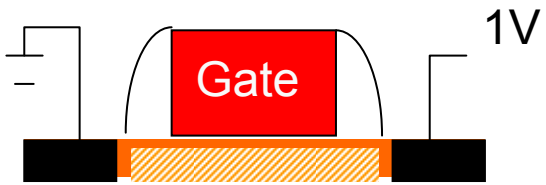
Fully Depleted Device Fundamentals



PDSOI

Gate controls this.

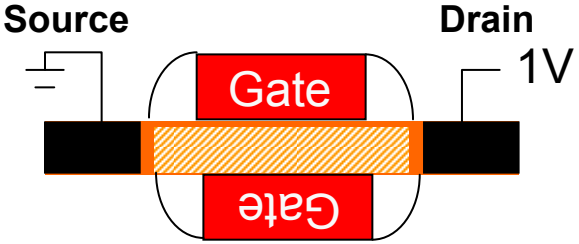
Gate can not control below that. So current can leak through there.



FDSOI

Gate controls this.

No leakage path.



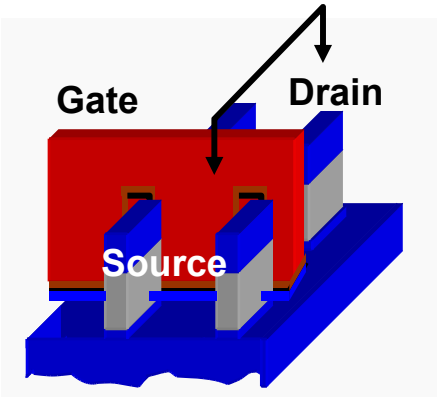
FinFET

Gates control this.

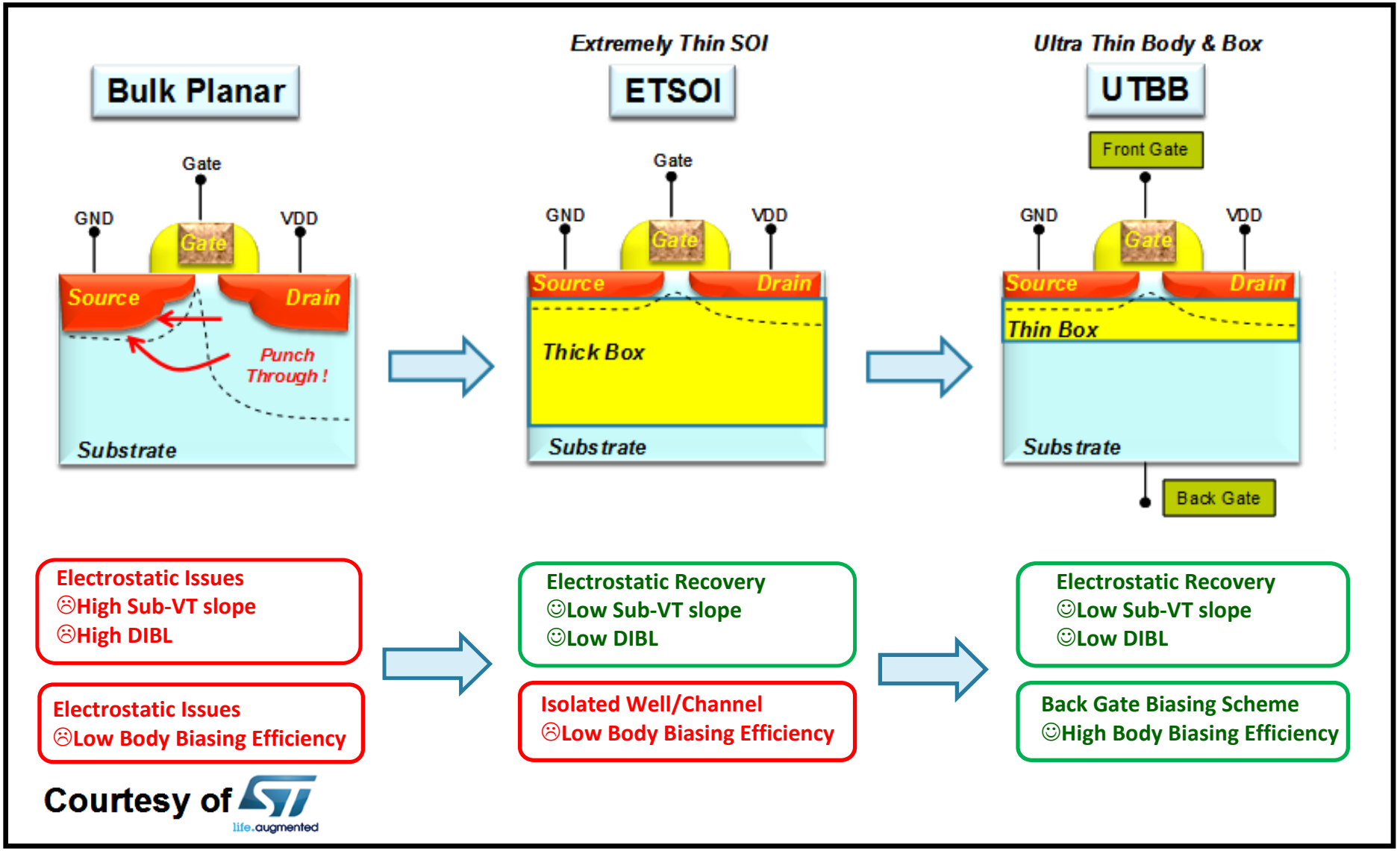
No leakage path.

Have more Si and thus can carry more current.

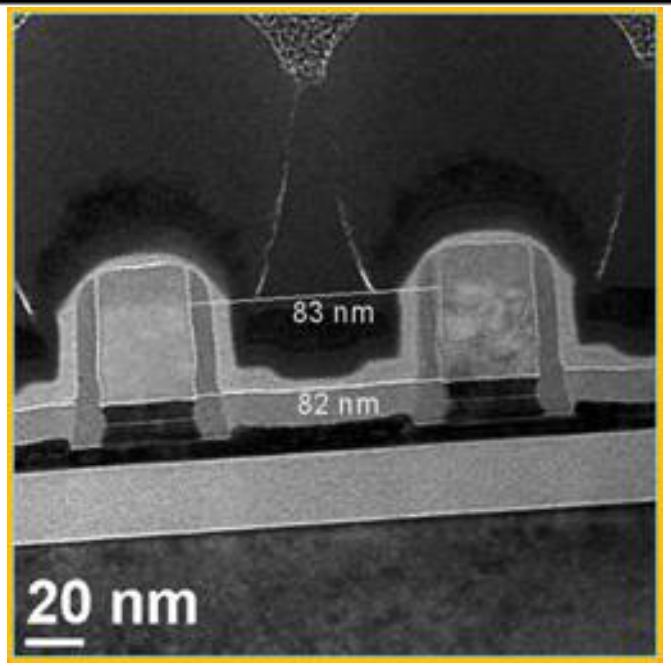
- **Better Electrostatics → Stronger Gate Control**
  - Lower V_t for the same leakage
  - Shorter channel for the same V_t
- **Reduced Channel Doping → Better SRAMs**
  - Less doping-driven threshold fluctuation
  - Lower supply voltage (V_{min}) – by about 150mV
  - Lower voltages means lower power – up to 40%

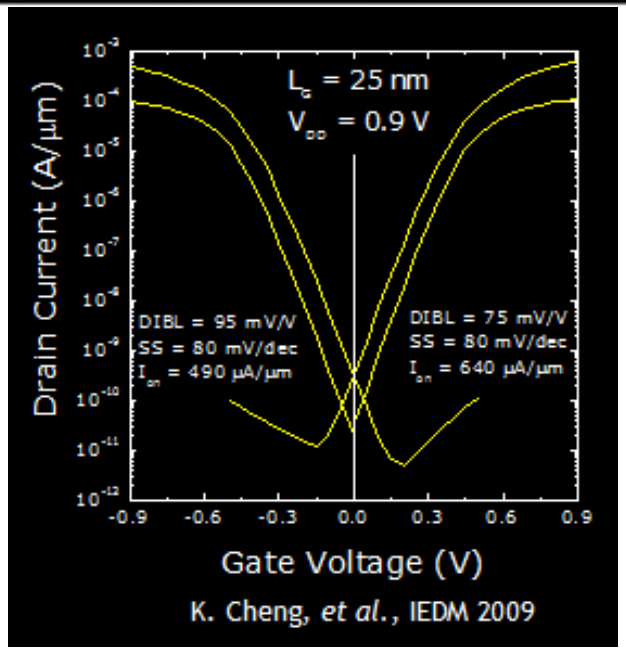


FDSOI Technologies



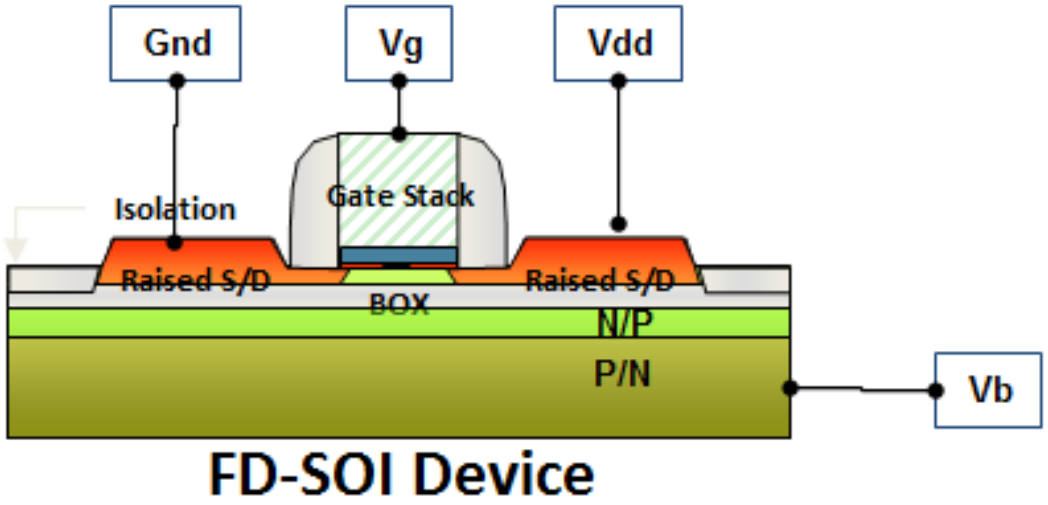
FDSOI Advantages





- Planar technology that leverages conventional CMOS processing and design methodology
- Excellent short channel control
- Superior performance for low-power (LP) applications
- Undoped body means much lower random dopant fluctuations (RDF)
- FDSOI with competitive performance demonstrated in 20nm GR

FDSOI Back-gating for Enhanced Flexibility



FD-SOI Device

Independent multi-gate device allows the following:

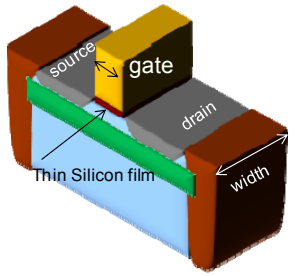
- Dynamically changing Vt on devices (trade leakage for performance)
- Adjust out typical process induced Vt variation (tighter control of Vt)
- Device optimization depending on the use condition: Multi-Vt enablement

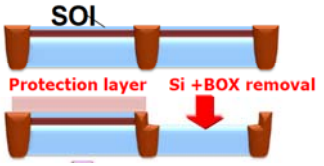
28nm UTBB FDSOI - Process Integration

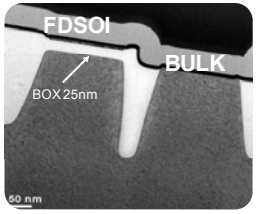
- **Gate-first type FEOL, same as ST/ISDA 28LP**
- **No HP/G-type complex stressors**
- **FE process: 80% common with ST/ISDA 28LP**
  20% specific
  - **10% less steps in UTBB vs. 28LP**
  - **Same LDD implants for all GO1 devices, incl. SRAM**
  - **No pocket implants**
  - **~ 20 implant steps saved vs. 28LP (2 VTs case)**
- **BE process: identical to ST/ISDA 28LP**
  - **Already qualified for volume production**
- **Same defect density vs. ISDA 28LP**
  - **Improved vs. "HP" technologies**

Courtesy of life.augmented

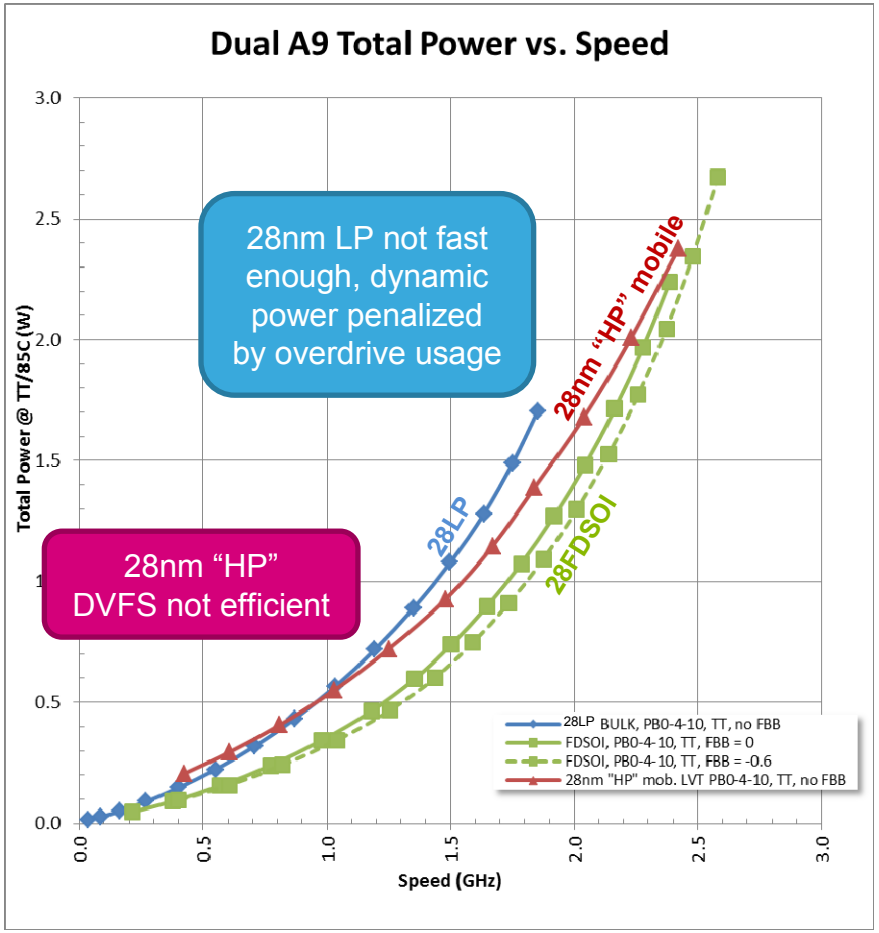
- STI isolation
- NW/PW/DNW
- **BPN/BPP**
- **BOX removed**
- HK
- MG
- SPACER
- **EPI (raised S/D)**
- LDD implantation
- S/D implantation
- NiPtSi Silicidation
- Std backend

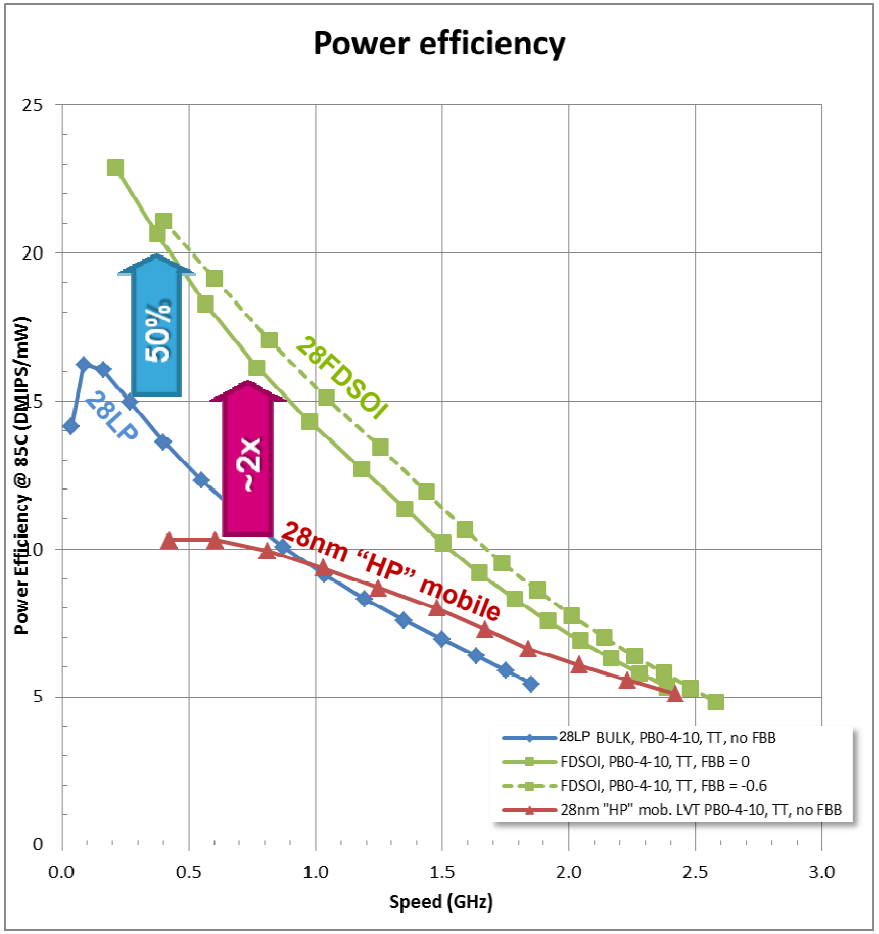






28nm UTBB FDSOI - Performance & Power

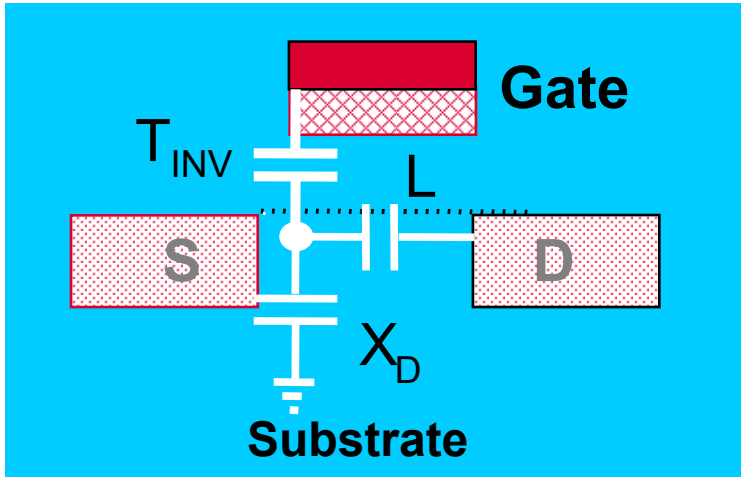




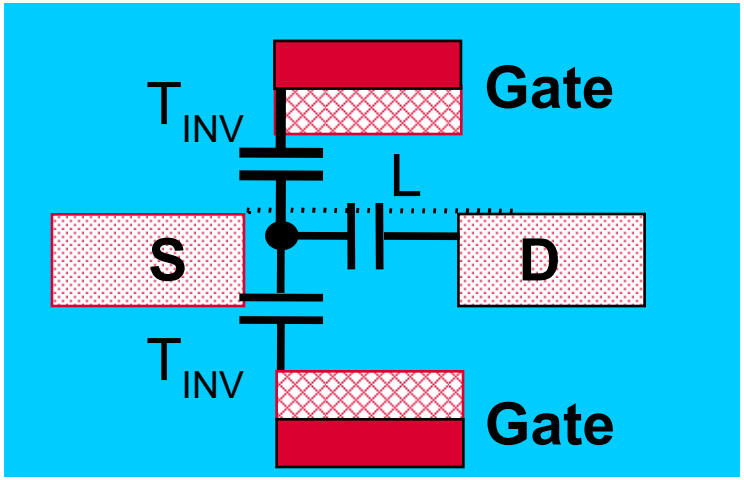
Courtesy of

Why Double-Gate CMOS

Bulk, PDSOI, UTTB-SOI



Double-Gate FET



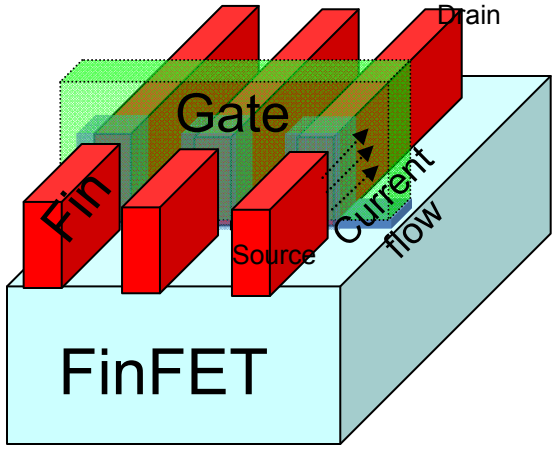
- No voltage divider action with substrate
  Near-ideal sub-threshold swing (→ lower V_T for same off-current)
- Scale to smallest $\mathbf{L_{POLY}}$ for a given $\mathbf{T_{OX}}$ and $\mathbf{T_{Si}}$
  Source shielded from drain by two gates
- **Net**: Improved density, performance, power.

Why FinFET is the Double-Gate Solution

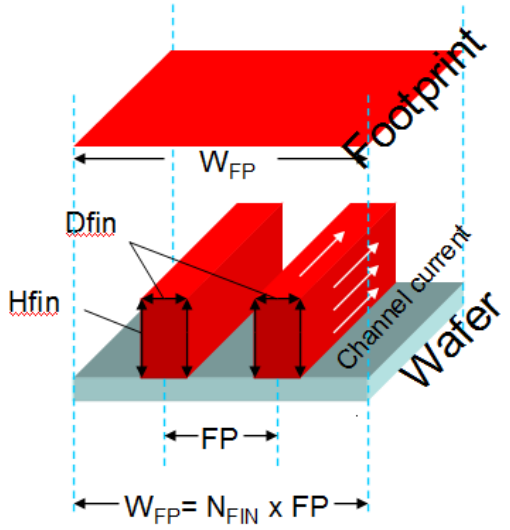
Many *intrinsic* advantages in FinFET

Quasi-planar processing enables

- **self-aligned double gates**
- **dense front side contacts to both gates**
- **symmetric front-side access to both sides of source-drain**



Added benefit: "fin effect" means W_{eff} larger than footprint



FinFET Advantages

Performance

Example of Device Benefit of FinFET at 20nm Node

	Lgate (nm)	Tinv (nm)	Tfin (nm)	Ssat (mV/dec.)	DIBL (mV/V)
FinFET	30	1.3	13	66	25
Planar	30	1.3	n/a	80	82

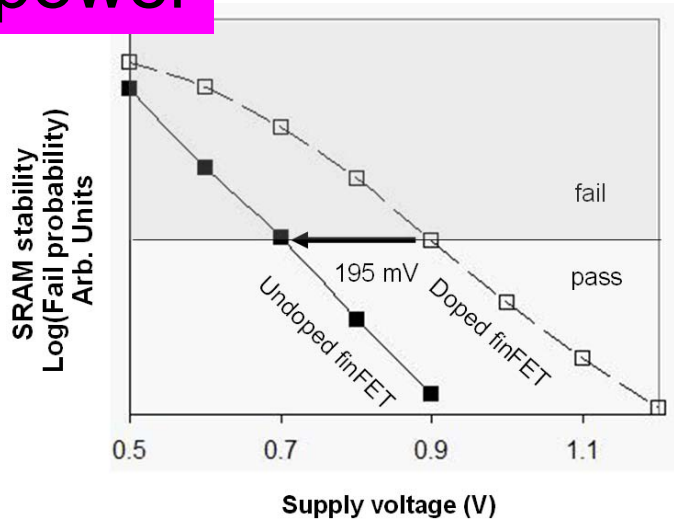
High-Speed Benefit
(Better SCEs for same Lgate/Tinv)

	Lgate (nm)	Tinv (nm)	Tfin (nm)	Ssat (mV/dec.)	DIBL (mV/V)
FinFET	30	1.8	10	79	82
Planar	30	1.3	n/a	80	82

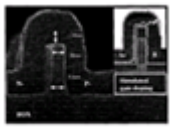
Low-Power Benefit
(Equivalent SCEs for higher Tinv)

Lower SRAM power

- Undoped fin minimizes dopant contribution to variability
- Other mechanisms such as work-function variations remain extant
- **Net**: Large overall reduction in mismatch

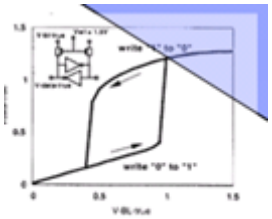


A Decade of FinFET R&D at IBM/Alliance



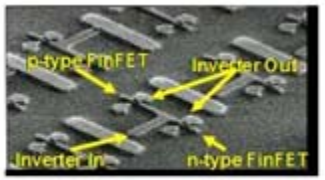
J. Kedzierski IEDM

High speed FinFET device N&P (2001)



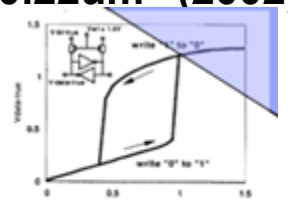
E.Nowak IEDM

FinFET CMOS demo (2002)



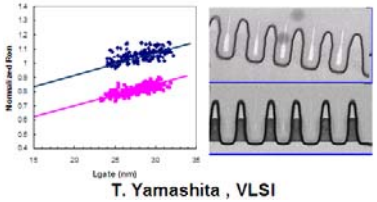
E.Nowak CICC

FinFET fully-depleted RO demo (2003)



E.Nowak IEDM

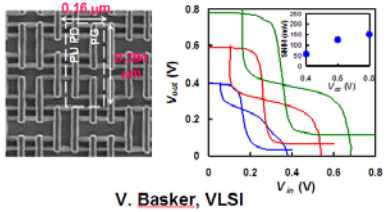
Functional SRAM 0.22um^2 (2002)



T. Yamashita , VLSI

Conformal doping in FinFET (2011)

0.063um^2 SRAM with FinFET (2010)

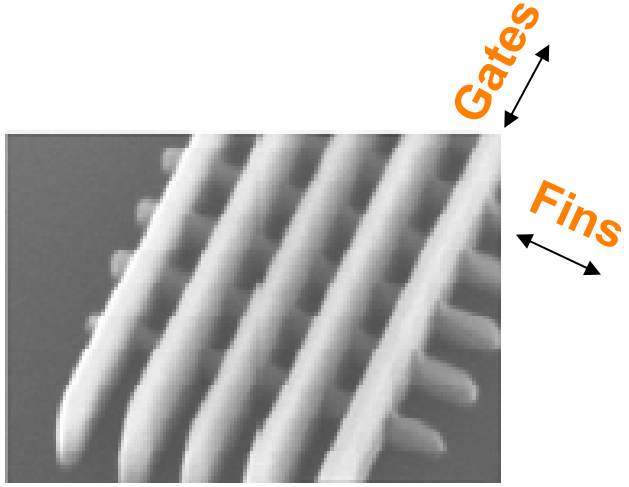


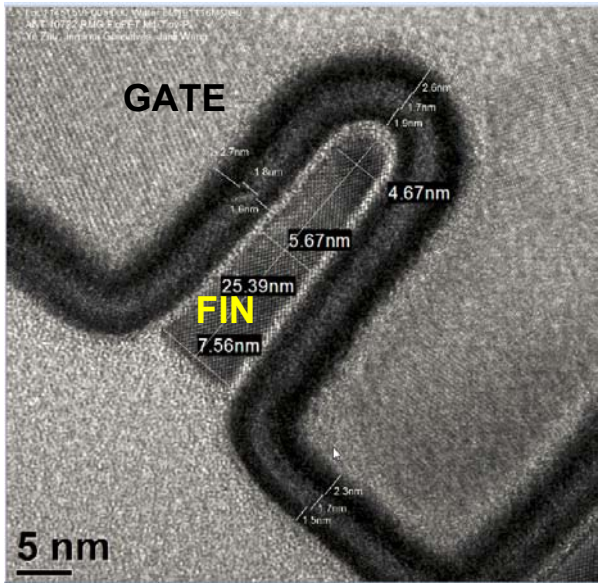
V. Basker, VLSI

SOI FinFETs: Processing Innovations

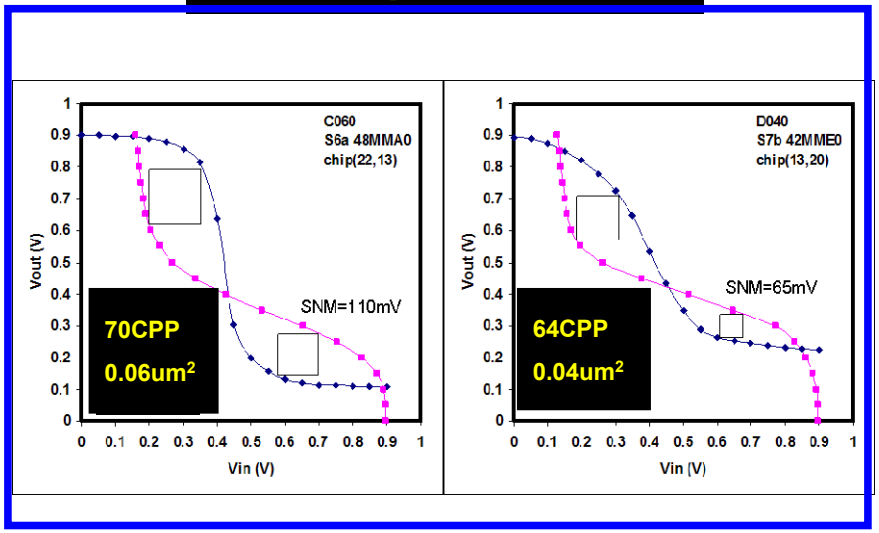
Key Innovations:

- Highly scaled FIN defined by Sidewall-Image-Transfer (SIT)
- RMG w/ new metal fill solution and reliability package
- Dual in-situ doped epitaxial source/drain for low resistance

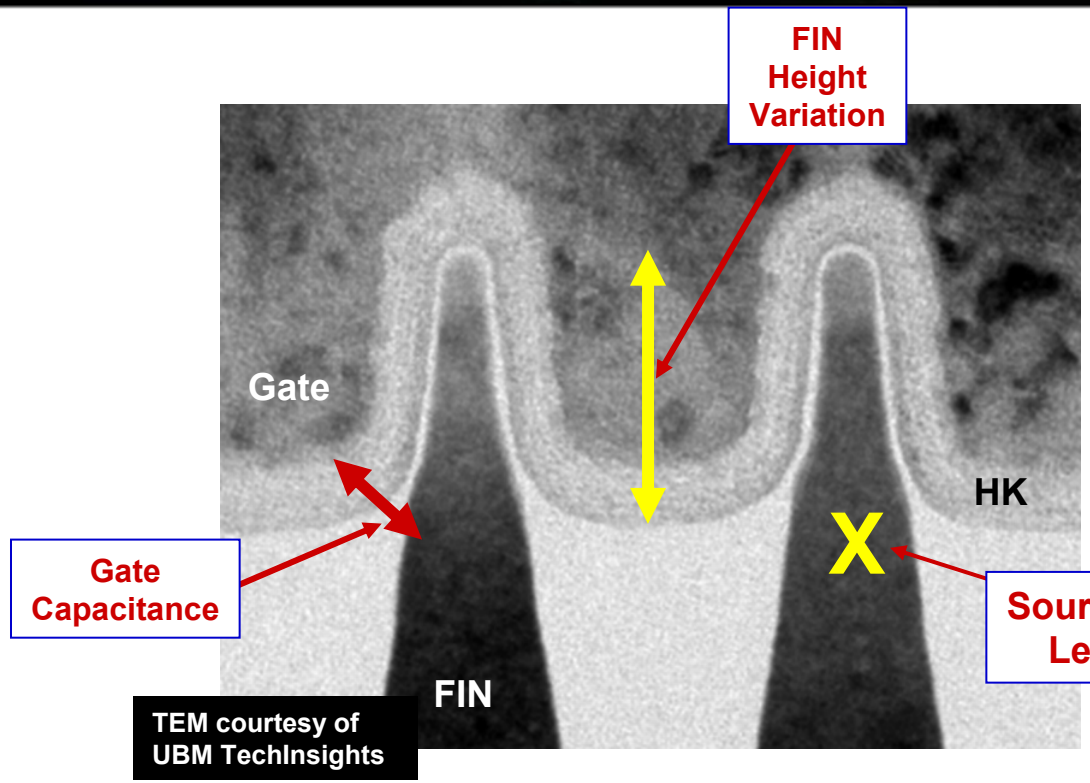


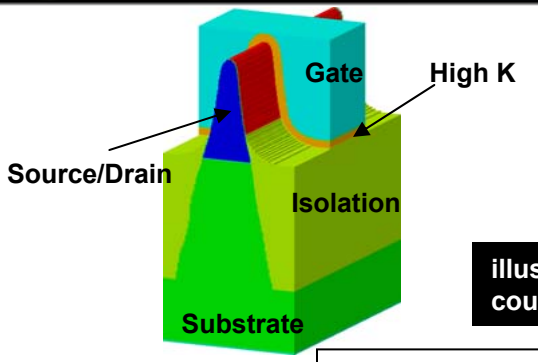


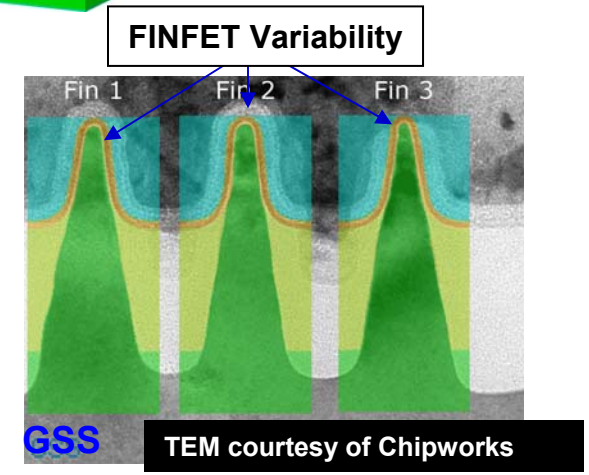
World's Smallest Flycell w/ Optical Litho



Junction-isolated Bulk FinFET





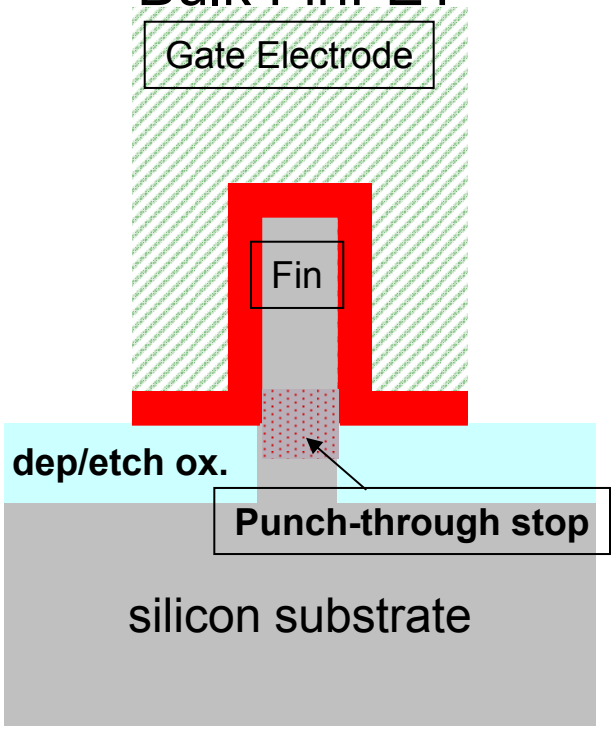


Several Key power / performance issues of junction-isolated bulk FinFETs:

- *Gate Height Variation from STI recess degrades performance*
- *Gate Capacitance degrades performance and adds power*
- *Source / Drain Leakage increases power (junction and GIDL)*

FinFET Isolation Schemes

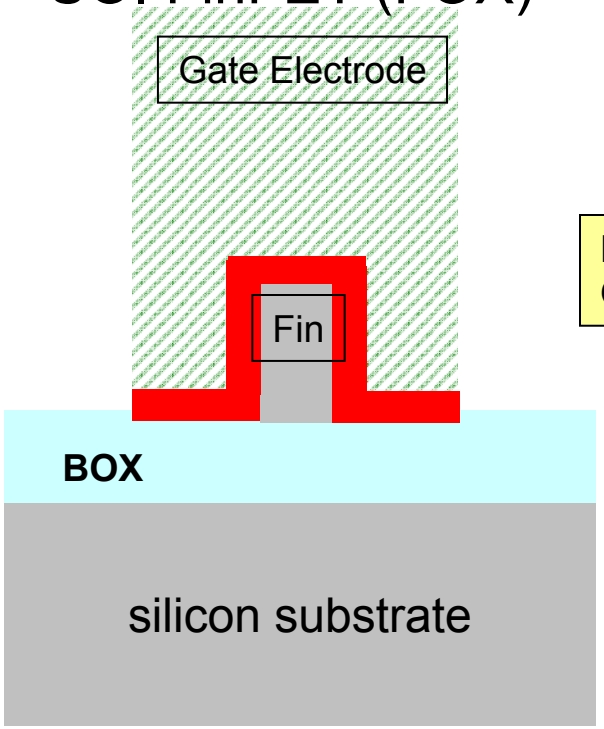
Junction-Isolated Bulk FinFET



Fin on bulk

- Fin height controlled by ox etch
- Complex isolation scheme
- Fin doping control possible issue
- Uses bulk wafer

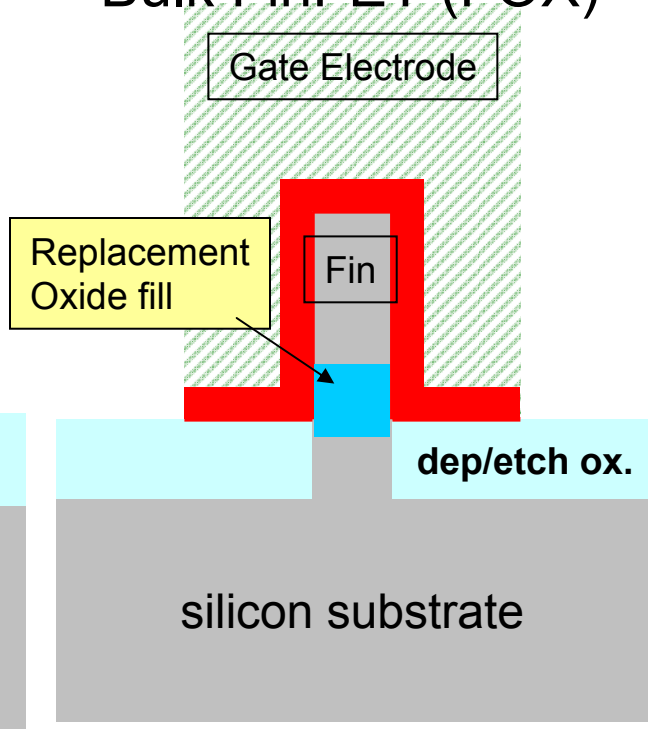
Dielectric-Isolated SOI FinFET (FOX)



Fin on SOI

- Fin height set by substrate
- Simpler isolation scheme
- Requires SOI wafer

Dielectric-Isolated Bulk FinFET (FOX)



Fin on oxide over bulk

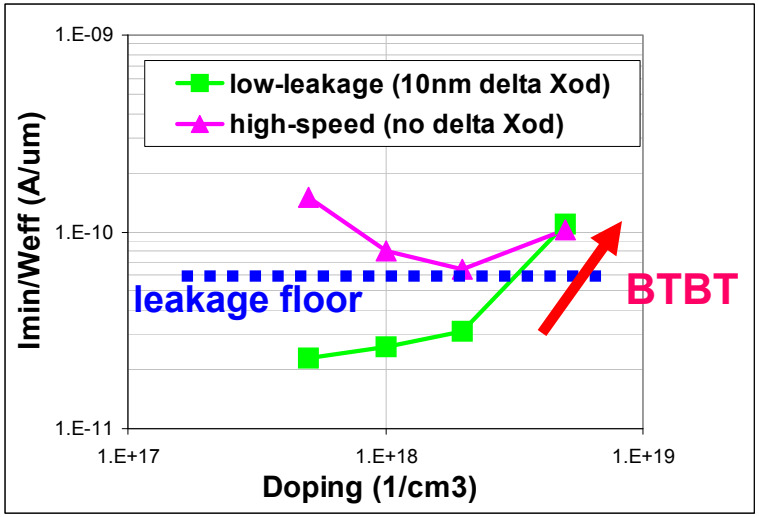
- Doping isolation requirement removed
- Isolation scheme still complex
- Uses bulk wafer

SOI - Bulk FinFET Comparison

Metric	Comparative Analysis
History Effect	No floating body in either: timing like Bulk planar CMOS
Isolation	Biggest challenge for bulk FinFET. Capacitance/leakage tradeoff.
Variability	Height control very challenging in bulk fin. Isolation doping requirement also adds within-fin nonuniformity.
Analog FETs	No body contact in either. SOI better due to uniform fin doping.
Self-heating	Worse in SOI FinFET – minor consideration for most applications. High duty factor circuits may suffer up to 5% drive current penalty.
Passives	Bulk FinFET can more easily introduce bulk planar passives. SOI FinFET enables planar passives with superior isolation properties.

- **FUNDAMENTALLY the same – design for both not a problem.**
- **SIGNIFICANT issues in manufacturing – will be addressed by future generation dielectric isolation or other scheme.**

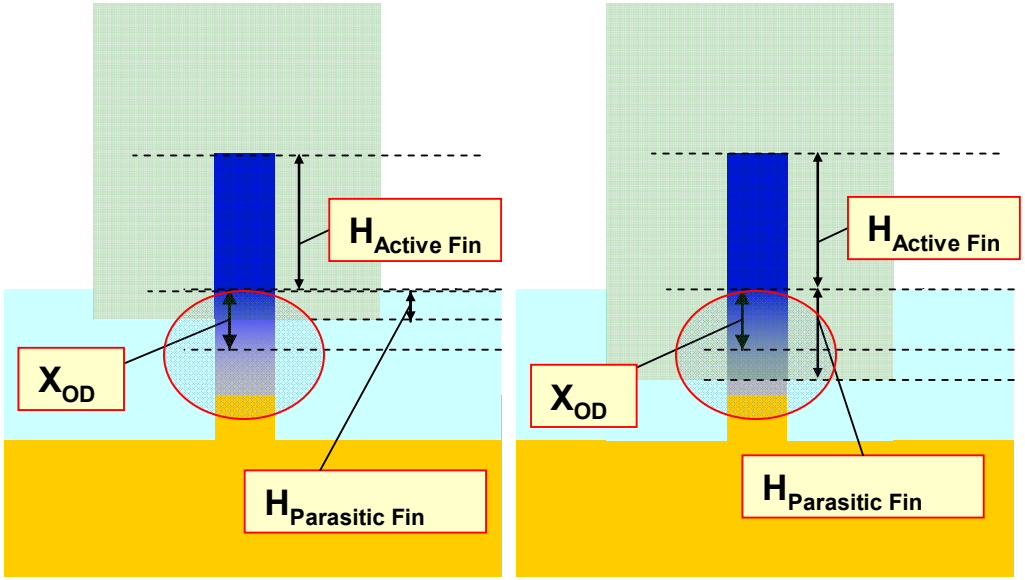
Junction-isolated FinFET Tradeoffs

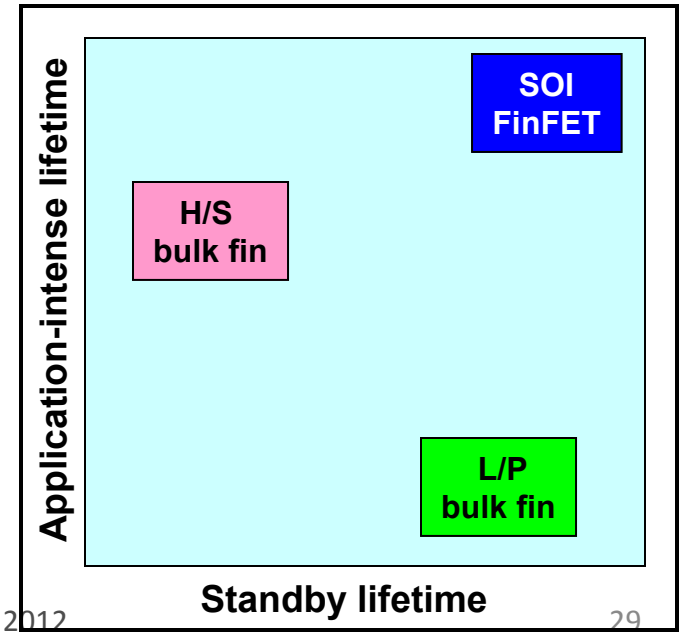


S/D Isolation Methods

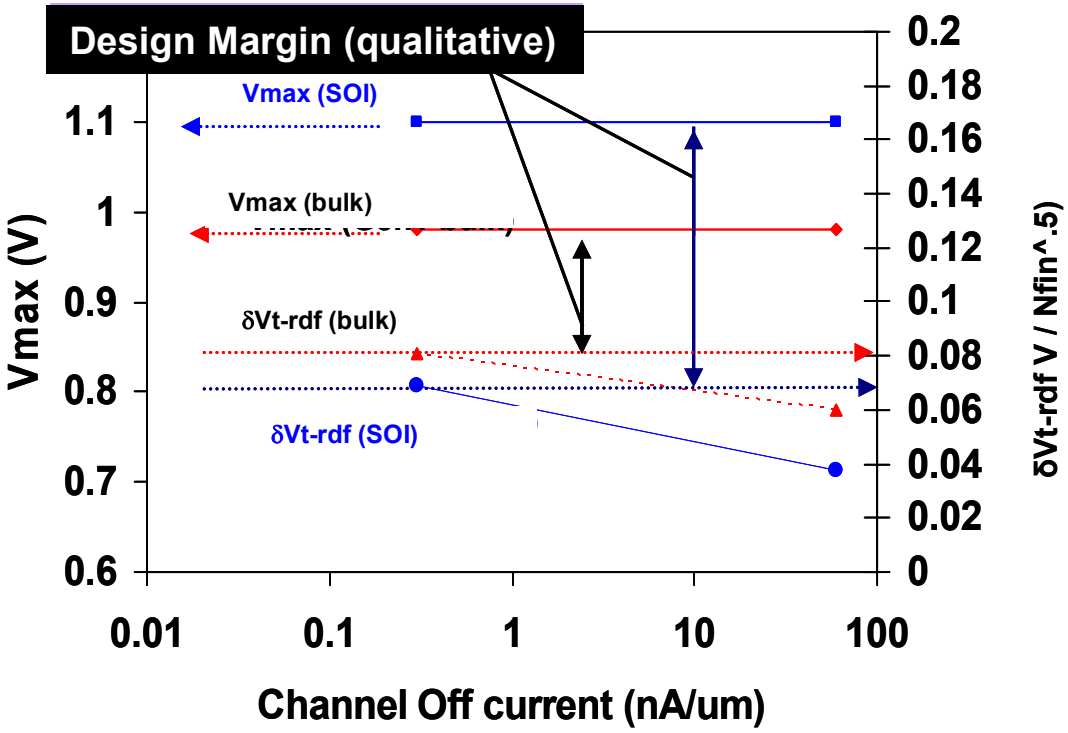
High Doping
- ✓ minimizes Cgate
- ✗ high leakage floor
- → H/S applications

Deep Gate
- ✓ low leakage floor
- ✗ Cgate penalty
- → L/P applications



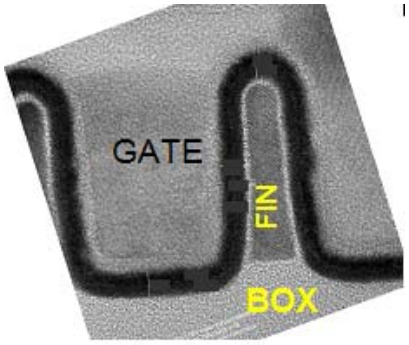


SOI vs Junction-isolated FinFETs



- V_{DD} Range is modulated by isolation design
- High channel doping increases RDFs (AVT) →Higher Vmin for SRAM.
- High channel doping Increases E_{OX} for given V_T → Lower Vmax (BTI and TDDB).
- High AVT also increases Die Iddq for given Ioff → Increased product leakage spec.

FinFET Variability and Manufacturing Challenges

Challenge	Solution	Results
Fin Profile Variability **- Shape/taper** **- Height control**	**Three SOI benefits:** **✓Natural height stop** **✓Relaxed etch requirements for straighter profile** **✓No fill/etch-back needed for isolation**	**Near ideal shape** 

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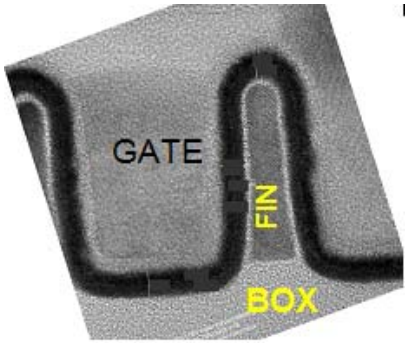
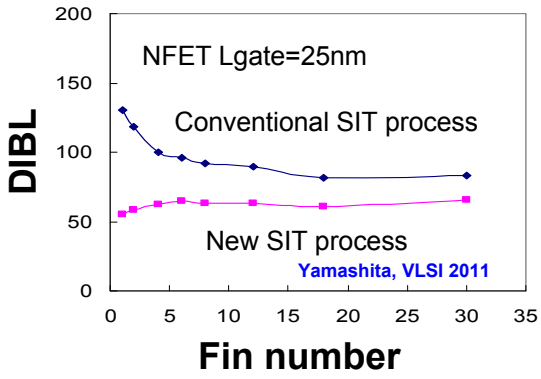
Fin Profile Variability **- Shape/taper** **- Height control**	**Three SOI benefits:** ✓**Natural height stop** ✓**Relaxed etch requirements for straighter profile** ✓**No fill/etch-back needed for isolation**	**Near ideal shape** 
End Fin Variability	**Cut-last process to eliminates end-fin systematic offset**	 **DIBL improvement**

FinFET Variability and Manufacturing Challenges

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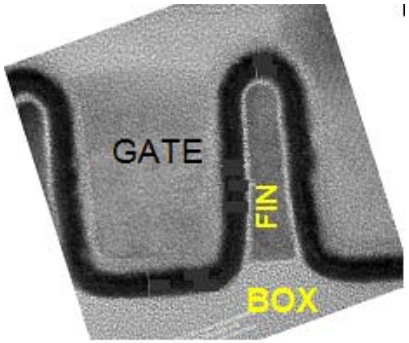
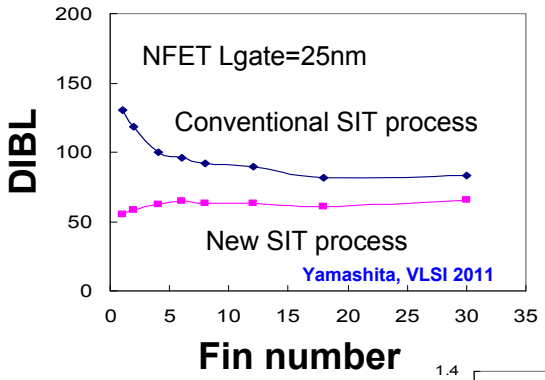
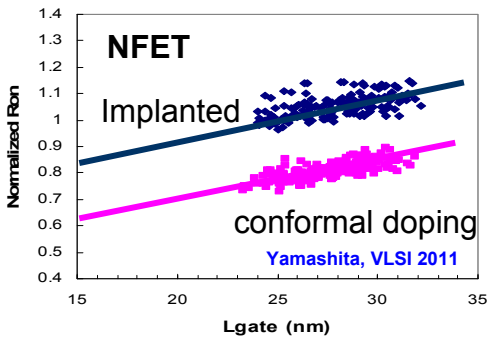
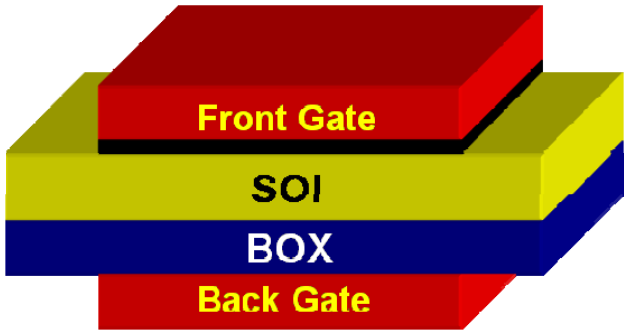
Fin Profile Variability **- Shape/taper** **- Height control**	**Three SOI benefits:** **✓Natural height stop** **✓Relaxed etch requirements for straighter profile** **✓No fill/etch-back needed for isolation**	**Near ideal shape** 
End Fin Variability	**Cut-last process to eliminates end-fin systematic offset**	 **DIBL improvement**
Fin Doping **- Vertical nonuniformity in extn and S/D** **- Doping damage in thin body**	**Conformal doping techniques**	**Rodlin reduction** 

Fully Depleted Devices for the Next Node

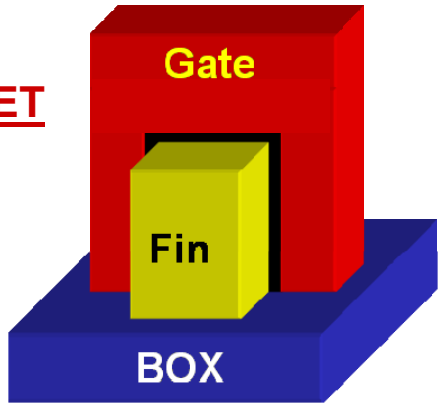
FDSOI



FDSOI:

- Excellent Short Channel Control
- Conventional planar processing
- Back Gate control possible – helps multi-Vt
- Body thickness may limit ultimate scalability
- Strong potential for today's expanding Low Power Applications market

FinFET



FinFET:

- Excellent Short Channel Control
- Complex process -- variability & manufacturability challenges
- Width Quantization can pose SRAM design challenges
- Device electrically wider than physical footprint
- Better Scalability: 2x or more relaxation in body thickness requirement
- Capability to meet long-term density, performance, & power requirements

Evolution and Expansion of SOI in VLSI Technologies: Planar to 3D

I. **SOI History and Advantages**
   - High Performance Logic Applications
   - Embedded Memories
   - Analog Mixed-Signal Applications

II. **Fully Depleted Devices**
   - Fundamentals
   - FDSOI
   - FinFETs

III. **Business Considerations**

SOI Advantages & Challenges

	PDSOI SOI vs Bulk	
Device Performance	++	
Device Leakage	=	
Cost (substrate + process)	--	
Design compatibility	--	
Manufacturability (variability, CLY, complexity, cycle time, TTM)	=	
Supply Chain (high volume, multi-sourcing, industry perception)	--	

Paradigm Shift in SOI Value Proposition

	PDSOI SOI vs Bulk	FINFET SOI vs Bulk
Device Performance	++	+
Device Leakage	=	+
Cost (substrate + process)	--	=
Design compatibility	--	=
Manufacturability (variability, CLY, complexity, cycle time, TTM)	=	++
Supply Chain (high volume, multi-sourcing, industry perception)	--	=

SOI - Bulk FinFET Cost Comparison

14nm FINFET

SOI vs. Bulk (Implant Isolation)

	Bulk Unique Process Adds	Comments
Substrate Contact	($0-$30) savings	Substrate contact
Well contacts	$125-$175	(2.5% - 3.5%) Area impact from well contacts
STI Isolation	$175-$300	Liner / Fill / CMP / Etch Back / Cleans 10:1 STI aspect ratio
Isolation Implant	$60-$180	(2 - 6) Extra Implants for well isolation
Total	$360-$655	

- Assumption of high volume full wafer processing cost at 22nm process is $5000
- **Analysis does not include any yield (CLY) benefit of improved variability with SOI FINFETs**

3 SOI / FOX Substrate Suppliers Ready

Soitec claims breakthrough for FinFET production

Soitec's new FD-3D wafer type can dramatically decrease time-to-market for companies thinking about making the move from planar to FinFET transistors.
Wafer maker Soitech has announced a new fully depleted silicon wafer which, the company claims, makes it considerably easier and cheaper to build semiconductors using 3D transistors.

MEMC Introduces Advanced Semiconductor Wafer To Enable High Volume Manufacturing of Multigate Devices

Published: July 6, 2012
ST. PETERS, Mo., July 6, 2012 /PRNewswire/ -- **MEMC Electronic Materials, Inc.** (NYSE: WFR) announced today the introduction of MEMC FOX-Si, an innovative and cost-effective silicon wafer designed specifically for delivering advanced FinFET technology with oxide dielectric isolation (FOX).

SOITEC AND SHIN- ETSU HANDOTAI ANNOUNCE NEW SMART CUT PARTNERSHIP AND EXTENDED TECHNOLOGY COOPERATION
This agreement will accelerate the development and capacity expansion for silicon on insulator (SOI) wafers to meet the market opportunity for FinFETs on SOI and Fully Depleted planar circuits

The combined capacity of the existing suppliers is 2.3-2.4 million wafers/yr by 2014 (substantially early)

Additional factory capacity can be put in place by the substrate suppliers :

- ***With a 12 months notification, incremental capacity of 3 million wafers/yr***

Summary

- SOI has enabled industry leadership in planar CMOS exemplified by both digital and analog mixed-signal applications
- Innovative future opportunities for SOI as Industry moves to Fully Depleted Architectures and beyond
  Uniformity and Variability control are at the forefront!
- Paradigm shift in SOI value proposition as FinFET era arrives

Acknowledgments: D. Harame, T. Hook, S. Iyer, J. Jagannathan, A. Kumar, E. Nowak