DALHOUSIE UNIVERSITY
Department of Electrical & Computer Engineering
Digital Circuits - ECED 2200

Experiment 1 - Basic Logic Gates

Objectives:

1. To study the truth tables of various basic logic gates
2. To verify DeMorgan's Theorem
3. To implement an INVERTER using NAND or NOR gates
4. To implement an OR gate using NAND gates

Note: There is no lab report required for this lab. Fill out the observation sheets, and submit them into Brightspace folder for Lab1a.

Required IC's:

Binary Explorer Board	7404 INV Gate
7408 AND Gate	7402 NOR Gate
7432 OR Gate	7486 XOR Gate
7400 NAND Gate	Mystery Chip

Note: The internal architecture of each IC can be found on page 7.

Theory:

Basic Logic Gates

The symbols and the Boolean expression for each basic logic gate are shown on page 6 of this lab.

DeMorgan's Theorem

DeMorgan proposed two theorems that are used frequently in Boolean algebra. The first theorem states:

The complement of two variables ANDed is equivalent to the OR of the complements of the individual variables.

This theorem can be expressed using the following formula:

$$\overline{A} + \overline{B} = \overline{A \bullet B}$$

The second theorem states:

The complement of two variables ORed is equivalent to the AND of the complements of the individual variables.

This theorem can be expressed using the following formula:

$$\overline{A} \bullet \overline{B} = \overline{A + B}$$

Part 1. Analysis of Basic Logic Gates

Procedure:

Setup the circuits shown on page 4 to analyze the operation of the various basic logic gates. For each gate:

1. Vary the inputs of each gate and measure the output. Do this for all possible combinations of inputs.

2. Construct the truth table for each gate.

Part 2. Verifying DeMorgan's Theorem

Procedure:

Set up circuits to verify DeMorgan's two theorems. For each circuit:

1. Vary the inputs to each circuit and measure the output for all possible combinations of inputs.

2. Using the above results construct the truth table for each circuit. Show that these circuits verify both of DeMorgan's Theorems.

Part 3. Implementing an INVERTER using NAND or NOR gates

Procedure:

Set up one of the two circuits shown on page 5. For the circuit you choose:

1. Vary the input and construct the truth table.
2. Do you conclude that the circuit behaves like an INVERTER? If yes/no why?

Part 4. Implementing an OR gate using NAND gates

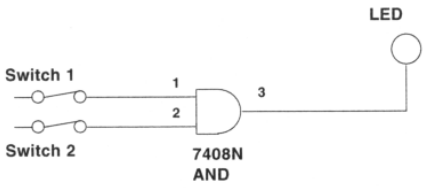
$$A + B = \overline{\overline{A}} + \overline{\overline{B}} = \overline{\overline{A} \bullet \overline{B}}$$

Procedure:

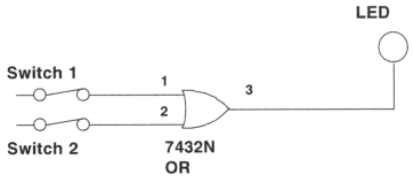
Setup a circuit to implement an OR gate using NAND gates only. For this circuit:

1. Vary the inputs and make the truth table
2. Do you conclude that the circuit behaves like and OR gate? If yes/no why?

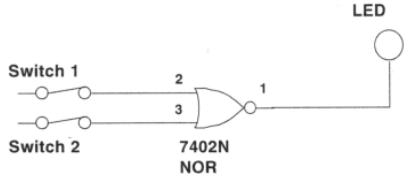
AND Gate



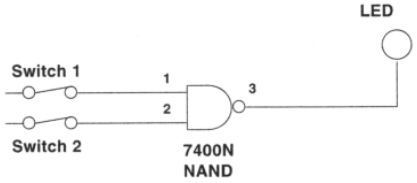
OR Gate



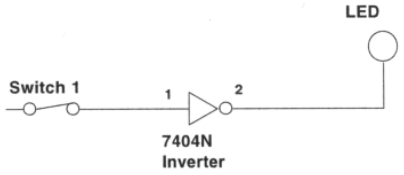
NOR Gate



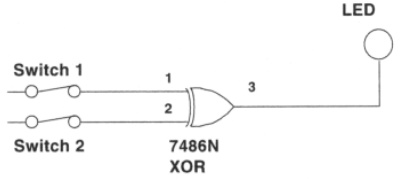
NAND Gate



INVERTING Gate



Exclusive OR Gate



Vcc= 5V at Pin 14 on each Chip
Ground is at Pin 7 on each Chip

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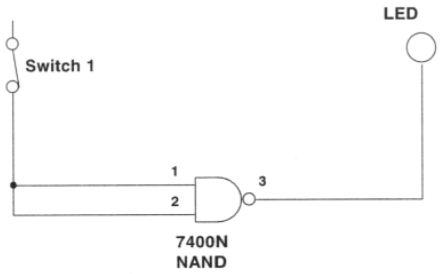
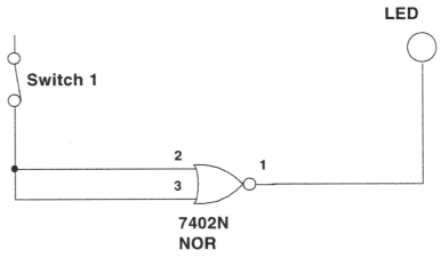
Approved by:	Sheet **1** of **2**	

Inverter Using NAND



Inverter Using NOR



Vcc=5V at Pin 14 on each Chip
Ground is at Pin 7 on each Chip

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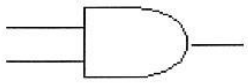
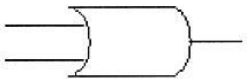
Summary of Logic Gates

AND



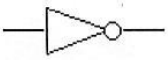
A	B	A • B
0	0	
0	1	
1	0	
1	1	

OR



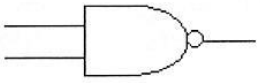
A	B	A + B
0	0	
0	1	
1	0	
1	1	

NOT



A	$\overline{A}$
0	
1	

NAND

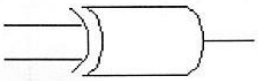


A	B	$\overline{(A \bullet B)}$
0	0	1
0	1	1
1	0	1
1	1	0

NOR

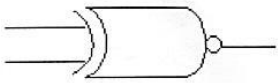
A	B	$\overline{(A + B)}$
0	0	
0	1	
1	0	
1	1	

XOR



A	B	A ⊕ B
0	0	
0	1	
1	0	
1	1	

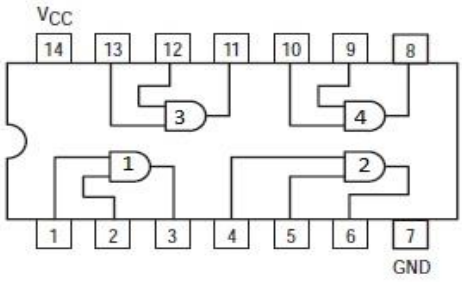
XNOR



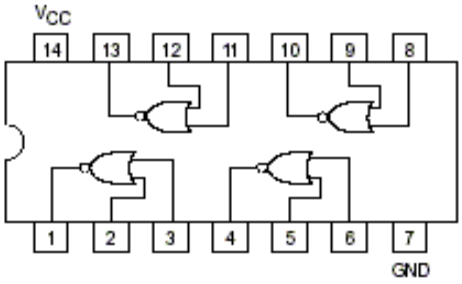
A	B	$\overline{(A \oplus B)}$
0	0	
0	1	
1	0	
1	1	

Summary of Internal architecture of each IC

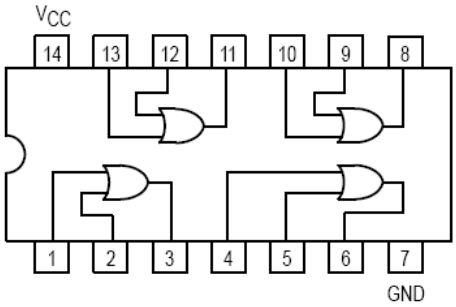
7408 AND Gate



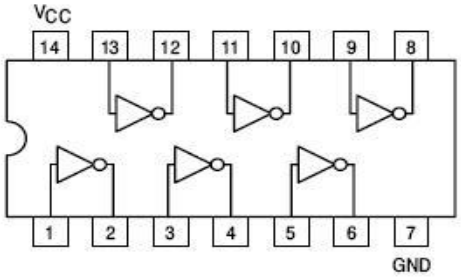
7402 NOR Gate



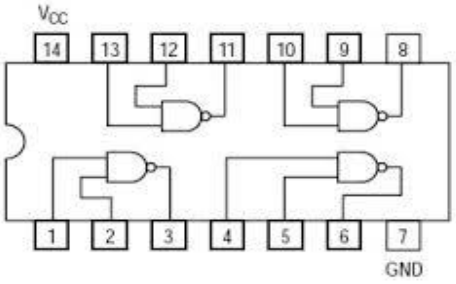
7432 OR Gate



7404 INV Gate



7400 NAND Gate



7486 XOR Gate