EXPERIMENT.1

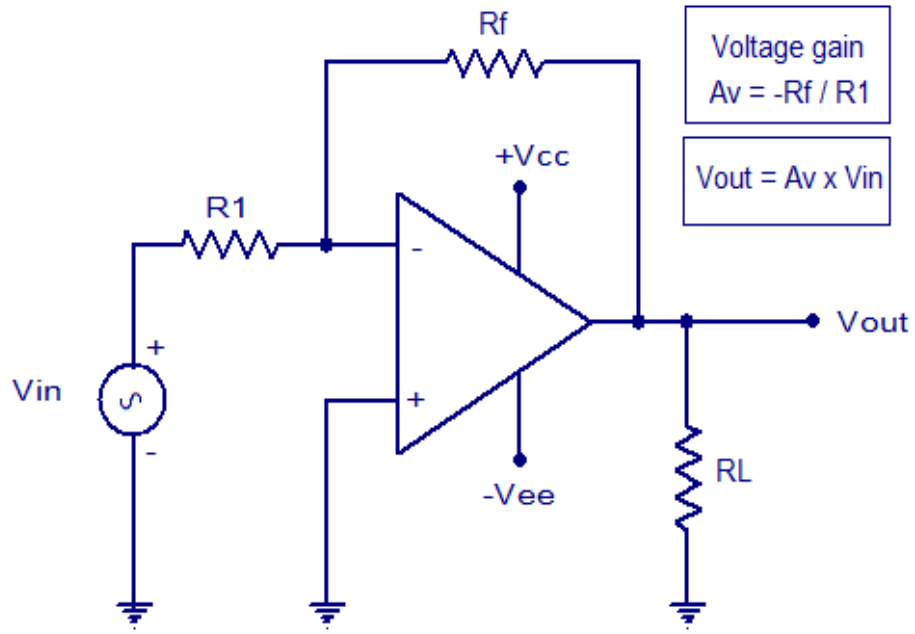
INVERTING AND NON-INVERTING AMPLIFIERS USINGOP AMPS

AIM: Design and realize Inverting and Non-inverting amplifier using 741 Op-amp.

Apparatus Required: CRO, Function Generator, Bread Board, 741 IC, ±12V supply, Resistors 1KΩ, 10KΩ, and connecting leads.

Theory:

An inverting amplifier using opamp is a type of amplifier using opamp where the output waveform will be phase opposite to the input waveform. The input waveform will be amplifier by the factor Av (voltage gain of the amplifier) in magnitude and its phase will be inverted. In the inverting amplifier circuit the signal to be amplified is applied to the inverting input of the opamp through the input resistance R1. Rf is the feedback resistor. Rf and Rin together determine the gain of the amplifier. Inverting operational amplifier gain can be expressed using the equation Av = – Rf/R1. Negative sign implies that the output signal is negated. The circuit diagram of a basic inverting amplifier using opamp is shown below.



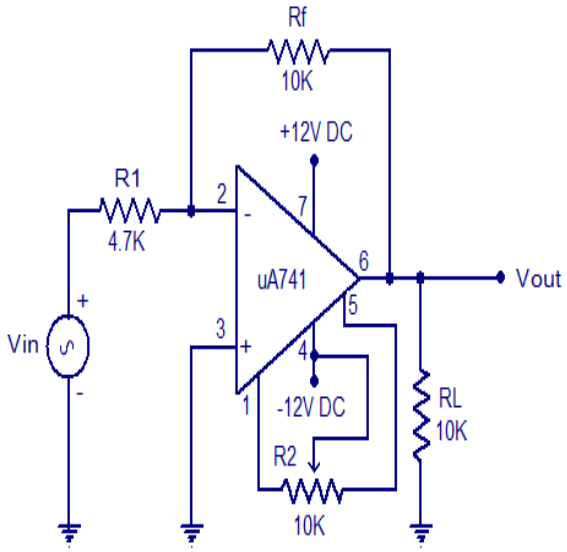
opamp inverting amplifier

The input and output waveforms of an inverting amplifier using opamp is shown below. The graph is drawn assuming that the gain (Av) of the amplifier is 2 and the input signal is a sine wave. It is clear from the graph that the output is twice in magnitude when compared to the input (Vout = Av x Vin) and phase opposite to the input.

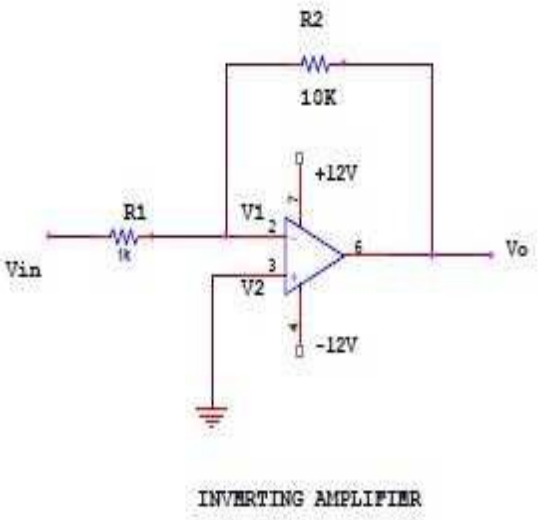
Practical inverting amplifier using 741.

A simple practical inverting amplifier using 741 IC is shown below. uA 741 is a high performance and of course the most popular operational amplifier. It can be used in a verity of applications like integrator,

differentiator, voltage follower, amplifier etc. uA 741 has a wide supply voltage range (+/-22V DC) and has a high open loop gain. The IC has an integrated compensation network for improving stability and has short circuit protection. Signal to be amplified is applied to the inverting pi (pin2) of the IC. Non inverting pin (pin3) is connected to ground. R1 is the input resistor and Rf is the feedback resistor. Rf and R1 together sets the gain of the amplifier. With the used values of R1 and Rf the gain will be 10 LL L A B M A N U A L (E . C . D E P T ,) Page 6 I N T E G R A T E D C I R C U I T S A N D A P P L I C A T I O N S 1 5 1 0 0 3 (Av = -Rf/R1 = 10K/1K = 10). RL is the load resistor and the amplified signal will be
available across it. POT R2 can be used for nullifying the output offset voltage. If you are planning to assemble the circuit, the power supply must be well regulated and filtered. Noise from the power supply can adversely affect the performance of the circuit. When assembling on PCB it is recommended to mount the IC on the board using an IC base.



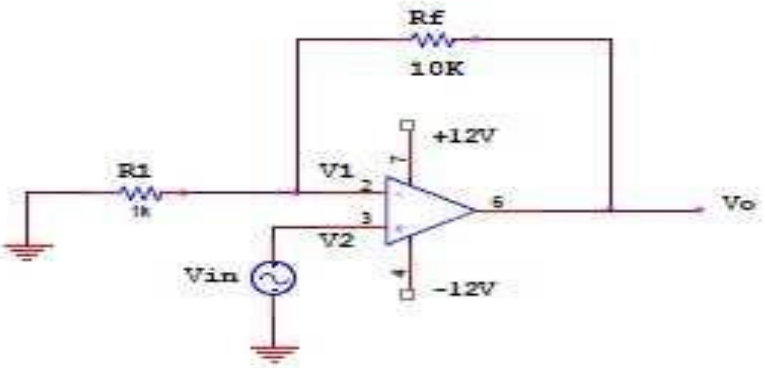
opamp inverting amplifier



In the inverting amplifier only one input is applied and that is to the inverting input (V2) terminal. The Non inverting input terminal (V1) is grounded.
Since, V1=0 V& V2=Vin
Vo= -A Vin
The negative sign indicates the output voltage is 1800 out of phase with respect to the input and amplified by gain A.

Practical Non-inverting amplifier using 741:

The input is applied to the non-inverting input terminal and the Inverting terminal is connected to the ground.
V1= Vin & V2=0 Volts
Vo= A Vin
The output voltage is larger than the input voltage by gain A & is in phase with the input signal.

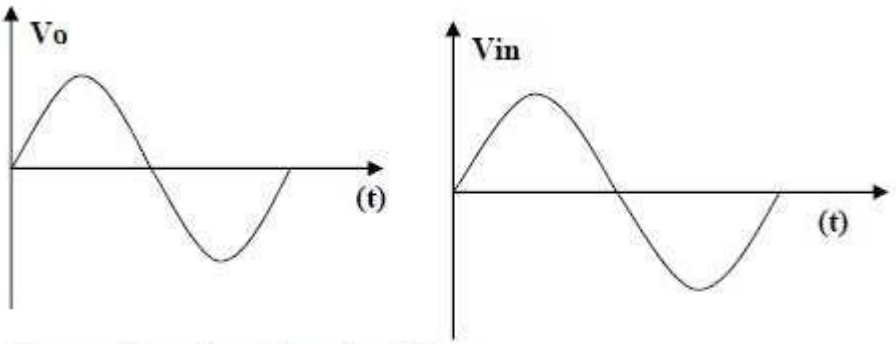


NON-INVERTING AMPLIFIER

Procedure:

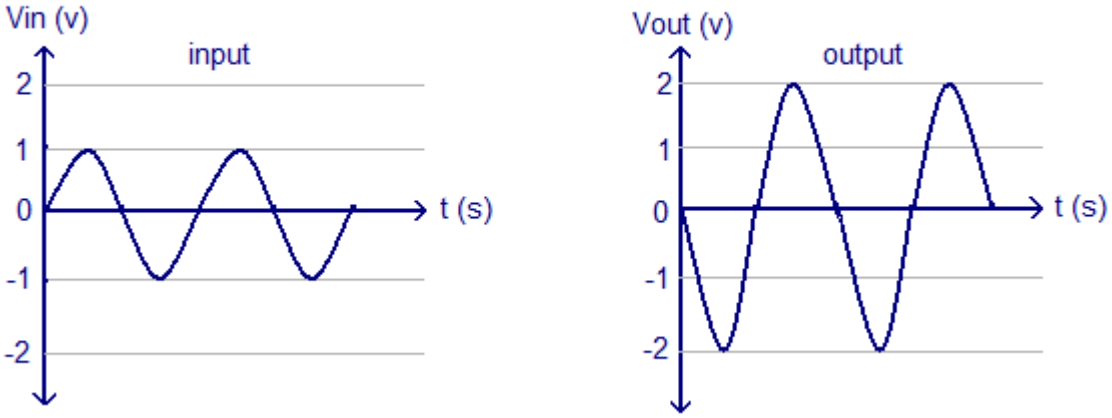
1) Connect the circuit for inverting, non inverting amplifier on a breadboard.
2) Connect the input terminal of the op-amp to function generator and output terminal to CRO.
3) Feed input from function generator and observe the output on CRO.
4) Draw the input and output waveforms on graph paper.

Output Waveform:



Output: Non- Inverting Amplifier

Input and output waveforms of an opamp inverting amplifier (gain assumed to be 2)



RESULT: Hence verified and drawn the operation and respective waveforms of inverting and non-inverting amplifier**.**

VIVA VOICE QUESTIONS:

1. Define an integrated circuit and classify them.
2. What is an op-amp and what are its types?
3. How to define the symbol of op-amp?
4. What are the various terminals of op-amp 741 IC?
5. What is the operating voltage range of IC 741?

EXPERIMENT.2

OPAMPAPPLICATIONS- ADDER, SUBTRACTOR.

AIM:

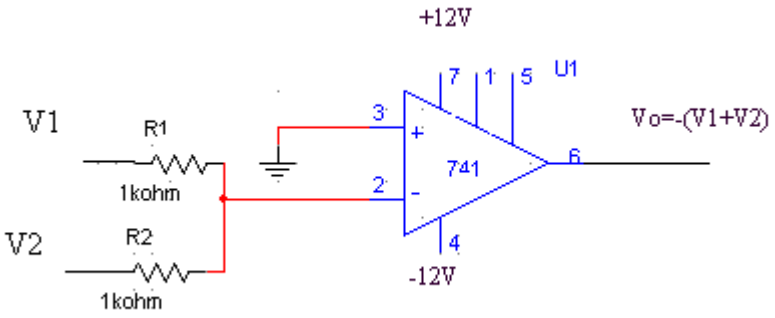
To study the applications of IC 741 as adder, subtractor.

APPARATUS:

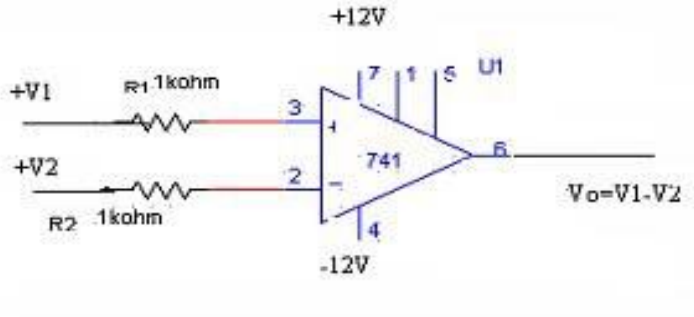
1. IC 741
2. Resistors (1KΩ)—4
3. Function generator
4. Regulated power supply
5. IC bread board trainer
6. CRO
7. Patch cards and CRO probes

CIRCUIT DIAGRAM

Adder:



Subtractor:



THEORY:

ADDER:

Op-Amp may be used to design a circuit whose output is the sum of several input signalssuchascircuitiscalledasummingamplifierorsummer.Wecanobtaineither inverting or non-inverting summer.

Thecircuitdiagramsshowsatwoinputinvertingsummingamplifier.Ithastwo input voltages $V_1$and V_2, two input resistors R_1, R2and a feedback resistor R_f.

Assumingthatopampisinidealconditionsandinputbiascurrentisassumedtobezero,there is no voltage drop across the resistor $R_{comp}$and hence then on inverting input terminal is at ground potential.
By taking nodal equations.

$V_1/R_1+V_2/R_2+V_0/R_f=0$
$V_0=-[(R_f/R_1)\ V_1+(R_f/R_2)\ V_2]$
And here $R_1=R_2=R_f=1K\Omega$
$V_0=-(V_1+V_2)$
Thus output is inverted and sum of input.

SUBTRACTOR:

A basic differential amplifier can be used as a subtractor. It has two input signals V1and V2and two input resistances R1andR2 and a feedback resistor R_f.The input signals scaled to the desired values by selecting appropriate values for the external resistors.

From the figure, the output voltage of the differential amplifier with a gain of‘1’ is
$V_0=-R/R_f(V_2-V_1)$
$V_0=V_1-V_2$.
Also $R_1=R_2=R_f=1K\Omega$.

Thus, the output voltage V_0 is equal to the voltage V_1 applied to then on inverting terminal minus voltage V_2applied to inverting terminal. Hence the circuit is subtractor.

OBSERVATIONS:
ADDER:

V_1(volts)	V_2(volts)	Theoretical $V_0=-(V_1+V_2)$	Practical $V0=-(V_1+V_2)$

SUBTRACTOR:

V_1(volts)	V_2(volts)	Theoretical $V_0=(V_1-V_2)$	Practical $V0=(V_1-V_2)$

PROCEDURE:

ADDER:

1. connections are made as per the circuit diagram.
2. Apply input voltage1) V_1=5v,V_2=2v
   2) V_1=5v,V_2=5v
   3) V_1=5v,V_2=7v.
3. Using Millimeter measure the dc output voltage at the output terminal.
4. For different values of $V_1$and V_2measure the output voltage.

SUBTRACTOR:

1. Connections are made as per the circuit diagram.
2. Apply input voltage1) V_1=5v,V_2=2v
   2) V_1=5v,V_2=5v
   3) V_1=5v,V_2=7v.
3. Using multi meter measure the dc output voltage at the output terminal.
4. For different values of $V_1$and V_2measure the output voltage.

PRECAUTIONS:

1. Make null adjustment before applying the input signal.
2. Maintain proper Vcc levels.

RESULT: Performed and tabulated the addition and subtraction operation on IC 741 op-amp.

VIVA-VOICE QUESTIONS:

1. What are an adder and subtractor?
2. Write the formulae for sum of three inputs for an op-amp.
3. What are the various DC characteristics of op-amp?
4. What are the various AC characteristics of op-amp?

EXPERIMENT.3

OPAMPAPPLICATIONS-COMPARATOR CIRCUITS

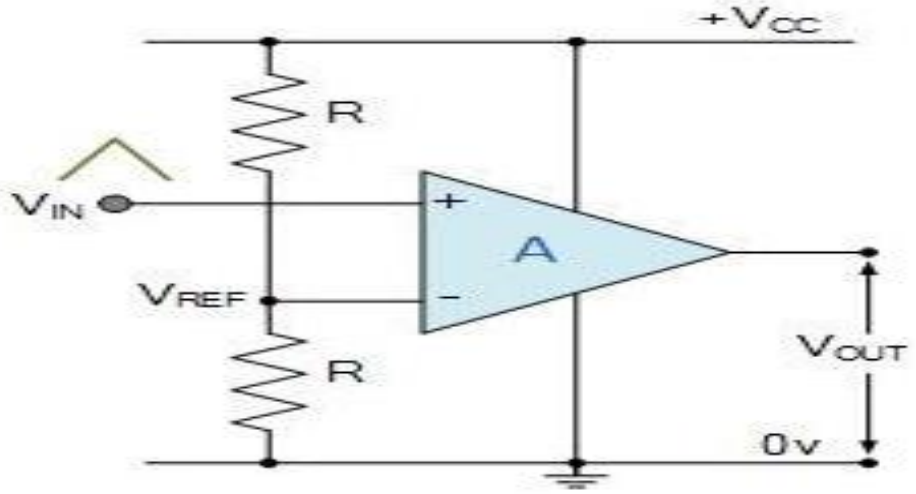
AIM:

To study the applications of IC 741 as comparator.

APPARATUS:

1. IC 741
2. Resistors (1KΩ)—4
3. Function generator
4. Regulated power supply
5. IC bread board trainer
6. CRO
7. Patch cards and CRO probes

CIRCUIT DIAGRAM



THEORY:

COMPARATOR:

A comparator is a circuit which compares a signal voltage applied atoneinputofanop-ampwithaknownreferencevoltageattheotherinput.Itisbasicallyanopen loop op-amp with output ±Vsat as in the ideal transfer characteristics.

It is clear that the change in the output state takes place with an increment in input Vi of only2mv.Thisistheuncertaintyregionwhereoutputcannotbedirectly defined. There are basically 2 types of comparators.

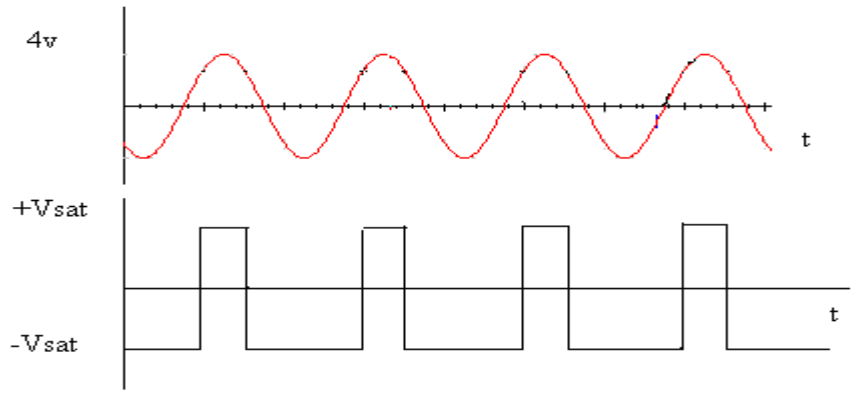
1. Non inverting comparator and.
2. Inverting comparator.

The applications of comparator are zero crossing detector, window detector, time marker generator and phase meter.

OBSERVATIONS:

Voltage input	V_{ref}	Observed square

MODEL GRAPH:



PROCEDURE:

1. Connections are made as per the circuit diagram.
2. Select the sine wave of10V peak to peak ,1K Hz frequency.

3. Apply the reference voltage 2V and trace the input and output wave forms.
4. Superimpose input and output waveforms and measure sine wave amplitude with reference to $V_{ref.}$
5. Repeat steps3and 4with reference voltages as 2V,4V,-2V,-4Vand observe the waveforms.
6. Replace sine wave input with 5V dc voltage and V_{ref}=0V.
7 Observe dc voltage at output using CRO.
8. Slowly increase V_{ref}voltage and observe the change in saturation voltage.

PRECAUTIONS:

1. Make null adjustment before applying the input signal.
2. Maintain proper Vcc levels.

RESULT: Hence performed comparison of time varying signal with a known reference voltage and drawn graphs

VIVA-VOICE QUESTIONS:

1. What is a comparator?
2. What is reference voltage?
3. Classify comparators?

EXPERIMENT.4

OP-AMP741 AS INTEGRATOR

AIM:

To design and test an op-amp integrator

EQUIPMENTSANDCOMPONENTS:

APPARATUS

1. DC power supply	1 No.
2. CRO	1 No
3. BreadBoard	1No
4. FunctionGenerator-	1 No.

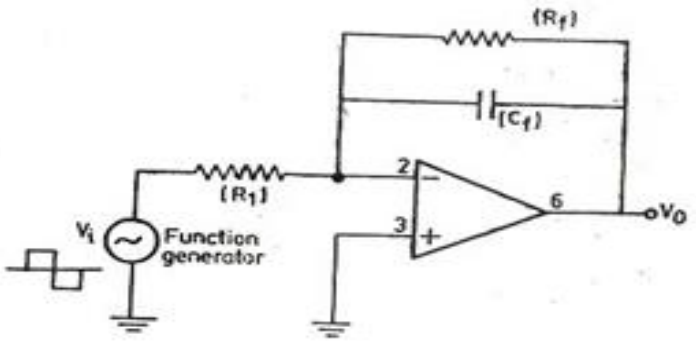
COMPONENTS:

1. 15 kΩ Resistor– 2 No.
2. 820 Resistor– 1 No.
3. 1.5 kΩ Resistor– 1 No.
4. 0.01 F Capacitor-2No
5. 0.5nF Capacitor-1No
6. IC741 - 1 No.

THEORY

The operational amplifier can be used in many applications. It can be used as differentiator and integrator. In integrator the circuit performs the mathematical operation of integration that is the output wave form is the integrative of the input waveform or good integration, one must ensure that the time period of the input signal is smaller than or equal to RfC1.the practical integrator eliminates the problem of instability and high frequency noise.

CIRCUITDIAGRAM:



PROCEDURE:

1. connect the integrator circuit as shown in fig.adjust the signal generator to produce a 5 volt peak sine wave at100 Hz.
2. observe input Vi and Vo simultaneously on the oscilloscope measure and record the peak value of Vo and the phase angle of Vo with respect to Vi.
3. Repeat step2 while increasing the frequency of the input signal. Find the maximum frequency at which circuit offers differentiation. Compare it with the calculated value of f_a Observe & sketch the input and output for square wave.
4. Connect the integrator circuit shown in Fig2.Set the function generator to produce a square wave of 1V peak-to-peak amplitude at 500Hz.View simultaneously output $V_o$and V_i.
5. Slowly adjust the input frequency until the output is good triangular waveform. Measure the amplitude and frequency of the input and output waveforms.
6. Verify the following relationship between R_1C_f and input frequency for good integration $f>f_a$ & $T<R_1C_1$ Where R_1C_f is the time constant
7. Now set the function generator to a sine wave of 1V peak-to-peak and frequency 500Hz. adjust the frequency of the input until the output is a negative going cosine wave. Measure the frequency and amplitude of the input and output waveforms.

OBSERVATIONS:

1. The time period and amplitude of the output waveform of differentiator circuit
2. The time period and amplitude of the integrator waveform

CALCULATIONS:

Integrator: Design an integrator that integrates a signal whose frequencies are between1 KHz and10 KHz.

$$f_b \quad \frac{1}{2R_1C_f}$$

The frequency at which the gain is 0 dB.

$$f_a \quad \frac{1}{2R_fC_f}$$

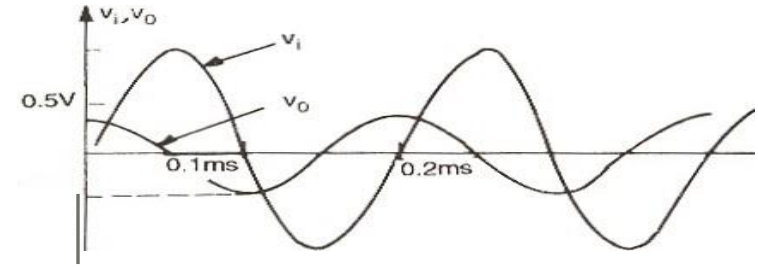
f_a: Gain limiting frequency,

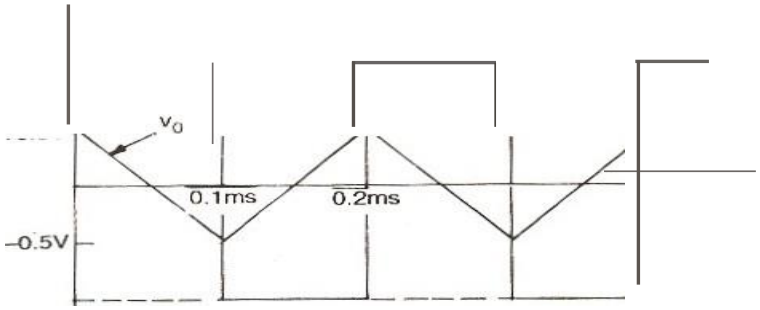
The circuit acts as integrator for frequencies between f_a and f_b Generally $f_a<f_b$ [Ref. Frequency response of the integrator] Therefore choose f_a=1KHz

F_b=10 KHz Let C_f=0.01 F Therefore R_1=1.59k Choose R_1=1.5 K R_f=15 K

GRAPH:

Integrator:





RESULT: Hence performed the integration operation of op-amp and calculated its frequency?

Integrator

$$f_a = \frac{1}{2R_fC_f}$$

T=_____

VIVA-VOICE QUESTIONS:

1. What is an integrator?
2. In which condition an RC circuit acts as an integrator?
3. Define cut-off frequency of an integrator?

EXPERIMENT.5

OP-AMP741 AS DIFFRENTIATOR

AIM:

To design and test an op-amp differentiator and integrator

EQUIPMENTSANDCOMPONENTS:

APPARATUS

1. DC power supply - 1 No.
2. CRO - 1 No.
3. BreadBoard - 1 No.
4. FunctionGenerator- 1 No.

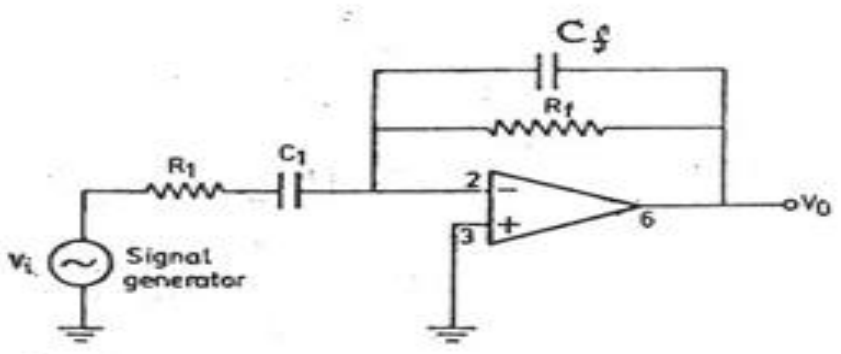
COMPONENTS:

1. 15 kΩ Resistor– 2 No.
2. 820 Resistor– 1 No.
3. 1.5 kΩ Resistor– 1 No.
4. 0.01 F Capacitor-2No
5. 0.5nF Capacitor-1No
6. IC741 - 1 No.

THEORY

The operational amplifier can be used in many applications. It can be used as differentiator and integrator. In differentiator the circuit performs the mathematical operation of differentiation that is the output wave form is the derivative of the input waveform or good differentiation, one must ensure tha the time period of the input signal is larger than or equal to RfC1.the practical differentiator eliminates the problem of instability and high frequency noise.

CIRCUITDIAGRAM:



PROCEDURE:

1. connect the differentiator circuit as shown in fig.adjust the signal generator to produce a 5 volt peak sine wave at100 Hz.
2. observe input Vi and Vo simultaneously on the oscilloscope measure and record the peak value of Vo and the phase angle of Vo with respect to Vi.
3. Repeat step2 while increasing the frequency of the input signal. Find the maximum frequency at which circuit offers differentiation. Compare it with the calculated value of f_a Observe & sketch the input and output for square wave.
4. Connect the integrator circuit shown in Fig2.Set the function generator to produce a square wave of 1V peak-to-peak amplitude at 500Hz.View simultaneously output $V_o$and V_i.
5. Slowly adjust the input frequency until the output is good triangular waveform. Measure the amplitude and frequency of the input and output waveforms.
6. Verify the following relationship between R_1C_f and input frequency for good integration $f>f_a$ & $T<R_1C_1$ Where R_1C_f is the time constant
7. Now set the function generator to a sinewave of 1V peak-to-peak and frequency 500Hz. Adjust the frequency of the input until the output is a negative going cosine wave. Measure the frequency and amplitude of the input and output waveforms.

OBSERVATIONS:

1. The time period and amplitude of the output waveform of differentiator circuit
2. The time period and amplitude of the integrator waveform

CALCULATIONS:

Design a differentiator to differentiate an input signal that varies infrequency from10 Hz to 1 kHz.

$$f_a = \frac{1}{2R_fC_1}$$

f_a=1 kHz, the highest frequency of the input signal

Let C_1=0.01 F, Then

R_f=15.9 k

Therefore choose R_f=15.0 k

$$f_b = \frac{1}{2R_1C_1}$$

Choose: f_b=20x f_a=20 KHz

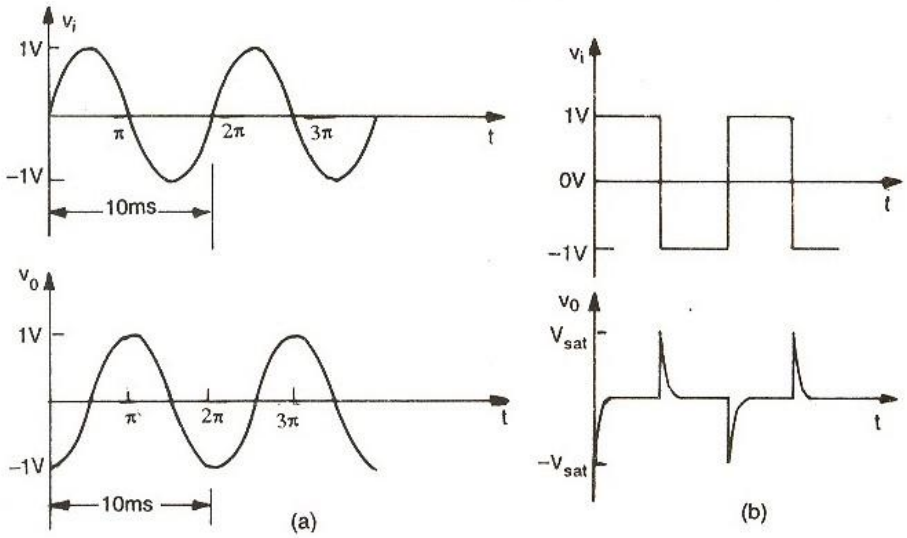
Hence R_1=795

Therefore choose R_1=820

Since $R_1C_1=R_fC_f$ (compensated attenuator)
C_f=0.54 nF
Therefore choose C_f=0.5nF

GRAPH:

Differentiator



RESULT: Hence performed the integration operation of op-amp and calculated its frequency?

Differentiator

$$f_b \quad \frac{1}{2R_1C_f}$$

T>R_f C_1=_____

VIVA-VOICE QUESTIONS:

1. What is differentiator?
2. In which condition an RC circuit acts as differentiator?
3. Define cut-off frequency of differentiator?
4. Compare differentiator and integrator?

EXPERIMENT.6

ACTIVE FILTERAPPLICATIONS-LPF, HPF [FIRSTORDER]

AIM:

To study Op-Amp as first order LPF and first order HPF and to obtain frequency response.

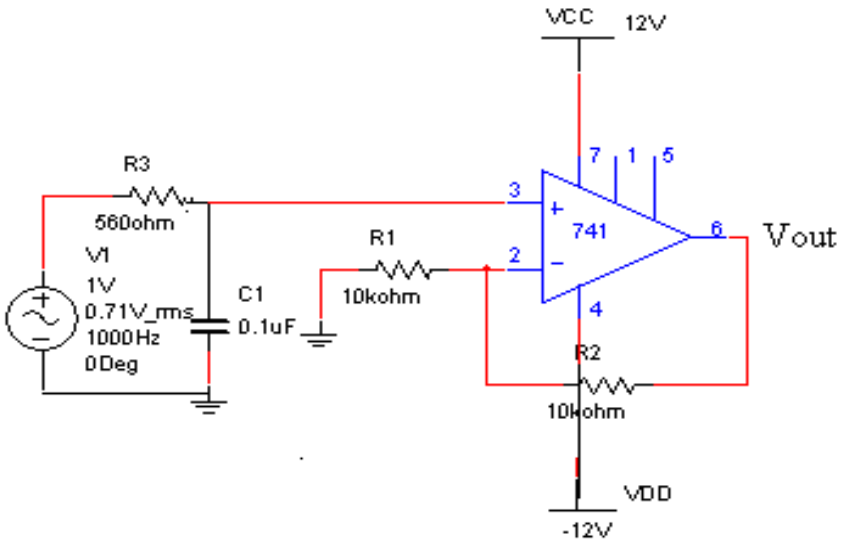
APPARATUS:

1. IC 741.
2. Resistors (10KΩ--2, 560Ω, 330Ω
3. Capacitors(0.1Ω)
4. Bread board trainer
5. CRO
6. Function generator
7. Connecting wires
8. Patch cards.

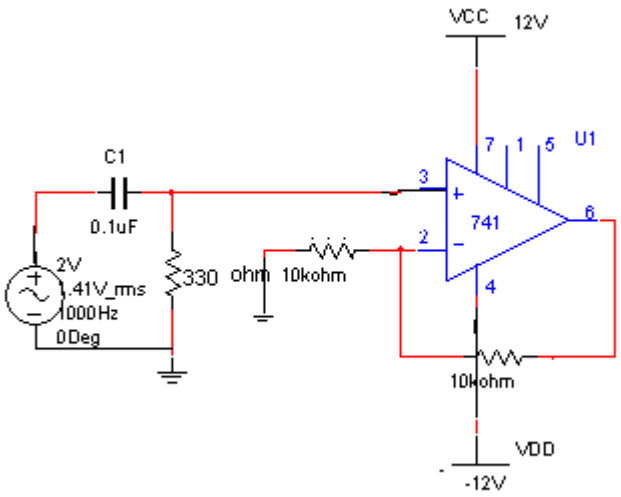
CIRCUIT

DIAGRAM: (a)

LPF



(a)HPF



THEORY: LOWPASS

FILTER:

The first order low pass butterworth filter uses an Rc network for filtering. The op-amp is used in then on inverting configuration, hence it does not load down the RC network. Resistor R1 and R2 determine the gain of the filter.

$V_0/Vin=A_f/(1+jf/f_h)$

$A_f=1+R_f/R_1$=pass band gain of filter .
F=frequency of the input signal.
$F_h= 1/2\Pi RC$ =High cutoff frequency of filter .
V0/Vin =Gain of the filter as a function of frequency

The gain magnitude and phase angle equations of the LPF the can be obtained by converting V0/Vin into its equivalent polar form as follows

$|V_0/Vin|=A_f/(\sqrt{1+(f/f_l)^2})$

$\Phi = - \tan^{-1}(f/f_h)$

WhereΦisthephaseangleindegrees.TheoperationoftheLPFcanbeverified

from the gain magnitude equation.

1. At very low frequencies i.e $f<f_h$, $|V_0/Vin|=A_f$.
2. At $f=f_h$, $|V0/Vin|=A_f/\sqrt{2}$.
3. At $f>f_h$, $|V0/Vin|<A_f$.

HIGH PASS FILTER:

High pass filters are often formed simply by interchanging frequency. Determining resistors and capacitors in LPFs that is, a firstorder HPF is formed froma firstorderLPFbyinterchangingcomponents'R'and'C'figure.Showsafirstorder butterworth HpF with a lower cutoff frequency of 'Fl'. This is the frequency at which magnitude of the gain is 0.707times its pass band value. Obviously all frequencies, with the highest frequency determinate by the closed loop band width of op-amp.

For the first order HPF ,the output voltage is

$$V0 =[1+ R_f/R_1]\ j2\Pi RCVin/(1- j2\Pi fRC)$$

$$V_0/Vin=A_f[j(f/f_l)/(1=j(f/f_l)]$$

Where A_f+ R_f/R_1a pass band gain of the filter.

F=frequency of input signal.
$F_l=1/2\Pi RC$ = lower cutt off frequency
Hence, the magnitude of the voltage gain is

$$|V_0/Vin|=A_f(f/f_l)/\sqrt{1+(f/f1)^2}.$$

Since, HPFs are formed from LPFs simply by interchanging R'sandC's. The design and frequency scaling procedures of the LPFs are also applicable to HPFs.

PROCEDURE:

1. Connections are made as per the circuit diagram.
2. Apply sine wave of amplitude $4V_{p-p}$ to the non inverting input terminal.
3. Values the input signal frequency.
4. Note down the corresponding output voltage.
5. Calculate gain in db.
6. Tabulate the values.
7. Plot a graph between frequency and gain.
8. Identify stop band and pass band from the graph.

OBSERVATIONS:

Low Pass Filter

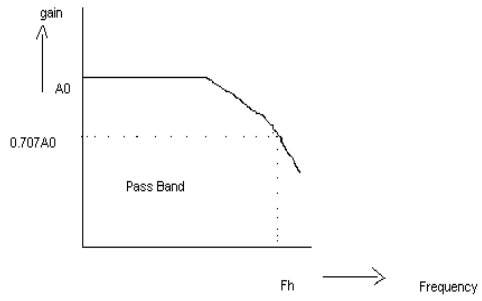
Frequency(Hz)	V0(V)	Gain in db= 20log(V0/Vi)

High Pass Filter

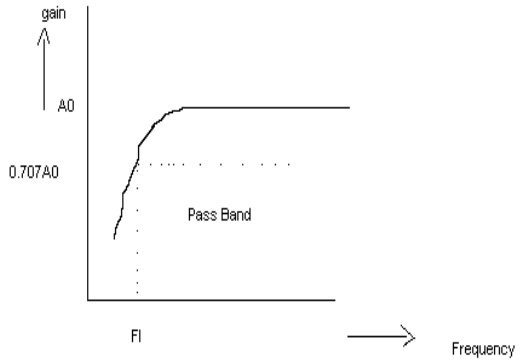
Frequency(Hz)	V0(V)	Gain in db= 20log(V0/Vi)

MODEL GRAPH:

High Pass Filter



Low Pass Filter



PRECAUTIONS:

1. Make null adjustment before applying the input signal.
2. Maintain proper Vcc levels.

RESULT: Performed filter operation of op-amp 741 and plotted the graph.

VIVA-VOICE QUESTIONS:

1. What is a filter circuit?
2. Classify various filters?
3. Calculate the cut-off frequency of low pass filter.
4. What is 3db frequency.

EXPERIMENT.7

WAVEFORM GENERATOR USING OP AMP 741

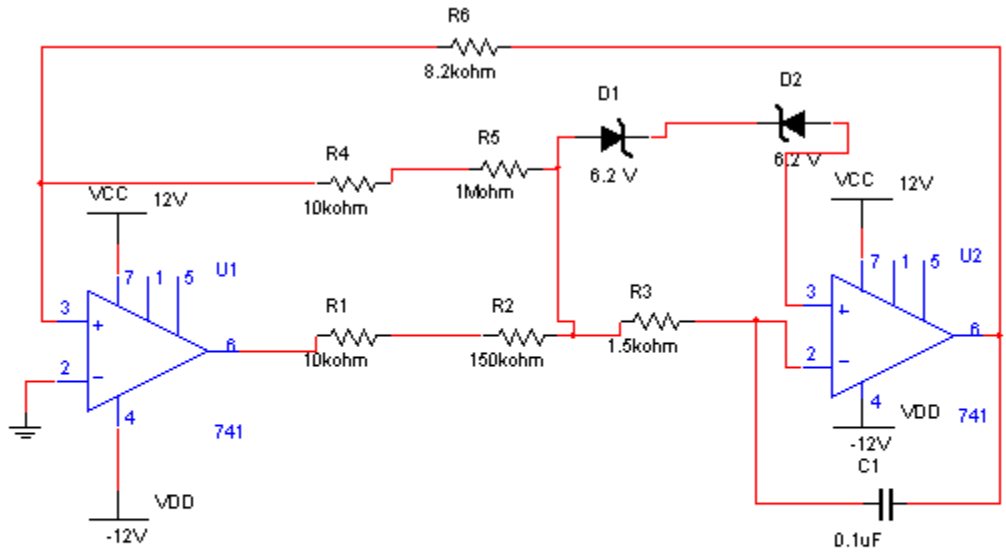
AIM:

To generate triangular and square waveforms and to determine the time period Of the waveforms.

APPARATUS:

1. Op-Amp IC 741 –2 Nos
2. Bread board IC trainer
3. Capacitor 0.1µF
4. Zener diodes (6.2V)—2 Nos
5. Resistors—10KΩ, 150KΩ1.5KΩ, 1MΩ, 8.2KΩCRO
6. Patch cards
7. Connecting wires

CIRCUIT DIAGRAM:



THEORY:

The function generator consists of a comparator U1and an integrator A2.The comparator U2 compares the voltage at point P continuously with the inverting input i.e., atzerovolts.WhenvoltageatPgoesslightlybeloworabovezerovolts,theoutputof U1 is at the negative or positive saturation level, respectively.

To illustrate the circuit operation let us set the output of U1at positive saturation +Vsat(approximately +Vcc). This +Vsat is an input to the integrator U2.Theoutputof U2 ,therefore will be a negative going ramp. Thus, one end of the voltage divider R2-R3 is the positive saturation voltage +Vast of U1 and the other is the negative going ramp ofU2. When the negative going ramp attains a certain value–Vramp, point p is slightly below zero volts; hence the output of U1 will switch from positive saturation to negative saturation–Vsat (approximately–Vcc). This means that the output of U2 will now stop going negatively and will begin to go positively. The output of U2 will continue to increase until it reaches +Vramp. At this time the point P is slightly above zero volts. The sequence then repeats. The frequencies of the square are a function of the d.c supply voltage. Desired amplitude can be obtained by using approximate zeners at the output ofU1.

THEORETICAL VALUES:

Time period, $T=4R_5C\ (R_3+R_4)/(R_1+R_2) =0.492$ msec.
Positive peak ramp = $Vz\ R_5/(R_1+R_2) =0.05$ volts.

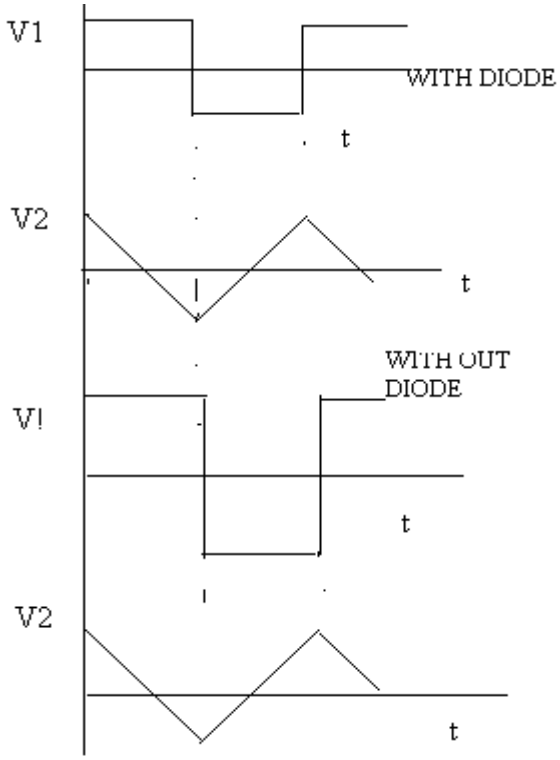
PRACTICAL VALUES:

Timeperiods of triangular wave= Time
periods of square wave= Positive peak
ramp=
Voltage of square wave=

PROCEDURE:

1. The circuit is connected as shown in the figure.
2. The output of the comparator U1 is connected to the CRO through chennal1,to generate a square wave.
3. The output of the comparator U2 is connected to the CRO through chennal2, to generate a triangular wave.
4. The time periods of the square wave and triangular waves are noted and they are found to be equal.

MODEL GRAPH:



PRECAUTIONS:

1. Make null adjustment before applying the input signal.
2. Maintain proper Vcc levels.

RESULT: Generated and plotted sine, square and triangular waveforms using op-amp.

VIVA-VOICE QUESTIONS:

1. **What are basic waveforms available?**
2. **Define sine wave?**
3. **Calculate the time period of square wave?**

EXPERIMENT.7

IC 555 TIMER-MONOSTABLE CIRCUIT

AIM:

To construct and study the operation of a monostable multivibrator using555IC timer.

APPARATUS:

1. 555 IC timer
2. Capacitors (0.1µF,0.01µF)
3. Resistors 10KΩ
4. Bread board IC trainer
5. CRO
6. Connecting wires and Patch cards

THEORY:

Monostable multivibrator is also known as triangular wave generator. It has one stable and one quasi stable state. The circuit is useful for generating single output pulse of time duration in response to a triggering signal. The width of the output pulse depends only on external components connected to the op-amp. The diode gives a negative triggering pulse. When the output is +Vsat, a diode clamps the capacitor voltage to 0.7V. then, a negative going triggering impulse magnitude Vi passing through RC and the negative triggering pulse is applied to the positive terminal.

Let us assume that the circuit is in stable state. The output V0 is at +Vsat. The diode D1conducts and Vc the voltage across the capacitor 'C' gets clamped to 0.7V .the voltage at the positive input terminal through R1 R2 potentiometer divider is +ß Vsat. Now, if a negative trigger of magnitude Vi is applied to the positive terminal so that the effective signal is less than 0.7V. the output of the Op-Amp will switch from +Vsat to– Vsat. The diode will now get reverse biased and the capacitor starts charging exponentially to–Vsat. When the capacitor charge Vc becomes slightly more negative than –ß Vsat, the output of the op-amp switches back to +Vsat. The capacitor 'C' now starts charging to +Vsat through R until Vc is 0.7V.

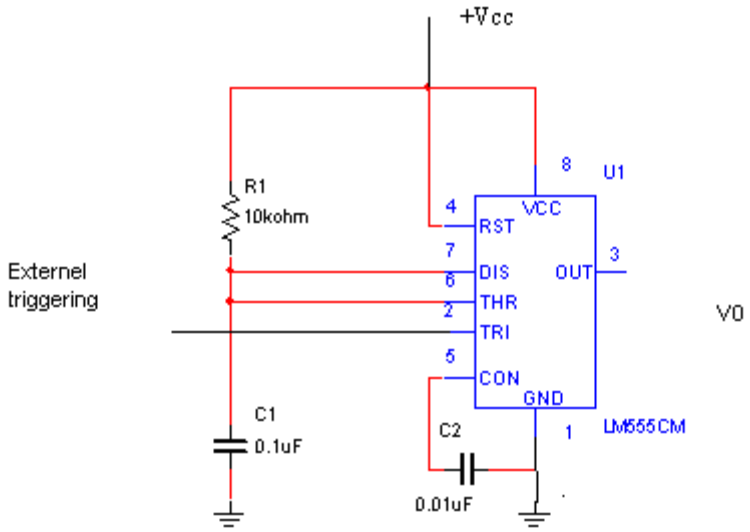
$$V_0 = V_f + (V_i - V_f)\, e^{-t/RC}.$$

$$ß = R_2/(R_1+R_2)$$

If $V_{sat} >> V_p$ and $R_1 = R_2$ and ß=0.5,

Then, T=0.69RC.

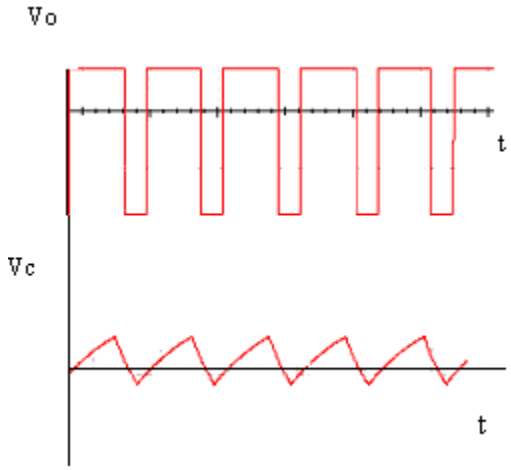
CIRCUIT DIAGRAM:



PROCEDURE:

1. Connections are made as per the circuit diagram.
2. Negative triggering is applied at the terminal 2.
3. The output voltage is measured by connecting the channel-1 at pin3.
4. Theoutputvoltageacrosscapacitorismeasuredbyconnectingthechannel-2at the point 'P'.
5. Theoretically the time period is calculated by $T=1.1R_1C_1$ where R_1 =10KΩ C_1=0.1μF.
6. Practically the charging and discharging timers are measured and theoretical Value of time period is measured with practical value

MODELGRAPH:



PRECAUTIONS:

1. Make the null adjustment before applying the input signal.
2. Maintain proper Vcc levels.

RESULT: Studied the operation of Monostable multivibrator using 555 timers.

VIVA-VOICE QUESTIONS:

1. What is multivibrator?
2. How the 555 given to the circuit.
3. What are the applications of Monostable multivibrator?
4. What is the pulse width of Monostable multivibrator?

EXPERIMENT.9

IC 555 TIMER-ASTABLECIRCUIT

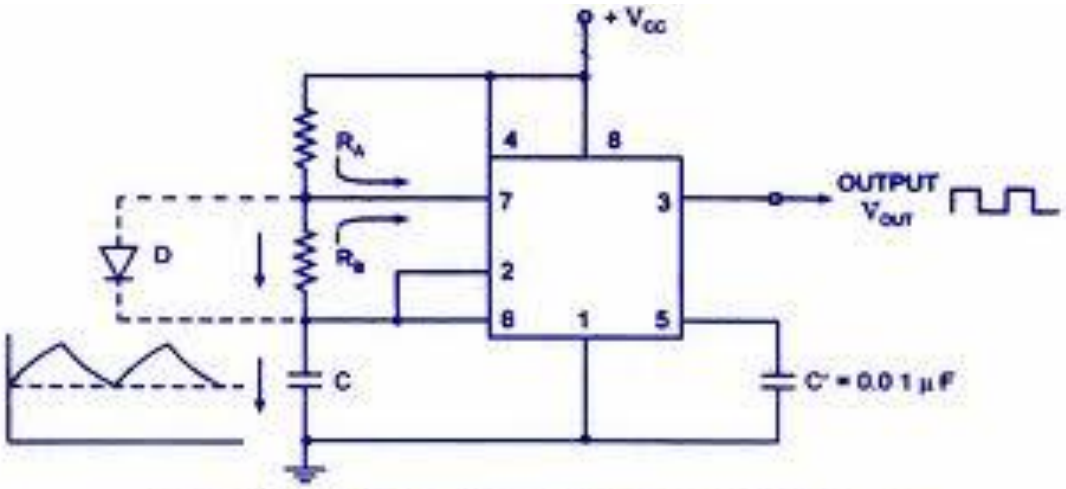
AIM:

To construct and study the operation of A stable multivibrator using 555 timer

APPARATUS:

1. IC 555 Timer
2. Resistors (10 KΩ,4.7 KΩ)
3. Diode (IN 4007)
4. Capacitors (0.1µF,0.01µF)
5. CRO
6. Patch cards
7. CRO Probes
8. Connecting wires

CIRCUIT DIAGRAM:



Circuit of The Timer 555 as an Astable Multivibrator

THEORY:

A simple OPAMP a stable multivibrator is also called square wave generator and free running oscillator .The principle for the generation of square wave output is to force an OP_AMP to operate in the saturation region β=R2/(R1+R2) of the output is feedback to input. The output is also feedback to the negative input terminal after integrating by means of a RCLPF whenever the negative input just exceeds Vref, switching takes place resulting in a square wave output. In a stable multivibrator both states are quasi stable states.

When the output is +Vsat, the capacitor is now starts charging towards +Vsat through resistance R the voltage is held at +βVsat. This condition continuous until the charge on C just exceed Vsat. Then the capacitor begins to dis charge towards– Vsat. Then the capacitor charges more and more negatively until its voltage just– βVsat. The frequency is determined by the time it takes the capacitor to charge from– β Vsat and +β Vsat

$$Vc(t)= Vf+(Vi-Vf)e^{-t/RC}$$

$$Vc(t)= Vsat-Vsat(1+\beta)e^{-t/RC}$$

We get $T1=RC \ln((1+\beta)/(1-\beta))$

$T=2T1=2 RC \ln ((1+\beta)/(1-\beta)), Vo(p-p)=2Vsat$

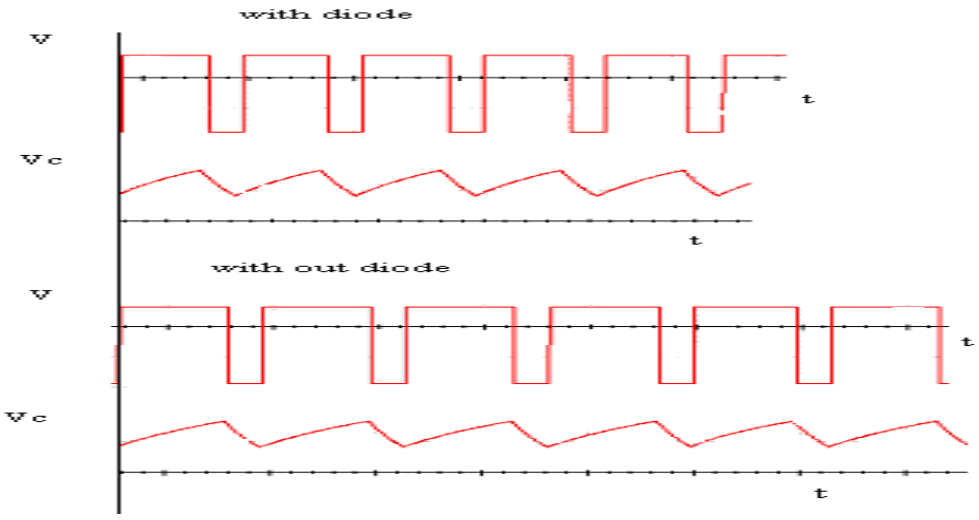
PROCEDURE:

1. Connections are made as per the circuit diagram.
2. Pins 4 and 8 are shorted and connected to power supply Vcc (+5V)
3. Between pins 8 and 7 resistor R1 of10KΩ is connected and between 7 and 6 resistor R2 of 4.7KΩ is connected. Pins 2 and 6 short circuited.
4. In between pins 1 and 5 a Capacitor of0.01μF is connected.
5. The out put is connected across the pin 3 and GND.
6. In between pins 6 and GND a Capacitor of 0.1μF is connected.
7. Theoretically with out diode charging time Tc is given by
   Tc=0.69(R1+R2) C1,
   Discharging time Td is given by Td=0.69R2C1
   The frequency f is given by f=1.45/ (R1+2R2)C1
   %of Duty cycle is (Tc/ (Tc+Td))*100.
8. Practically Td and Tc are measured and wave forms are noted and theoretical Values are verified with practical values
9. Connect diode between pins 7 and 2.
10. Theoretically with diode connected charging time is given by Tc=0.69R1C1 Discharging time is given by Td=0.69R2C1
11. Practically Td and Tc are noted and verified with theoretical values

OBSERVATIONS:

With diode		without diode	
Theoretical	Practical	Theoretical	Practical

MODEL GRAPH:



PRECAUTIONS:

1.Make null adjustment before applying the input signal.
2.Maintain proper Vcc levels.

RESULT: Studied the operation of Monostable multivibrator using 555 timers.

VIVA-VOICE QUESTIONS:

1. What is an astable multivibrator?
2. How the 555 circuit acts as an astable multivibrator?
3. What are the applications of astable multivibrator?
4. What is the pulse width of astable multivibrator?

EXPERIMENT.10

SCHMIT TRIGGER USING IC 741

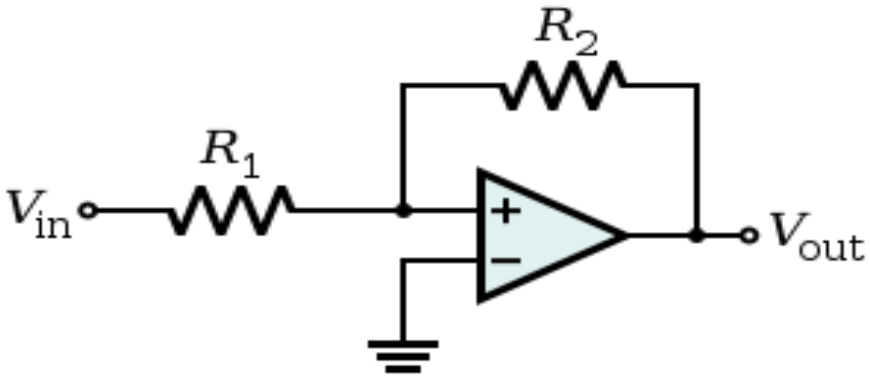
Aim:

To construct the Schmitt trigger using Ic 741

Apparatus:

5. 741 IC
6. Function Generator
7. Bread board
8. Resistors
9. Power supply
10. Connection wire

Circuit Diagram



PROCEDURE:

1.Connect the circuit as shown in the figure.
2.Apply the input sine wave at pin number 2 of IC 741.
3.Observe the square wave output at pin 6
4.Measure UTP and LTP and compare them with theoretical values.

PRECAUTIONS:

1.Loose connections should be avoided.
2.Switch on the supply after verification of the circuit
3.Waveforms and readings should be taken with out parrellax error.

RESULT: Hence designed and conducted experiment on 555 timer as a schmitttrigger.

VIVA-VOICE QUESTIONS:

1. What is schmitttrigger?
2. How it convets sine wave into rectangular?
3. Wgat is hysterisis?

EXPERIMENT.9

IC 565 PLL

AIM:

1. To study the operation of NE565 PLL
2. To use NE565 as a multiplier

EQUIPMENTSANDCOMPONENTS:

APPARATUS		
1. DC power supply	-	1 No.
2. CRO	-	1 No.
3. Bread Board	-	1 No.
4. Function	-	1 No.

COMPONENTS:

1. 6.8 kΩ Resistor– 1 No.
2. 0.1 F Capacitor– 1 No
5. 0.001 F Capacitor– 2 Nos
6. IC565 - 1 No.

THEORY:

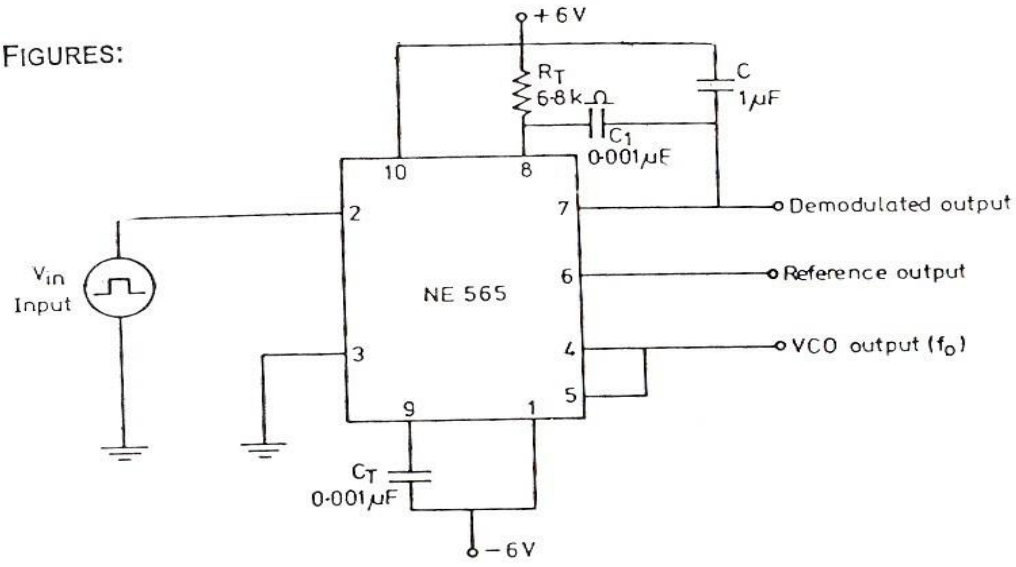
The 565 is available as a14-pin DI P package. It is produced by sign at c corporation. The output frequency of the VCO can be re written as

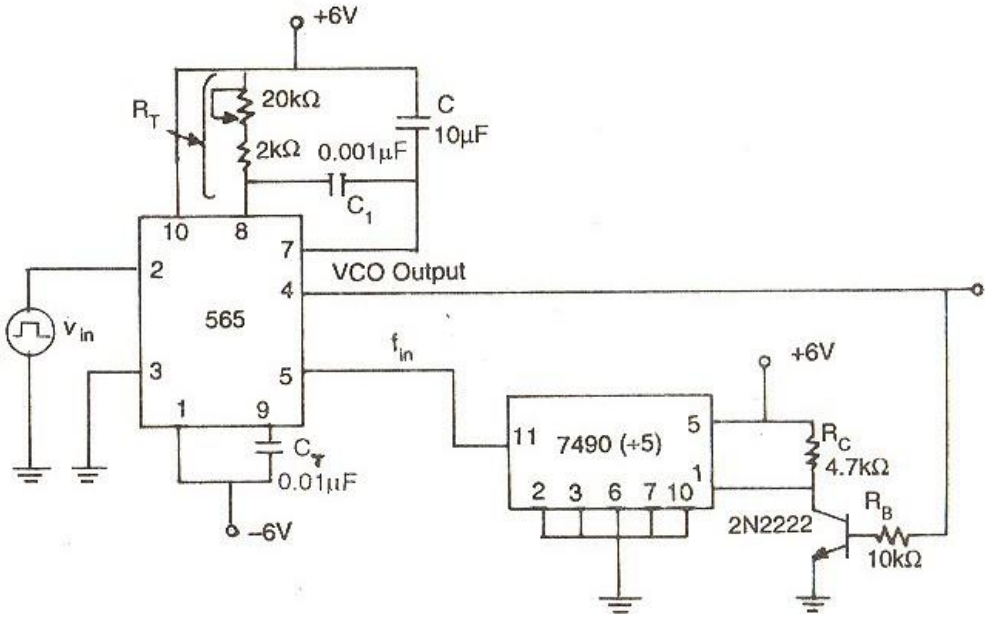
$$f_o \quad \frac{0.25}{R_T C_T} \quad Hz$$

Where R_T and C_T are the external resistor and capacitor connected to pin8 and pin9. A value between 2k and 20k is recommended for R_T.The VCO free running frequency is adjusted with $R_T$and C_T to be at the centre for the input frequency range.

CIRCUITDIAGRAM:

FIGURES:





PROCEDURE:

i. Connect the circuit using the component values as shown in the figure

ii .Measure the free running frequency of VCO at pin4 with the input signal V_{in}set=zero. Compare it with the calculated value=$0.25/R_TC_T$

iii. Now apply the input signal of 1Vpp squarewaveata1kHz topin2

iv. Connect1 channel of the scope to pin2 and display this signal on the scope.

v . Gradually increase the input frequency till the PLL is locked to the input frequency. This frequency f_1 gives the lower ends of the capture range. Go on increase the input frequency, till PLL tracks the input signal, say to a frequency f_2.This frequency f_2 gives the upper end of the lock range. If the input frequency is increased further the loop will get unlocked.

vi. Now gradually decrease the input frequency till the PLL is a gain locked. This is the frequency f_3, the upper end of the capture range .Keep on decreasing the input frequency until the loop is unlocked. This frequency f_4 gives the lower end of the lock range

vii. The lock range $f_L=(f_2- f_4)$ compare it with the calculated value of $\frac{7.8fo}{12}$

Also the capture range is $f_c=(f_3- f_1)$. Compare it with the calculated value of capture range.

$$f_c = \frac{f_L}{(2\pi)(3.6)(10^3)xC}$$

viii. To use PLL as a multiplie5r,makeconnectionsas show in fig. The circuit uses a 4-bitbinarycounter7490 usedasadivide-by-5circuit.

ix.Settheinputsignalat1Vpp squarewaveat500Hz

x..Vary the VCO frequencybyadjustingthe20KpotentiometertillthePLLis locked. Measure the output frequency

xi. Repeatstep9 and10 for input frequency of 1kHzand1.5kHz.

OBSERVATIONS:

fo = _____

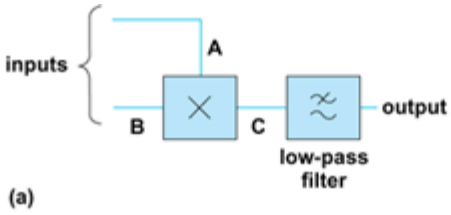
f_L=_____

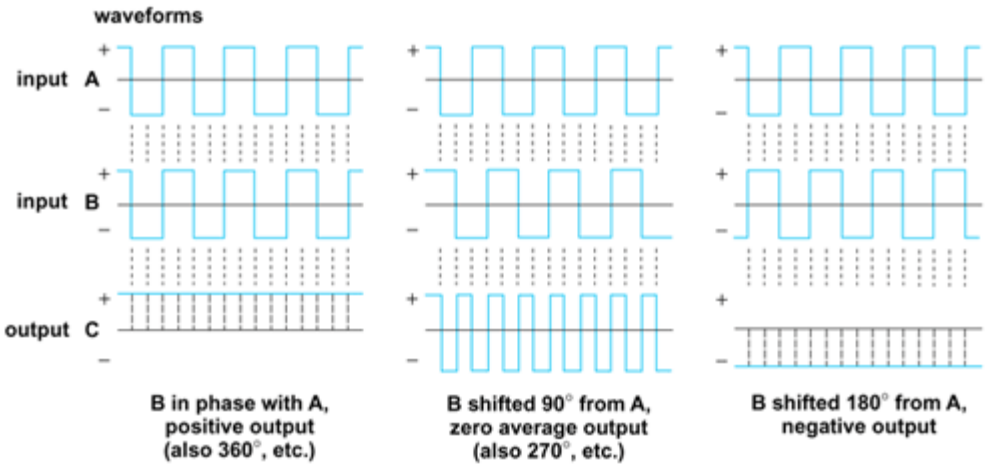
f_C=_____

CALCULATIONS:

$$f_L=(f_2- f_4) = \frac{7.8fo}{12}$$

$$f_c=(f_3- f_1) = \frac{f_L}{(2\pi)(3.6)(10^3)xC}$$





RESULT: Hence observed the characteristics of PLL IC 565.

fo=_____

fL=_____

fC=_____

VIVA-VOICE QUESTIONS:

1. Define lock range?
2. Define capture range?
3. What are the applications of PLL.

12. VOLTAGE REGULATORUSING IC 723

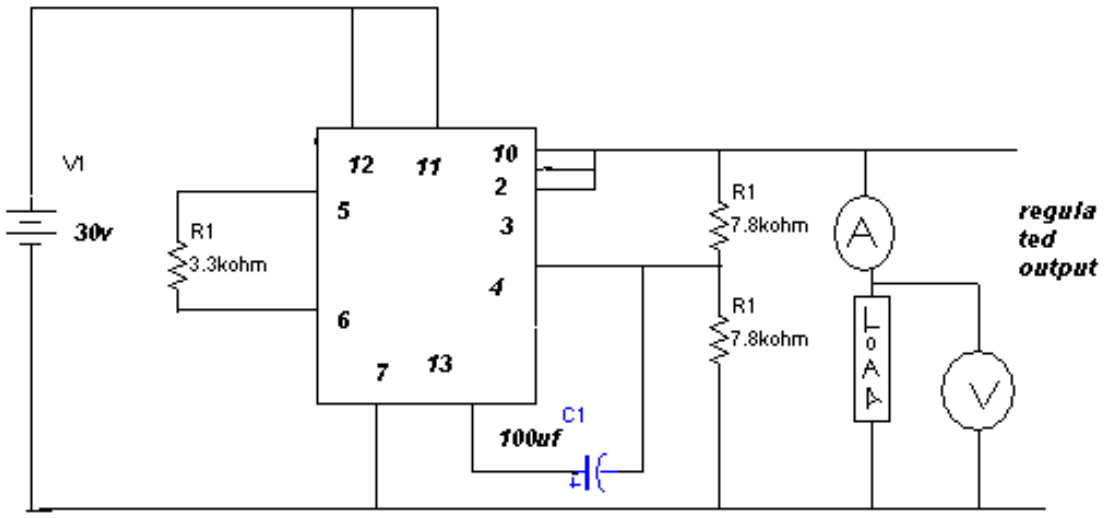
AIM:

To plot the regulation characteristics of the given IC LM 723.

APPARATUS:

1. Bread board
2. IC LM 723
3. Resistors(7.8KΩ ,3.9KΩ)
4. RPS
5. DRB
6. Capacitors 100µF
7. Patch cards
8. Connecting wires

CIRCUIT DIAGRAM:



THEORY:

A voltage regulator is a circuit that supplies constant voltage regardless of changes in load currents. Except for the switching regulators, all other types of regulators are called line arregulators.ICLM723is general purpose regulator. The input voltage ofthis 723ICi s40V maximum. Output voltage adjustable from 2Vto30
V. 150mA output current external pass transistor. Output currents in excess of 10Amperepossiblebyaddingexternaltransistors.Itcan be used as either a linear or a switching regulator. The variation of DC output voltage as a function of DC load current is called regulation.

% Regulation = [(Vnl-Vfl)/Vfl]*100

PROCEDURE:

(1).LINE REGULATION

1. Connections are made as per the circuit diagram
2 .Power supply is connected to12 and 7 terminals
3. Volt meter is connected to10 and 7 terminals
4. By increasing the input voltage corresponding volt meter reading is noted.

(2).LOAD REGULATION

1. Connect the load to the terminals 10 and GND.
2. Keep the input voltage constant at which line regulation is obtained
3. The maximum load value is calculated from IC ratings.
4. Now, we decrease the load resistance and note down the corresponding value of the output in volt meter.
5. Plot the graph for load verses load regulation.

OBSERVATIONS:

(1).LINEREGULATION: Vnl=

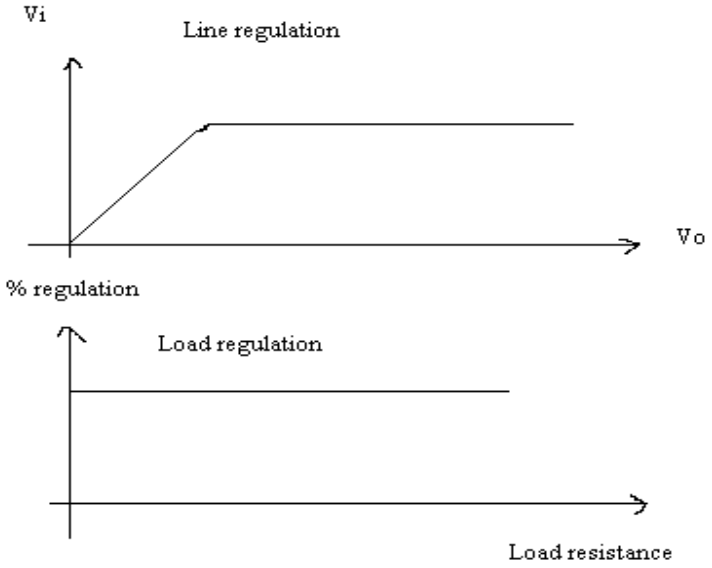
Line voltage (V)	Outputvoltage(V)

(2).LOAD REGULATION:

Regulated output(V)	Load current(mA)	Load resistance(KΩ)	Load regulation

% REGULATION=[(Vnl-Vfl)/Vfl]*100

MODEL GRAPH:



PRECAUTIONS:

1. While taking the readings of regulated output voltage load regulation ,keep the input voltage constant at15V.
2. Do not increase the input voltage more than 30 V while taking the reading for no load condition?

RESULT: Performed line and load regulation on 723 voltage regulator.

VIVA-VOICE QUESTIONS:

1. Define line regulation?
2. Define load regulation?
3. What are the applications of voltage regulators?

13.Three Terminal Voltage Regulators (7805, 7809 And 7912)

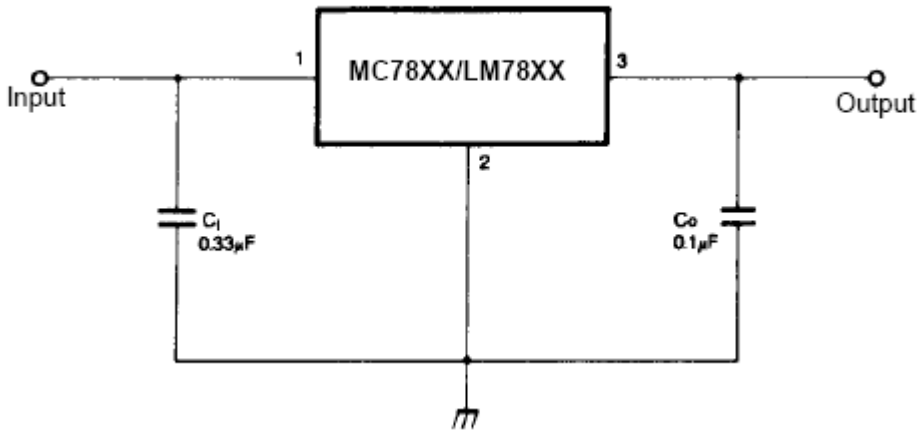
AIM:

To verify the operation of three terminal fixed voltage regulators 7805, 7809, 7912 and also to find out their line and load regulation.

APPARATUS:

S.No.	Name of the component	Range	Quantity
1.	7805	--	1
2.	7809	--	1
3.	7912	--	1
4.	Capacitors	0.33µf 0.1µf	1 1
5.	Multimeter	(0-30)v	1
6.	Power Supply		1

CIRCUIT DIAGRAM:



THEORY:

Three terminal voltage regulators have three terminals which are unregulated input (V_{in}), regulated output (V_o) and common or a ground terminal. These regulators do not require any feedback connections.

Positive voltage regulators:

78xx is the series of three terminal positive voltage regulators in which xx indicate the output voltage rating of the IC.

7805:

This is a three terminal regulator which gives a regulated output of +5V fixed. The maximum unregulated input voltage which can be applied to 7805 is 35V.

7809:

This is also three terminal fixed regulator which gives regulated voltage of +9V.

Negative voltage regulators:

79xx is the series of negative voltage regulators which gives a fixed negative voltage as output according to the value of xx.

7912:

This is a negative three terminal voltage regulator which gives a output of -12V.

Line Regulation:

It is defined as the change in the output voltage for a given change in the input voltage. It is expressed as a percentage of output voltage or in millivolts.

$\%R_L = \Delta V_o/\Delta V_{in}$ x 100

Load Regulation:

It is the change in output voltage over a given range of load currents that is from full load to no load. It is usually expressed in millivolts or as a percentage of output voltage.

$$\%R_{Load} = [(V_{nl}-V_{fl})/V_{nl}] \times 100$$

PROCEDURE:

1. Connect the circuit as shown in the figure.
2. Apply unregulated voltage from 7.5V to 35V and observe the output voltage.
3. Calculate the line and load regulation for the regulator.
4. Plot the graphs from the observations.
5. Repeat the same for the remaining regulators.

RESULTS: Hence performed various regulation operations ICs 7805, 7809, 7912.

VIVA-VOICE QUESTIONS:

1. What are three terminal voltage regulators?
2. Give applications of three terminal regulators.