Experiment: Single-Phase Full-Bridge sinewave Inverter

Objective

The objective of this lab is to analyze the operating performance of the single-phase full-bridge inverter under sinusoidal PWM.

References

[1] David Gao, and Kai Sun, “DC-AC Inverters”, in “Electric Renewable Energy Systems”, pp. 354-381, 2016.

[2] A. E. Ross, "Theoretical Study of Pulse-Frequency Modulation," in Proceedings of the IRE, vol. 37, no. 11, pp. 1277-1286, Nov. 1949.

[3] S. R. Doradla, C. Nagamani and S. Sanyal, "A Sinusoidal Pulsewidth Modulated Three-Phase AC to DC Converter-Fed DC Motor Drive," in IEEE Transactions on Industry Applications, vol. IA-21, no. 6, pp. 1394-1408, Nov. 1985.

[4] N. Mohan, T. M. Undeland, W. P. Robbins, “Power Electronics: Converters, Applications, and Design”, 3rd Edition, Wiley.

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Introduction

The single-phase full-bridge inverter converts a fixed DC voltage into a controlled AC voltage. The topology of this converter shown in Fig. 1 (a). It consists of an input capacitor C and four switches (usually insulated-gate bipolar transistors (IGBT) or MOSFETS). When switches Q_1 and Q_4 are ON, the output voltage will be equal to V_d and when switches Q_3 and Q_2 are ON, the output voltage will be equal to $-V_{dc}$. If the switches are turned on and off at a fundamental frequency, e.g., 60 Hz, an AC output voltage with a fundamental frequency of 60 Hz will be produced at the output terminals of the inverter. This method called the square-wave pulse-width modulation (PWM). A sample output voltage waveform is shown in Fig. 1 (b). The converter output is connected to an RL load. Hence, the output current will be exponential in nature. When, the output voltage is positive, the current will rise and when its negative, the current will fall. It should be noted that whenever two switches turn OFF, their parallel diodes will conduct to de-energize the load inductance. This is done to avoid voltage jumps. In addition, the switches in one leg must not be turned on at the same time. Otherwise, the input DC source will be shorted.

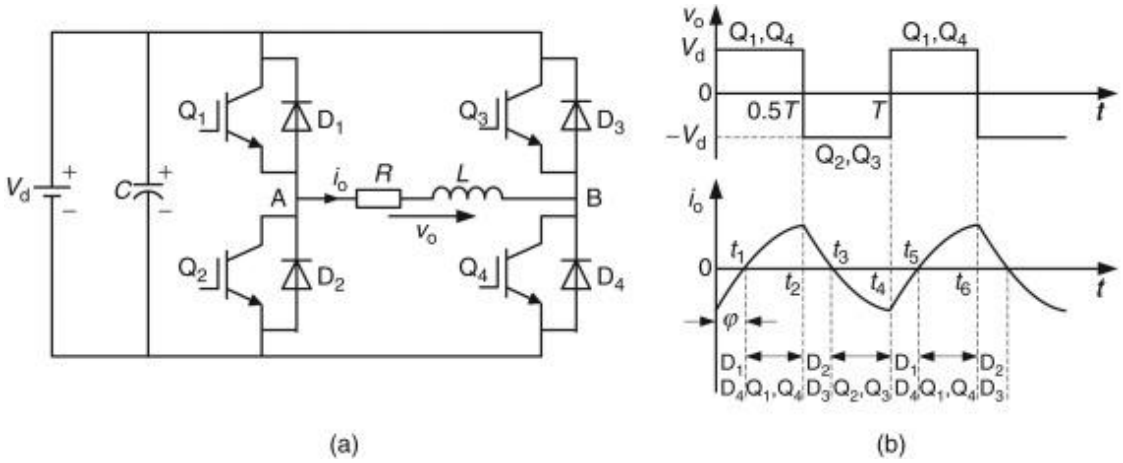

Fig. 1. (a) The full-bridge inverter and (b) sample output voltage and output current waveforms.

The main goal in design and control of inverters is to generate an output voltage with the lowest possible total harmonic distortion (THD). This is achieved through topology design, control design, or filter design. The most common way to achieve this goal is though control design. To analyze the quality of the output voltage waveform shown in Fig. 1 (b), Fourier series expansion is used. The waveform has quarter-wave symmetry. Hence, the cosine coefficients of the Fourier series expansion will be zero. Therefore, the Fourier series expansion is written as

$$v_o(\omega t) = \sum_{n=1,3,5,7,\ldots} \frac{4V_d}{n\pi} \sin(n\omega t)$$

By dividing the amplitude of all harmonics by the amplitude of the fundamental, the per-unitized Fourier series is as found as

$$v_o^{\,normalized}(\omega t) = \sum_{n=1,3,5,7,\ldots} \frac{1}{n} \sin(n\omega t)$$

The amplitude of each harmonic is inversely proportional to its order. Therefore, if the magnitude of the harmonics were to be plotted against their order, the plot would be the plot of the function $\frac{1}{n}$.

The frequency spectrum of the output voltage waveform is shown in Fig. 2. The harmonics decrease by a factor of $\frac{1}{n}$. The current spectrum will be closer to that of a sine wave. This is because an RL load acts as a low-pass filter.

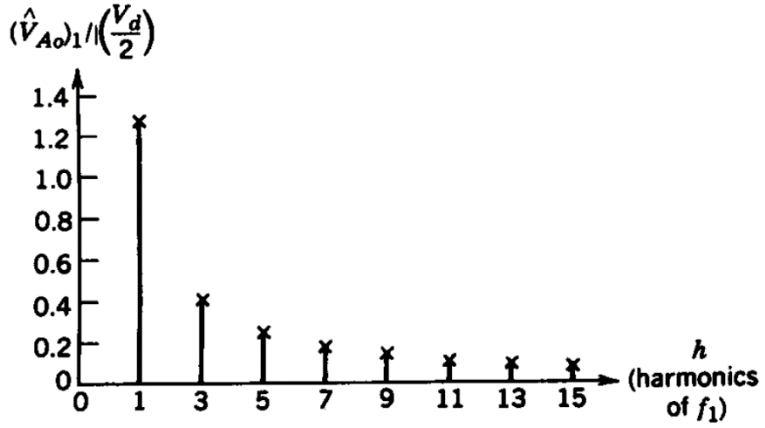

Fig. 2. Harmonic spectrum of Vo.

The harmonic performance of the output voltage cannot be controlled by using square-wave modulation. The low order harmonics are very significant, and this means that the output voltage is far away from the desired quality. In addition, this will increase the size of the filter which will also increase the size and cost of the inverter.

To overcome the disadvantages of the square-wave PWM, another modulation technique is used for controlling the full-bridge inverter. This method, which called the sinusoidal PWM, will enable the control of the AC output voltage and improve the harmonic performance of the inverter. However, it should be noted that this method increases the switching frequency of the inverter and increases its internal losses.

The sinusoidal PWM compares a triangular or sawtooth waveform v_{tri} which varies from -1 to +1 with a sine wave $v_{control}$. The triangular/sawtooth waveform is called the carrier waveform while the sine wave is called the reference waveform. The two waveforms shown in Fig. 3 (a). Whenever $v_{control} > v_{tri}$, the output voltage will be set to V_d. Contrarily, the output voltage will be set to $-V_d$ when $v_{control} < v_{tri}$. The resulting output voltage waveform v_o along with its fundamental harmonic are shown in Fig. 3 (b). The frequency of v_{tri} will be equal to the switching frequency f_s. The modulation index for this method is defined as

$$m_a = \frac{\hat{v}_{control}}{\hat{v}_{triangle}} = \hat{v}_{control}$$

The frequency modulation ratio defined as

$$m_f = \frac{f_s}{f_r}$$

Where f_r is the frequency of $v_{control}$ which is equal to the fundamental frequency of the output voltage.

The fundamental component of the output voltage can be controlled through controlling m_a. The relationship between the fundamental harmonic and m_a is defined as

$$\hat{V}_{o,1} = m_a \frac{V_d}{2}$$

Therefore, the maximum output voltage that can be generated by this modulation technique is $\frac{V_d}{2}$.

The frequency components of the output voltage are dependent on both m_a and m_f. As m_f increases, the harmonic spectrum of the output voltage improves. However, after a specific m_f, the amplitude of the harmonics becomes independent of m_f. Varying m_a controls the fundamental harmonic. However, if losses are neglected, the energy supplied by the DC bus is always equal to the energy consumed by the AC side. Therefore, the amplitude of the significant harmonics will also change with m_a.

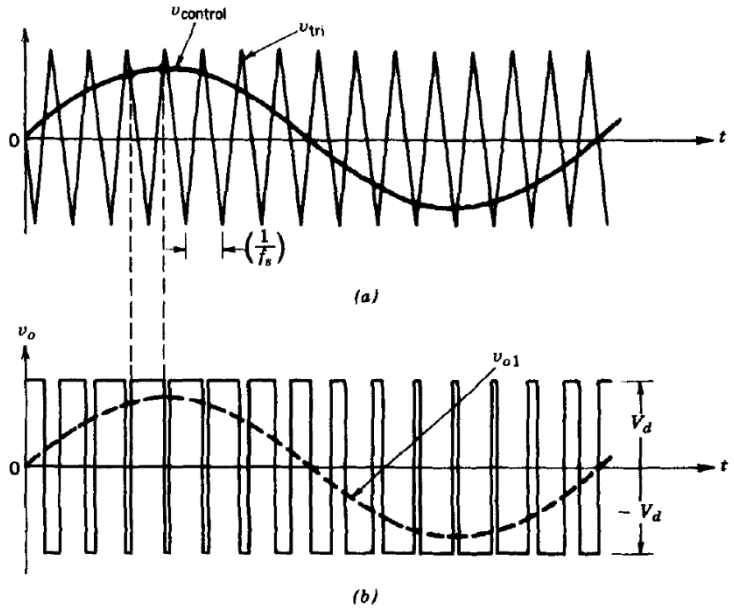

Fig. 3. (a) Sinusoidal PWM reference and carrier waveforms and (b) resulting output voltage.

A sample frequency spectrum for the sinusoidal PWM is shown in Fig. 4. The significant harmonics are centered around multiples of m_f and their sidebands. For frequency modulation ratios of $m_f \leq 9$, the harmonic amplitudes are almost independent of m_f. This is usually the case except for very high-power applications. Theoretically, the significant harmonics occur at

$$f_h = \left(jm_f \pm k \right) f_1$$

In other words, the harmonic order h corresponds to the k[th] sideband of j times the frequency modulation ratio m_f. For odd values of j, the harmonics exist only for even values of k. For even values of j, the harmonics exist only for odd values of k.

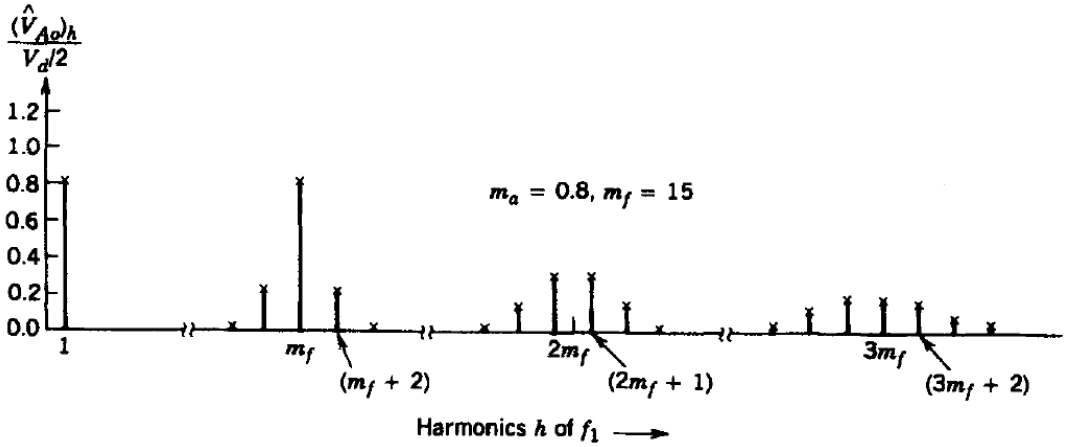

Fig. 4. Harmonic spectrum of Vo for sinusoidal PWM.

The normalized harmonics for $m_f > 9$ are summarized in Table. 1. It should be noted that m_f should be an odd integer. This will result in odd- and half-wave symmetries in the output voltage. Therefore, only odd harmonics will be present, and the even harmonics will be zero. In addition, the sine coefficients will be finite while cosine coefficients will be zero.

Table. 1. Harmonic amplitudes for sinusoidal PWM with $m_f > 9$.

h \ m_a	0.2	0.4	0.6	0.8	1.0
1 Fundamental	0.2	0.4	0.6	0.8	1.0
m_f	1.242	1.15	1.006	0.818	0.601
$m_f \pm 2$	0.016	0.061	0.131	0.220	0.318
$m_f \pm 4$					0.018
$2m_f \pm 1$	0.190	0.326	0.370	0.314	0.181
$2m_f \pm 3$		0.024	0.071	0.139	0.212
$2m_f \pm 5$				0.013	0.033
$3m_f$	0.335	0.123	0.083	0.171	0.113
$3m_f \pm 2$	0.044	0.139	0.203	0.176	0.062
$3m_f \pm 4$		0.012	0.047	0.104	0.157
$3m_f \pm 6$				0.016	0.044
$4m_f \pm 1$	0.163	0.157	0.008	0.105	0.068
$4m_f \pm 3$	0.012	0.070	0.132	0.115	0.009
$4m_f \pm 5$			0.034	0.084	0.119
$4m_f \pm 7$				0.017	0.050

Note: $(\hat{V}_{AO})_h/\frac{1}{2}V_d$ [$= (\hat{V}_{AN})_h/\frac{1}{2}V_d$] is tabulated as a function of m_a.

The switching frequency of the inverter should be as high as possible to achieve optimum harmonic performance. However, higher switching frequency will increase the switching losses of the inverter. In most applications, the switching frequency is selected to be either less than 6 kHz or greater than 20 kHz.

For small frequency modulation ratios, the control and triangular waveforms should be synchronized to each other. This means that the frequency modulation ratio must be an odd integer. For large values of the frequency modulation ratio, the control and triangular waveforms can be asynchronous. In this method, the frequency of the triangular waveform is kept constant while the frequency of the control waveform varies.

It is possible to increase the modulation index beyond 1. In this case, the output voltage will increase beyond $\frac{V_d}{2}$. However, it should be noted that the output voltage will no longer vary linearly with m_a. In addition, the output voltage will go into saturation after a specific point. The sinusoidal PWM will turn into square-wave modulation after a specific m_a. This means that the

control and triangular waveforms no longer intersect each other. This phenomenon demonstrated by the graph in Fig. 5.

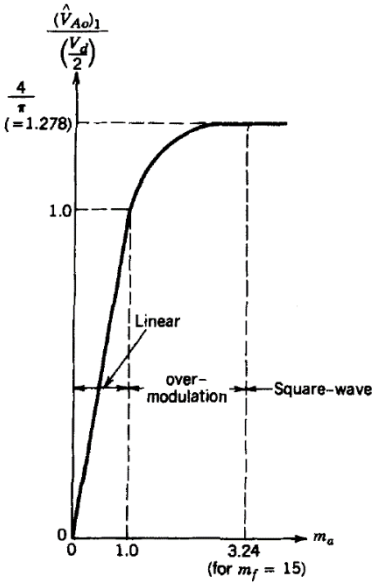

Fig. 5. Fundamental harmonic versus m_a for sinusoidal PWM.

Suggested Procedure

I. Simulation

Build the circuit shown in Fig. 6 using LTSPICE and the function generate Channel 1 for the Sinewave signal source. Channel 2 for the triangle wave carrier source The output of the comparator and MOSFET inverter M5 for gate drive signal sources. The full-bridge inverter is supplied by a +10Vdc source. There are four MOSFET transistors. Add 2N7000, TP0606, 1N4002, LM311 models to LTspice library as sub circuits. The four back EMF diodes are 1N4002 diodes. The output passes thought the lowpass filter to load resistance i1kΩ and inductance. The series 150Ω is the current limit resistor to prevent overloading the DC power source.

Output low pass filter is the series L1= 7mH, RL1 = 150Ω, Cload = 10uF The 150 also prevents the inrush current for overloading the DC source. The low pass filter is set above the input sinewave frequency Vsine and below the triangle wave ceria frequency. The filter is set pureleslt such that you can the ripple on the output. If you double the carrier frequency, you reduce the ripple voltage because it move higher into reject band.

Sinusoidal PWM signal controls the switching of the full-bridge inverter. A function generator sources the triangle waveform (Channel 2) of the function generator. Controls the frequency of carrier. Set this frequency to a multiply of the sine wave so it will be easier maintain a stable waveform on the scope. The function generator provides the input sinewave source (Channel 1) denoted by “Vsine”. The two waveforms are compared two each other and the resulting PWM sinewave gate control signals. The single MOSFET M5 inverts the gate drive for the other haft bridge. The output gating signals sent to the switches to control the bridge inverter. The reason behind using a dead-time controller is that the gating signals have rise and fall times. Therefore, during the turn-on or turn-off transition times of the gating signals, two switches on the same leg

will turn on at the same time. This will cause a short circuit on the DC supply side and damage the input DC source. This phenomenon called “shoot-through”. The Pmos and Nmos that we are using have ON resistance of 5Ω and hence the current is low enough not to damage the power supply or the devices. The ground reference for LTspice connected to the Vneg

LTspice requires that the **models** for 1N4002 diodes, 2N7000, TP0606, and LM311 added to the sub circuit library folder. Add the LM311.asy to the sys library folder.

The files are located on the class web site https://www.courses.ece.vt.edu/ece3354/

The files:

LM311.sub model sub circuit for LM311 comparator

1N4002.sub model sub circuit for 1N4002 rectifier diode

2N7000.sub model sub circuit for 2N7000 Nmos (M2, M4)

TP0606.sub model sub circuit TP0606 Pmos (M1, M3)

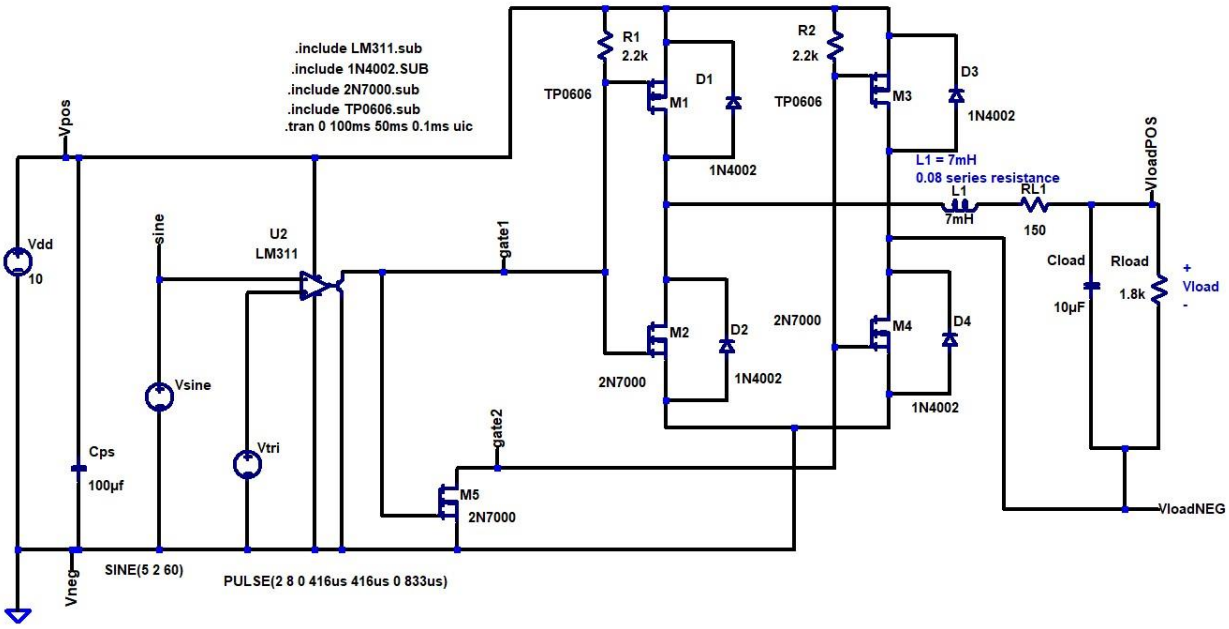

Fig. 6. Designed circuit for simulation in LTSPICE.

Built the circuit in Fig. 6 using LTSPICE. Run the simulation by setting the switching frequency to 1200Hz Use ground reference **voltage probe.** Plot the Triangle waveform and the control in sine waveform Provide the plots for the two gate signals.

Observe the output voltage signal “Vload” which is (Vload = VloadPOS - VloadNEG) use a **differential voltage probe**. (Plot the output voltage before the filter L1, Cload and after the filter Vload. VloadPOS with reference probe on VloadNEG.

For the LTspice simulation

Vsine = “Sine” 6.0Vpp offset 5Vdc at 60 Hz (Channel 1)

Vtri = “Pulse” set up as a triangle waveform 8.0V to 2.0V 50% duty cycle (Rise time = haft period, Fall time = half the period) at **1200Hz** (Channel 2)

Change the switching frequency of the triangle waveforms for the exipment

Vtri = “Pulse” set up as a triangle waveform 8.0V to 2.0V 50% duty cycle (Rise time = haft period, Fall time = half the period) at **2400Hz** (Channel 2)

Make the measurements at two different switching frequencies.

Triangle frequeny	Vout Vpp	Vout rippel Vpp	Sine input Vpp	Trangel input Vpp			

Experimental Verification

The designed circuit for hardware verification of the single-phase full-bridge inverter shown in Fig. 7. The input DC voltage is 10V. Connect an input capacitor to the DC source to filter the DC voltage and provide energy for the input side. Four MOSFET transistors (Two TP0606 PMOS and Two 2N7000 NMOS) switches used to build the inverter. Four 1N4002 diodes connected in parallel with the MOSFETS to provide a path for de-energization of the load inductances. An output LC filter used to filter out the fundamental harmonic of the output voltage. The LM311 comparetor is the modulation and control of the inverter.

Sinusoidal control waveform (**channel 1**) Vsine = 8Vpp offset 5Vdc at 60 Hz.The ramp voltage Triangle waveform Vramp = “Ramp” 8.5V to 1.5V, 50% duty cycle at 1200Hz (**Channel 2)** from the Function generator. An function generates the triangle waveform (Channel 2) of the function generator. Controls the switching frequency of carria if set this freqincy to a multiply of the sine wase it will beaser get a stable wave form on the scope Are compared for implementing sinusoidal PWM gate drive signal. Q5 the NMOS inverts the output of the comparator for the other gate drive signal. The output of the bridge is low pass filtered to remove the high frequency carrea and its harmonics.

Plot the voltages before and after the LC filter. Provide the plot for the Triangle waveform (channel 2) and the control sine waveform .Also, provide the plots for the two gate drive signals. **The inductor L1 with the 150Ω series resister is the primary L1P in series with the secondary L1S** of the transformer that the student wound for the previous labs. L1 is Primary 16T in series Secondary 16T yielding a total of 32T which will give an inductance of 7mH. The 150Ω resister added because of the low winding resistance and small inductive reactance, which will result in high input current, which will exceed the current capability of the student's power supplies.

Vsine = "Sine" 6.0Vpp offset 5Vdc at 60 Hz (Channel 1)

Vtri = "Ramp" 8.0V to 2.0V 50% duty cycle at **1200Hz** (Channel 2)

Change the switching frequency of the triangle waveformt ofthe exipment

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Triangle frequeny	Vout Vpp	Vout rippel Vpp	Sine input Vpp	Trangel input Vpp			

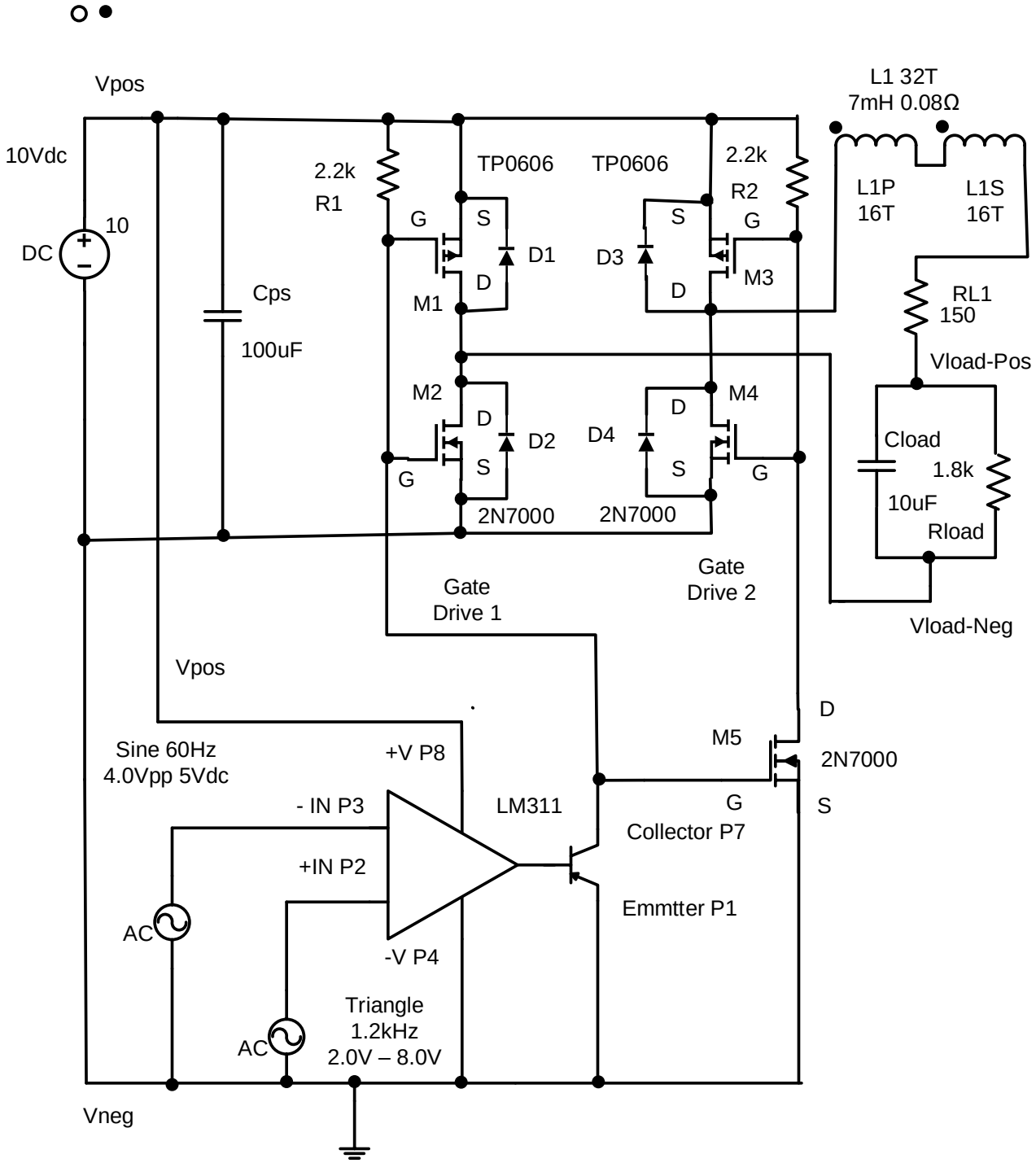

Fig. 7. Designed circuit for hardware testing.

D1, D2, D3, and D4 = 1N4002 or 1N4001.

L1 student wound transformer on toroid core 16-turn primary, 16-turn secondary wired in additive series to yield a **32-turn inductor**.

LM311 8 Pin DIP comparator.

M1, M3 = TP0606 PMOS transistor

M2, M4, M5 = 2N7000 NMOS transistor

Suggested Structure for Reports

You hand-written report must include

1. A brief analysis of the operation of a full-bridge inverter under sinusoidal PWM.

2. Plot of your simulation and experimental results and explain your observations.

3. must include schematics of your built circuit and LTspice schematic.

4 expline the effect of chaning the switch frequeny and why.