Extended Range ZVS Active-Clamped Current-Fed Full-Bridge Isolated Dc/Dc Converter for Fuel Cell Applications: Analysis, Design and Experimental Results

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***Abstract*— This paper presents analysis and design of zero-voltage switching (ZVS) active-clamped current-fed full-bridge isolated dc/dc converter for fuel cells applications. The designed converter maintains ZVS of all switches from full-load down to very light load condition over wide input voltage variation. Detailed operation, analysis, design, simulation and experimental results for the proposed design are presented. The additional auxiliary active clamping circuit absorbs the turn-off voltage spike limiting the peak voltage across the devices allowing the selection and use of low voltage devices with low on-state resistance. In addition, it also assists in achieving ZVS of semiconductor devices. The converter utilizes the energy stored in the transformer leakage inductance aided by its magnetizing inductance to maintain ZVS. ZVS range depends upon the design, in particular the ratio of leakage and magnetizing inductances of the transformer. Rectifier diodes operate with zero-current switching. An experimental converter prototype rated at 500W has been designed, built and tested in the laboratory to verify the analysis, design and performance for wide variations in input voltage and load.**

***Index Terms*— Fuel Cells, High-frequency DC/DC Converter, Zero voltage switching (ZVS), Renewable energy systems**

I. INTRODUCTION

CLEAN and green energy for distributed generation and modern/future transportation system has been of increasing interest to the academic and industrial researchers or community for sustainable and smart living. Power converter is an essential interface for the conversion of non-conventional energy sources into useful and regulated electrical ac or dc form. Power converter is a weak link and its efficiency determines the utilization of the source and controls the power output. Its cost, volume, and weight are the deciding factors for the overall cost and volume of the installation system. Therefore, the design and development of low cost, high-efficient and small size power conversion systems is still an attention of researchers [1-2]. Even though renewable energy sources like solar and wind energy are available free of cost, their output is not secure due to their intermittent nature. Fuel cells output is secure and continuous in all seasons as long as the continuity of fuel supply is maintained and produce heat as byproduct that can be used for co-generation/heating and thus increases the overall efficiency of the system. Distributed generation for standalone and grid-tied applications for residential and remote power systems are important applications. Two-stage inverter, i.e. high-frequency (HF) transformer isolated dc/dc converter followed by an inverter has been adopted by industries and has been proposed with different configurations and modulations in literature to achieve the given objectives. HF transformer isolated dc/dc converter [2-19] translates the low fuel cell stack voltage to higher than the peak of the utility line or inverter output voltage specification with necessary isolation. Soft-switching is necessary to operate the converter at HF and to realize small size, light weight and low cost converter. It reduces the thermal stress on the components, switching losses, and improves the efficiency, particularly at light load where the switching and conduction losses are comparable or switching losses dominate the conduction losses. Many dc/dc converter topologies have been presented for this application [2-35] but most of them are not able to maintain soft-switching over the wide power variation and entire operating range of fuel-cell voltage. Converter presented in [25] is hard-switched and two devices are connected in parallel to improve the efficiency and switching frequency is 50 kHz. Interleaved current-fed full-bridge converter reported in [26] is a hard-switched converter and therefore operated at 10 kHz, which increases the size of magnetics/filters and therefore, of the converter. Full-bridge voltage-fed converter has several problems: rectifier diode ringing, duty cycle loss, snubber across secondary, pulsating current at input increases filter size and has limited zero-voltage switching (ZVS) range [14]. Many additional components are used to achieve ZVS in [28] which is not a simpler solution and exhibits lower efficiency.

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A topology similar to [4] is presented in [29], but secondary side switches lose ZVS at light load and higher input voltage, the ZVS range is calculated in [14]. A non-isolated bidirectional converter with active-clamping has been proposed [30] for ZVS up to 40% load but operation with wide input voltage variation is not reported. A solution to achieve ZVS over 1:2 source voltage variation using several extra components is given [31] without discussing ZVS for variation in load.

A comparison of soft-switched dc/dc converters for fuel cells to utility interface is given in [14] and it was shown that a two-inductor half-bridge current-fed isolated dc/dc converter with active-clamp [2, 13, 15, 17, 34-35] is suitable for such applications. Active-clamp snubs the voltage turn-off spike and aids in ZVS of HF switches but cannot maintain ZVS for the wide operating range of load and input voltage. Also, it has power limitation and is not modular. Full-bridge current-fed topology is modular in nature and is easy to be interleaved due to single inductor topology with less sensor requirements and less state variable and is suitable for high power. This topology has been discussed in [20-22]. It should be noted that the magnetizing inductance makes the transformer leakage inductance current continuous and also increases the number of state variables [21]. Therefore, the operation, analysis and design get modified due to the third state variable and this was completely neglected in the earlier analysis and design [20, 22]. However, the analysis and design for full range ZVS is not mentioned. To achieve ZVS for wide variation in input voltage and load while maintaining high efficiency has been a challenge, especially for low voltage higher current input applications. This paper introduces a design as a solution to cover ZVS for wide operating range. Hard-switching topology for low switching frequency operation is discussed in [23-24].

In this paper, an active-clamped current-fed full-bridge dc-dc converter shown in Fig. 1 with wide/extended range ZVS design and analysis is proposed. This paper proposes a design without involving extra active and/or passive components. The proposed converter design maintains soft-switching for this wide operating range and maintains higher efficiency. The authors do not claim on the topology. It has been discussed in [20-22]. The analysis including magnetizing inductance effect is studied in [21]. However, the authors claim on the modified analysis (explaining mode by mode operation) along with the new design with optimum inductance ratio to maintain soft-switching over wide input voltage and output power. Analytical equations have been reported to calculate the components' rating and the performance of the converter.

The objectives of this paper are to present the detailed operation, steady-state analysis, design, simulation and experimental results of this converter with extended ZVS range. Steady state operation and analysis during different intervals of operation of the converter including the effect of magnetizing inductance/current are given in Section II. A complete design procedure for extended range soft-switching illustrated by design example is presented in Section III. Simulation results using PSIM 9.0.4 are presented in Section IV to verify the analysis and design. An experimental converter prototype rated at 500W was built and tested in the laboratory to validate the design and to test the operation of the converter for wide variations in input voltage and load. Experimental results obtained are presented in Section IV.

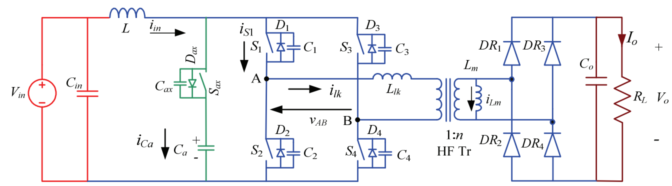


Fig. 1. Active-clamped ZVS current-fed full-bridge DC-DC converter.

II. Operation and Analysis of the Converter

The Steady-state operation and analysis of the proposed design including the effect of magnetizing inductance/current is presented in this Section. The following assumptions are made to study and understand the operation and analysis of the converter: 1) Input inductor L is large so that the current through it is considered constant. 2) Clamp capacitor C_a is large to maintain constant voltage across it. 3) All components including devices and diodes are ideal.

Steady-state operating waveforms are shown in Fig. 2. Switches S_1 and S_4 are operated by identical gating signals, and S_2 and S_3 are operated by the common gating signals. Gating signals of switch pair S_2, S_3 are shifted in phase by 180^o with gating signals of switch pair S_1, S_4 with an overlap. The overlap varies with duty cycle, which varies with input voltage variation. Fixed frequency duty cycle modulation is used for control. The duty cycle of the main switches is always kept greater than 50% to prevent increased circulating current through the auxiliary active-clamp circuit. Operation of converter with duty ratio below 50% results in unwanted conduction losses causing lower converter efficiency, particularly at partial load as the auxiliary circuit loss becomes comparable to the loss in the main switches. The switching frequency of auxiliary switch S_{ax} is double of that of main switches. It is controlled by gating signal complementary to the main switches' gating signals. So, the duty cycle of the auxiliary switch is always less than 50%. The operation of the converter during different intervals in a HF half cycle is explained using the equivalent circuits shown in Fig. 3.

Interval 1 (Fig. 3a; $t_0 < t < t_1$): In this interval, all four main switches $S_1 \sim S_4$ are on. Auxiliary switch S_{ax} is off. Input inductor L is storing energy. Power is transferred to the load by the energy stored in the output filter capacitor C_o. Transformer magnetizing current circulates through its leakage inductance, given by

$$i_{lk} = i'_{Lm} = - I'_{Lm,peak} \quad (1)$$

where i_{lk} is transformer input or leakage inductance current, i'_{Lm} is magnetizing current reflected to primary side and $I'_{Lm,peak}$ is the peak value of magnetizing current, given by

$$I'_{Lm,peak} = \frac{n \cdot V_0 \cdot T_{DR}}{2 \cdot L_m} \quad (2)$$

where, L_{lk} and L'_m are the leakage inductance and magnetizing inductance of the transformer referred to primary. T_{DR} is rectifier diode conduction time.

Voltage across the auxiliary capacitor C_a is

$$V_{Ca} = \frac{V_{in}}{2 \cdot (1-D)} \quad (3)$$

Voltage across the auxiliary switch is

$$V_{Sax} = V_{Ca} = \frac{V_{in}}{2 \cdot (1-D)} \quad (4)$$

Duty ratio of main switches $D = T_{on}/T_s$; T_{on} = conduction time of main switch and T_s = switching time period.

Interval 2 (Fig. 3b; $t_1 < t < t_2$): At $t = t_1$, main switches S_2 and S_3 are turned off. Current in the input boost inductor (I_{in}) is diverted into the auxiliary circuit path causing zero current through all main switches. The magnetizing current flows through leakage inductance L_{lk}, anti-parallel diodes D_1, D_4 of main switches S_1 and S_4. Therefore, switch currents through S_1 and S_4 quickly dips to negative, which is equivalent to peak value of the reflected magnetizing current. Device capacitances C_2 and C_3 of main switches S_2 and S_3 start charging and auxiliary switch snubber capacitor C_{ax} starts discharging linearly. On secondary side, rectifier diodes are reverse biased and power is still transferred to the load by the output filter capacitor. The constant current ($I'_{Lm,peak}$) continues to flow through magnetizing inductance. At the end of this interval, voltages across the main switch S_2 and auxiliary switch S_{ax} reach $V_{S2}(t_2) = V_{S3}(t_2) = V_o/n$ and $V_{Sax}(t_2) = V_{Ca}$-V_o/n, respectively.

Interval 3 (Fig. 3c; $t_2 < t < t_3$): This interval is very short. Snubber capacitors which are partially charged in interval 2, are still going through charging and discharging. The main switch voltages v_{S2} and v_{S3} increase from V_o/n to V_{Ca}. A positive voltage equal to ($V_{C2} - V_o/n$) appears across the transformer leakage inductance and current through it, i_{lk} rises linearly. Output voltage V_o appears across the magnetizing inductance L_m and current through it starts increasing linearly. Rectifier diodes DR_1 and DR_4 are forward biased and start conducting when the leakage inductance current i_{lk} rises above i'_{Lm} and power is transferred to the load. The leakage inductance current i_{lk} is given by

$$i_{lk} = -I'_{Lm,peak} + \frac{v_{S2} - (V_o/n)}{L_{lk}} \cdot (t - t_2) \quad (5)$$

The magnetizing inductance current i_{Lm} is given by

$$i_{Lm} = -I_{Lm,peak} + \frac{V_o}{L_m} \cdot (t\text{-}t_2) \quad (6)$$

$I_{Lm,p}$ is the peak current through magnetizing inductance (on secondary side). Current through the switch S_1 is given by

$$i_{S1} = -I'_{Lm,peak} + \frac{v_{S2} - (V_o/n)}{L_{lk}} \cdot (t - t_2) \quad (7)$$

The auxiliary clamp capacitor current i_{Ca} decreases linearly and the balance $I_{in} - i_{Ca}$ is transferred to transformer through the switches S_1 and S_4 and thus to the load.

At the end of this interval, the auxiliary switch snubber capacitor C_{ax} is discharged completely to zero and C_2 and C_3 are charged to its full voltage, equal to V_{Ca}. Final values are: $v_{Cax}(t_3) = v_{Sax}(t_3) = 0; v_{S2}(t_3) = v_{C2}(t_3) = v_{S3}(t_3) = v_{C3}(t_3) = V_{Ca} = \frac{V_{in}}{2(1-D)}$

Interval 4 (Fig. 3d; $t_3 < t < t_4$): In this interval, the anti-parallel body diode D_{ax} of the auxiliary switch S_{ax} starts conducting and S_{ax} can be gated for ZVS turn on. Leakage inductance current i_{lk} is increasing with the slope of [(V_{Ca} - V_o/n)/L_{lk}]. In this interval, switch current (through S_1 and S_4) changes direction to positive magnitude. Current through the magnetizing inductance is increasing with the same slope.

Transformer leakage inductance current i_{lk} is given by

$$i_{lk} = i_{lk}(t_3) + \frac{V_{Ca} - (V_o/n)}{L_{lk}} \cdot (t - t_3) \quad (8)$$

Current through the switch S_1 is given by

$$i_{S1} = i_{S1}(t_3) + \frac{V_{Ca} - (V_o/n)}{L_{lk}} \cdot (t - t_3) \quad (9)$$

Magnetizing inductance current is given by

$$i_{Lm} = i_{Lm}(t_3) + \frac{V_o}{L_m} \cdot (t\text{-}t_3) \quad (10)$$

Current through auxiliary capacitor during this interval decreases and is given by

$$i_{Ca} = I_{Ca,peak} - \frac{V_{Ca} - \frac{V_o}{n}}{L_{lk}} \cdot (t\text{-}t_3) \quad (11)$$

At the end of this interval, i.e., $t = t_4$, i_{Ca} reaches zero, i_{lk} reaches I_{in} and also switch current i_{S1} reaches I_{in}.

Final values are: $i_{lk}(t_4) = I_{in}$; $i_{Ca}(t_4) = 0$; $i_{S1}(t_4) = i_{S4}(t_4) = I_{in}$.

Interval 5 (Fig. 3e; $t_4 < t < t_5$): In this interval, the auxiliary switch S_{ax} is turned on with ZVS. Current i_{lk} rises above I_{in} with the same slope as interval 4 and current i_{Ca} falls linearly below zero. Magnetizing current i_{Lm} is increasing with the same slope as interval 4. The equations for this interval are

$$i_{lk} = I_{in} + \frac{\left(V_{Ca} - \frac{V_o}{n}\right)}{L_{lk}} \cdot (t\text{-}t_4) \quad (12)$$

$$i_{S1} = I_{in} + i_{Ca} \quad (13)$$

$$i_{Ca} = I_{in} - i_{lk} = -\frac{\left(V_{Ca} - \frac{V_o}{n}\right)}{L_{lk}} .(t\text{-}t_4) \quad (14)$$

Peak value of the switch current is given by:

$$I_{S1,peak} = 2I_{in} + \frac{nV_o}{f_s \cdot L_m} \cdot (1 - D) \quad (15)$$

At the end of this interval, current i_{Ca} rises to negative peak of $-(I_{in} + I'_{Lm,peak})$ and therefore the currents i_{lk} and i_{S1} reaches their peak value. Final values: $i_{Ca}(t_5) = -I_{Ca,,peak}$; $i_{lk}(t_5) = I_{lk,peak}$; $i_{S1}(t_5) = I_{S1,peak}$.

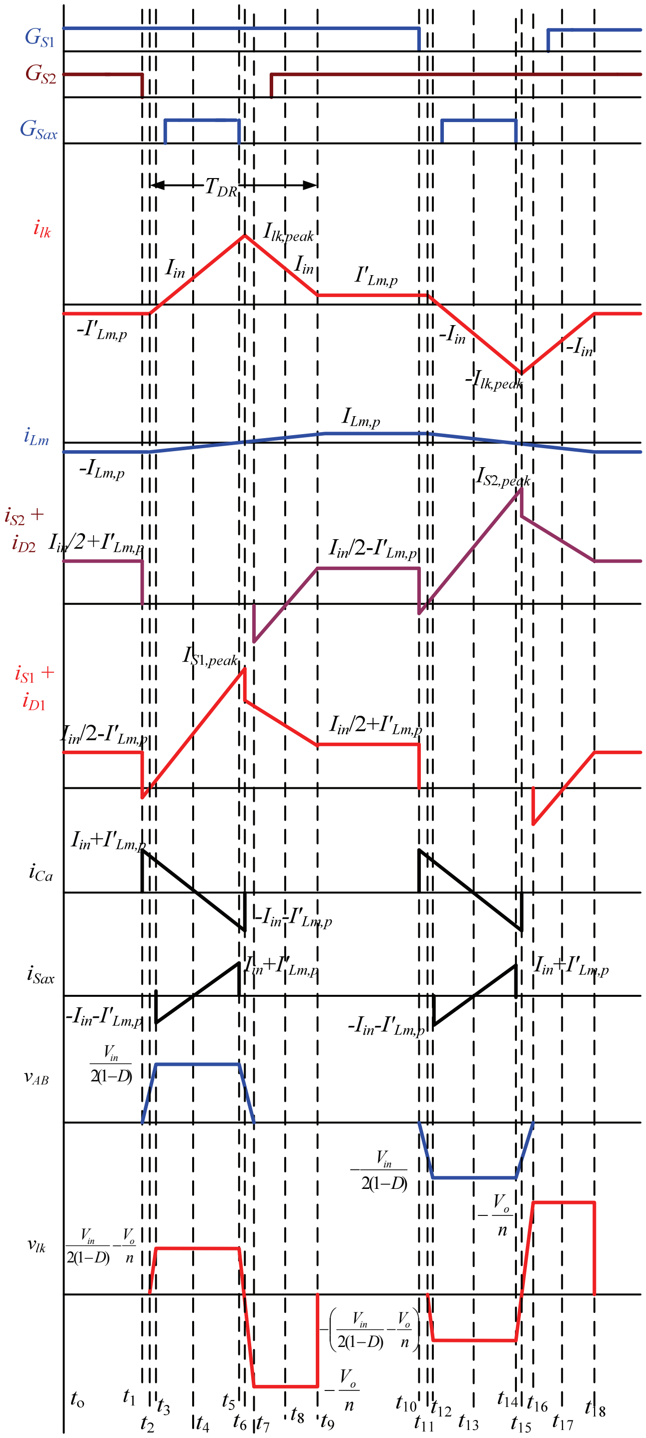
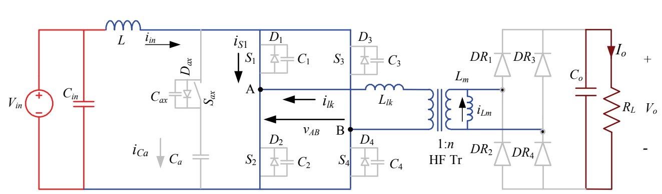


Fig. 2. Steady state operating waveforms of current-fed full-bridge DC-DC converter with active-clamp.



(a)

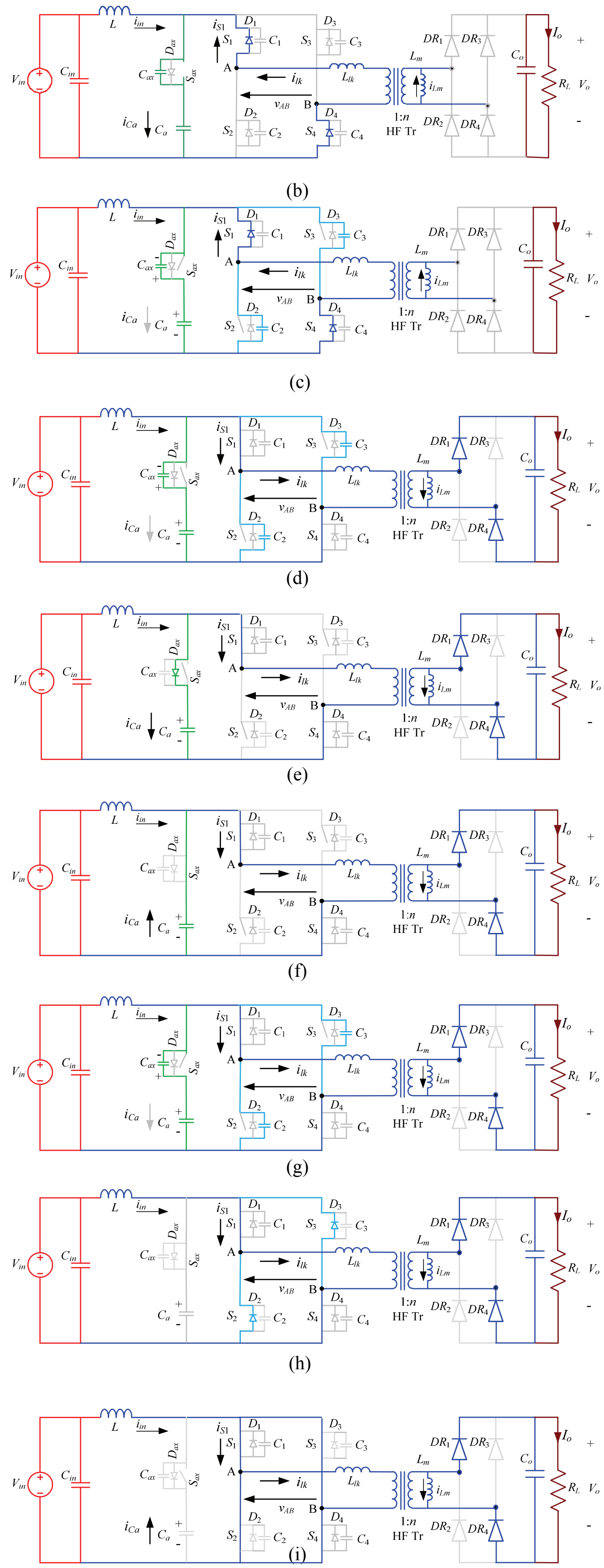


Fig. 3. Equivalent circuits during different intervals of operation of the converter for the waveforms shown in Fig. 2.

Interval 6 (Fig. 3f; $t_5 < t < t_6$): The auxiliary switch S_{ax} is turned off at $t = t_5$. Current i_{lk} charges C_{ax} and discharges C_2 and C_3. The leakage inductance L_{lk} resonates with snubber capacitors C_{ax} and C_2+C_3. This time interval is very short and the leakage inductance current i_{lk} drops by a small value. The resonant frequency is given by

$$\omega_r = \frac{1}{\sqrt{L_{lk} \cdot (C_2 + C_3 + C_{ax})}} \tag{16}$$

Voltage across the capacitor C_2 or switch S_2 is given by

$$v_{S2} = V_{Ca} - v_{Sax} \tag{17}$$

where the voltage across the switch S_{ax} (or capacitor C_{ax}) is given by

$$v_{Sax} = I'_{lk,peak} \cdot \sqrt{\frac{L_{lk}}{(C_2 + C_3 + C_{ax})}} \cdot \sin(\omega_r \cdot (t - t_5)) \tag{18}$$

$$i_{lk} = I_{lk,peak} \cdot \cos(\omega_r \cdot (t - t_5)) \tag{19}$$

Main switch current is given by

$$i_{S1} = I_{S1,peak} \cdot \cos(\omega_r \cdot (t - t_5)) \tag{20}$$

At the end of this interval, C_2 and C_3 discharge to V_o/n and C_{ax} charges to (V_{Ca} - V_o/n). Final values are:

$v_{Sax}(t_6) = V_{Ca} - V_o/n$; $v_{S2}(t_6) = V_o/n$;

Interval 7 (Fig. 3g; $t_6 < t < t_7$): Current i_{lk} is still charging C_{ax} and discharging C_2 and C_3 in a resonant fashion. It is short interval too and the current i_{lk} decreases a very little in this interval. At the end of this interval, the capacitors C_2 and C_3 discharges completely to zero and capacitor C_{ax} charges to its initial value. Final values are: $v_{S2}(t_7) = 0$; $v_{Sax}(t_7) = V_{Ca}$.

Interval 8 (Fig. 3h; $t_7 < t < t_8$): In this interval, anti-parallel body diodes D_2 and D_3 of main switches S_2 and S_3 respectively start conducting and now S_2 and S_3 can be gated for ZVS turn on. Current i_{lk} decreases with a negative slope of [$V_o/(n \cdot L_{lk})$].

$$i_{lk} = I_{lk}(t_7) - \frac{V_o}{n \cdot L_{lk}} \cdot (t - t_7) \tag{21}$$

$$i_{D2} = i_{lk} - I_{in} \tag{22}$$

This interval ends when current $i_{lk} = I_{in}$. Final values are: $i_{D2}(t_6) = 0$; $i_{lk}(t_6) = I_{in}$.

Interval 9 (Fig. 3i; $t_8 < t < t_9$): In this interval, switches S_2 and S_3 are turned on with ZVS. Currents i_{S2} and i_{S3} start increasing and the current i_{lk} is decreasing with the same slope. Current i_{lk} is transferred to the switches S_2 and S_3. The interval ends when current i_{lk} equals to the current i'_{Lm}. Switch S_2 and S_3 current reaches to $I_{in}/2 - I'_{Lm,peak}$ and S_1 and S_4 current reaches to $I_{in}/2 + I'_{Lm,peak}$.

$$i_{lk} = I_{in} - \frac{V_o}{n \cdot L_{lk}} \cdot (t - t_8) \tag{23}$$

$$i_{S2} = \frac{V_o}{n \cdot L_{lk}} \cdot (t - t_8) \tag{24}$$

$$i_{S1} = I_{in} - \frac{V_o}{n \cdot L_{lk}} \cdot (t - t_8) \tag{25}$$

Final values: $i_{S2}(t_9) = I_{in}/2 - I'_{Lm,peak}$; $i_{S1}(t_9) = I_{in}/2 + I'_{Lm,peak}$; $i_{lk}(t_9) = i'_{Lm}(t_9) = I'_{Lm,peak}$.

For the next half cycle, the intervals are repeated in the same sequence with other symmetrical devices conducting to complete the full HF cycle. The analysis is done to obtain the design equations to design and select the components as well as to evaluate the converter's performance theoretically.

Based on this analysis, the design equations were derived and presented in next Section.

III. Extended Range Soft-switching Design of the Converter

In this Section, converter design procedure for extended ZVS range is illustrated by a design example for the following specifications: Input voltage V_{in} = 22 to 41 V, output voltage V_o = 350 V, output power P_o = 500W, minimum load = 10% (50 W), switching frequency for H-bridge devices f_s = 100 kHz and for auxiliary clamp switch is 200 kHz.

(1) Average input current is $I_{in} = P_o/(\eta V_{in})$. Assuming an ideal efficiency η of 100%, I_{in} = 22.7 A.

(2) D_{max} is selected at minimum input voltage, i.e., V_{in} = 22 V and full load which decides the maximum switch voltage rating $V_{SW(max)}$ using

$$V_{sw,\max} = \frac{V_{in}}{2 \cdot (1 - D_{\max})} \tag{26}$$

For D_{max} = 0.8, $V_{SW(max)}$ = 55 V.

(3) Inductor values L_{lk} and L_m: Selection of leakage inductance L_{lk} and parallel inductance L_m is performed at minimum input voltage and full load condition using (27) obtained from i_{lk} and i_{Lm} waveforms.

$$L_{lk} = \frac{R_L}{f_s}\left[\frac{(V_{in}/V_o)^2}{4 \cdot (1 + L_{lk}/L_m^{'})} - \frac{(V_{in}/V_o) \cdot (1\text{-}D_{\max})}{2n}\right] \tag{27}$$

Selecting the inductance values for a certain rated power P_o and switching frequency f_s depends upon the transformer turns ratio n, inductor ratio L'_m/L_{lk} and the maximum duty cycle D_{max} at full load calculated earlier. Here L'_m refers to equivalent magnetizing inductance referred to primary.

Now the transformer turns ratio $n = N_s/N_p$, is selected to maintain D > 0.5, i.e., voltage regulation with load and fuel cell stack voltage variation given by

$$D = 1 - \frac{2n \cdot V_o}{V_{in}}\left[\frac{(V_{in}/V_o)^2}{4 \cdot (1 + L_{lk}/L_m')} - \frac{L_{lk} \cdot f_s}{R_L}\right] \tag{28}$$

and realizable value of L_{lk} including transformer leakage (which is an issue mainly for power rating above 1 kW) given by (27). Also, n should be such that L_{lk} is positive, using (27)

$$n > 2 \cdot (1\text{-}D_{\max}) \cdot \frac{V_o}{V_{in}} \cdot (1 + L_{lk}/L_m') \tag{29}$$

Therefore, minimum value of n = 6.4 for $L_m' = \infty$ (large value of magnetizing inductance) or n = 7 for L_m'/L_{lk} = 10. Fig. 4(a) shows the calculated values of L_{lk} with respect to inductance ratio L_m'/L_{lk} for three values of turns ratio n.

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Inductance ratio L_m'/L_{lk} is selected based on the ZVS range, and main switch RMS current given by (30), which should be low for high efficiency.

RMS current through the main switch is given by

$$I_{sw,rms} = \sqrt{I_{in}^2\left[\frac{3}{4}-\frac{D}{2}+\frac{T_{DR}}{3T_s}\right]+\left(I'_{Lm,peak}\right)^2\left[\frac{2}{3}+\frac{D}{3}-\frac{4T_{DR}}{3T_s}\right]+I_{in}I'_{Lm,peak}\left[D-1+\frac{T_{DR}}{3T_s}\right]} \tag{30}$$

Here T_{DR} is rectifier diode conduction time given by

$$T_{DR} = \frac{n\cdot V_{in}}{2\cdot V_o\cdot f_s\left(1+\frac{L_{lk}}{L'_m}\right)} \tag{31}$$

During derivation, snubber charging/discharging intervals (t_1-t_3, t_5-t_7, t_{10}-t_{12}, t_{14}-t_{16}) of short duration are neglected.

Fig. 4(b) shows the calculated values of switch RMS current with respect to L_m'/L_{lk} for four values of turns ratio n. Smaller value of L_m'/L_{lk} will achieve ZVS at light load but increase peak and rms currents through the switches, leading to low efficiency of the converter.

For smaller turns ratio, i.e., n = 7, value of L_{lk} is low (Fig. 4(a)) and it reduces ZVS range as seen in (30). For higher transformer turns ratio, i.e., n = 10, value of L_{lk} is high (Fig. 4(b)) and increases ZVS range. Choosing a design (at 22 V, full load) with smaller value of D, say 0.6 for example (instead of 0.8), will result in smaller value of leakage inductance L_{lk}, which will not be able to store sufficient energy to maintain ZVS for the wider input voltage range and light load conditions. Also, choosing a design (at 22 V, full load) according to Fig. 4(a) for turns ratio $n > 8$, for example n = 9 or 10, will require higher transformer turns ratio, resulting in auxiliary switch duty cycle $D_{Sax} = 2(1-D) >= 1$, which is not possible and is the limitation of this converter. Therefore, n = 8 with $D > 0.5$ is chosen.

Turns ratio n = 8 gives realizable value of L_{lk}, maintains voltage regulation at light load for given wide input voltage variation. Therefore, transformer turns ratio n = 8 is selected.

Fig. 4(b) indicates that for a given value of n, switch rms current decreases as the ratio L_m'/L_{lk} increases. For the selected value of n = 8, reduction in rms current is negligible for L_m'/L_{lk} > 25. Therefore, an inductance ratio of L_m'/L_{lk} = 25 is selected.

From the above discussions, using D_{max} = 0.8, n = 8 and L_m'/L_{lk} = 25, calculated values of inductances are L_{lk} = 0.4 μH and L_m = 0.64 mH.

(4) Values of input boost inductor is given by

$$L = (V_{in})(D\text{-}0.5)/[(\Delta I_{in})(f_s)] \tag{32}$$

where ΔI_{in} is the boost inductor ripple current.

For ΔI_{in} = 0.5 A, L = 132μH. Maximum voltage across the inductor = V_{Ca} = 55 V, given by (3).

(5) Inductors' ratings: The RMS current through the leakage and magnetizing inductances are

$$I_{Llk,rms} = \sqrt{I_{in}^2\left[\frac{8T_{DR}}{3T_s}\right]+\left(I'_{Lm,peak}\right)^2\left[\frac{4D}{3}-\frac{1}{3}\right]+I_{in}\cdot I'_{Lm,peak}\left[\frac{8}{3}(D-1)+\frac{4T_{DR}}{T_s}\right]} \tag{33}$$

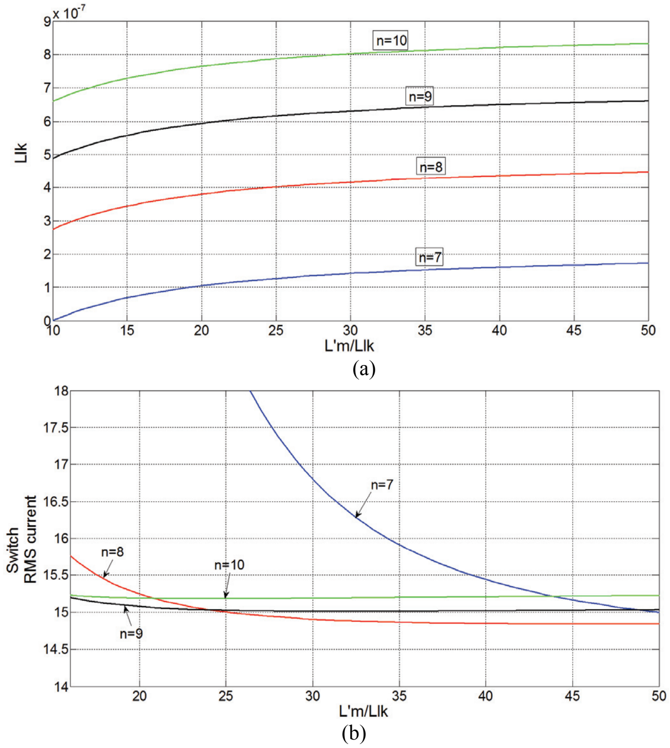


Fig. 4. Variation of (a) value of leakage inductance L_{lk} (H), and (b) switch RMS current (A), with respect to inductance ratio L_m'/L_{lk} for various transformer turns ratio n for the design example.

$$I_{Lm,rms} = \frac{I'_{Lm,peak}}{n}\sqrt{1-\frac{4T_{DR}}{3T_s}} \tag{34}$$

Using (2), $I'_{Lm,peak}$ = 5.29 A. $I_{Lm,rms}$ is calculated to be 0.55A. Peak magnetizing inductance current = $I'_{Lm,peak}/n$ = 0.66A. Using (31) and (33), $I_{lk,rms}$ = 20.11A. Peak current through L_{lk} is, $I_{lk,peak} = 2I_{in}+I'_{Lm,peak}$ = 50.7 A. Maximum voltage across L_{lk} = V_o/n = 43.75 V. Maximum voltage across $L_m = V_o$= 350 V.

(6) Switch current ratings: RMS current through the main switches $I_{sw,rms}$ can be calculated by (30). RMS current through the auxiliary switch is given by

$$I_{auxsw,rms} = \left(I_{in}+I'_{Lm,peak}\right)\cdot\sqrt{2(1-D)/3} \tag{35}$$

The values of $I_{sw,rms}$ and $I_{aux,rms}$ are calculated to be 15A and 10.22 A respectively.

Peak currents through main switches $I_{sw,peak} = 2I_{in}+I'_{Lm,peak}$ = 50.7 A and auxiliary switch $I_{aux,peak} = I_{in}+I'_{Lm,peak}$ = 28 A.

Average current through auxiliary switch as well as anti-parallel diodes is given by

$$I_{auxsw,av} = \left(I_{in}+I'_{Lm,peak}\right)\cdot\left[\frac{(1-D)}{4}\right] \tag{36}$$

Here, $I_{auxsw,av}$ = 1.4A. Average current through the main switches $I_{sw,av} = I_{in}/2$ = 11.35 A.

(7) Auxiliary capacitor: Substituting in (3), V_{in} = 22 V and D = 0.8, V_{Ca} = 55 V. The value of auxiliary capacitor C_a is

$$C_a = \frac{I_{Ca,peak}\cdot\sqrt{2(1-D)/3}}{4\cdot\pi\cdot f_s\cdot\Delta V_{Ca}} \tag{37}$$

Peak current through C_a is $I_{Ca,peak} = I_{in}+I'_{Lm,peak} = 28$A. For a ripple voltage of $\Delta V_{Ca} = 2$ V, $C_a \cong 4$ μF.

RMS current through auxiliary capacitor is

$$I_{Ca,rms} = I_{Ca,peak} \cdot \sqrt{\left(\frac{2}{3}(1-D)\right)} \qquad (38)$$

Here, $I_{Ca,\mathrm{rms}} = 10.22$ A. Auxiliary capacitor carries a current of 200 kHz (twice the switching frequency).

(8) Output rectifier diodes: Average rectifier diode current is given by

$$I_{DR,avg} = P_o/(2V_o) \qquad (39)$$

Here, $I_{DR,avg} \cong 0.7$ A. Voltage rating of rectifier diodes, $V_{DR} = V_o = 350$ V.

(9) Output capacitor: Value of output filter capacitor C_o is

$$C_o = \frac{(I_0)\cdot\left(\frac{T_s}{2} - T_{DR}\right)}{\Delta V_o} \qquad (40)$$

ΔV_o = Allowable ripple in output voltage. $C_\mathrm{o} = 4.9$ μF for $\Delta V_\mathrm{o} = 0.75$ V. Its voltage rating is equal to $V_o = 350$ V.

(10) Snubber design: The equation for the calculation of snubber capacitors is given by

$$(C_1 + C_4 + C_{Sax})_{eff} = \frac{t_f \cdot \left(I_{in} + I'_{Lm,peak}\right)}{\frac{V_{in}}{2(1-D)}} \qquad (41)$$

Here, t_f = fall time of the switches during turn-off. $C_1 = C_4 = C_{oss,S1}$; $C_{a1} = (C_1 + C_4 + C_{sax})_{eff} - 2C_{oss,S1}$.

For the selected main and auxiliary switches IPP06CN10NG ($V_{ds} = 100$ V, $I_D = 100$ A, $R_{dson} = 6.2$ mΩ, $C_{oss} = 1$ nF, $t_f = 10$ ns), the calculated value of snubber capacitor across the auxiliary switch is $C_{a1} = 2.1$ nF. Snubber capacitors' voltage rating is equal to switch voltage, given by (4) and is 55 V.

(11) ZVS Conditions: (A) To achieve ZVS of auxiliary switch, in interval 2, the dead-gap between the main switch gating signal G_{S2} and auxiliary switch gating signal G_{Sax} should be of sufficient duration to allow charging of the snubber capacitors across the main switches C_2 and C_3 and discharging of snubber capacitor across the auxiliary switch C_{ax}, by the boost inductor current I_{in}. The time required is given by

$$T_{dg1} = \frac{(C_2 + C_3 + C_{ax})\cdot\left(\frac{V_{in}}{2(1-D)}\right)}{I_{in}} \qquad (42)$$

(B) For ZVS of main switches, in interval 5 the charging of the snubber capacitor C_{ax} and discharging of C_2 and C_3 should be done by the leakage inductance current in a quarter of the resonant period and is equal to the dead-gap between the auxiliary switch gating signal G_{Sax} and main switch gating signal G_{S2} and is given by

$$T_{dg2} = \frac{\pi}{2}\sqrt{L_{lk}\cdot(C_2 + C_3 + C_{ax})} \qquad (43)$$

$T_{dg1} = 12$ ns and $T_{dg2} = 65$ ns. Identical dead-gaps $T_{dg1} = T_{dg2} = 65$ ns is provided between main and auxiliary gating signal.

The designed values are summarized in Table 1.

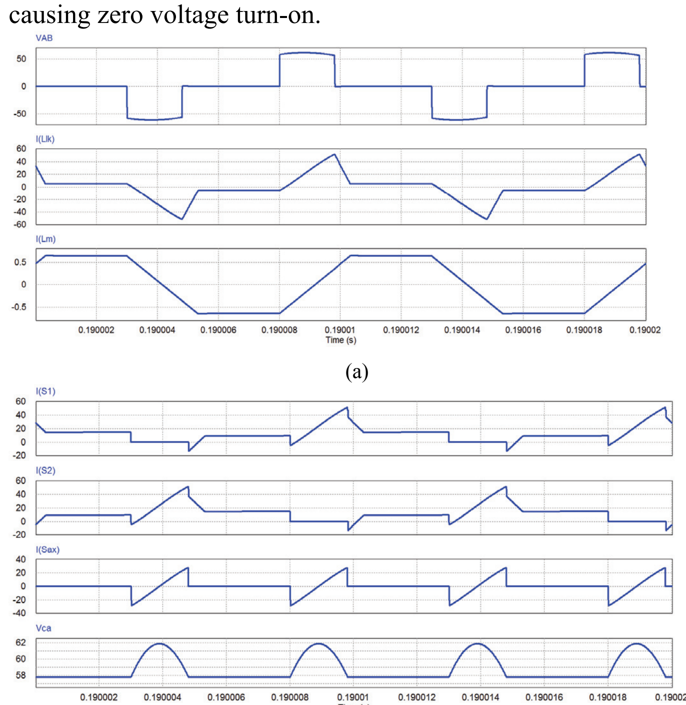
Table. 1. Values of the parameters obtained from design equations.

V_{in}	22-41 V	V_o	350V
P_o	500 W	f_s	100 kHz
L	132 μH	C_o	4.9 μF
L_{lk}	0.4 μH	L_m	0.64 mH
n	8	C_a	4 μF

IV. Simulation and Experimental Results

The designed converter rated at 500W was first simulated using PSIM 9.0.4 and then built in the laboratory to verify the analysis, design and performance of the converter. Simulation results for two extreme operating conditions of $V_{in} = 22$ V, full load and $V_{in} = 41$ V, 10% load are presented in Fig. 5 and Fig. 6, respectively. The components' values obtained from design and given in Table 1 are used as simulation parameters.

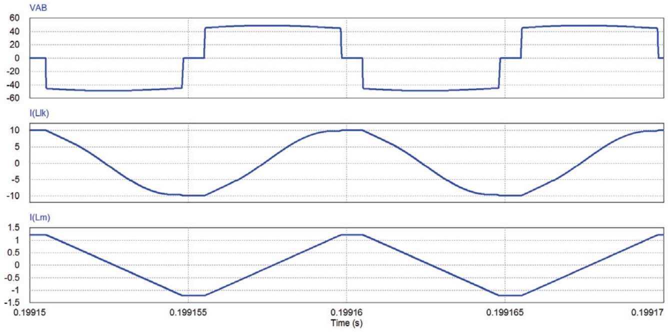
Simulation waveforms coincide with the theoretical operating waveforms shown in Fig. 2. When both the main switches are on, $v_{AB} = 0$, i'_{Lm} is flowing through i_{lk} and are constant. Whenever, one main switch is off, v_{AB} appears across the transformer and the current i_{lk} and i_{Lm} change direction. At higher voltage and light load condition (Fig. 6), the duty cycle is low and therefore v_{AB} appears for longer time. It makes the currents i_{lk} and i_{Lm} to be constant for a very small duration and their appearance look like triangular in shape with higher peak value compared to full load condition. Figs. 5-6 show that the anti-parallel diodes of the switches (main and auxiliary) conduct prior to the conduction of corresponding switches causing zero voltage turn-on.



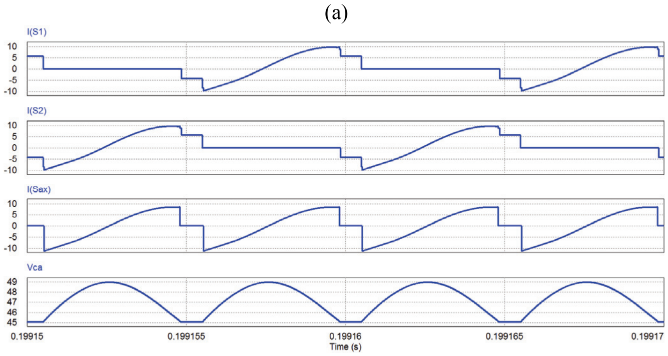
(a)

(b)

Fig. 5. Simulation waveforms at $V_{in} = 22$ V and full load: (a) voltage v_{AB}, leakage inductance current i_{lk}, and magnetizing inductance current i_{Lm} (b) main switches' currents i_{S1} and i_{S2}, auxiliary switch's current i_{Sax} and voltage across auxiliary capacitor V_{Ca}.



(a)



(b)

Fig. 6. Simulation waveforms at V_{in} = 41 V and 10% load: (a) voltage v_{AB}, leakage inductance current i_{lk}, and magnetizing inductance current i_{Lm} (b) main switches' currents i_{S1} and i_{S2}, auxiliary switch's current i_{Sax} and voltage across auxiliary capacitor V_{Ca}.

It is clear that the leakage inductance current i_{lk} is continuous due to the circulation of magnetizing current when all the H-bridge switches are on. It should be noticed that with increase in input voltage and/or reduction in load current, the duty cycle of main switches reduces, which results in increase in peak value of magnetizing inductance current. It adds to leakage inductance current to achieve ZVS of main switches even at such a wide variation in input voltage and load. At light load condition, anti-parallel body diode conduction time is increased due to magnetizing current assuring ZVS.

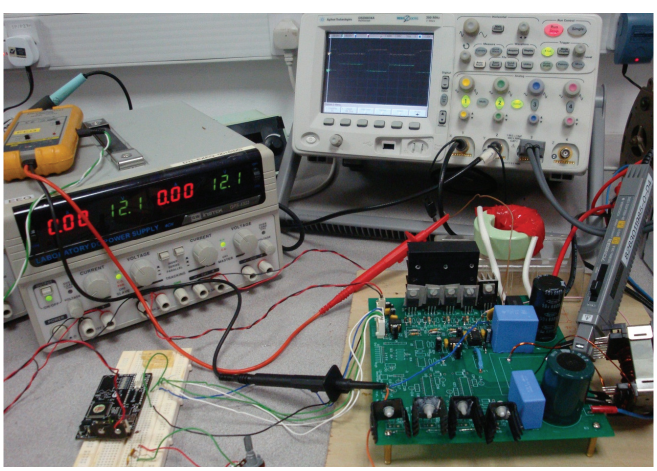


Fig. 7. Experimental laboratory prototype of 500 W current-fed full-bridge isolated dc/dc converter.

To obtain the simulation results for given input voltage (22V in Fig. 5 and 41 V in Fig. 6) and for given load condition (245Ω at full load in Fig. 5 and 2450Ω at 10% load in Fig. 6) simulation is run for several HF cycles until the state variables reach a steady-state. Ideal components/devices were used.

Experimental prototype, as shown in Fig. 7, was built for the specifications and design given in Section III. The details are as follows: IPP06CN10NG (main and auxiliary switches); RUR-860 (rectifier diodes); HF transformer: PC40ETD44-Z ferrite core, primary turns = 9, secondary turns = 72, L_{lk} (primary side) = 0.4 µH, L_m (secondary side) = 332mH; parallel inductor: T106-26, 83 turns, L_p = 0.641mH; boost inductor: MPP Powder core, T250-40, 32 turns, L = 200 µH.

Due to imperfect ratio of L_{lk}/L_m than the desired design value (given in the design section), an extra small size inductor L_p is added in our experimental converter used for verification of analysis in our lab. In a practical industrial converter, one can control the magnetizing inductance value close to the required magnetizing inductance to avoid the use of external inductance. Also, slight changes in this value should not affect the performance too much.

Gating signals for the switches have been generated using Cypress PSoC 5 (Programmable system-on-chip) board.

IR2181 driver ICs are used for gating the MOSFETs. Variable resistors (rheostats) are used as load for testing. The developed converter prototype has been tested at full load and 10% load for V_{in} = 41 V, and at full load and 20% load for V_{in} = 22 V. The experimental results are shown in Figs. 8-11.

Parts (b) to (e) of Figs. 8-11 clearly confirm the ZVS of main and auxiliary switch over wide variation in fuel cell voltage and load. In waveforms shown in part (b) of Figs. 8-11, gating signals (v_{GS}) are applied to main switches after voltage across them (v_{DS}) reaches zero. The ZVS turn on of main switches is also confirmed by part (d) of Figs. 8-11 since anti-parallel diode is conducting before the switch starts conducting.

Similarly, in part (e) of Figs. 8-11, anti-parallel diode of the auxiliary switch is conducting first causing ZVS turn-on of the auxiliary switch. This can be observed in gating signal (v_{GS}) and voltage across the auxiliary switch (v_{DS}) as shown in part (c) of Figs. 8-11. Voltage across the transformer v_{AB} and the leakage inductance current i_{lk} confirm ZCS of rectifier diodes (negligible ringing), as shown in part (a) of Figs. 8-11.

It is observed from these curves that the experimental values coincide with the calculated values. The experimental waveforms (Figs. 8-11) illustrate that the converter maintains ZVS for all switches over the complete range of load variation for wide input voltage range (22 to 41V). The designed converter maintains ZVS down to 20% load at V_{in} = 22V and down to 5% load at V_{in} = 41V.

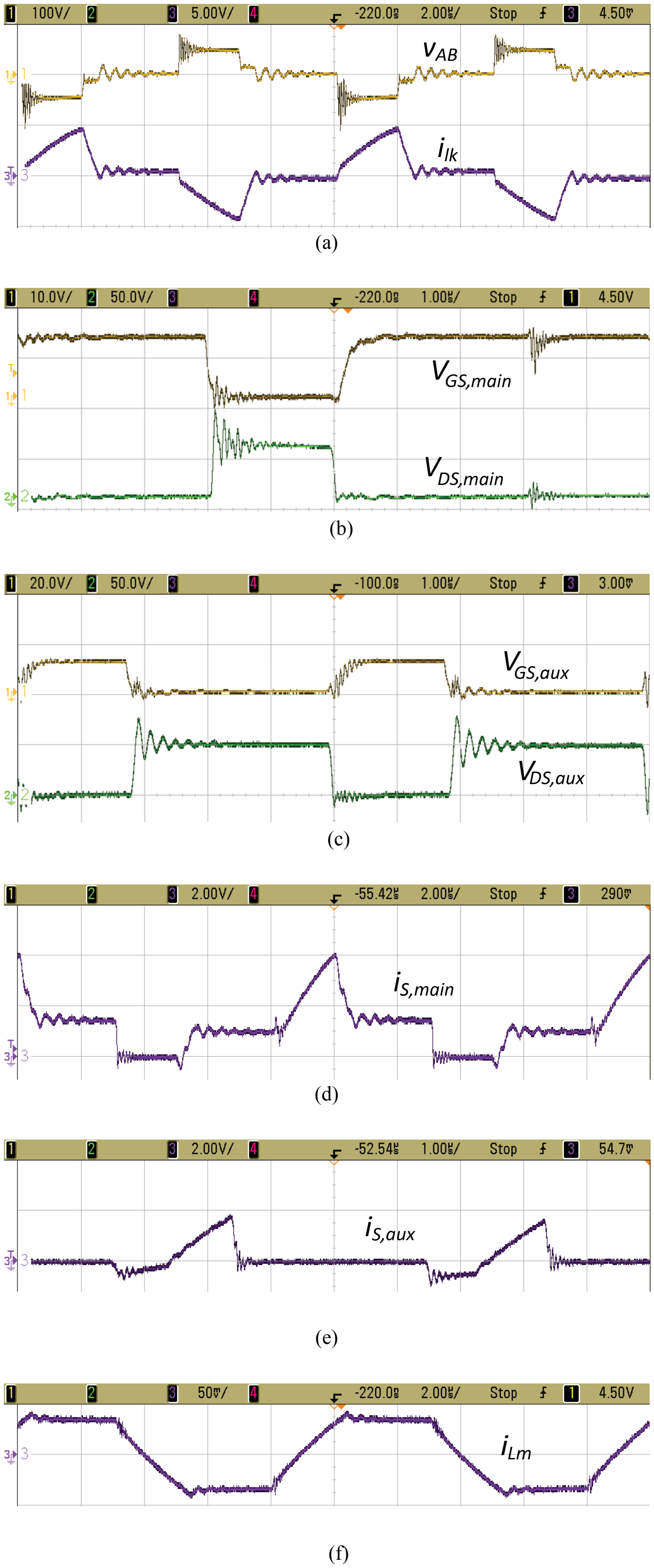


Fig. 8. Experimental waveforms at V_{in} = 22 V and full load: (a) Voltage v_{AB} (100V/div) and leakage inductance current i_{lk} (50A/div), (b) main switch voltage v_{DS} (50V/div) and gate voltage v_{GS} (10V/div), (c) auxiliary switch voltage v_{DS} (50V/div) and gate voltage v_{GS} (20V/div), (d) main switch current i_{S1} (20A/div), (e) auxiliary switch current i_{Sax} (20A/div) and (f) magnetizing inductance current i_{Lm} (0.5A/div).

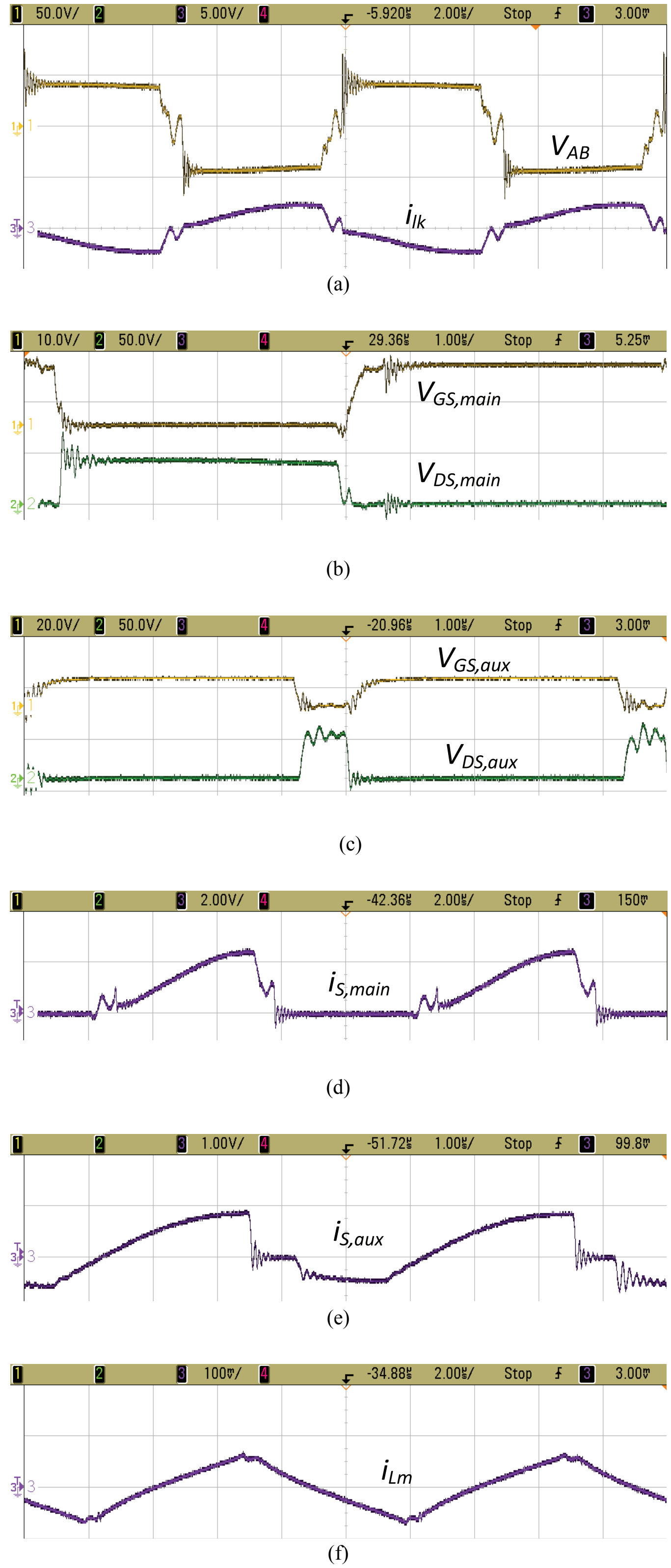


Fig. 9. Experimental waveforms at V_{in} = 41V and full load: (a) Voltage v_{AB} (50V/div) and leakage inductance current i_{lk} (50A/div), (b) main switch voltage v_{DS} (50V/div) and gate voltage v_{GS} (10V/div), (c) auxiliary switch voltage v_{DS} (50V/div) and gate voltage v_{GS} (20V/div), (d) main switch current i_{S1} (20 A/div), (e) auxiliary switch current i_{Sax} (10A/div) and (f) magnetizing inductance current i_{Lm} (1A/div).

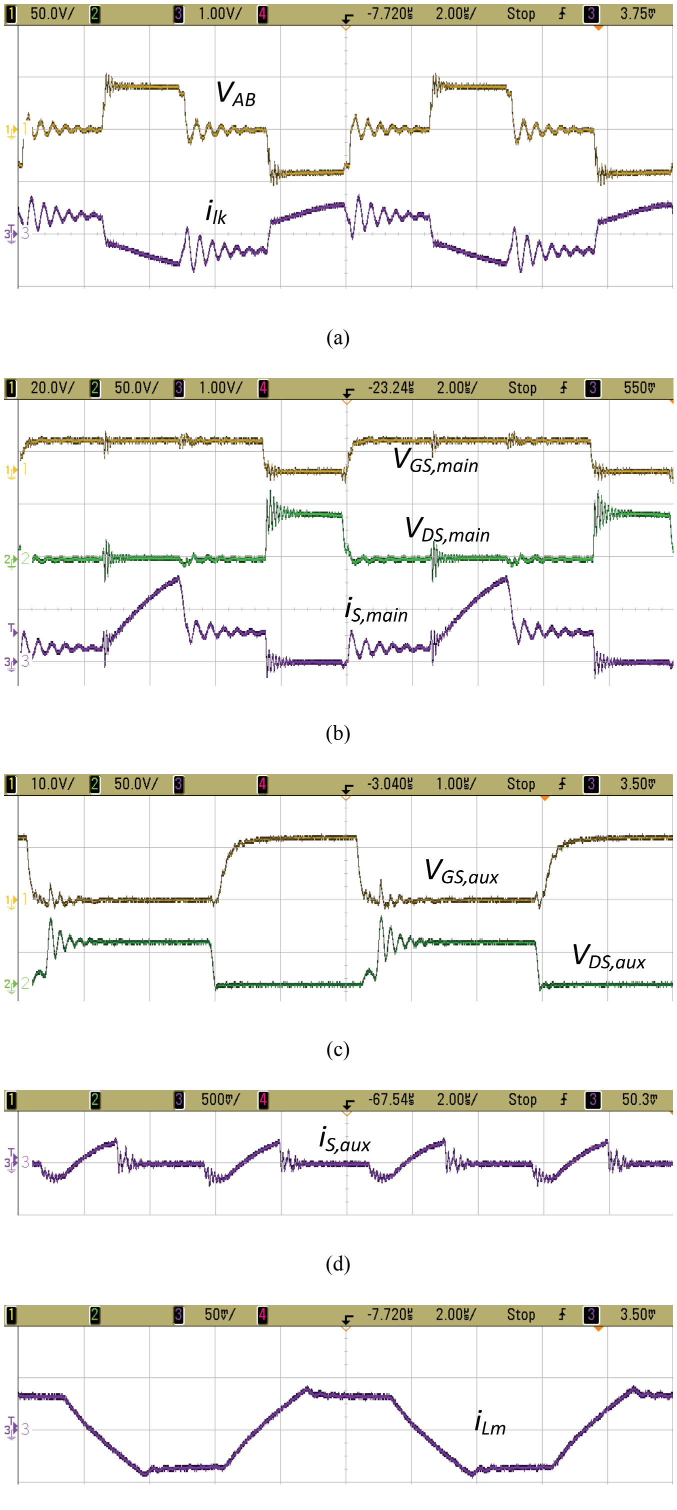


Fig. 10. Experimental waveforms at V_{in} = 22 V and 20% load: (a) Voltage v_{AB} (50V/div) and leakage inductance current i_{lk} (10A/div), (b) main switch voltage v_{DS} (50V/div), gate voltage v_{GS} (20V/div) and current i_{S1} (10A/div), (c) auxiliary switch voltage v_{DS} (50V/div) and gate voltage v_{GS} (10V/div), (d) auxiliary switch current i_{Sax} (5A/div) and (e) magnetizing inductance current i_{Lm} (0.5A/div).

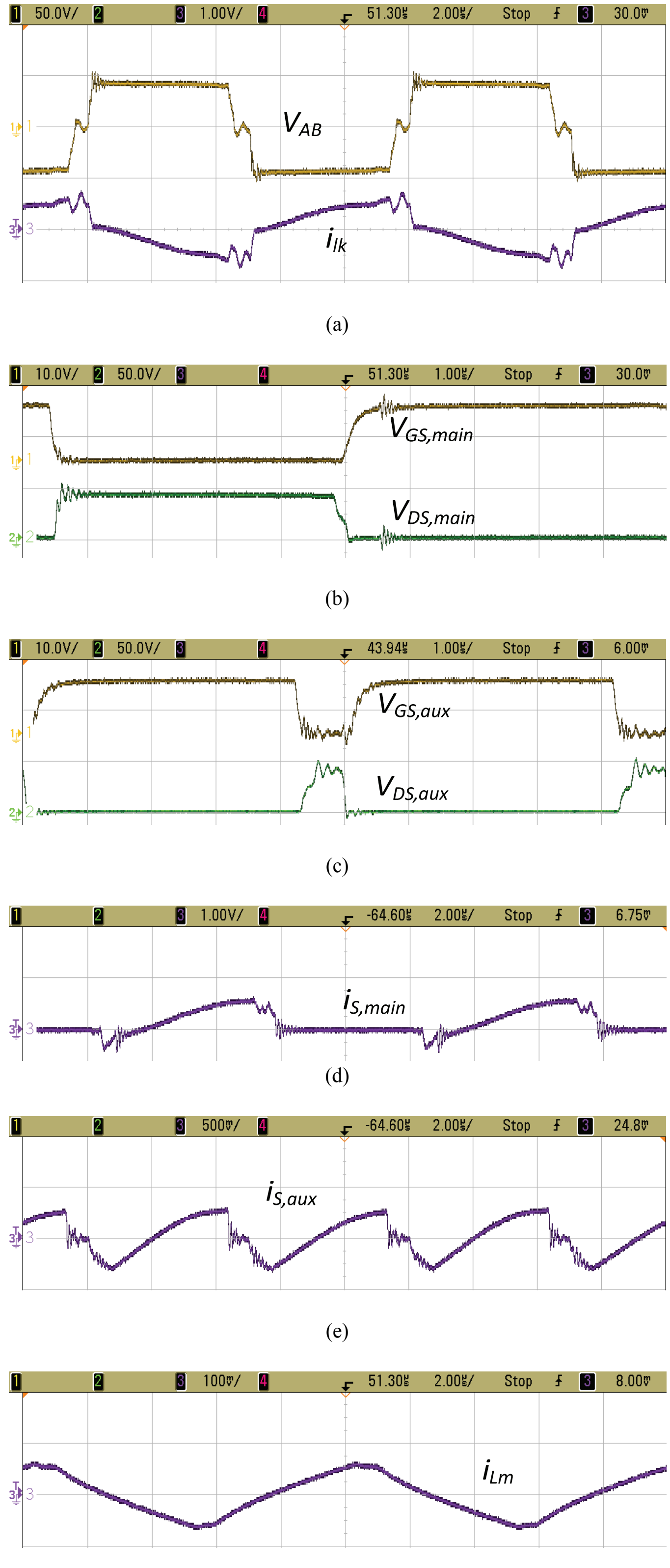


Fig. 11. Experimental waveforms at V_{in} = 41 V and 10% load: (a) Voltage v_{AB} (50V/div) and leakage inductance current i_{lk} (10A/div), (b) main switch voltage v_{DS} (50V/div) and gate voltage v_{GS} (10V/div), (c) auxiliary switch voltage v_{DS} (50V/div) and gate voltage v_{GS} (10V/div), (d) main switch current i_{S1} (10A/div), (e) auxiliary switch current i_{Sax} (5A/div) and (f) magnetizing inductance current i_{Lm} (1A/div).

V. Summary and Conclusions

To achieve ZVS for wide source voltage variation and varying output power/load while maintaining high efficiency has been a challenge, especially for low voltage higher current input applications. A ZVS active-clamped current-fed full-bridge isolated converter has been re-studied in this paper. The magnetizing inductance increases the leakage inductance current value at light load and therefore, the energy stored in leakage inductance to maintain ZVS of main switches as well as auxiliary switch.

Detailed steady-state operation and analysis of current-fed full-bridge converter have been presented. Design to attain soft-switching over an extended range of input voltage and load i.e. output power has been presented. Simulation results using PSIM 9.0.4 have been presented. An experimental prototype of the converter rated at 500W has been designed, built and tested for variations in input voltage and load in order to validate the analysis. Experimental results verify the accuracy of the analysis and show that the proposed configuration is able to maintain ZVS of all switches over a wide range of load and input voltage variation due to the variation in fuel flow and stack temperature. Theoretically, the converter is able to maintain ZVS till 20% load at 22 V and 5% load 41 V.

In a practical fuel cell application, when the load current drops due to reduced fuel flow, the light or reduced power below rated power is transferred at higher fuel cell voltage. It can be clearly seen and understood also from the fuel cell V-I characteristic. If the load current or power is around 10% of the rated power, then the fuel cell stack voltage increases nearly to 41 V. Hence, the possibility of the condition V_{in} = 22V at 10% load is only during transition period when load is suddenly changed from full load to 10% due to fuel flow adjustment. Hence it is justifiable to have ZVS range of 20% load at low input voltage and below 10% at higher input voltage will cover the operating range at steady-state. Rated converter efficiency of 94% is obtained for the developed lab prototype rated at 500 W. The converter has limitation that duty cycle of the main switch should be greater than 50%.

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