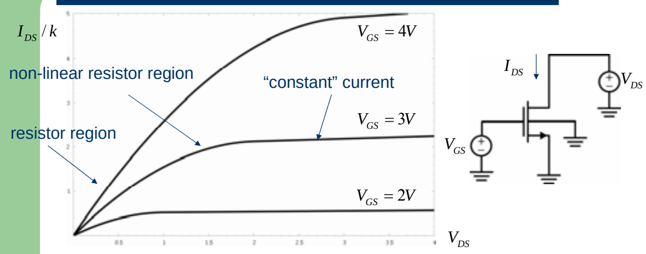
Lecture 42: Review of active MOSFET circuits

Prof. J. S. Smith

Observed Behavior: I_D-V_{DS}

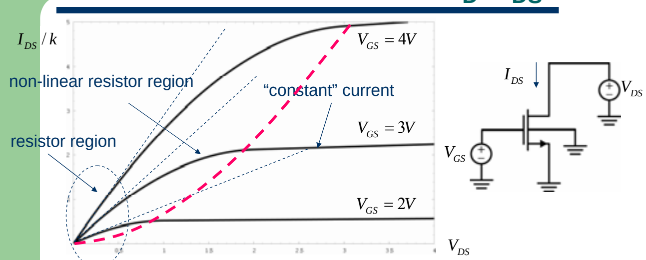


- For low values of drain voltage, the device is like a resistor
- As the voltage is increases, the resistance behaves non-linearly and the rate of increase of current slows
- Eventually the current stops growing and remains essentially constant (current source)

Final Exam

- Covers the course from the beginning
- Date/Time: SATURDAY, MAY 15, 2004 8-11A
- Location: BECHTEL auditorium
- One page (Two sides) of notes

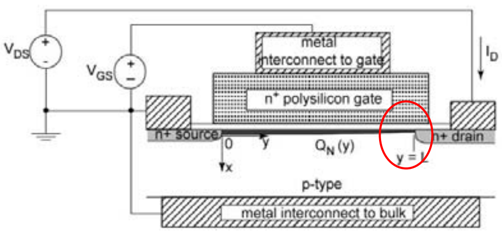
Observed Behavior: I_D-V_{DS}



As the drain voltage increases, the E field across the oxide at the drain end is reduced, and so the charge is less, and the current no longer increases proportionally. As the gate-source voltage is increased, this happens at higher and higher drain voltages.
The start of the saturation region is shaped like a parabola

Finding $I_D = f(V_{GS}, V_{DS})$

- Approximate inversion charge $Q_N(y)$: drain is higher than the source → less charge at drain end of channel



Average Inversion Charge

Source End　　Drain End

$$Q_N(y) \approx -\frac{C_{ox}(V_{GS}-V_T)+C_{ox}(V_{GD}-V_T)}{2}$$

$$Q_N(y) \approx -\frac{C_{ox}(V_{GS}-V_T)+C_{ox}(V_{GS}-V_{SD}-V_T)}{2}$$

$$Q_N(y) \approx -\frac{C_{ox}(2V_{GS}-2V_T)-C_{ox}V_{SD}}{2} = -C_{ox}(V_{GS}-V_T-\frac{V_{DS}}{2})$$

- Charge at drain end is lower since field is lower
- Notice that this only works if the gate is inverted along its entire length
- If there is an inversion along the entire gate, it works well because Q is proportional to V everywhere the gate is inverted

Inversion Charge at Source/Drain

The charge under the gate along the gate, but we are going to make a simple approximation, that the average charge is the average of the charge near the source and drain

$$Q_N(y) \approx \frac{Q_N(y=0)+Q_N(y=L)}{2}$$

$$Q_N(y=0) = -C_{ox}(V_{GS}-V_{Tn})$$

$$Q_N(y=L) = -C_{ox}(V_{GD}-V_{Tn})$$

$$V_{GD} = V_{GS} - V_{DS}$$

Drift Velocity and Drain Current

"Long-channel" assumption: use mobility to find v

$$v(y) = -\mu_n E(y) \approx -\mu_n(-\Delta V/\Delta y) = \frac{\mu_n V_{DS}}{L}$$

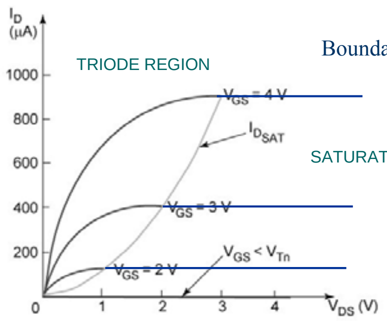
And now the current is just charge per area, times velocity, times the width:

$$I_D = -WvQ_N \approx W\mu\frac{V_{DS}}{L}C_{ox}(V_{GS}-V_T-\frac{V_{DS}}{2})$$

$$I_D \approx \frac{W}{L}\mu C_{ox}(V_{GS}-V_T-\frac{V_{DS}}{2})V_{DS}$$

Inverted Parabolas

Square-Law Characteristics



Boundary: what is $I_{D,SAT}$?

Square-Law Current in Saturation

Current stays at maximum (where $V_{DS} = V_{GS} - V_{Tn}$)

$$I_D = \frac{W}{L}\mu C_{ox}(V_{GS} - V_T - \frac{V_{DS}}{2})V_{DS}$$

$$I_{DS,sat} = \frac{W}{L}\mu C_{ox}(V_{GS} - V_T - \frac{V_{GS} - V_T}{2})(V_{GS} - V_T)$$

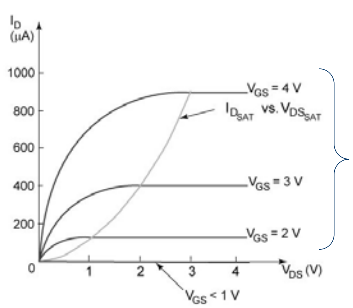
$$I_{DS,sat} = \frac{W}{L}\frac{\mu C_{ox}}{2}(V_{GS} - V_T)^2$$

Measurement: I_D increases slightly with increasing V_{DS}
model with linear "fudge factor"

$$I_{DS,sat} = \frac{W}{L}\frac{\mu C_{ox}}{2}(V_{GS} - V_T)^2(1 + \lambda V_{DS})$$

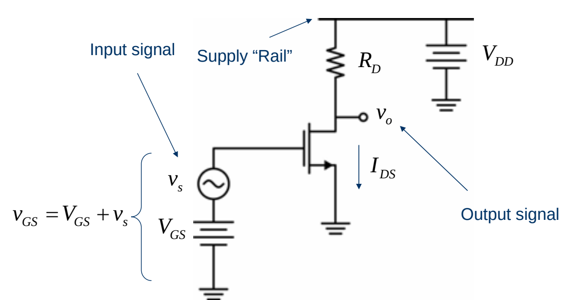
The Saturation Region

When $V_{DS} > V_{GS} - V_{Tn}$, there isn't any inversion charge at the drain … according to our simplistic model



Why do curves flatten out?

A Simple Circuit: An MOS Amplifier

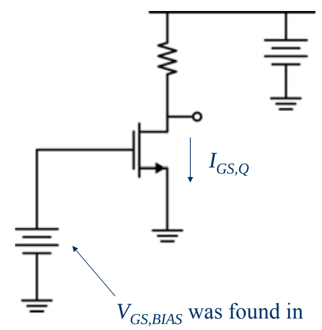


Small Signal Analysis

- Step 1: Find DC operating point. Calculate (estimate) the DC voltages and currents (ignore small signals sources)
- Substitute the small-signal model of the MOSFET/BJT/Diode and the small-signal models of the other circuit elements.
- Solve for desired parameters (gain, input impedance, …)

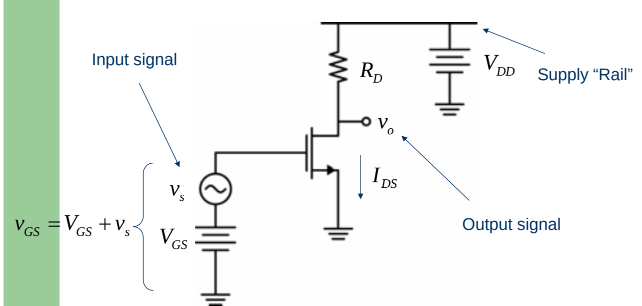
Small-Signal Analysis

Step 1. Find DC Bias – ignore small-signal source

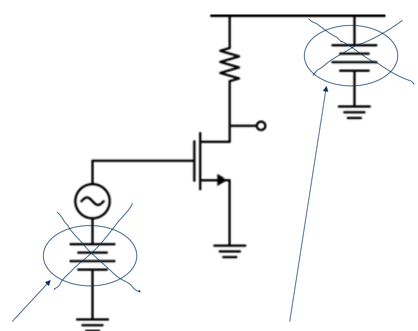


$V_{GS,BIAS}$ was found in Lecture 15

A Simple Circuit: An MOS Amplifier



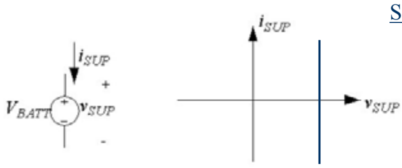
Small-Signal Modeling



What are the small-signal models of the DC supplies?

Shorts!

Small-Signal Models of Ideal Supplies

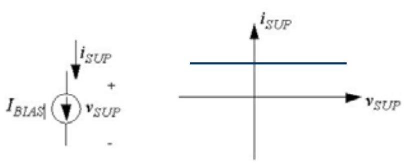


Small-signal model:

$$g_{supply} = \frac{\partial i_{supply}}{\partial v_{supply}} = \infty$$

$$r_{supply} = 0$$

short



$$g_{supply} = \frac{\partial i_{supply}}{\partial v_{supply}} = 0$$

$$r_{supply} = \infty$$

open

Low-Frequency Voltage Gain

Consider first ω → 0 case … capacitors are open-circuits

$$v_{out} = -g_m v_s \left(R_D \,\|\, r_o\right)$$

$$A_v = -g_m \left(R_D \,\|\, r_o\right)$$

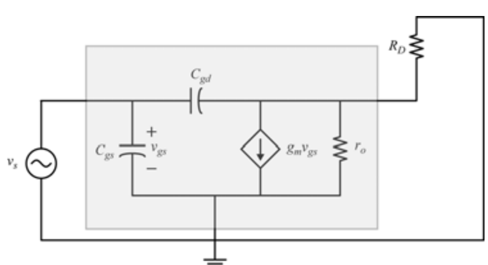
Design Variable

Transconductance

$$g_m = \mu_n C_{ox} \frac{W}{L}(V_{GS} - V_T) = \frac{2 I_{D,SAT}}{V_{GS} - V_T}$$

Design Variables

Small-Signal Circuit for Amplifier



Voltage Gain (Cont.)

Substitute transconductance:

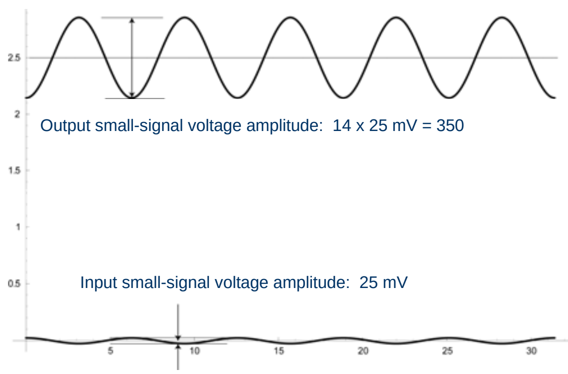
$$A_v = \left(-\frac{2 I_{D,SAT}}{V_{GS} - V_T}\right)\left(R_D \,\|\, r_o\right) \longrightarrow g_m R_D$$

Output resistance: typical value $\lambda_n = 0.05\ V^{-1}$

$$r_o = \left(\frac{1}{\lambda_n I_{D,SAT}}\right) = \left(\frac{1}{0.05 \cdot 0.1}\right) k\Omega = 200\, k\Omega$$

Voltage gain: $A_v = -\left(\frac{2 \cdot 0.1}{0.32}\right)\left(25 \,\|\, 200\right) = -14.3$

Input and Output Waveforms



Maximum Output Amplitude

$v_{out}(t)$= -2.18 V cos(ωt) → $v_s(t)$ = 152 mV cos(ωt)

How accurate is the small-signal (linear) model?

$$\frac{v_s}{V_{GS} - V_{Tn}} = \frac{0.152}{0.32} \approx 0.5$$

Significant error in neglecting third term in expansion of $i_D = i_D(v_{GS})$

What Limits the Output Amplitude?

1. $v_{OUT}(t)$ reaches V_{SUP} or 0 … or

2. MOSFET leaves constant-current region and enters triode region

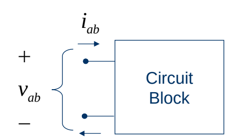
$$V_{DS} \le V_{DS,SAT} = V_{GS} - V_{Tn} = 0.31\,\text{V}$$

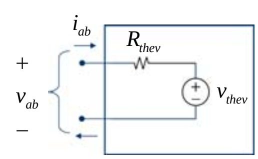
$$v_{o,MIN} = V_{DS,SAT} = 0.32\,\text{V}$$

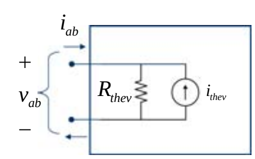
$$amp = 2.5 - 0.32\text{V} = 2.18\text{V}$$

One-Port Models (EECS 40)

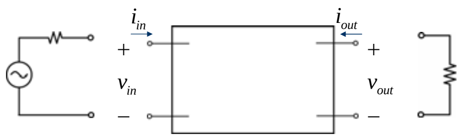
- A terminal pair across which a voltage and associated current are defined





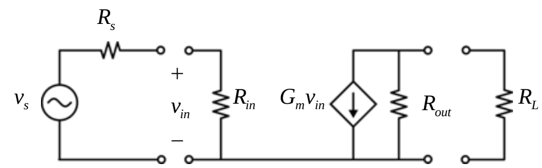


Small-Signal Two-Port Models

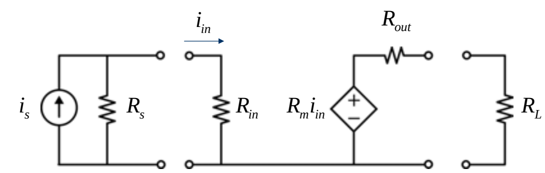


- We assume that input port is linear and that the amplifier is *unilateral*:
  - Output depends on input but input is independent of output.
- Output port : depends linearly on the current and voltage at the input and output ports
- Unilateral assumption is good as long as “overlap” capacitance is small (MOS)

Two-Port Small-Signal Amplifiers

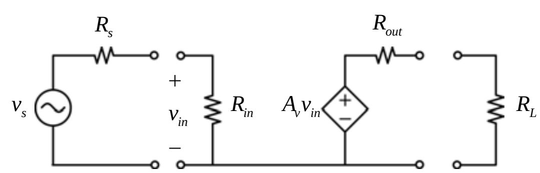


Transconductance Amplifier

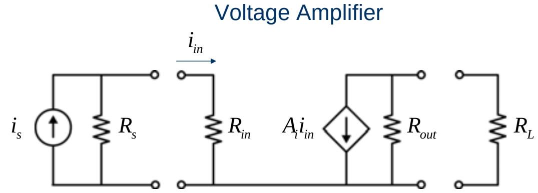


Transresistance Amplifier

Two-Port Small-Signal Amplifiers

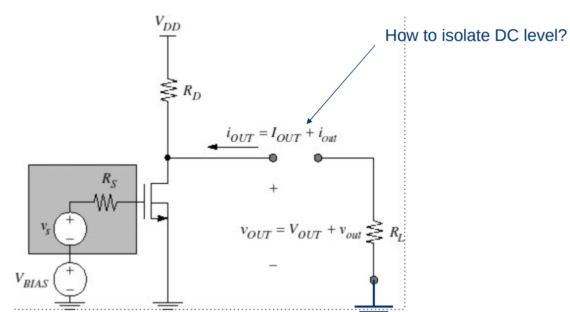


Voltage Amplifier



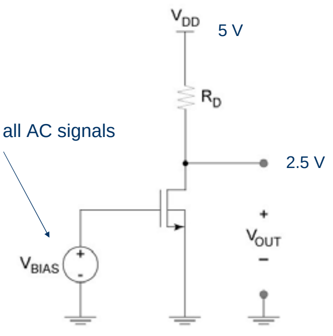
Current Amplifier

Common-Source Amplifier (again)



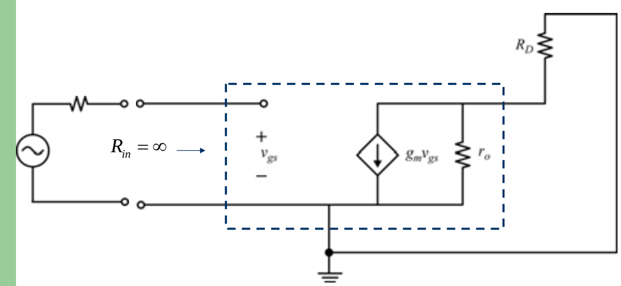
DC Bias

Neglect all AC signals



Choose I_{BIAS}, W/L

Small-Signal Analysis

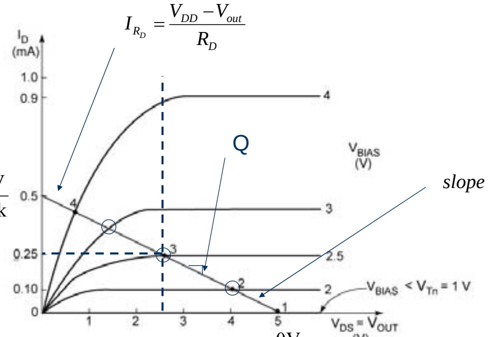


Load-Line Analysis to find *Q*

$$I_{R_D} = \frac{V_{DD} - V_{out}}{R_D}$$

$$I_D = \frac{5\text{V}}{10\text{k}}$$

$$slope = \frac{1}{10\text{k}}$$

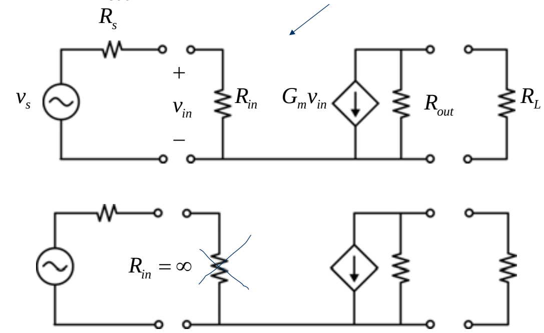


$$I_D = \frac{0\text{V}}{10\text{k}}$$

Two-Port Parameters:

Find R_{in}, R_{out}, G_m

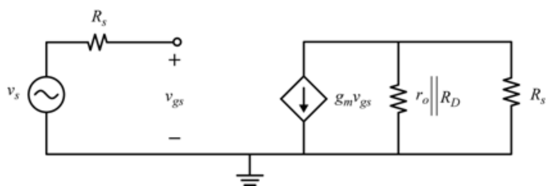
Generic Transconductance Amp



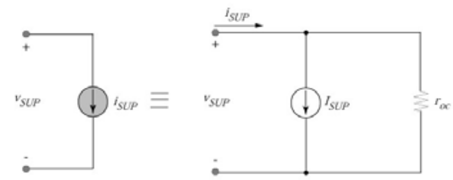
$G_m = g_m$ $R_{out} = r_o \parallel R_D$

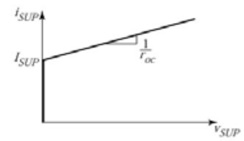
Two-Port CS Model

Reattach source and load one-ports:



Current Source Supply





- Solution: Use a current source!
- Current independent of voltage for ideal source

Maximize Gain of CS Amp

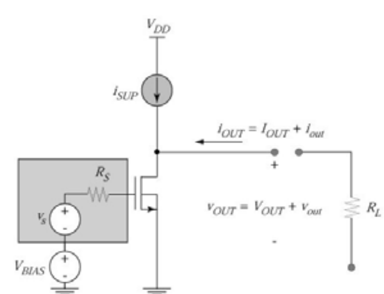
$$A_v = -g_m R_D \| r_o$$

- Increase the g_m (more current)
- Increase R_D (free? Don't need to dissipate extra power)
- Limit: Must keep the device in saturation

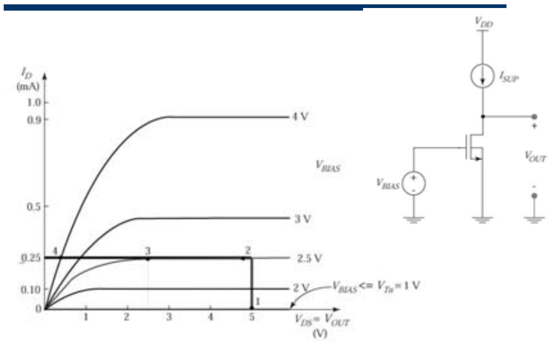
$$V_{DS} = V_{DD} - I_D R_D > V_{DS,sat}$$

- For a fixed current, the load resistor can only be chosen so large
- To have good swing we'd also like to avoid getting too close to saturation

CS Amp with Current Source Supply

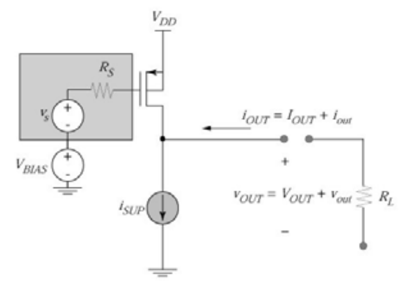


Load Line for DC Biasing



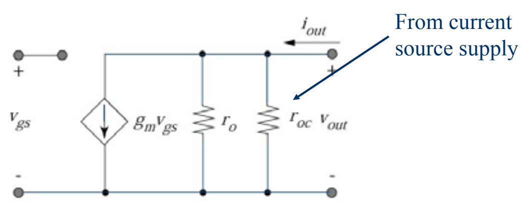
Both the I-source and the transistor are idealized for DC bias analysis

P-Channel CS Amplifier



DC bias: $V_{SG} = V_{DD} - V_{BIAS}$ sets drain current $-I_{Dp} = I_{SUP}$

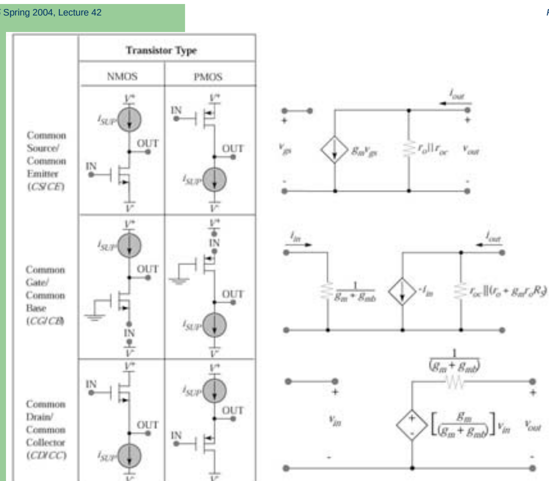
Two-Port Parameters



$$R_{in} = \infty$$

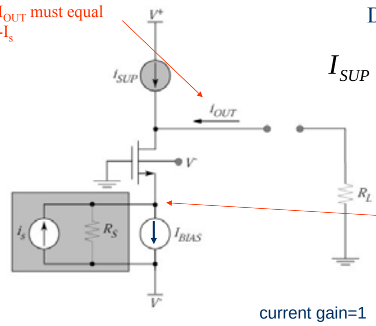
$$G_m = g_m$$

$$R_{out} = r_o \,||\, r_{oc}$$



Common Gate Amplifier

Notice that I_{OUT} must equal $-I_s$



DC bias:

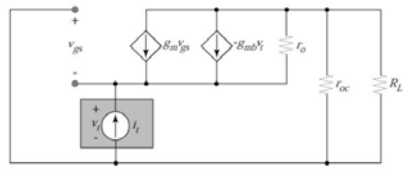
$$I_{SUP} = I_{BIAS} = I_{DS}$$

Gain of transistor tends to hold this node at ss ground: low input impedance load for current input

current gain=1
Impedance buffer

CG Input Resistance

$$v_{gs} = -v_t$$

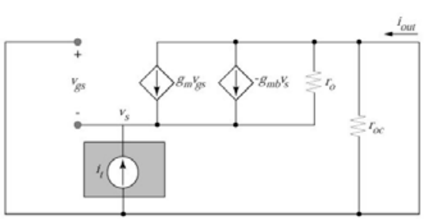


At input: $i_t = -g_m v_{gs} + g_{mb} v_t + \left(\frac{v_t - v_{out}}{r_o}\right)$

Output voltage: $v_{out} = -i_d (r_{oc} \| R_L) = i_t (r_{oc} \| R_L)$

$$i_t = g_m v_t + g_{mb} v_t + \left(\frac{v_t - (r_{oc} \| R_L) i_t}{r_o}\right)$$

CG as a Current Amplifier: Find A_i



$$i_{out} = i_d = -i_t$$

$$A_i = -1$$

Approximations…

- We have this messy result

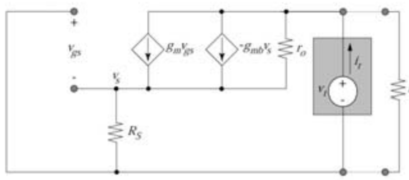
$$\frac{1}{R_{in}} = \frac{i_t}{v_t} = \frac{g_m + g_{mb} + \frac{1}{r_o}}{1 + \frac{r_{oc} \| R_L}{r_o}}$$

- But we don't need that much precision. Let's start approximating:

$$g_m + g_{mb} >> \frac{1}{r_o} \qquad r_{oc} \| R_L \approx R_L \qquad \frac{R_L}{r_o} \approx 0$$

$$R_{in} = \frac{1}{g_m + g_{mb}}$$

CG Output Resistance



$$\frac{v_s}{R_S} - g_m v_{gs} - (-g_{mb} v_s) + \frac{v_s - v_t}{r_o} = 0$$

$$v_s \left(\frac{1}{R_S} + g_m + g_{mb} + \frac{1}{r_o} \right) = \frac{v_t}{r_o}$$

Approximating the CG R_{out}

$$R_{out} = r_{oc} \,||\, [r_o + g_m r_o R_S + g_{mb} r_o R_S + R_S]$$

The exact result is complicated, so let's try to make it simpler:

$$g_m \approx 500\mu S \quad g_{mb} \approx 50\mu S \quad r_o \approx 200k\Omega$$

$$R_{out} \cong r_{oc} \,||\, [r_o + g_m r_o R_S + R_S]$$

Assuming the source resistance is less than r_o,

$$R_{out} \approx r_{oc} \,||\, [r_o + g_m r_o R_S] = r_{oc} \,||\, [r_o (1 + g_m R_S)]$$

CG Output Resistance

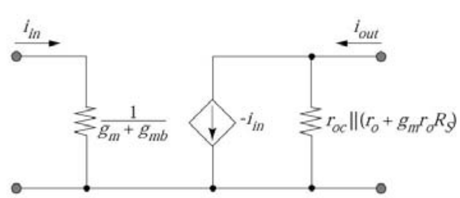
Substituting $v_s = i_t R_S$

$$i_t R_S \left(\frac{1}{R_S} + g_m + g_{mb} + \frac{1}{r_o} \right) = \frac{v_t}{r_o}$$

The output resistance is $(v_t / i_t) \,||\, r_{oc}$

$$R_{out} = r_{oc} \,||\, \left(R_S \left(\frac{r_o}{R_S} + g_m r_o + g_{mb} r_o + 1 \right) \right)$$

CG Two-Port Model

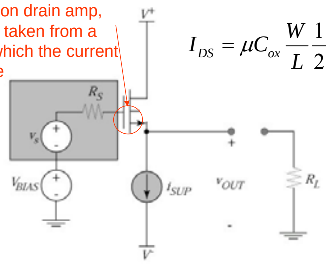


Function: a current buffer

- Low Input Impedance
- High Output Impedance

Common-Drain Amplifier

In the common drain amp, the output is taken from a terminal of which the current is a sensitive function

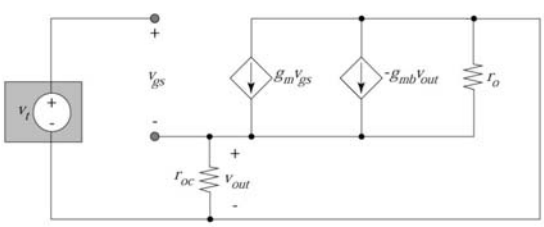


$$I_{DS} = \mu C_{ox} \frac{W}{L} \frac{1}{2} (V_{GS} - V_T)^2$$

$$V_{GS} = V_T + \sqrt{\frac{2 I_{DS}}{\mu C_{ox} \frac{W}{L}}}$$

Weak I_{DS} dependence

CD Voltage Gain



Note $v_{gs} = v_t - v_{out}$

$$\frac{v_{out}}{r_{oc} \| r_o} = g_m v_{gs} - g_{mb} v_{out}$$

$$\frac{v_{out}}{r_{oc} \| r_o} = g_m (v_t - v_{out}) - g_{mb} v_{out}$$

CD Voltage Gain (Cont.)

KCL at source node: $\frac{v_{out}}{r_{oc} \| r_o} = g_m (v_t - v_{out}) - g_{mb} v_{out}$

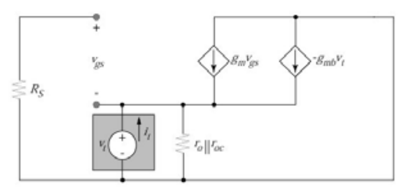
$$\left(\frac{1}{r_{oc} \| r_o} + g_{mb} + g_m \right) v_{out} = g_m v_t$$

Voltage gain (for v_{SB} not zero):

$$\frac{v_{out}}{v_{in}} = \frac{g_m}{\frac{1}{r_{oc} \| r_o} + g_{mb} + g_m}$$

$$\frac{v_{out}}{v_{in}} \approx \frac{g_m}{g_{mb} + g_m} \approx 1$$

CD Output Resistance



Sum currents at output (source) node:

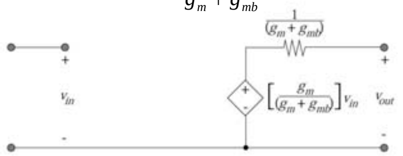
$$R_{out} = r_o \| r_{oc} \| \frac{v_t}{i_t} \qquad i_t = g_m v_t + g_{mb} v_t$$

$$R_{out} \approx \frac{1}{g_m + g_{mb}}$$

CD Output Resistance (Cont.)

$r_o \| r_{oc}$ is much larger than the inverses of the transconductances → ignore

$$R_{out} \approx \frac{1}{g_m + g_{mb}}$$

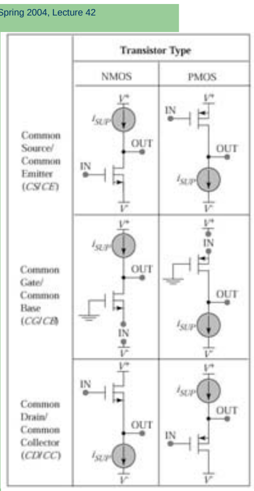


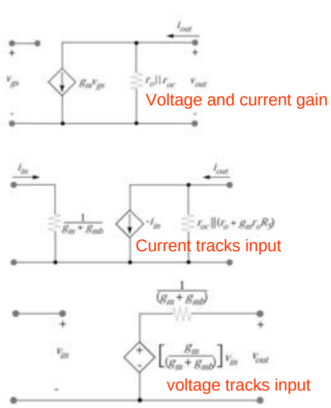
Function: a voltage buffer

- High Input Impedance
- Low Output Impedance

Bias sensitivity

- When a transistor biasing circuit is designed, it is important to realize that the characteristics of the transistor can vary widely, and that passive components vary significantly also.
- Biasing circuits must therefore be designed to produce a usable bias without counting on specific values for these components.
- One example is a BJT base bias in a CE amp. A slight change in the base-emitter voltage makes a very large difference in the quiescent point. The insertion of a resistor at the emitter will improve sensitivity.



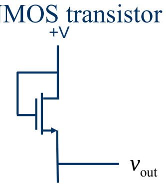


Insensitivity to transistor parameters

- Most of the circuit parameters are independent of variation of the transistor parameters, and depend only on resistance ratios. That is often a design goal, but in integrated circuits we will not want to use so many resistors.

NMOS pullup

- Rather than using a big (and expensive) resistor, let's look at a NMOS transistor as an active pullup device

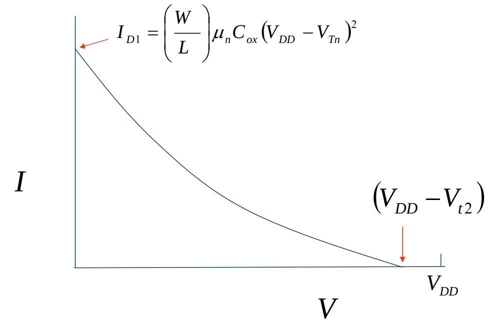


Note that when the transistor is connected this way, it is not an amplifier, it is a two terminal device. When the gate is connected to the drain of this NMOS device, it will be in saturation, so we get the equation for the drain current:

$$I_D = \left(\frac{W}{2L}\right)\mu_n C_{ox}\left(V_{SG} - V_{Tn}\right)^2\left(1 + \lambda_n V_{SD}\right)$$

IV for NMOS pull-up

- The I-V characteristic of this pull-up device:



Small signal model

- So we have:

$$I_D = \left(\frac{W}{2L}\right)\mu_n C_{ox}\left(V_{SG} - V_{Tn}\right)^2\left(1 + \lambda_n V_{SD}\right)$$

$$= \left(\frac{W}{2L}\right)\mu_n C_{ox}\left(\Delta V - V_{Tn}\right)^2\left(1 + \lambda_n \Delta V\right) \approx \left(\frac{W}{2L}\right)\mu_n C_{ox}\left(\Delta V - V_{Tn}\right)^2$$

- The N channel MOSFET's transconductance is:

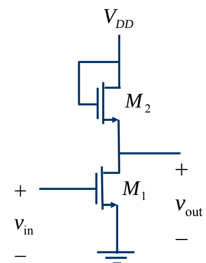
$$g_m = \frac{\partial}{\partial v_{SG}}\left(i_D\right)\Big|_Q = \left(\frac{W}{L}\right)\mu_n C_{ox}\left(V_{SG} - V_{Tn}\right) \cong \sqrt{2\left(\frac{W}{L}\right)\mu_n C_{ox}\left(I_D\right)}$$

- And so the small signal model for this device will be a resistor with a resistance:

$$r = \left(\frac{1}{g_m}\right)$$

Active Load

- We can use this as the pullup device for an NMOS common source amplifier:



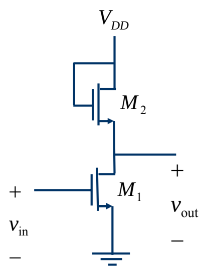
$$I_{D1} = \left(\frac{W_1}{2L_1}\right)\mu_n C_{ox}\left(V_{gs1} - V_{Tn1}\right)^2$$

$$I_{D2} = \left(\frac{W_2}{2L_2}\right)\mu_n C_{ox}\left(V_{gs2} - V_{Tn2}\right)^2$$

$$V_0 = V_{DD} - V_{gs2}$$

$$V_0 = V_{DD} - V_{t2} - \sqrt{\frac{2I_2}{\mu_n C_{ox}\left(W_2 / L_2\right)}}$$

Active Load



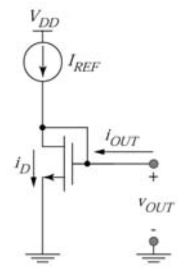
Since $I_2=I_1$ we have:

$$V_0 = V_{DD} - V_{t2} - \sqrt{\frac{2I_1}{\mu_n C_{ox}(W_2/L_2)}}$$

And since: $V_{gs1} = V_i$

$$V_0 = V_{DD} - V_{tn1} - \sqrt{\frac{(W_1/L_1)}{(W_2/L_2)}}(V_i - V_{t1})$$

CMOS Diode Connected Transistor



- Short gate/drain of a transistor and pass current through it
- Since VGS = VDS, the device is in saturation since VDS > VGS-VT
- Since FET is a square-law (or weaker) device, the I-V curve is very soft compared to PN junction diode

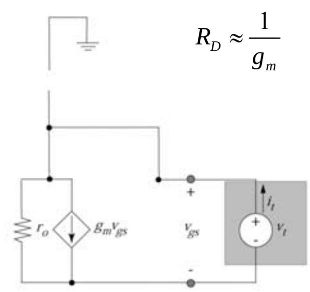
Behavior

- If the output voltage goes higher than one threshold below VDD, transistor 2 goes into cutoff and the amplifier will clip.
- If the output goes too low, then transistor 1 will fall out of the saturation mode.
- Within these limitations, this stage gives a good linear amplification.

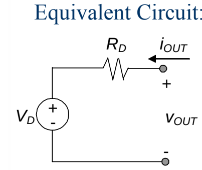
Diode Equivalent Circuit

$$R_D = \left(\left. \frac{di_{OUT}}{dv_{OUT}} \right|_{I_{OUT}=0} \right)^{-1} = \frac{v_t}{i_t}$$

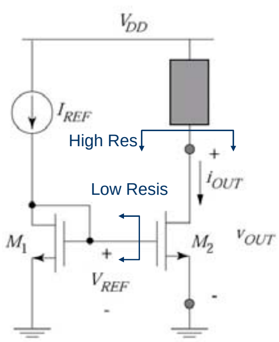
$$R_D \approx \frac{1}{g_m}$$



Equivalent Circuit:

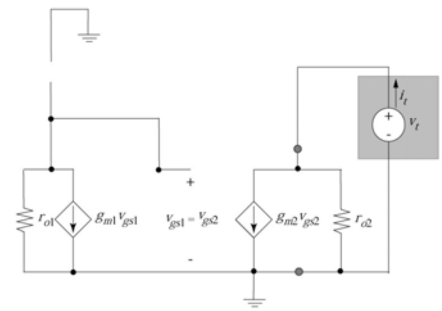


The Integrated "Current Mirror"

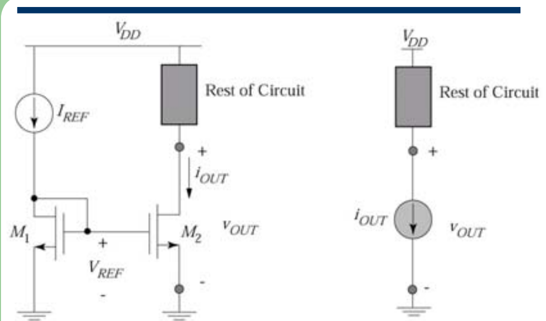


- M_1 and M_2 have the same V_{GS}
- If we neglect CLM (λ=0), then the drain currents are equal
- Since λ is small, the currents will nearly mirror one another even if V_{out} is not equal to V_{GS1}
- We say that the current I_{REF} is mirrored into i_{OUT}
- Notice that the mirror works for small and large signals!

Small-Signal Resistance of *I*-Source



Current Mirror as Current Sink

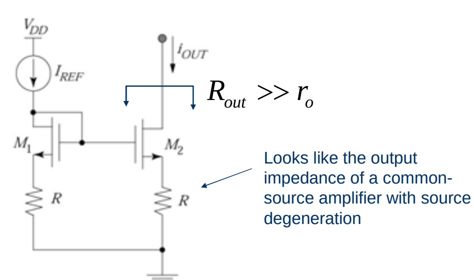


- The output current of M_2 is only weakly dependent on v_{OUT} due to high output resistance of FET
- M2 acts like a current source to the rest of the circuit

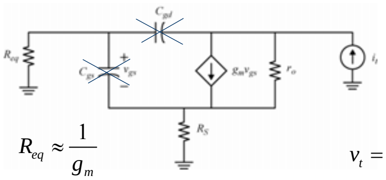
Improved Current Sources

Goal: increase r_{oc}

Approach: look at *amplifier* output resistance results … to see topologies that boost resistance



Effect of Source Degeneration



$$v_t = (i_t - g_m v_{gs})r_o + v_{R_S}$$

$$v_{gs} \approx -v_{R_S}$$

$$v_{R_S} = i_t R_S$$

$$R_{eq} \approx \frac{1}{g_m}$$

$$v_t = (i_t + g_m R_S i_t) r_o + i_t R_S$$

$$R_o = \frac{v_t}{i_t} \approx (1 + g_m R_S) r_o$$

- Equivalent resistance loading gate is dominated by the diode resistance … assume this is a small impedance
- Output impedance is boosted by factor $(1 + g_m R_S)$

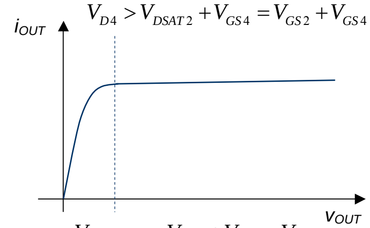
Drawback of Cascode *I*-Source

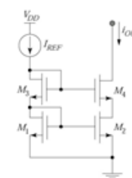
Minimum output voltage to keep both transistors in saturation:

$$V_{OUT,MIN} = V_{DS4,MIN} + V_{DS2,MIN}$$

$$V_{DS2,MIN} > V_{GS2} - V_{T0} = V_{DSAT2}$$

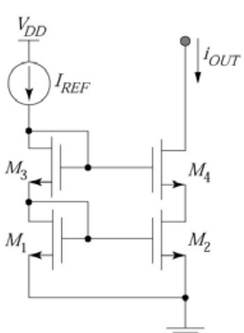
$$V_{D4} > V_{DSAT2} + V_{GS4} = V_{GS2} + V_{GS4} - V_{T0}$$





$$V_{OUT,MIN} = V_{GS2} + V_{GS4} - V_{T0}$$

Cascode (or Stacked) Current Source



Insight: V_{GS2} = constant AND
V_{DS2} = constant

Small-Signal Resistance r_{oc}:

$$R_o \approx (1 + g_m R_S) r_o$$

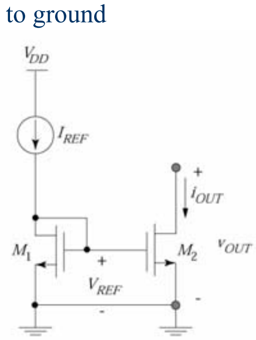
$$R_o \approx (1 + g_m r_o) r_o$$

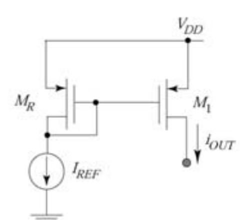
$$R_o \approx g_m r_0^2 >> r_o$$

Current Sinks and Sources

Sink: output current goes to ground

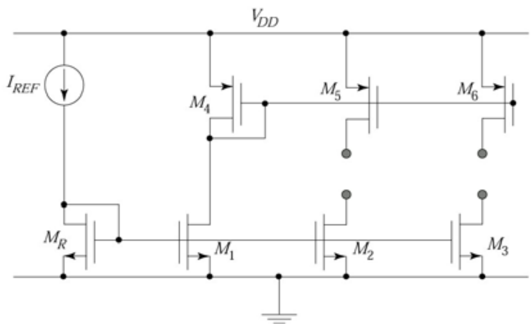
Source: output current comes from voltage supply





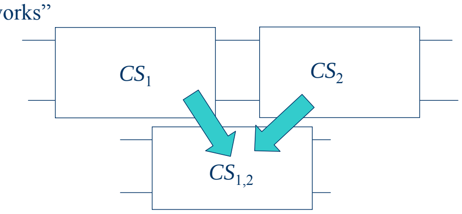
Current Mirrors

We only need one reference current to set up all the current sources and sinks needed for a multistage amplifier.



Start: Two-Stage Voltage Amplifier

- Use two-port models to explore whether the combination "works"



Results of new 2-port: $R_{in} = R_{in1,}\ R_{out} = R_{out2}$

$$A_v = -G_{m1}\left(R_{in2} \,||\, R_{out1}\right)\times\left(-G_{m2}R_{out2}\right)$$

$$A_v = G_{m1}G_{m2}\left(R_{in2} \,||\, R_{out1}\right)\left(R_{out2}\right)$$

Summary of Cascaded Amplifiers

General goals:

1. Boost the gain (except for buffers)
2. Improve frequency response
3. Optimize the input and output resistances:

	R_{in}	R_{out}
Voltage:	∞	0
Current:	0	∞
Transconductance:	∞	∞
Transresistance:	0	0

Cascading stages

Input resistance: ∞

Voltage gain (2-port parameter):

$$A_v = -g_{m1}\left(r_{o1} \,||\, r_{oc1}\right)\times g_{m2}\left(-r_{o2} \,||\, r_{oc2}\right)$$

Output resistance:

$$R_{out} = \frac{1}{g_m + g_{mb}}$$