4 Fully Depleted Devices
FDSOI and FinFET

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CONTENTS

4.1 Overview 71
4.2 Introduction: Challenges of Conventional CMOS Technology 72
4.3 Gate-Length Scaling in Fully Depleted Devices 76
4.4 Planar Fully Depleted Devices 77
    4.4.1 Process Challenges 79
    4.4.2 Performance Boosters 80
    4.4.3 Scalability 81
4.5 FinFETs: Bulk and SOI 82
    4.5.1 Process Considerations 86
    4.5.2 Performance Boosters for FinFETs 87
    4.5.3 Extendibility 88
4.6 Nanowires and Vertical Transistors 90
4.7 Conclusions 91
References 93

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4.1 OVERVIEW

In this chapter, we first review the major issues facing conventional complementary metal–oxide–semiconductor (CMOS) scaling. We then introduce the basics of a fully depleted device operation and discuss how fully depleted devices overcome the barriers that limit conventional scaling. In addition, bulk and silicon (Si) on insulator (SOI) FinFETs are compared and contrasted. The attributes of a planar fully depleted silicon on insulator (FDSOI) are reviewed and also compared with FinFETs. Finally, the ultimate fully depleted device option, a nanowire transistor, is presented and its benefits and drawbacks are shown.

In order to meet the requirement of doubling the transistor density from one node to the next, the contacted gate pitch (CGP) is reduced by 30% per node as shown in Figure 4.1. The lithography community has developed several innovative solutions to pattern features smaller than the wavelength of light using diffraction techniques, immersion lithography, double patterning, cut masks, and other approaches. The advent of extreme ultraviolet (EUV) lithography has also facilitated

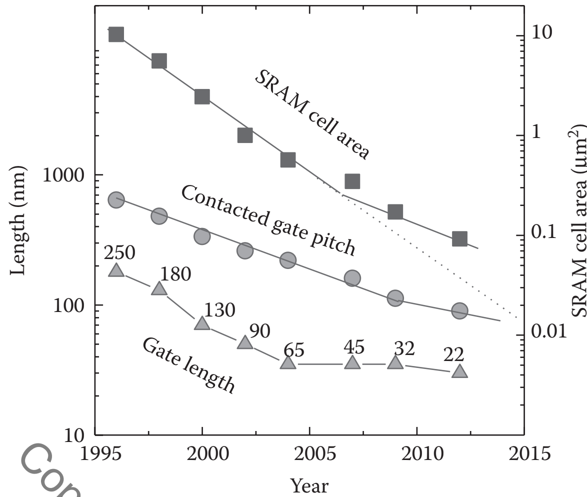

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FIGURE 4.1 CMOS scaling trend over a period of roughly two decades. The CGP is scaled by 0.7 per node, which enables the total number of transistors to increase by a factor of 2 for a given area. (Note that device isolation and metal pitch are also scaled at roughly the same rate as CGP to enable overall density scaling.) Interestingly, during the period from the 65 nm node to the 32 nm node, the CGP scaled but the gate length did not scale much.

the miniaturization of critical features. However, the demand on the gate length is particularly challenging. In previous technology nodes, the distances between gates have been large relative to the gate length. In present and future technology nodes, however, the distance between gates is small relative to the gate length itself. This necessitates the need for gate-length scaling. Beyond the physical challenge of shrinking device dimensions, there is a significant challenge to maintain the electrostatic integrity of the transistors. In the past, this was accomplished through gate dielectric scaling, channel doping, and extension optimization. These conventional techniques are no longer capable of controlling short-channel effects. New device architectures are needed to continue the scaling trend. In addition to controlling electrostatics, transistor performance is key to every technology node. Thus, transistors must be simultaneously scaled with good electrostatics as well as performance. This chapter describes the issues associated with conventional scaling and explores the alternatives to conventional scaling.

4.2 INTRODUCTION: CHALLENGES OF CONVENTIONAL CMOS TECHNOLOGY

For the past several decades, the consumer electronics market has benefited enormously from the continued scaling of semiconductor devices. Additionally, big businesses have enjoyed unprecedented increases in productivity largely due to CMOS scaling. The increased density and miniaturization of transistors due to CMOS scaling have been accomplished through advances in patterning, device design, and

TABLE 4.1
Dennard's Scaling Theory

Parameter	Scaling Factor
Device dimension *tox*, *L*, *W*	1/*k*
Doping concentration *Na*	*K*
Voltage *V*	*1/k*
Current *I*	*1/k*
Capacitance *eA/t*	*1/k*
Delay time per circuit *VC/I*	*1/k*
Power dissipation per circuit	*VI* 1/*k* 2
Power density *VI/A*	1

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process technology. Although CMOS scaling has been an evolutionary process, several abrupt changes have enabled the industry to keep on track.

A prescription for conventional scaling was proposed by Dennard et al. in 1974 [1]. The semiconductor industry moved forward for many generations according to Dennard's scaling theory as shown in Table 4.1. The major benefits of scaling are that the circuits switch faster with less power consumption and device dimensions scale so circuit density increases. The industry followed this scaling theory for several decades.

One of the hallmarks of scaling is that the distance between transistors or CGP decreases for every generation of technology and this enables a significantly smaller static random-access memory (SRAM) cell size. A plot of the gate length, CGP, and the SRAM cell size as a function of technology node and year is shown in Figure 4.1. As the gate length decreases, however, it becomes more challenging to maintain electrostatic control of the gate over the channel and the transistor becomes more difficult to turn off. In order to prevent this, electrostatics or short-channel effects can be controlled by thinning the gate dielectric to provide stronger coupling between the gate and the channel. The channel doping (halo dose) can also be increased to control the short-channel effects and the source–drain (S/D) extension junctions can be made shallower to reduce the influence of the drain potential on the channel.

Figure 4.1 shows significant gate-length scaling from the 250 to the 65 nm node. However, a dramatic slowdown of gate-length scaling from the 65 to the 22 nm node can also be observed. This slowdown is in part due to the physical limitation of gate dielectric scaling. When a conventional SiO_2 gate dielectric is scaled below about 2.0 nm, it must be heavily nitrided or it will not pass reliability requirements. Also, gate leakage can be excessive at these thin film thicknesses. Nitrided gate dielectrics are used to scale the equivalent oxide thickness (EOT) to about 1.2 nm with acceptable reliability and gate leakage. The slowdown in gate dielectric scaling not only prevents appreciable gate-length scaling but also poses a significant challenge for device performance. Drive current and gate dielectric scaling are nearly linearly proportional. That is, when the gate dielectric gets thinner, the drive current increases. Although advancements in high-κ gate dielectrics have enabled some gate-oxide scaling, this scaling may not be a consistently sustainable element

leading to continued gate-length scaling. The CGP requirement for nodes beyond 22 nm requires gate-length scaling to ensure that the gate can fit into the pitch. This problem has been temporarily put on hold with the advent of self-aligned contacts. However, gate-length scaling is needed for advanced technology nodes.

Conventional device design methodology seeks to scale gate length while enabling higher drive currents with fixed or lower off-currents. If S/D extensions can be made shallower through advanced doping and annealing then the gate can gain more control over the channel and the gate length can be scaled. In addition, if the S/D extensions can be made more abrupt, they can be placed in closer proximity to the channel and the drive current can be increased due to the enhanced coupling between the inversion layer and the extension when the transistor is turned on. The halo, which is opposite-type doping compared with the extension, can also help to form an abrupt extension by cutting the tail of the extension. That is, the extension tail can diffuse and extend into the channel. The halo can counteract the electrical effects of the diffuse extension tail, thereby forming a more abrupt extension. However, channel or halo doping has several detrimental effects. First, as the gate gets smaller, more halo doping is needed to help control the charge sharing between the source and the drain. This higher channel doping leads to mobility degradation. If the channel doping is too high, the junction formed between the halo and the extension leads to significant gate-induced drain leakage (GIDL), which results in an increased off-current. Ironically, the halo, which is used to control short-channel effects, when used in extremely short-channel devices ultimately causes higher off-currents. Additionally, the junction between the source and the drain regions and the well tends to increase the off-current. Figure 4.2 shows the leakage mechanisms for a conventional transistor.

In addition, the halo doping causes excessive threshold voltage variations through random dopant fluctuations (RDF), especially for small active area devices such as SRAM field-effect transistors (FETs). This is especially problematic for low-power applications where minimum voltage requirements are important.

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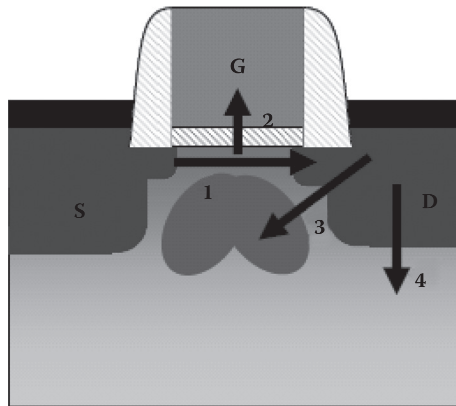

FIGURE 4.2 Leakage mechanisms for conventional transistors: (1) subthreshold leakage, (2) gate leakage, (3) GIDL, and (4) junction leakage.

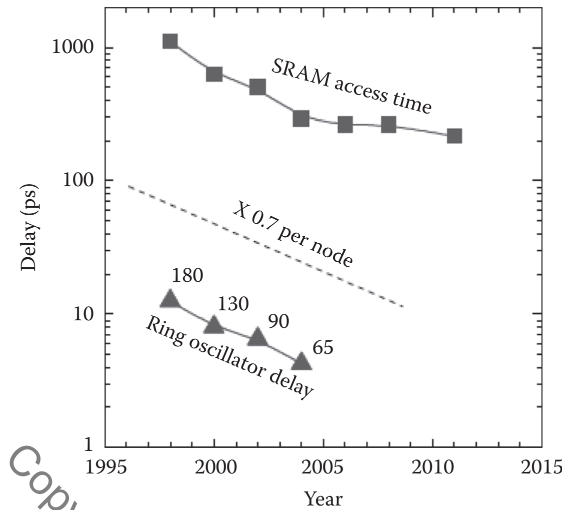

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FIGURE 4.3 Scaling trend of ring oscillator delay (FO = 1) and SRAM access time over several technology nodes. Performance slowdown is evident for 65–32 nm nodes despite an increase in the dc performance.

Figure 4.3 shows the performance trends for some recent technology nodes. Up until about the 130 nm node, performance gains were achieved through standard scaling according to Dennard's scaling theory. Since the 90 nm node, innovations in local mechanical stress techniques such as stressed contact etch stop layers [2], embedded silicon–germanium (SiGe) [3], and the stress memorization technique (SMT) [4] were introduced. These techniques were used to enhance channel mobility and made up the performance boosters that were needed for several generations during the time period when gate dielectrics and gate-length scaling stayed relatively constant.

Another aspect of technology performance is parasitic capacitance. As the CGP decreases, the gate to contact distance gets smaller, leading to increased parasitic capacitance. Although we will not completely address the issue in this chapter, parasitic capacitance is a very important part of advanced technologies. While the ac performance can be improved by increasing the dc performance of the devices through mobility enhancement techniques, this leads to increased power unless higher mobility is traded for a lower operating voltage. Gate-height scaling and low-κ spacers [5] can reduce parasitic capacitance. A reduction in parasitic capacitance leads to improvements in the ac performance without increasing power. Whichever device architecture is used, parasitic capacitance cannot be ignored. On the contrary, any new device architecture for advanced technology nodes will have extremely tight ground rules and therefore will require innovative approaches to mitigate parasitic capacitances.

Conventional scaling is nearing its limits due to the lack of gate dielectric scaling and also the ineffectiveness of channel doping at high halo doses. In order to

continue the technology scaling trend, new device architectures are needed. These new architectures must have the ability to scale gate length and improve device performance.

4.3 GATE-LENGTH SCALING IN FULLY DEPLETED DEVICES

Gate-length scaling for fully depleted devices* is governed by fundamentally different principles compared with conventional transistors. While gate dielectric scaling, extension, and halo engineering are all somewhat useful, it is the body thickness that is the strongest parameter in gate-length scaling for fully depleted devices. There are two main classes of fully depleted devices, planar FDSOI devices and FinFETs. In the case of FDSOI, the relationship between the gate length and the channel thickness should be about 4:1 for the channel thickness to control the short-channel effects. In the case of FinFET, the ratio of gate length to channel thickness should be about 2:1, thus allowing for a thicker channel at the same gate length. However, it should be noted that it may be easier to form a thinner planar channel and monitor the thickness throughout the process with well-established techniques than to form and monitor a 3-D fin structure, even though the fin can be made somewhat thicker. Figure 4.4 shows the relationship between drain-induced barrier lowering (DIBL) and channel thickness for fully depleted and conventional devices [6].

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$$\text{Conventional DIBL} = 0.8\frac{\varepsilon_{Si}}{\varepsilon_{ox}}\left(1+\frac{X_j^2}{L_{el}^2}\right)\frac{T_{ox}}{L_{el}}\frac{T_{dep}}{L_{el}}V_{ds}$$

$$\text{FDSOI DIBL} = 0.8\frac{\varepsilon_{Si}}{\varepsilon_{ox}}\left(1+\frac{T_{Si}^2}{L_{el}^2}\right)\frac{T_{ox}}{L_{el}}\frac{T_{Si}}{L_{el}}V_{ds}$$

$$\text{FinFET DIBL} = 0.8\frac{\varepsilon_{Si}}{\varepsilon_{ox}}\left(1+\frac{T_{Si}^2/4}{L_{el}^2}\right)\frac{T_{ox}}{L_{el}}\frac{T_{Si}/2}{L_{el}}V_{ds}$$

FIGURE 4.4 The relationship between DIBL and channel thickness (T_{Si}) for conventional and fully depleted devices. From the equations, it can be seen that the DIBL is a strong function of the junction depth (X_j) for conventional devices, while it is a strong function of the channel thickness T_{Si} in the case of fully depleted devices [16]. Smaller X_j and thinner T_{Si} lead to better DIBL for conventional and fully depleted devices, respectively. T_{ox}, gate oxide thickness; L_{el}, electrical channel length; T_{dep}, depletion width in a bulk planar MOSFET; V_{ds}, source-drain voltage; ε_{Si} and ε_{ox}, permittivity of Si and gate oxide, respectively.

* Note that although the term *fully depleted* is commonly used to refer to devices with a relatively thin channel, such as planar FDSOI and SOI or bulk FinFET, where the device electrostatic is mostly governed by the channel thickness, a better terminology is to refer to these devices as thin channel. Fully depleted is only meaningful in SOI devices in contrast to partially depleted SOI and does not necessarily mean that the channel is thin enough to control device electrostatics.

4.4 PLANAR FULLY DEPLETED DEVICES

FDSOI is a planar device architecture built on an SOI substrate. The thin channel is used to suppress the leakage from source to drain and to eliminate the junction leakage path. Figure 4.5 is a schematic representation of an FDSOI transistor showing the leakage paths. The path for junction leakage and GIDL is suppressed by utilizing an extremely thin channel isolated from the substrate by a buried oxide (BOX). The thin channel on the BOX forces isolated junctions and shallow extensions. It also reduces the coupling between the drain potential and the channel, especially if a relatively thin BOX is used, by terminating the electric fields that originate from the drain in the substrate as opposed to the channel, and thus enabling the gate to have more control over the channel.

Even without halo and aggressive gate-oxide scaling, short-channel transistors with excellent electrostatics have been demonstrated. Figure 4.6 shows the transfer and output characteristics of FDSOI transistors with 22 nm gate lengths. The channel thickness is 6 nm, the subthreshold slope is well below 100 mV/dec, and the DIBL is well controlled [7].

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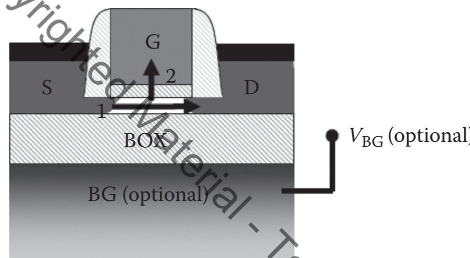

FIGURE 4.5 Schematic of an FDSOI transistor showing the two major leakage paths: (1) subthreshold leakage and (2) gate leakage. Junction leakage is eliminated as a result of the BOX isolation and GIDL is minimized as a result of the undoped channel.

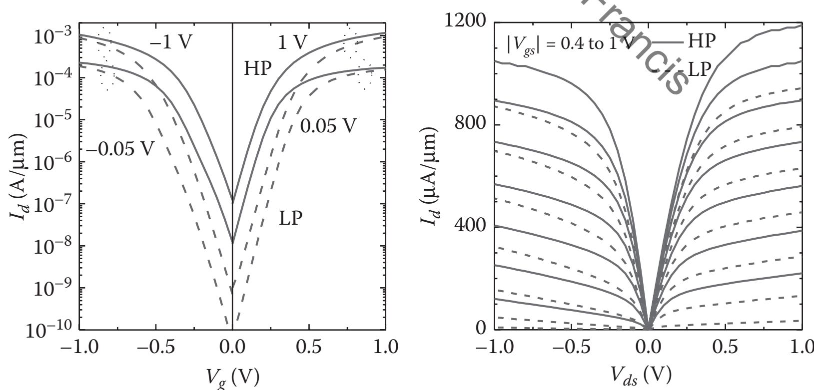

FIGURE 4.6 I_d–V_g and I_d–V_d characteristics of FDSOI transistors with a channel thickness of 6 nm and gate length of 22 nm showing excellent subthreshold behavior and competitive drive currents. (From Cheng, K. et al., *Symposium on VLSI Technology*, pp. 128–129, 14–16 June, Honolulu, HI, 2011.)

To avoid channel doping, threshold voltages can be adjusted by using a different work function metal gate for each FET type. Another approach for V_t adjustment for FDSOI technologies is to use ground-plane doping and/or back-gate biasing [8]. To enable V_t tuning, FDSOI can be built on SOI substrates with thin BOX ($T_{BOX} < 50$ nm). Figure 4.7 schematically shows an example of a combination of dual work function integration, ground-plane doping, and proper use of the channel material (Si vs. SiGe) to offer a wide range of V_t without doping the channel or changing the gate length. The possibility of V_t tuning without the need for channel doping is especially important as it leads to record low device variability by avoiding RDF [8].

The threshold voltage response to ground-plane doping and back-gate bias is shown in Figure 4.8. Ground-plane (back-gate) doping can be used to create a threshold voltage difference between a given FET type. Plots of a negative channel

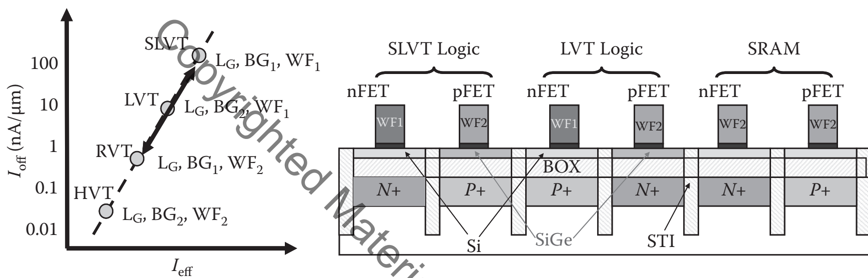

FIGURE 4.7 A possible multi-V_t scheme for FDSOI with thin BOX. Ground-plane doping, gate work function, and channel material (Si vs. SiGe) are used to adjust V_t without introducing channel doping. In addition, back bias can be used to tune V_t either statically or dynamically after device fabrication.

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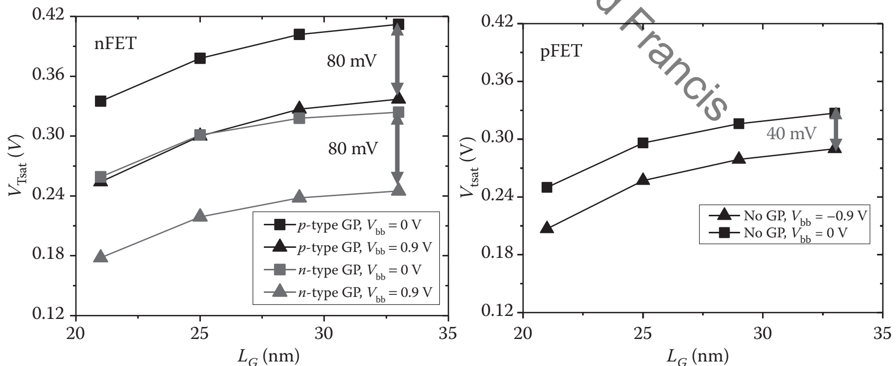

FIGURE 4.8 Threshold voltage as a function of L_G for thin BOX FDSOI FETs with different ground-plane doping and back-gate biasing. The plots show that ground-plane doping and back biasing are both effective techniques to modulate V_t. Notice that the roll-off characteristics are predominately independent of ground-plane doping and back biasing in the range of these conditions. (From Liu, Q. et al., *Symposium on VLSI Technology*, pp. 61–62, 15–17 June, Honolulu, HI, 2010.)

field-effect transistor (nFET) threshold voltage with *n*- and *p*-type ground-plane doping with a T_{BOX} of 25 nm are shown in Figure 4.6 [8]. The figure shows an approximately 80 mV difference in threshold voltages for thin BOX FDSOI FETs with *n*- and *p*-type ground-plane doping. The same figure also shows the response of the threshold voltage to back-gate biasing. The use of ground-plane doping and back-gate biasing is a practical approach to threshold voltage adjustment, which does not depend on channel doping. The back-gate biasing is a very powerful option that can be used to center V_t's even after processing. Back biasing can be used to compensate for small differences in process fluctuation, thereby improving yield. It can also be used for power management. That is, transistor V_t can be adjusted depending on the workload of the circuit. When and where a higher performance is needed, V_t can be lowered to deliver a higher drive current, while in standby mode V_t can be increased to reduce leakage. It should be noted that back biasing is possible in bulk planar devices and, in fact, circuit designers have used it in the past. However, in recent nodes it has become less effective as the V_t tuning range is very small. FDSOI enables a significantly larger range of V_t tuning by allowing either an *n*-type or a *p*-type ground plane for each transistor polarity, by eliminating the path for junction leakage, and by suppressing GIDL.

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4.4.1 Process Challenges

FDSOI fabrication in high-volume manufacturing faces several challenges. The film thickness uniformity and roughness of Si are critical parameters. Figure 4.9 shows the response of the threshold voltage to the channel film thickness. Precise control of the channel thickness is needed to minimize V_t variations [9]. Current state-of-the-art manufacturing techniques have been developed to ensure a film thickness control of better than ±5 Å within a wafer and from wafer to wafer [10]. In addition,

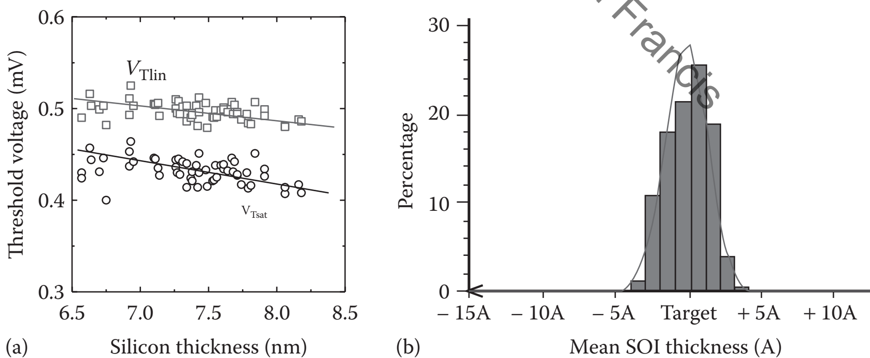

FIGURE 4.9 (a) Threshold voltage as a function of silicon thickness, indicating that the V_t sensitivity is about 25 mV/nm. (From Khakifirooz, A. et al., *International Symposium on VLSI Technology Systems and Applications (VLSI-TSA)*, pp. 110–111, 26–28 April, Hsinchu, Taiwan, 2010.) (b) Si thickness uniformity control attained in wafer production. The distribution of wafers is well within the ±5 Å specification. (From Bonnin, O., *Fully Depleted SOI Workshop*, 28 April, Hsinchu, Taiwan, 2011.)

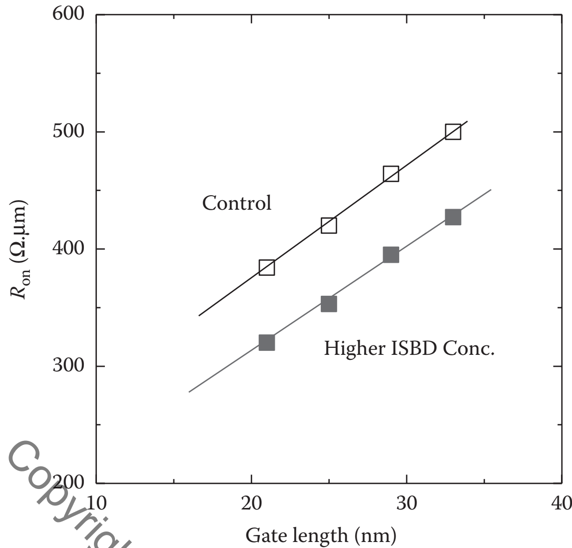

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FIGURE 4.10 Reduction in the transistor resistance obtained by using a SiGe raised/source–drain process with higher boron concentration in the epitaxy. (From Cheng, K. et al., *IEEE International Electron Devices Meeting (IEDM) Technical Digest*, pp. 3.2.1–3.2.3, 49–52 December, Washington, DC, 2009.)

a variety of well-established methods such as atomic force microscopy (AFM) and scatterometry can be used to monitor the thickness at different length scales throughout the process.

A thin silicon channel requires some attention to make sure that it is not completely consumed during gate and spacer patterning. Etch processes must be optimized and closely monitored. However, with some additional precautions, the silicon can be easily maintained. Selective epitaxy is also needed to reduce external resistance in the source and drain regions. New and innovative techniques have been used to prevent amorphization of silicon during extension formation. *In situ* boron and phosphorus doping have been out-diffused from SiGe and Si:C, respectively, to form abrupt and highly activated junctions. Figure 4.10 shows the improvement in total on-state resistance (R_{on}) that can be achieved by optimizing the *in situ* SiGe process used to simultaneously form extensions and raised S/D [11].

4.4.2 Performance Boosters

Although local mechanical stress techniques have been used to boost performance since the 90 nm node, pitch scaling has reduced the efficiency of the external stressors. Channel strain, on the other hand, is independent of the gate pitch, but requires new materials and new integration techniques. The SiGe channel has been used with gate-first technology since the 32 nm node mainly to obtain a low threshold voltage for positive channel field-effect transistor (pFETs). However, the technique has

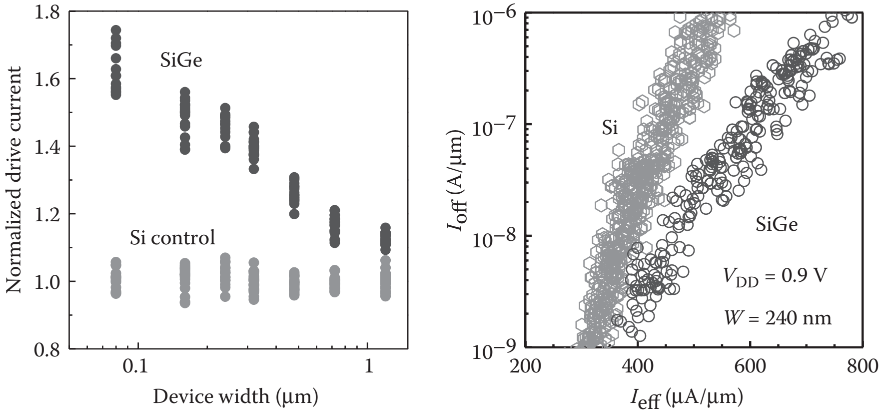

FIGURE 4.11 As the device width is reduced from 1 μm to about 50 nm, the drive current increases by over 50% demonstrating the effectiveness of the channel strain in the case of a 25% SiGe channel. The plot on the right shows the short-channel device performance improvement for SiGe channel strain at $W = 240$ nm compared with the Si channel. (From Cheng, K. et al., *IEEE International Electron Devices Meeting (IEDM) Technical Digest*, pp. 18.1.1–18.1.4, 10–13 December, San Francisco, CA, 2012.)

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been demonstrated to be very effective in boosting performance, especially in narrow devices [12]. In an FDSOI structure, however, the total channel thickness should be kept to less than about 6 nm. So, there is no room for an epitaxially grown bilayer of SiGe on Si. The Ge condensation technique was used to fabricate FDSOI devices with thin SiGe channels and significant performance enhancement over Si devices was demonstrated [13]. In addition, it was demonstrated that the biaxial strain in the SiGe channel transforms into uniaxial strain along the current flow direction as the active area becomes narrower [14]. For technologically relevant channel widths, there is a significant enhancement in the short-channel device performance as shown in Figure 4.11.

Similarly, strained Si directly on insulator (SSDOI) has been demonstrated to significantly enhance the nFET performance for FDSOI devices [13]. Earlier demonstrations of SSDOI technology used ion implantation to form extensions and S/Ds, which are known to relax the strain. Thus, the full benefit of SSDOI substrates was not shown until the advent of implant-free junctions formed by *in situ P*-doped or phosphorus doped epitaxy. With this approach, all of the strain in the channel is maintained and very impressive drive currents have been shown (Figure 4.12).

4.4.3 Scalability

Scalability is another key question for any device architecture. Typically, there is a significant investment in design infrastructure and yield learning for any particular device architecture. Thus, to realize a compelling return on investment, device architectures must be scalable for multiple generations. The main parameter in controlling

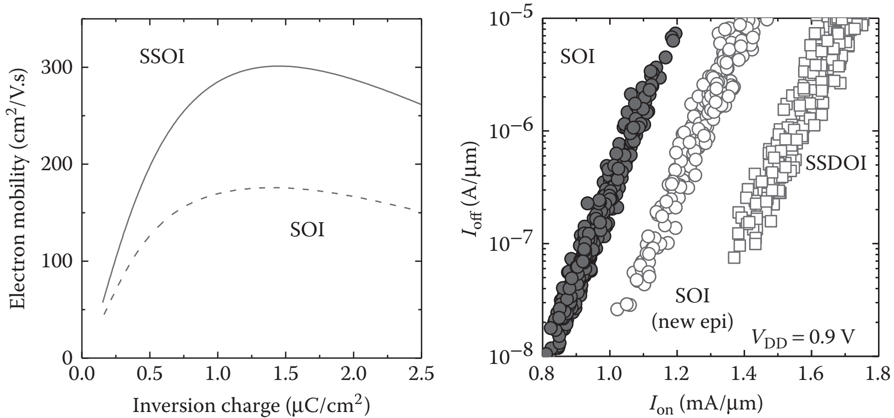

FIGURE 4.12 Electron mobility for FDSOI devices built on an SSDOI substrate showing a 75% improvement in long-channel mobility and a 27% improvement in short-channel performance. Optimized *in situ* phosphorus-doped source–drain epitaxy results in a 20% improvement in short-channel performance. (From Khakifirooz, A. et al., *Symposium on VLSI Technology*, pp. 117–118, 12–14 June, Honolulu, HI, 2012.)

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short-channel effects in FDSOI devices is T_{Si} scaling. As the channel becomes thinner, process challenges grow. A process must be specifically designed and optimized for extremely thin silicon. However, these challenges are not fundamental in nature and can be overcome with modest efforts. Figure 4.13 compares the transistor characteristics for FDSOI devices with 6 and 3.5 nm channels. The plots clearly show the improvement in drain-induced barrier lowering (DIBL) for the thinner channel with no degradation in its performance. Another parameter for gate-length scaling is reverse back bias. Even with the thicker channel, the reverse back bias enables a substantial improvement in short-channel control with small impact on the performance. BOX scaling enables a stronger V_t response for a given voltage or enables a similar V_t response for a lower voltage. BOX scaling also leads to improved short-channel control. Figure 4.14 shows simulation results for DIBL as a function of the BOX thickness, demonstrating the effectiveness of BOX thickness scaling to control short-channel effects.

4.5 FinFETs: BULK AND SOI

Bulk FinFET has been implemented in 22 nm node technology [15,16]. The device operation principles of bulk FinFET are very similar to conventional devices. Bulk FinFET can be thought of as a conventional FET with a very narrow width. Shallow trench isolation (STI) is pulled down so that the gate can wrap around the channel. Bulk FinFETs technologies may have some optional channel doping to adjust the

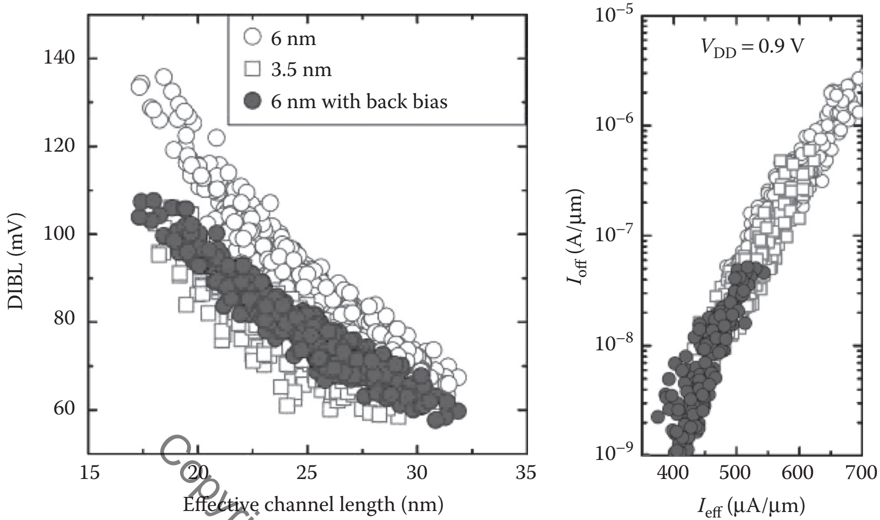

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FIGURE 4.13 DIBL vs. effective channel length comparing 6 and 3.5 nm channels. Also shown is a 6 nm channel device with reverse back bias to increase the confinement of electrons near the gate interface. The 3.5 nm channel device and the reverse back-biased devices show improvement in DIBL while maintaining a performance similar to non-back-biased 6 nm channel [17]. (From Khakifirooz, A. et al., *IEEE Electron Dev. Lett.*, 33, 149–151, 2012.)

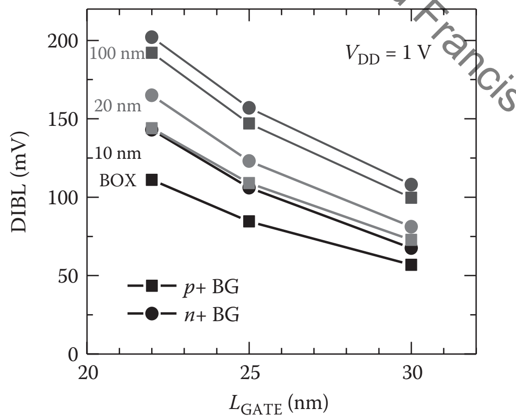

FIGURE 4.14 Simulation of DIBL vs. L_G demonstrating the improvement in DIBL as the BOX is made thinner.

threshold voltage. In contrast to the conventional FET where the channel doping is used to control short-channel effects, in the FinFET it is the fin thickness that predominantly controls the short-channel effects. One of the defining features of bulk FinFETs is that junctions are used to isolate the source from the drain to prevent punch-through or leakage from the source to the drain. The so-called punch-through implant is an opposite dopant type compared with the source and the drain, for example, boron in an nFET. It is typically a blanket implant that is placed underneath the source, drain, and channel. A schematic cross section perpendicular and parallel to the bulk fin showing the leakage paths is illustrated in Figure 4.15. One can see that since the gate is wrapping around the fin (Figure 4.15a), it has more control over the subthreshold leakage. Ironically, the cross section perpendicular to the gate (Figure 4.15b) looks identical to the cross section of the conventional FET shown in Figure 4.2. Thus, although the gate has more control over the channel, bulk FinFET architecture does not overcome the fundamental issues associated with junction leakage and GIDL. The SOI FinFET is shown in Figure 4.16 for comparison. As can be seen, there is no need for junction isolation in the SOI FinFET due to the natural isolation enabled by the BOX.

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Multiple thresholds can be achieved using a variety of different approaches. Three main variables for V_t adjustment of FinFET are doping the channel, gate work function, and L_G adjustment. Each one of these knobs has their advantages and disadvantages. Adding another gate stack with a work function that is appropriate to moving the V_t to the desired value is an attractive option. However, there is additional process complexity and yield concern associated with the addition of another gate stack. Therefore, this option has not been implemented in the current FinFET manufactured in the 22 or 14 nm node. Increasing channel doping can lead to excessive junction leakage, increased random doping fluctuation [18], and mobility degradation. On the other hand, channel implantation is a very straightforward approach to adjust V_t's with a high degree of flexibility, excellent accuracy, and precision. While there is no need for channel doping to control the device electrostatics and hence FinFET can have a lower doping level compared with bulk planar devices for a given threshold

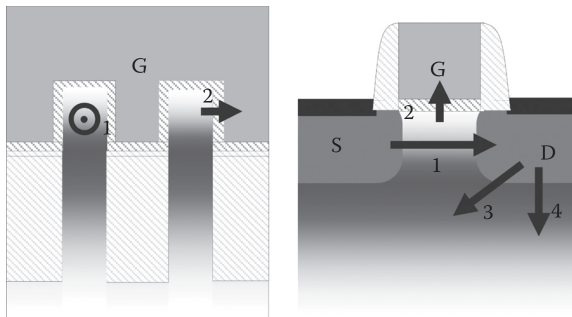

FIGURE 4.15 Schematic cross sections of bulk FinFET (a) perpendicular to the fin and (b) parallel to the fin showing leakage paths: (1) subthreshold leakage, (2) gate leakage, (3)≈GIDL, and (4) junction leakage.

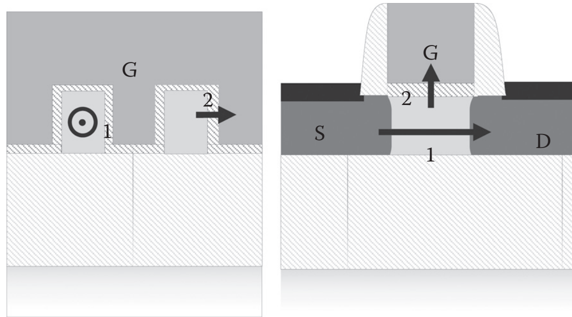

FIGURE 4.16 Schematic cross sections of an SOI FinFET (a) perpendicular to the fin and (b) parallel to the fin, showing leakage paths: (1) subthreshold leakage and (2) gate leakage. Unlike bulk FinFET, the S/D regions are isolated from the substrate by BOX and there is no need for a punch-through stop implant. However, channel doping might be needed to set the V_t.

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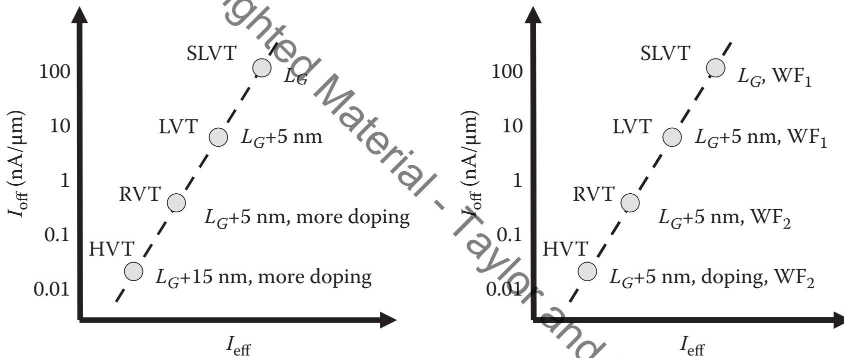

FIGURE 4.17 Plots of I_{off} vs. I_{eff} for FinFETs for two possible multi-V_t schemes. Gate stack work function, channel doping, and L_G can be used in different combinations to achieve multi-V_t options for bulk and SOI FinFETs.

voltage, due to the smaller volume of the depletion region compared with the bulk planar, higher doping density is required to achieve a given V_t shift. Increasing the gate length is another approach that was extensively used in conventional CMOS. As the gate length shortens, the V_t decreases due to the short-channel effect (threshold voltage roll-off). However, because fully depleted devices typically have much lower DIBL and the roll-off curve is flatter compared with conventional devices, a larger modulation of L_G is needed to have an appreciable impact on V_t. In some cases, an increase of 5–10 nm in L_G is needed to achieve targets for high V_t (HVT) devices. Since the CGP is very aggressive for advanced technologies, the increase in L_G needed for HVT devices cannot fit into the same pitch as the regular V_t devices. Thus, the HVT devices require a significant increase in CGP and this can lead to an overall increase in chip size. Figure 4.17a shows a typical multi-V_t solution, similar to

that proposed in [16,19] using a combination of channel doping and L_G modulation. The HVT in both technologies ended up needing a CGP that was 20% longer than the nominal device. Clearly, this is not a viable path forward as the technology continues to scale. Alternatively, as in the case of the FDSOI architecture (Figure 4.7), bulk or SOI FinFET can also use the SiGe channel as an additional knob to adjust V_t. This will be equivalent to one additional work function and hence a possible multi-V_t solution as shown in Figure 4.17b is conceivable.

4.5.1 Process Considerations

There are several significant process and integration challenges for FinFETs. Bulk FinFETs in particular have a very high aspect ratio. Typical fin height dimensions are in the range of 100–200 nm for fin height with a fin pitch of 40–70 nm or less. At these aggressive dimensions, STI fill becomes increasingly difficult. There are several solutions to the STI fill challenge including flowable oxides and cyclic deposition techniques where films are repeatedly deposited and etched to form a high-quality fill. Figure 4.18 shows a cross section of a bulk fin and an SOI fin. The taper on the bulk fin is considerably greater than that of the SOI fin. The additional taper angle is advantageous for facilitating STI fill without voids. On the other hand, the tapered fin can lead to degraded short-channel control and higher leakage since the fin thickens toward its base. Having a degraded short-channel control, the thicker portion of the fin will dominate the subthreshold leakage. On the other hand, STI fill is not an issue for SOI FinFETs because the BOX serves as a built-in isolation structure, which not only isolates neighboring fins but also neighboring devices where traditionally an STI was needed. The fin has a uniform thickness, which enables good short-channel control over the entire active area.

Fin height definition is another challenge that is unique to bulk FinFET. The channel of a bulk FinFET is defined by junction isolation as well as STI recess. This places a great demand on the STI etch-back or fin-reveal process. The channel height uniformity is directly proportional to the fin recess uniformity. Thus, if the fin recess has a nonuniformity of ±5%, the active area will be nonuniform by the same amount. The fin height for the SOI FinFET, on the other hand, is defined by the uniformity

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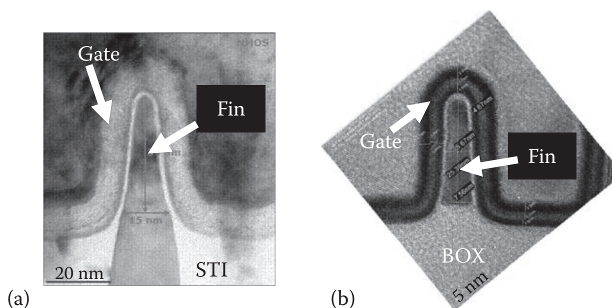

FIGURE 4.18 Cross sections of a typical (a) bulk and (b) SOI fin. The bulk fin is tapered to facilitate the STI fill while there is no need for STI in the SOI fin.

of the initial substrate since the fin etch lands on the BOX. As shown in the previous section, substrate film thickness uniformity can be extremely well controlled.

The punch-through stop junction is defined early in the process flow, which means that it is subject to a significant thermal budget that leads to diffusion of the dopants into the channel region. Overall, the smaller area of the FinFET junctions leads to lower junction leakage relative to conventional devices. However, as discussed earlier, more doping is required to adjust V_t's to enable multi-V_t devices. Thus, GIDL and junction leakage are concerns for bulk FinFET.

There are other process challenges for FinFETs relative to conventional and planar FDSOI technologies. Namely, spacer and gate etch are significantly different compared with planar FETs. Spacer formation is particularly challenging for three-dimensional architecture. In a conventional or planar FDSOI FET, the spacer etch must remove spacer nitride materials from horizontal surfaces while leaving the spacer nitride on the sidewall portion of the gate. Spacer etch for FinFETs, on the other hand, requires removing spacer materials from the horizontal surfaces and also the vertical portions of the fin that are not covered by the gate electrode. At the same time, the FinFET spacer etch must leave spacer nitride on the sidewall of the gate to prevent unwanted electrical connections or shorts from the raised S/D to the gate.

While there are many new process challenges for FinFET because it is a new device architecture, the process and integration communities have devised many innovative solutions that have enabled both bulk and SOI FinFET to be viable for high-volume production.

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4.5.2 Performance Boosters for FinFETs

Embedded stressors, SMT, and dual stress liner are local mechanical stress techniques that were used to enhance the channel mobility and boost the performance of conventional devices. Advanced technology nodes with aggressive CGP have little or no room to allow dual stress liner to be effective. There is also little room left in the S/D for efficient strain engineering through embedded SiGe or SMT. While it is argued that such strain engineering methods may still work in a FinFET structure [20], an analysis of the experimental data from first-generation FinFET technologies [15,16] shows small performance gain from strain elements. In addition to the ever-smaller area available for strain elements, the 3-D structure of FinFET poses new challenges in strain engineering. For example, technology computer-aided design (TCAD) simulations show a nonuniform strain profile along the height of the fin, with maximum strain observed at the top of the fin and significantly smaller strain at the bottom [21]. As such, the average strain in the channel is considerably smaller than the values observed in the bulk planar CMOS. It should be noted that the nonuniform strain distribution is not unique to FinFET as such profiles are also seen in bulk planar devices. However, in a planar device only the strain at the top surface is important, where it is actually at its maximum.

Channel strain engineering, similar to what was discussed in the previous section for planar FDSOI devices is more promising. In fact, the observation in Figure 4.11 with regard to an increase in the device performance as the transistor width narrows is very interesting. Since FinFET by its nature is a very narrow device, the transverse component of the strain is completely relaxed and the strain will be purely

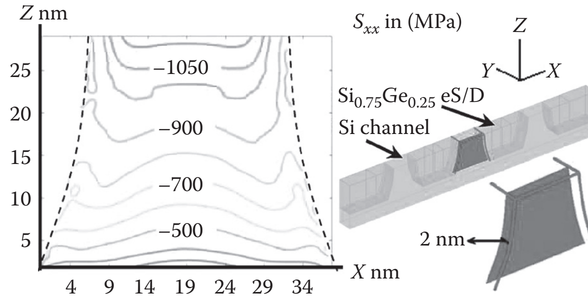

FIGURE 4.19 Strain distribution through the channel of a FinFET showing nonuniform strain along the fin height. (From Mujumdar, S., Maitra, K., and Datta, S., *IEEE Trans. Electron Dev.*, 59, 72–78, 2012.)

uniaxial. More than 25% of the nFET performance boost has already been demonstrated in FinFETs fabricated on strained SOI wafers [22]. More importantly, it has been shown that the strain benefit is observed even at 64 nm CGP. To date, no other strain element has been demonstrated to be effective at such device pitch. Similarly, SiGe fins can be used to enhance the pFET performance [23]. Nonetheless, a major concern with channel strain engineering in a FinFET structure is to form defect-free and strained fins that are tall enough to deliver a competitive current.

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4.5.3 Extendibility

Many technologists consider the major concern in device scaling to be the ability to shrink the gate length and still maintain good electrostatics. Studies have thus been performed to investigate the effect of scaling the fin thickness and the associated degradation in carrier mobility [24]. While this is a valid concern, an equally important question is how to scale the device width. In a planar technology, a typical device width scales at a rate of roughly 30% per generation. So, in the absence of performance boosters, current drive and front-end-of-line (FEOL) capacitance also scale at roughly 30% per node. If back-end-of-line (BEOL) capacitances also scale at the same rate, which is to the first order a valid assumption, given that the average wiring length scales as the technology shrinks, scaling of the device width results in a roughly 30% reduction in active power per generation at constant performance and the power density remains constant. Strain elements did not change this paradigm significantly: a higher performance comes at the price of higher active power and power density unless a higher drive current is traded for a lower operating voltage. This is true because an increased drive current in strained engineered devices is not obtained at the expense of increased FEOL capacitance. With the emergence of FinFET, however, a paradigm shift in CMOS design will show up. FinFETs typically have a higher effective device width at a given footprint when compared with planar devices. In fact, this is often used as an argument in favor of FinFET and is used to justify the normalization of a drive current per footprint as opposed to a true device width [15,16]. However, this higher drive current comes at the expense of higher FEOL capacitance. For instant, early experimental data showed degradation in both

the intrinsic and extrinsic transistor cutoff frequency (f_T) in FinFETs compared with bulk planar devices [25]. Hence, it is arguable whether FinFET offers the same power scaling from node to node that CMOS circuits enjoyed for many generations.

Moving forward, scaling of the device width and the associated scaling in the FEOL capacitance, drive current, and ultimately active power is a major question for circuit designers and technologists. Several paradigms are conceivable: (1) keep the fin density constant and increase the fin height; (2) shrink the fin spacing at a rate proportional to the metal pitch scaling and keep the fin height roughly unchanged; and (3) shrink the fin spacing at a rate proportional to the metal pitch scaling and scale the fin height at roughly the same rate. The first option may result in increased current density per generation. Proponents of this choice argue for possibly increased performance. However, as noted above, it comes at the expense of higher power density. Moreover, since the transistor footprint needs to be scaled in proportion to the metal pitch, the number of fins per transistor decreases, leading to less flexibility in the circuit design. As far as the fabrication process is concerned, a taller fin also complicates gate and spacer reactive ion etch (RIE) and needs strategies to limit the lateral growth of S/D epitaxy. It will also complicate the use of strained fins as discussed in Section 4.5.2.

The second option also leads to increased current per footprint at each node, but the number of available fins per transistor remains roughly the same. Gate and spacer RIE remain roughly unchanged. Figure 4.20 shows a possible projection of

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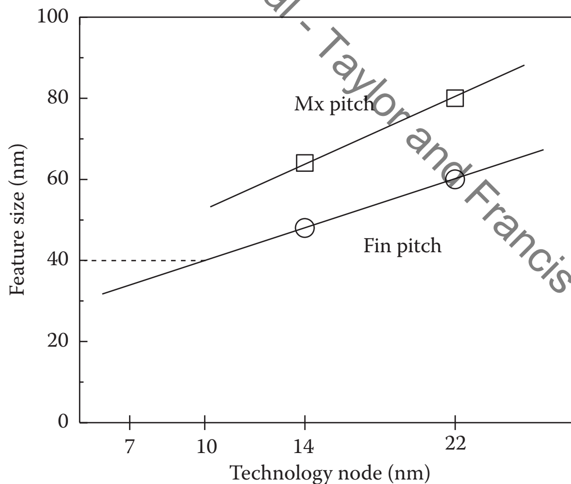

FIGURE 4.20 Scaling trend of the metal pitch and the fin pitch. At the 10 nm node, the fin pitch is expected to be around 40 nm, which is the limit of the sidewall image transfer (SIT) process if mandrels are printed with the current immersion lithography. In order to continue fin pitch scaling at the 7 nm node and beyond, either multiple applications of the SIT process or techniques such as directional self-assembly should be used. (Data points are from Auth, C. et al., *Symposium on VLSI Technology*, pp. 131–132, 12–14 June, Honolulu, HI, 2012; Wu, S.-Y. et al., *IEEE International Electron Devices Meeting (IEDM) Technical Digest*, pp. 9.1.1–9.1.4, 9–11 December, Washington, DC, 2013.)

metal pitch and fin pitch to 10 nm and beyond based on the data available at 22 and 16 nm FinFETs [15,16]. A fin pitch of roughly 40 nm is expected at the 10 nm node, which is at the limit of the sidewall image transfer (SIT) process if mandrels are defined by today's immersion lithography. Beyond this point, new methods such as the multiple application of the SIT process, EUV lithography, or directional self-assembly are needed to push the fin pitch to about 30 nm at the 7 nm node. Moreover, as the spacing between the fins becomes smaller, trimming unwanted portions of the fins, filling the gap with the gate stack material, and device isolation become more challenging.

Finally, the third option continues the historical trend of CMOS scaling by scaling the device width per each generation. It will also facilitate use of more exotic channel materials as the epitaxial growth of these materials often needs to deal with critical thickness and defect formation in thicker films.

4.6 NANOWIRES AND VERTICAL TRANSISTORS

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A further improvement in electrostatics without shrinking the body dimension can be accomplished by surrounding the body on all sides. Gate-all-around nanowires are often considered as the ultimate option for gate-length scaling [26]. Several challenges have to be addressed before a technologically relevant nanowire is demonstrated. First, the formation of the gate-all-around covering the bottom portion of the wire involves lateral undercutting of a dummy material, such as oxide or SiGe. This process often results in lateral etch not only in the desired direction to release the wire, but also toward the source and the drain. As a result, the gate overlap to the S/D extensions will be higher at the bottom of the wire, leading to higher parasitic capacitance. An efficient spacer formation process with uniform spacing around and at the bottom of the wire is also a challenge. Nanowires are often defined by the RIE process, meaning that further smoothing of the surface is needed [27]. Although the best electrostatic behavior will be obtained with a small round nanowire, to be competitive with FinFETs in terms of drive current per footprint as discussed in the first two scaling paradigms above, a stack of nanowires is probably preferred, with careful optimization of the wire dimensions to optimize the trade-off between current capability and electrostatics, as in Figure 4.21 [28].

Another possible scaling scenario is to use vertical transistors where the gate wraps around a nanowire or fin-like structure and the source and drain are formed on the top and bottom of the gate, as in Figure 4.22a. The main advantage of the vertical transistor is that it decouples the gate length and spacer thickness from the gate pitch. The transistor density is instead defined by the spacing between the source and drain contacts. Forming a contact with the bottom junction of the device is, however, a challenge. As such, vertical transistors are best suited as access transistors for memory elements, when only one of the S/D terminals is connected to the bit line and the other one is connected to the memory element directly below or above the transistor [29]. Forming layout-efficient vertical transistors that can be used in logic circuits for 7 nm and beyond remains a challenge. Moreover, while gate length is defined by a deposition process and not lithography and, as such, effects such as line edge roughness can be avoided, processes to form a spacer compatible with state-of-the-art

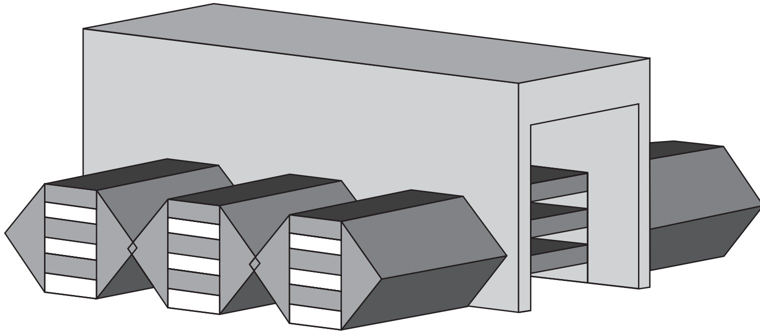

FIGURE 4.21 Schematic representation of a three-stack wide nanowire structure. Such a structure offers a larger conductive area at the expense of some degradation in electrostatics.

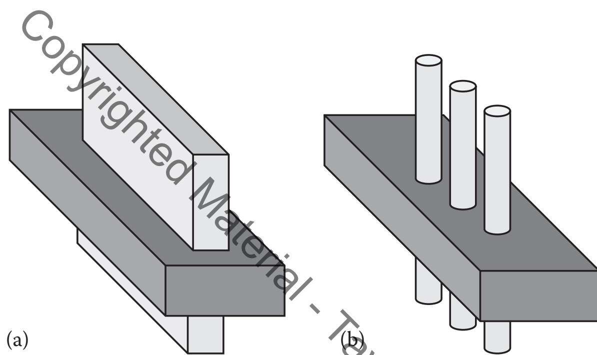

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FIGURE 4.22 (a) A fin-like vertical transistor and (b) a vertical nanowire transistor. For simplicity, only the gate and channel material are shown.

CMOS should be developed. Finally, there is no easy way to form transistors with different gate lengths, a prerequisite for a full-menu technology development.

4.7 CONCLUSIONS

This chapter provided an overview of the challenges faced by conventional CMOS scaling. Fully depleted devices, such as planar FDSOI and FinFET, are the alternative solutions at 14 nm and beyond. Table 4.2 provides a view of how these options compare with a bulk CMOS technology using the same ground rule.

Both devices have better electrostatics compared with the bulk planar devices and hence provide better drive current at the same off-current. In addition, FinFET has a higher device width per footprint and thus typically enjoys a 20%–50% boost in its drive current. To further increase the drive current, it is possible to use strained channel materials such as strained Si and SiGe for both planar FDSOI and FinFET. With a narrow channel, FinFET can enjoy a purely uniaxial strain; however, in the long run it is much easier to form thinner strained layers compatible with planar FDSOI if strain is to be increased. In terms of memory density, planar FDSOI is on par with bulk

TABLE 4.2
Comparison of Planar FDSOI and FinFET Technologies with a Bulk Planar Technology Using the Same Ground Rule

Technology	Planar FDSOI	FinFET
dc Performance	+	+ +
Channel strain engineering	+ +	+
Memory density		+
Power/performance trade-off	+ +	+
Design flexibility	+ +	– –
Time to market	+	– –
Cost	+	–
Foundry commitment and design ecosystem	–	+ +

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planar technology as far as the ground rules are concerned. However, significantly better device matching in FDSOI can be potentially traded for smaller SRAMs. FinFET memories can use fin pitch different from logic to obtain very dense cells, but this potential has yet to be realized in practice. In terms of power/performance trade-off, both devices in principle can lower the operating voltage of the circuit, thereby leading to significantly lower power at the same performance. However, this potential is mostly gated by device and circuit variability in practice. As such, the significant reduction in power promised by FinFET has not been delivered so far. Planar FDSOI, on the other hand, opens the unique possibility of correcting process variations with back bias and dynamic power management to deliver significantly lower power. In terms of design flexibility, with a higher drive current per footprint, FinFET requires a complete change in its design paradigm. Contrary to the general belief that width quantization in designing FinFET circuits is a major concern, we believe this is not a significant issue with the exception of SRAM cells, which are designed by the foundry. A higher drive current, on the other hand, directly translates to higher active power and power density. With V_{DD} scaling limited by process variations, designers need to design circuits more immune to variation. In addition, with a significantly different trade-off between FEOL and BEOL capacitances, an optimum FinFET circuit can be significantly different from earlier implementation in bulk planar technology. Planar FDSOI devices, however, have roughly the same FEOL/BEOL trade-offs compared with bulk planar. With reduced device variability and the possibility of correcting process variations with a back bias, we expect that it would be much simpler for designers to close timing requirements. With the simpler process integration and design flow of planar FDSOI compared with bulk planar and FinFET technology, the required learning cycles of both process development and design are significantly reduced, resulting in an expected shorter time to market. Similarly, it will be more cost-effective both to develop an FDSOI technology and to design circuits using this technology. However, a key element in the mainstream adoption of any technology is a commitment by major foundries to support the necessary ecosystem. Recently, major foundries have announced that FDSOI will be supported. Thus, FinFET and FDSOI will be readily available and fabless customers can choose the best device architecture for their applications.

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