Nanophotonic Interconnect Architectures Discussion Panel

Moderator: Christopher Batten, Cornell University

Panelists: José Martínez, Cornell University
Ashok Krishnamoorthy, Oracle
Norman Jouppi, HP

Workshop on Emerging Technologies for Interconnects
National Science Foundation
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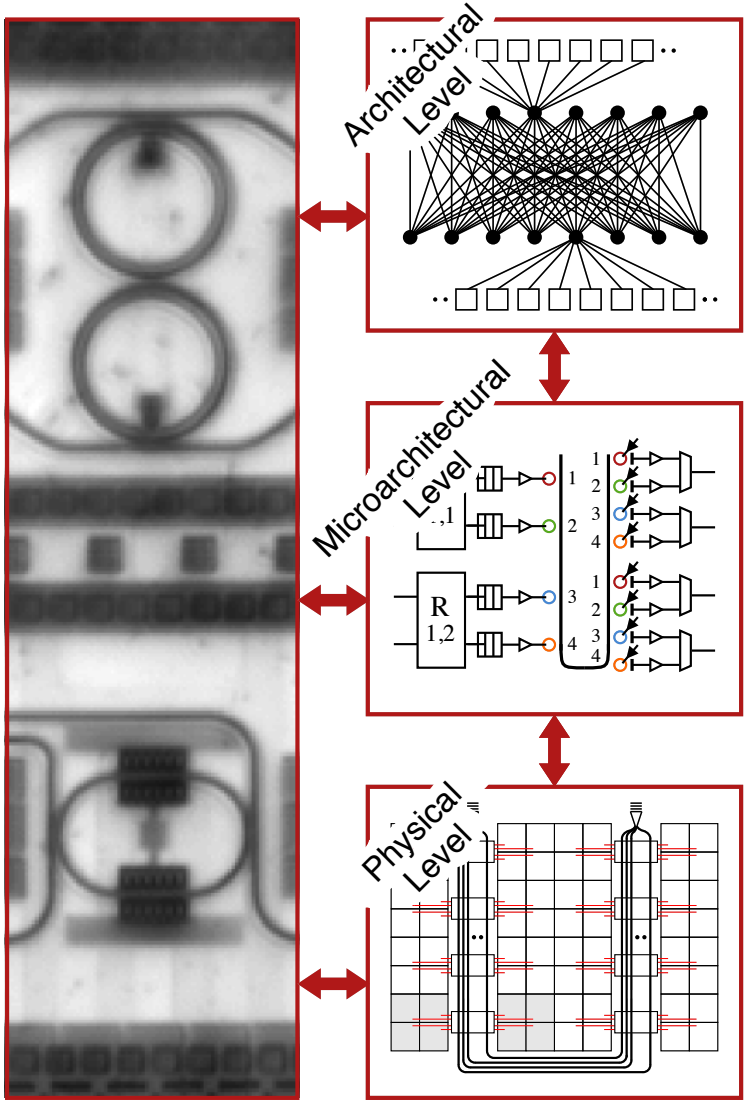
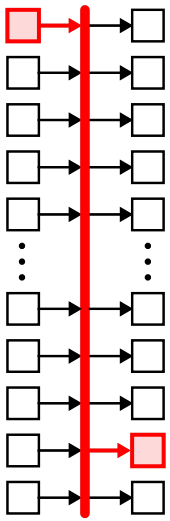
Designing Nanophotonic Interconnection Networks

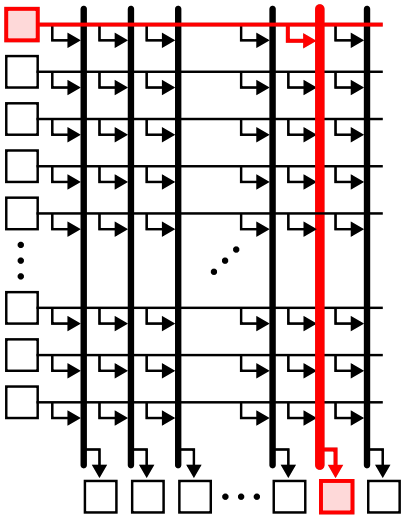


- Architectural-Level Design
  - Network topology, routing algorithm
  - Analytical bounds on performance
  - Electrical baseline network
- Microarchitectural-Level Design
  - Choose electrical vs. nanophotonic components
  - Flow control and arbitration
- Physical-Level Design
  - Map µarch design to physical substrate
  - Assign wavelengths to waveguides/fibers
  - Decide how to layout waveguides and organize fibers

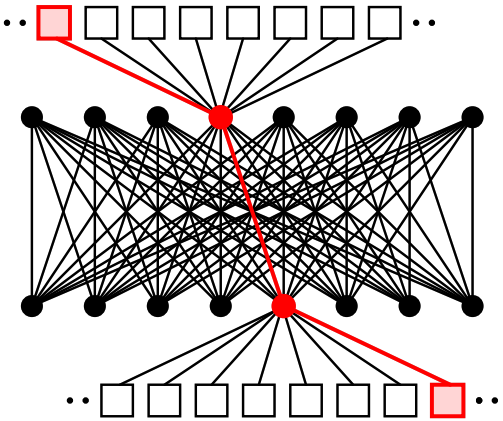
Architecture-Level Design



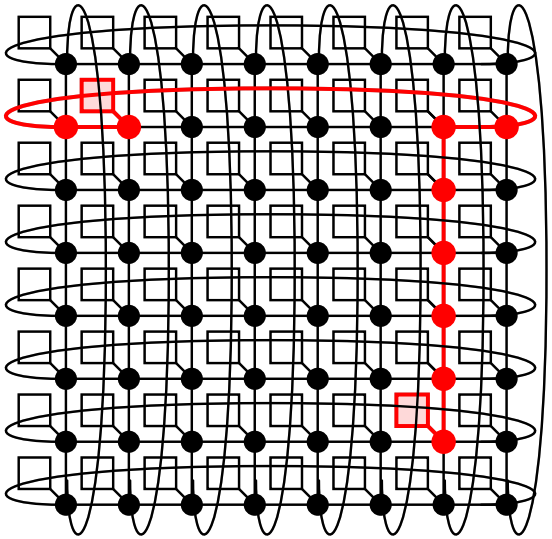
Bus



Crossbar



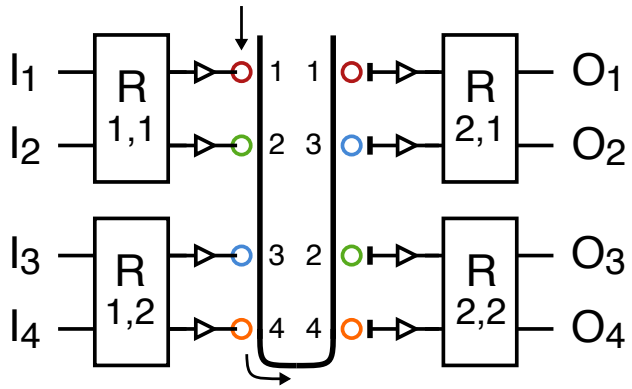
Butterfly



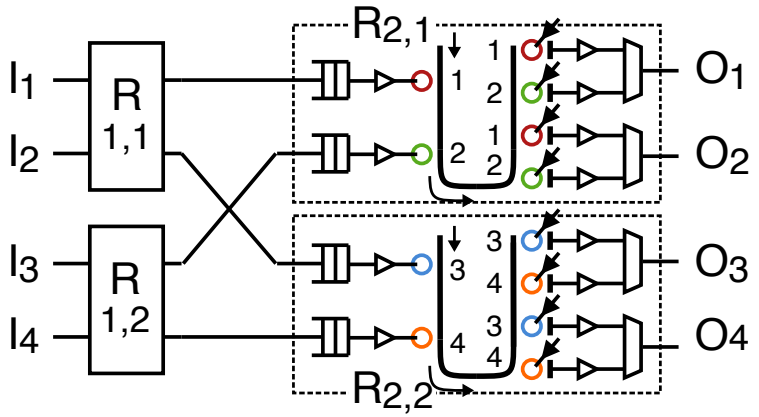
Torus

Increasing number of stages

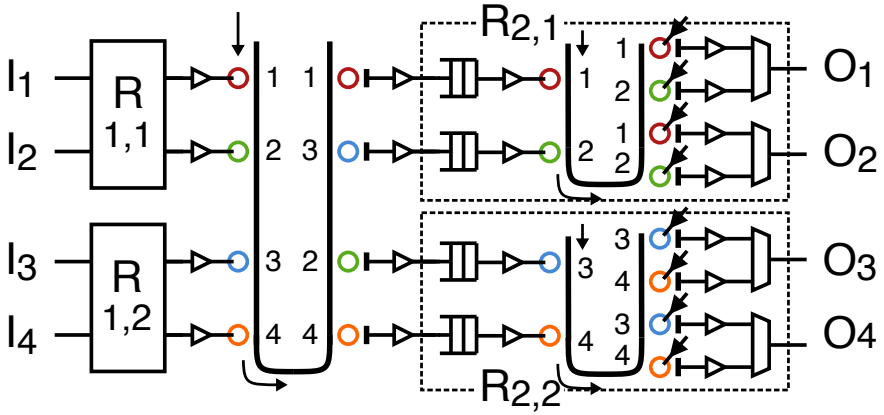
Microarchitecture-Level Design



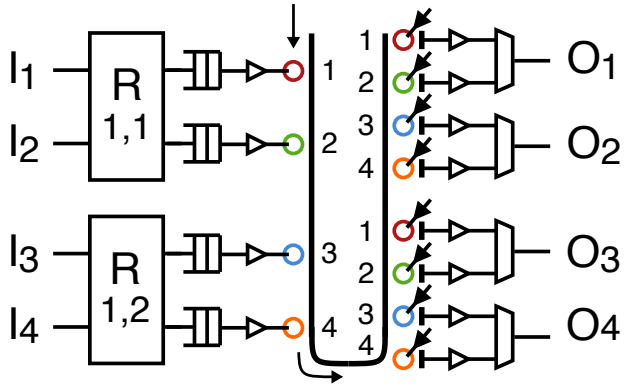
Nanophotonic Channels



Nanophotonic Second-Stage Routers

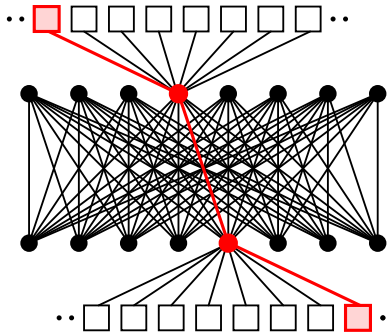


Nanophotonic Channels
and Second-Stage Routers



Unified Nanophotonic Channels
and Second-Stage Routers

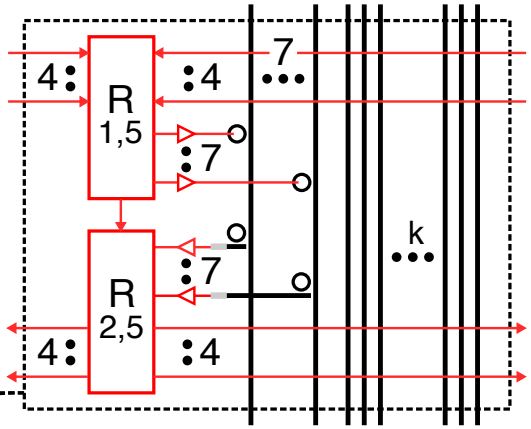
Physical-Level Design

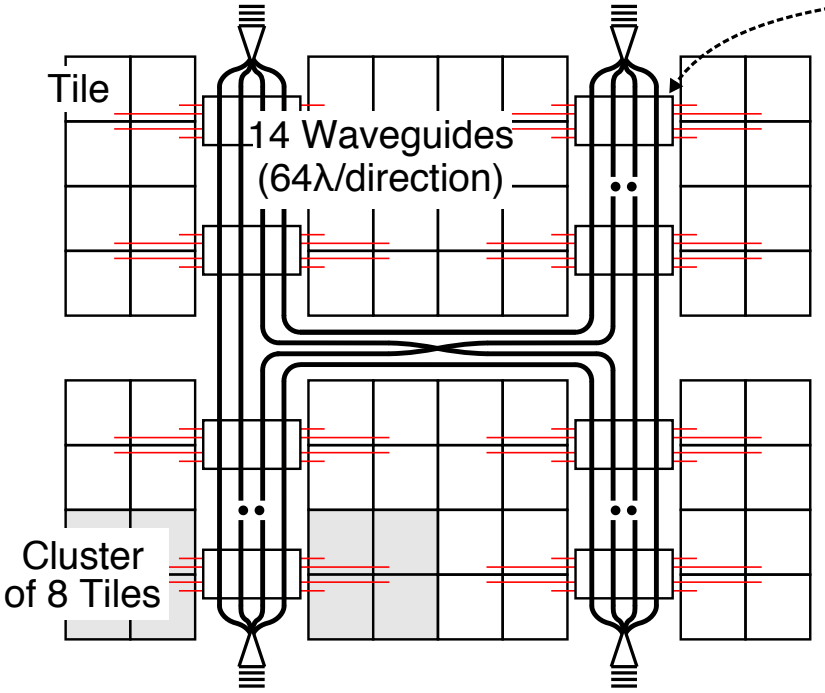


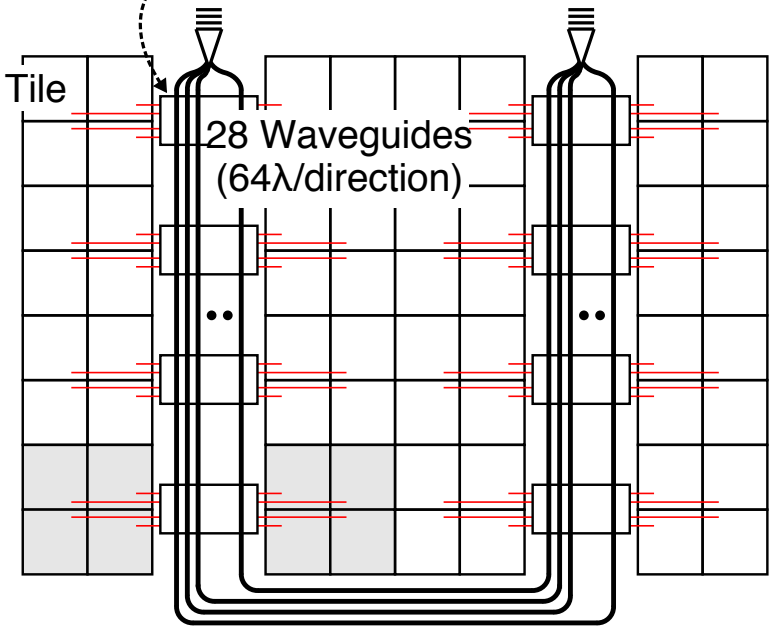
Architectural Level
8-ary 2-fly Butterfly Topology

Microarchitectural Level
Nanophotonic Channels, Electrical Routers

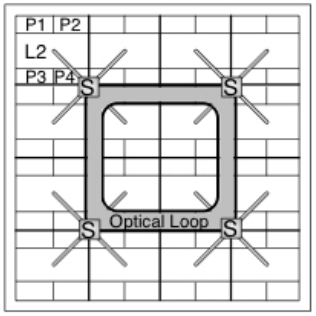
Physical Level
Grid vs Serpentine Layout



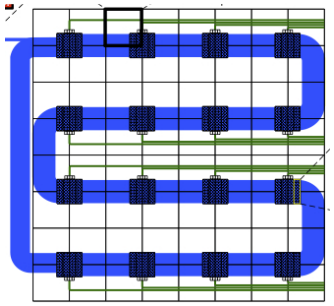




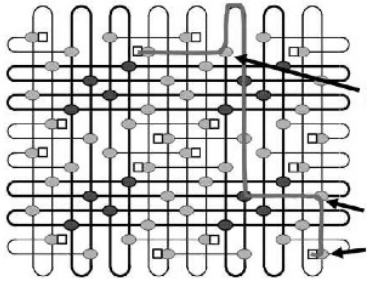
Recent Nanophotonic System-Level Research



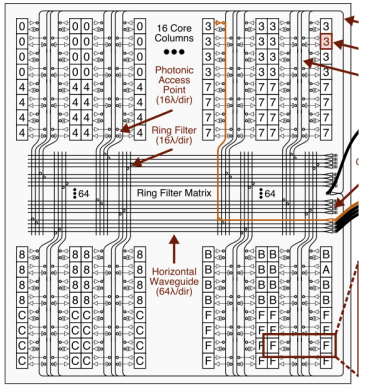
Kirman, MICRO'06



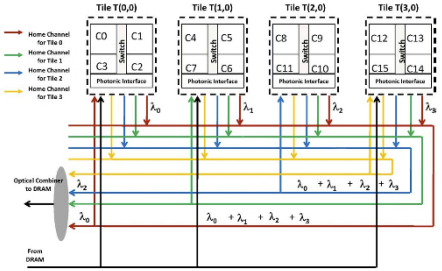
Vantrease, ISCA'08



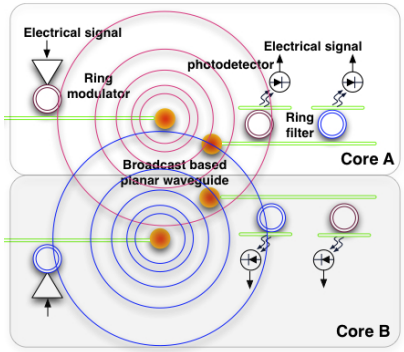
Shacham, TOC'08



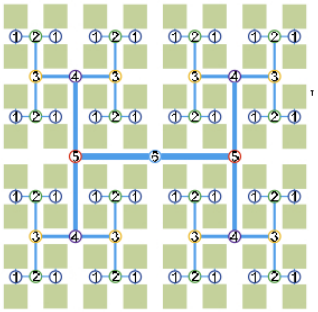
Batten, IEEE Micro'09



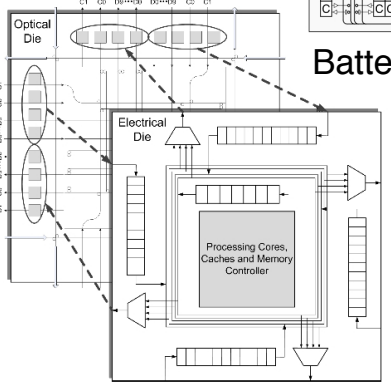
Morris, JSTQE'10



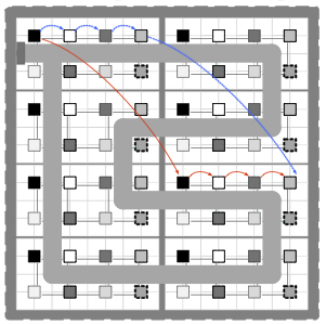
Li, DAC'09



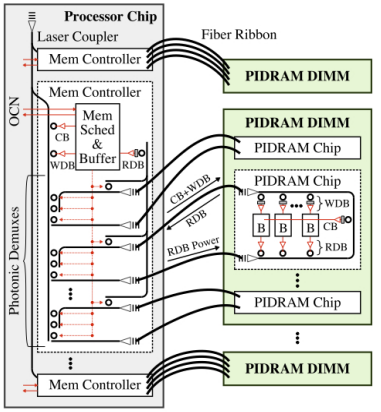
Gu, DATE'09



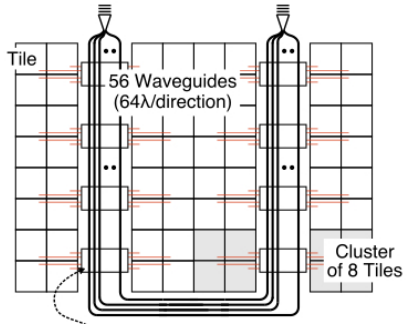
Cianchetti, ISCA'09



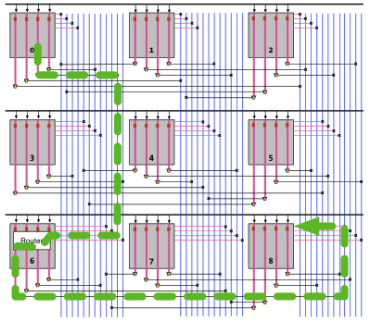
Pan, ISCA'09



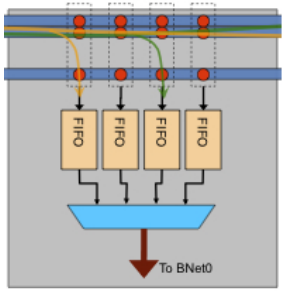
Beamer, ISCA'10



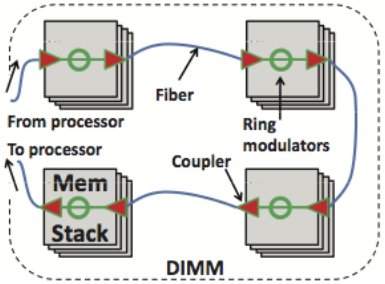
Joshi, NOCS'09



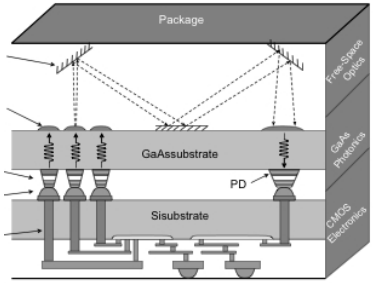
Koka, ISCA'10



Kurian, PACT'10

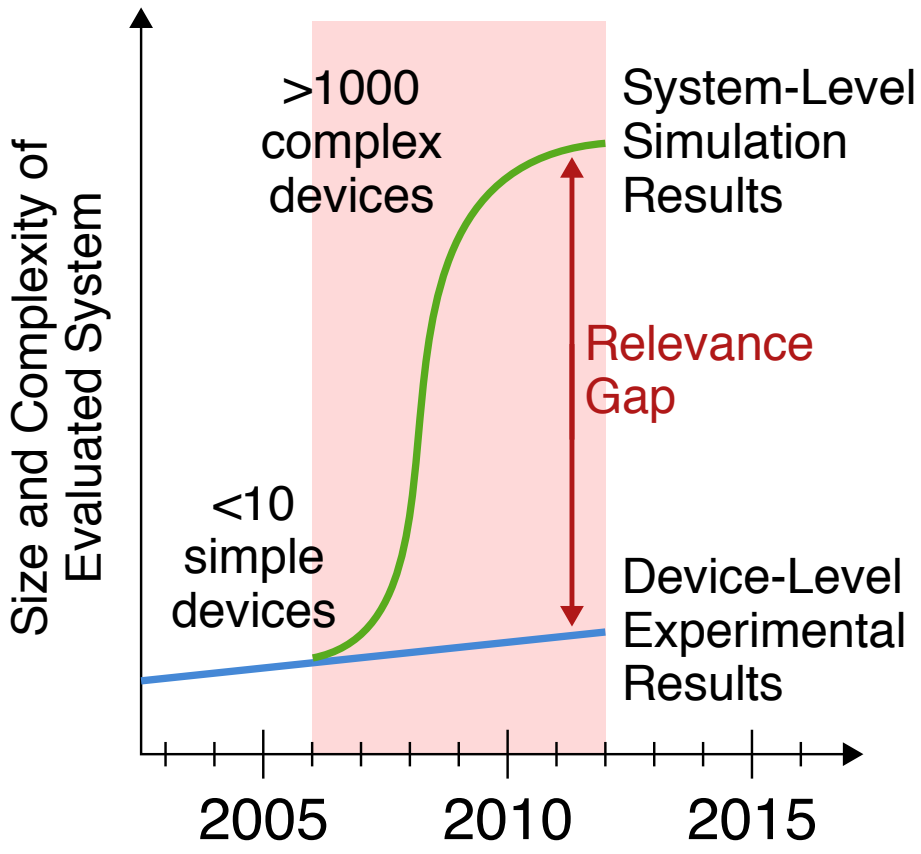


Udipi, ISCA'11



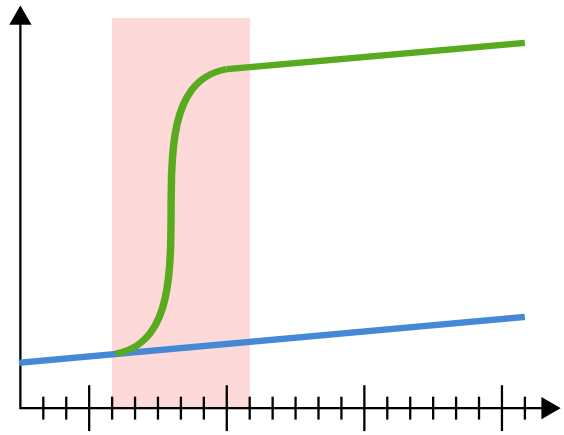
Xue, ISCA'10

Honeymoon Period of Nanophotonic System-Level Research

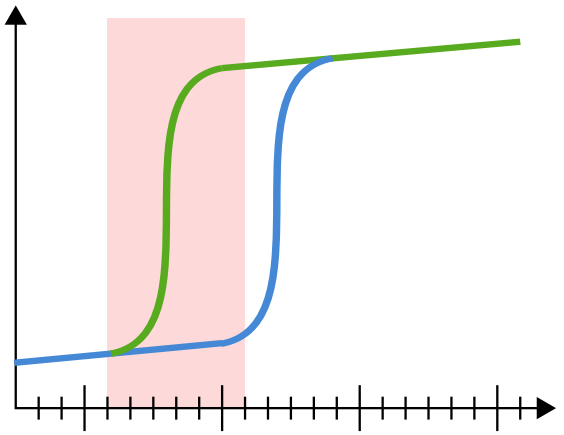


- Drove excitement in system-level community about this technology
- Illustrated potential benefit albeit with projected device parameters
- Less emphasis on practical issues required to really achieve these benefits
  - Transceiver circuits
  - Clocking
  - Off-chip laser design
  - Thermal tuning
  - Manufacturing
  - Reliability

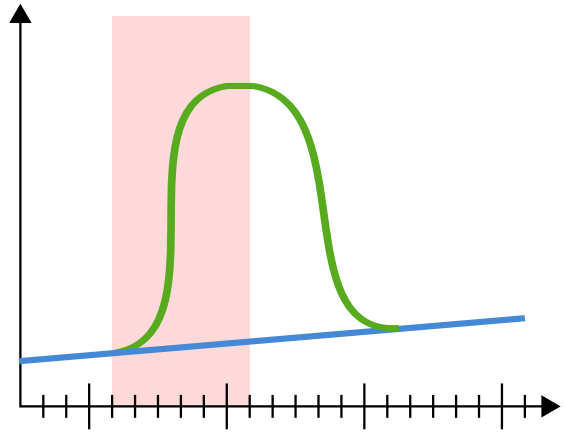
Possible Post-Honeymoon Research Trajectories?



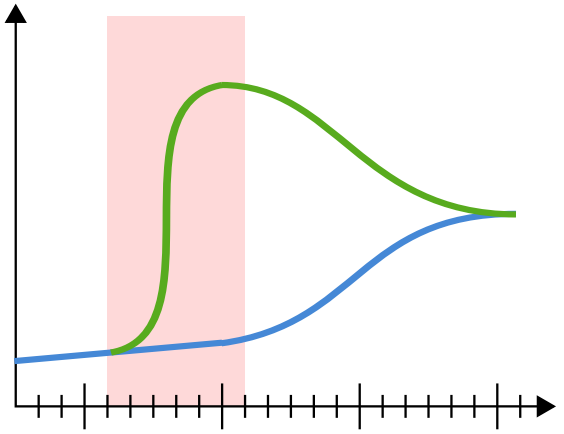
Communities Diverge
Maintaining Relevance Gap



Disruptive Device Breakthrough
Solves All Challenges

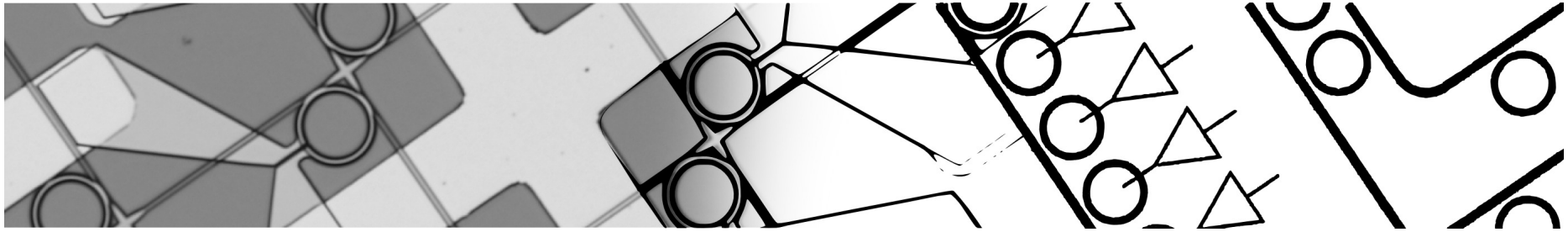


Stop Large-Scale System Research



Meet in the Middle

Goal for Nanophotonic Interconnect Architectures Discussion Panel



Identify critical challenges and key opportunities for system-level research on nanophotonic interconnection networks

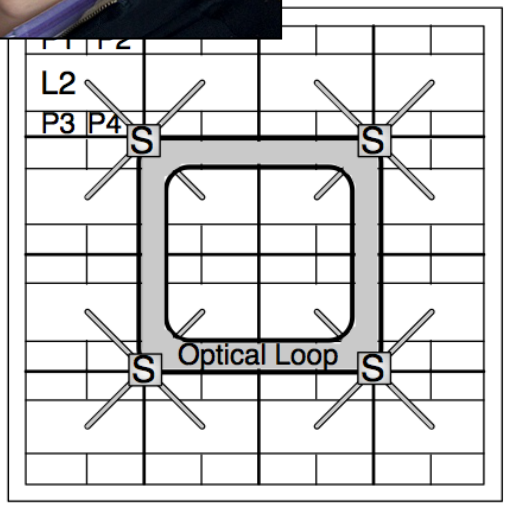
Nanophotonic Interconnect Architectures Panelists

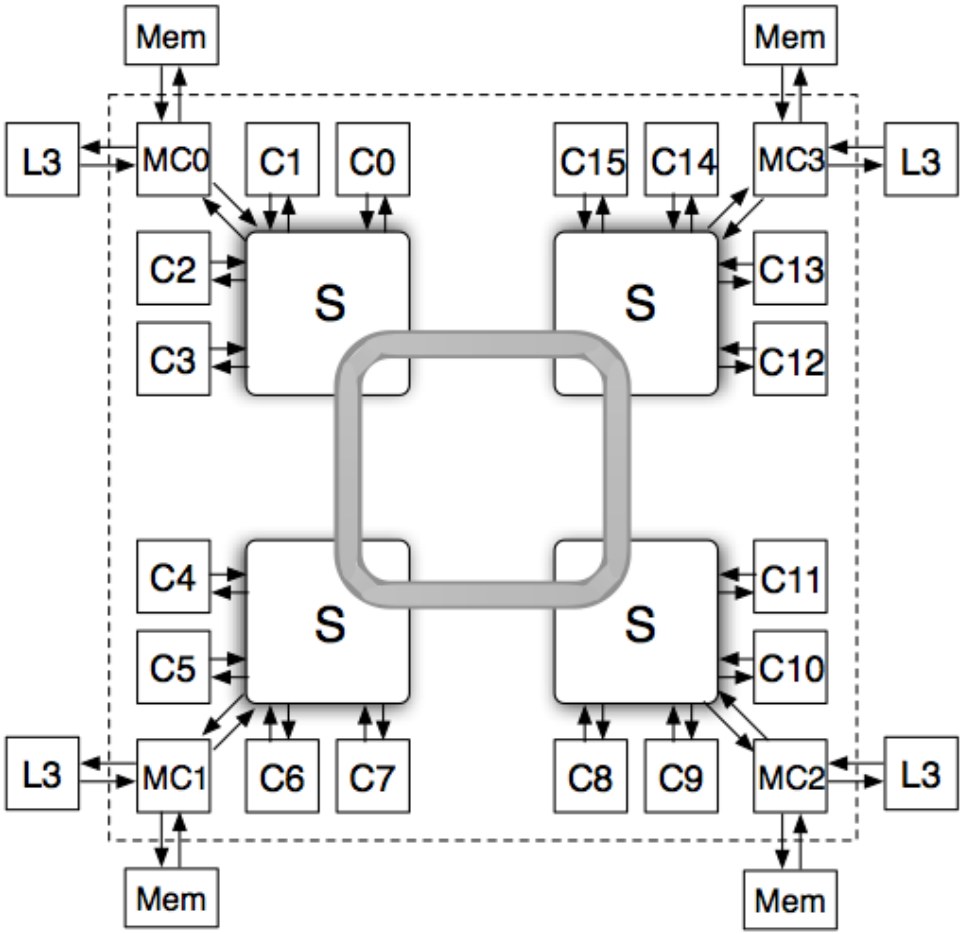
José Martínez
Cornell University

Ashok Krishnamoorthy
Oracle

Norman Jouppi
HP

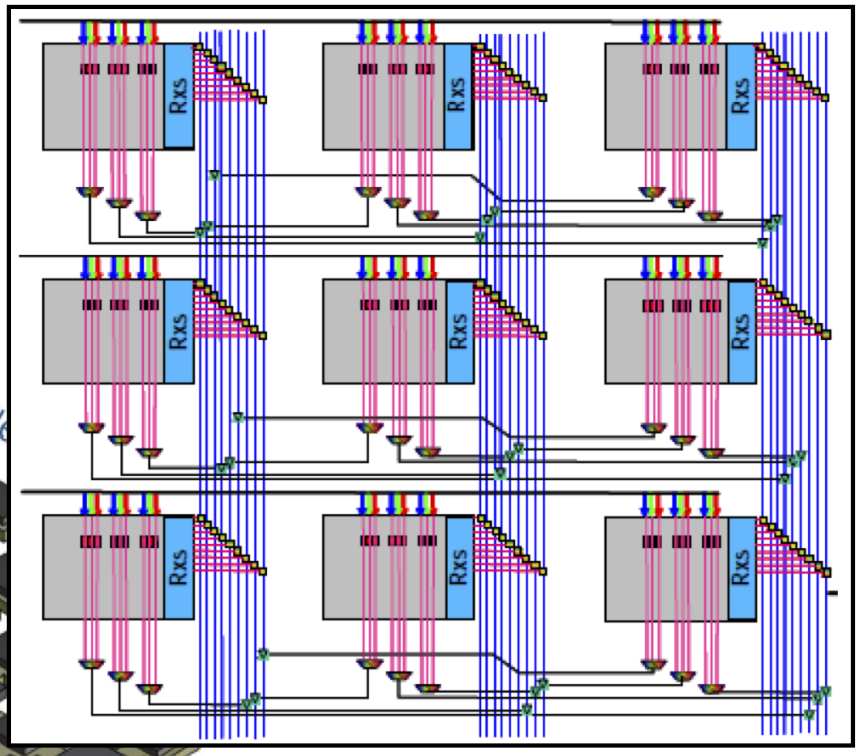
José Martínez, Cornell University

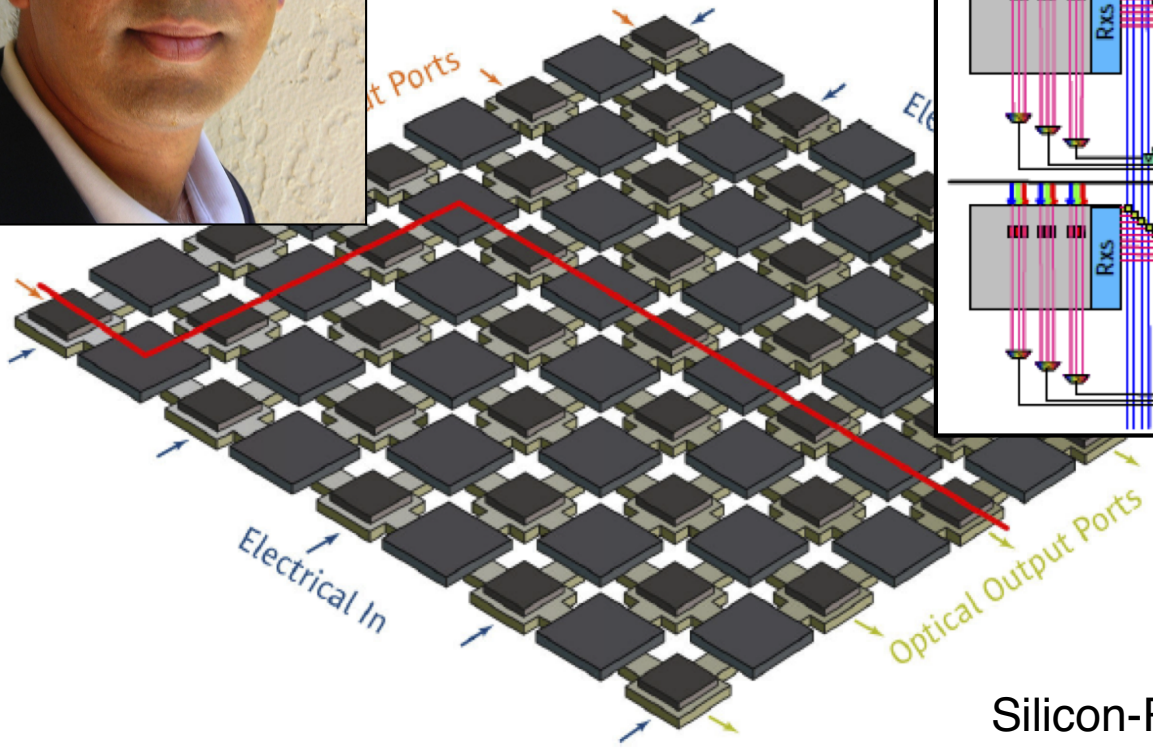




Opto-electrical on-chip bus [MICRO'06]
Power-efficient "point-to-point" on-chip network [ASPLOS'10]

Ashok Krishnamoorthy, Oracle

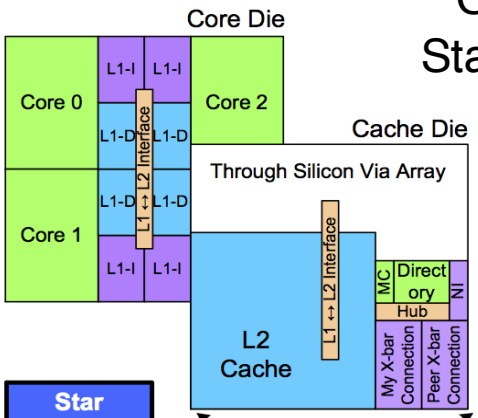


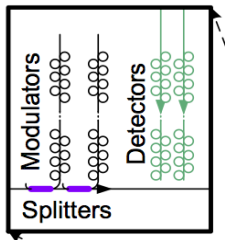


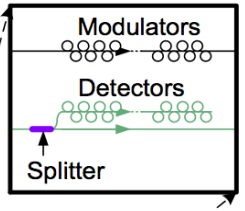
Silicon-Photonic Macrochip [ISCA'10]

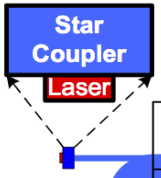
Norman Jouppi, HP

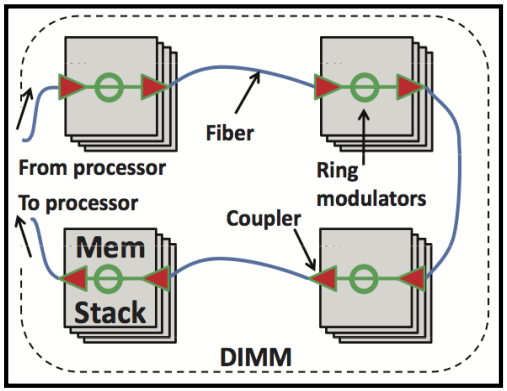
On-Chip Nanophotonic Crossbar [ISCA'08]
Stacked Optically Connected DRAM [ISCA'11]
Optical High-Radix Switches [ISCA'11]

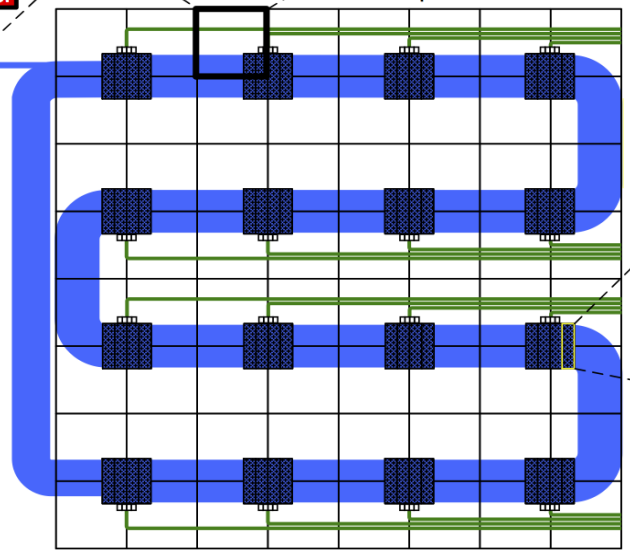


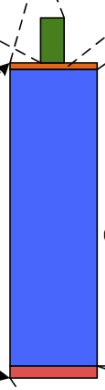


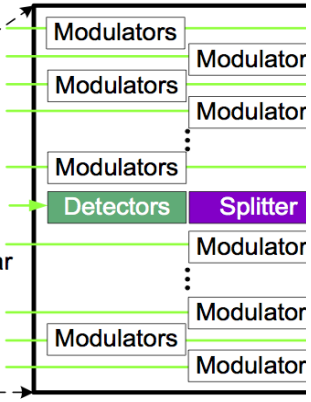


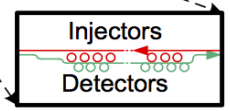








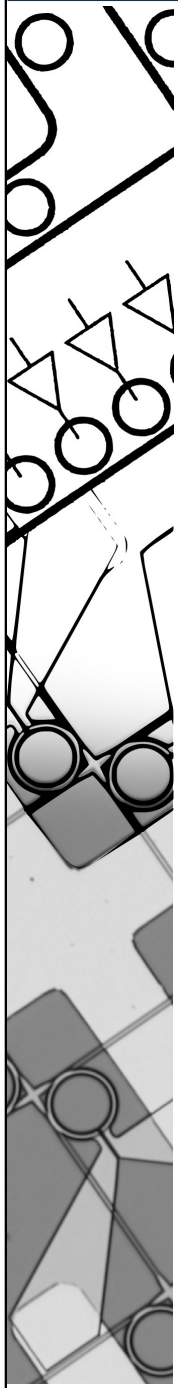




Optically Connected Memory

Broadcast

Arbitration



Discussion Topics

- What is the primary goal of system-level research in this area?
- What research methodology should be used to achieve this goal?
- What is fundamentally different from previous work on optical interconnects in massively parallel processors and/or previous work on electrical chip-level networks?
- From a system-level perspective, what is the single most challenging device or circuit design issue which could potentially prevent mainstream adoption?
- Where in the system should architects focus their efforts? Intra-chip? Intra-package? Inter-chip?
- Will nanophotonics fundamentally change the way we design the whole system? How we design processors, accelerators, cache coherence protocols, or memory hierarchies?