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Roadmaps for Multi Die Integration

Strategies and Drivers

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ROADMAPS FOR MULTI DIE INTEGRATION – STRATEGIES AND DRIVERS

CONTENTS

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A ONE-DAY TECHNICAL SYMPOSIUM & EXHIBITS

Roadmaps for Multi Die Integration
Strategies and Drivers

MORNING AGENDA

7:15 am	**Registration Opens**
8:15 am - 8:30 am	**Welcome and Introduction**
SESSION ONE:	**MULTI DIE INTEGRATION STRATEGIES** *Session Chair: Pat Tang, STATSChipPAC*
8:30 am - 9:00 am	**Multi-Die Integration Strategies and System Partitions in Mobile WWAN Devices** *Harrison Chang, Ph.D., Vice President, Universal Scientific Industries, Co., Inc.*
9:00 am - 9:30 am	**Multi Die Integration: A Case Study** *Y. S. Kim, VP of Engineering and R&D, Signetics Corporation*
9:30 am - 10:00 am	**Alternatives on the Road to 3D TSV** *E. Jan Vardaman, President, TechSearch International, Inc.*
10:00 am - 10:30 am	**Morning Break and Exhibits**
SESSION TWO:	**ENABLING MULTI DIE INTEGRATION** *Session Chair: Kumar Nagarajan, Maxim Integrated*
10:30 am - 11:00 am	**Silicon Interposer Design: Architecture Through Implementation** *Bill Acito, Product Engineer, Cadence Design Systems Inc.*
11:00 am - 11:30 am	**Multi Die Integration – Can Material Suppliers Meet the Challenge?** *Jeff Calvert, Global R&D Director, Advanced Packaging Technologies, Dow Electronic Materials*
11:30 am - 12:00 am	**The Strange World of Networking Memory** *David Chapman, VP Marketing & Applications Engineering, GSI Technology*
12:00 am - 1:00 pm	**Lunch and Exhibits**

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AFTERNOON AGENDA

KEYNOTE: **THE PROMISES AND PITFALLS OF 2.5D PACKAGING … A USER PERSPECTIVE**
1:00 pm - 1:30 pm *Anwar A. Mohammed, Senior Staff Scientist, Advanced Interconnect and Packaging U.S. R&D Center, Huawei Technologies*

SESSION THREE: **EMERGING TECHNOLOGIES FOR MULTI DIE PACKAGING**
Session Chair: John Xie, Ph.D., Altera Corporation

1:30 pm - 2:00 pm **High Density Organic Interposers for 2.5D/3D Multi-Chip Package**
Chaowen Chung, Ph.D., Marketing Director, Unimicron Technology Corp.

2:00 pm - 2:30 pm **Organic Interposer Advanced Packaging Build-Up Technology**
Joseph Dang, Field Applications Engineer, Kyocera America, Inc.

2:30 pm - 3:00 pm **Afternoon Break and Exhibits**

3:00 pm - 3:30 pm **Low Cost Solutions for 2.5D Packaging**
Young Do Kweon, Vice President, Samsung Electro-Mechanics Co., Ltd.

3:30 pm - 4:00 pm **Multi Die Integration for High Bandwidth Networking Devices: a User Perspective**
Ray Niu, Sr. Component Engineer, U.S. R&D Center, Huawei Technologies

SESSION FOUR: **PANEL – DRIVERS FOR MULTI-DIE PACKAGING**
4:00 pm - 5:00 pm *Moderators: Ivor Barber, LSI and Rich Rice, ASE (US) Inc.*
Panelists: Joseph Dang, Kyocera
Dave Love, GenapSys
Steve Smith, Synopsys
Alex Tsai, TSMC North America
E. Jan Vardaman, TechSearch International

5:00 pm - 6:00 pm **Sponsor and Exhibitor Reception**

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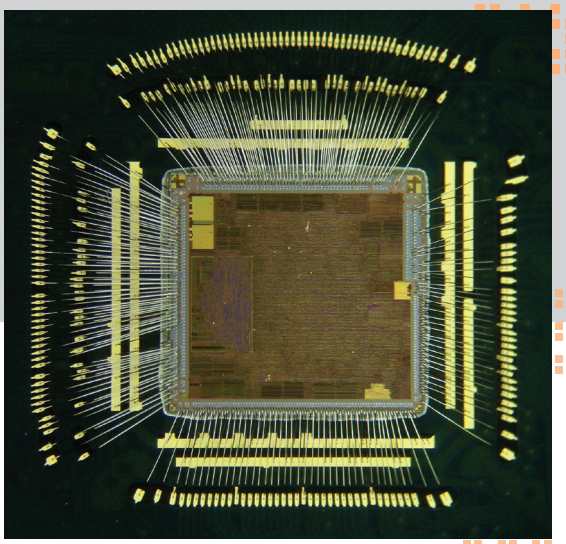

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Aehr Test Systems is a worldwide provider of systems for burning-in and testing memory and logic integrated circuits and has an installed base of more than 2,500 systems worldwide. Aehr Test has developed and introduced several innovative products, including the ABTS™, FOX™ and MAX systems and the DiePak® carrier. The ABTS system is Aehr Test's newest system for packaged part test during burn-in for both low-power and high-power logic as well as all common types of memory devices. The FOX system is a full wafer contact test and burn-in system. The MAX system can effectively burn-in and functionally test complex devices, such as digital signal processors, microprocessors, microcontrollers and systems-on-a-chip. The DiePak carrier is a reusable, temporary package that enables IC manufacturers to perform cost-effective final test and burn-in of bare die.

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Amkor Technology, Inc. is one of the world's largest providers of advanced semiconductor assembly and test services. Founded in 1968, Amkor has become a strategic manufacturing partner for many of the world's leading semiconductor companies and electronics OEMs, providing a broad array of advanced package design, assembly and test solutions. Amkor's operational base encompasses more than 5 million square feet of manufacturing facilities, product development centers, and sales & support offices in Asia, Europe and the United States. Amkor offers a suite of services, including electroplated wafer bumping, probe, assembly and final test. Amkor is a leader in advanced copper pillar bump and packaging technologies which enables next generation flip chip interconnect.

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NTK is a global leader in Organic and Ceramic Packaging. NTK's Packaging is aligned to support custom designs with varying volume requirements. Their package design support is geared to streamline electrical and thermal design optimization. Materials include HTCC, LTCC, and a variety of Organic and Laminate Materials and Technologies. NTK's proven simulation tools have enabled optimum package design for high speed communications in the 10G, 40G, 100G, and soon approaching 400G for both, ceramic and organic packages. Advanced ceramic-based applications available for Space Transformers for Probe, CCD and CMOS Image Sensors.

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Quik-Pak, a division of Delphon Industries, provides IC packaging and assembly services. The company's newest offering is its OmPP package. These pre-molded QFN packages are cost-effective, come in a variety of sizes and are ideal for prototype or production volume applications. Quik-Pak also specializes in a variety of services that together provide a full turn-key solution including wafer preparation, die/wire bonding, remolding and marking/branding. Custom assembly services are also offered for Flip Chip, Ceramic Packages, Chip-on-Board, Stacked Die, MEMS, etc.

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Signetics is a member of the Young Poong Group. With over 40 years in the industry, Signetics is the most experienced semiconductor assembly and test services provider in Korea. Signetics launched its semiconductor assembly and test operations in Youmchang-Dong in Seoul, South Korea in 1966 as part of Signetics Corporation, which was at the time, an IDM based in Sunnyvale, California. Signetics' technology portfolio includes Flip Chip, Stacked Die and System-in-package for both substrate and leadframe based packages. Turnkey services take their customer's device from wafer through final test. Signetics has been certified to the major quality standards including ISO/TS16949, ISO14001, Sony Green Partner and Samsung Eco Partner.

TechSearch International, Inc.

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TechSearch International was founded in 1987 as a market research and consulting company specializing in emerging semiconductor packaging trends. Multi- and single-client services encompass market research, technology trends, and strategic planning. Research topics include flip chip, WLP, CSPs, BGAs, 3D TSVs, multichip packages (MCPs) such as stacked die CSPs, PoP, and System-in-Package (SiP), embedded components, microvia substrates, high-brightness LEDs, medical electronics, semiconductor packaging and assembly material developments and markets, and Pb-free manufacturing trends.

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BIOGRAPHIES

SYMPOSIUM CO-CHAIRS

Ivor Barber graduated from Napier University in Edinburgh, Scotland in 1981 with a Bachelors degree in Technology. He has worked in package assembly and design at National Semiconductor, Fairchild Semiconductor and VLSI Technology. Ivor has spent the last 21 years at LSI Corporation in Milpitas in various Engineering and Management positions in Assembly, Package Characterization and Package Design. Ivor is currently Director of Package Design and Characterization at LSI Corporation. Ivor holds 12 US patents related to package design.

Rich Rice is Senior Vice President of Sales for ASE (U.S.) Inc., with responsibility for the North American region. Appointed in 2003, Mr. Rice oversees field sales and engineering support teams. Prior to joining ASE, Mr. Rice spent over ten years at Amkor Technology, where he held various management roles, including Vice President of Sales and Vice President of Business Development. Previously, Mr. Rice performed engineering roles at Nara Technologies and National Semiconductor Corporation. Mr. Rice holds a BS degree in Agricultural Engineering from the University of Illinois.

SESSION CHAIRS

Kumar Nagarajan is currently Director of Package Development at Maxim Integrated, responsible for new package development, Qualification and NPI. Kumar has over 18 years of package technology development experience, most recently at Xilinx as Director of Package Development and production engineering. Prior to Xilinx, he was responsible for flip chip package R&D at LSI. He received his Masters in Material Science from Stanford University; Masters in Industrial Engineering from SUNY, BS in Mechanical Engineering from Birla Institute of Technology, India.

Pat Tang is currently Deputy Director, Business Development and Technology Marketing at STATS ChipPAC, and he has more than twenty years of sales, marketing, business development and technology development experience in the semiconductor, telecommunications, and wireless industries. Prior to joining STATS ChipPAC, he was with IMSM, and the Corporate Vice President and General Manager Asia at Surfect Technologies, Inc., an Advanced Interconnect Technology Company. Pat was a Managing Principal with the PT Group, a management consulting and technology advisory firm. Pat also served as General Manager of the Asia Pacific region with Ultratech. He has held executive and technical positions with semiconductor equipment companies including Matrix Integrated Systems, Semitool, ASET, and Perkin Elmer. He was also involved with the start up and subsequent IPO of IPEC, a manufacturer of single wafer plasma and wet process cleaning and chemical mechanical polishing capital equipment. Pat earned an MBA from the University of San Francisco, and holds a professional engineer license in chemical engineering. He has taught at the graduate level in business management at the University of Phoenix, and published several papers in semiconductor lithography process technology.

John Xie, Ph.D. has been with Altera Corporation for 12 years. He leads packaging design engineering, process engineering and supply chain engineering team. His responsibilities include interconnect and packaging technology development, corporate new product development and introduction, system level interconnect co-design engineering, corporate 2.5D/3D integration manufacturing enablement, strategic supply chain engineering and relationship development, key customer engagement. Prior to Altera he was a technology development manager at Prolinx Labs Corporation. Dr. Xie graduated from the Department of Physics, Peking University, and holds a Ph.D. Degree in Physics from Institute of Physics, Chinese Academy of Sciences and Post Doctoral from Department of Physics, University of California, Berkeley and Lawrence Berkeley Laboratory. Dr. Xie has 24 published patents with 10 more pending; and over 40 academic and technical publications.

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ROADMAPS FOR MULTI DIE INTEGRATION – STRATEGIES AND DRIVERS

KEYNOTE SPEAKER

Anwar Mohammed is a Senior Staff Scientist leading the development of 2.5 D packages at Huawei Technologies. He holds double Masters Degrees and is presently pursuing his Doctorate in Packaging issues with the James Clark Engineering School at the University of Maryland. He is the author of over 20 national and international patents and published numerous papers and presentations dealing with packaging and interconnect issues. He has led challenging packaging programs for elite companies like National Semiconductors, Fairchild Semiconductors, Cree, Infineon and Huawei.

PRESENTERS

Bill Acito is the Product Engineer responsible for the Cadence IC packaging and SiP layout tools and has been with Cadence (and the ICP packaging tools) for 11 years. He has worked in the semiconductor manufacturing, yield management software, and package design industries in various roles for more than 25. He has a B.S. in Microelectronic Engineering from the Rochester Institute of Technology.

Jeff Calvert currently holds the position of Global R&D Director for the Advanced Packaging Technologies business of Dow Electronic Materials, a business unit of Dow Chemical Company. Jeff has over 20 years experience in managing electronic materials technology development programs for both the commercial semiconductor industry as well as the US Government. Jeff received his Ph.D. in Physical Inorganic Chemistry from the University of North Carolina at Chapel Hill. He has published over 100 journal articles in refereed publications and has over 40 US patents and patent applications.

Harrison Chang, Ph.D. graduated from NTUEE in 1985. He received his Ph.D. degree on Electromagnetics from the Department of Electrical Engineering, University of Maryland, College Park in 1993. Since then, his experience includes Deputy Professor in the Huafan University, Taiwan, Senior Engineer in Qualcomm, San Diego, Associate VP in BenQ, founder and CEO of the Indigo Mobile Technologies, and VP Engineer in Metalligence Technologies. He is now the VP in USI, heading the miniaturized technology development and product design, focusing on the SiP for WWAN modem and smart phone applications. He has more than 20 technical papers and four global patents.

David Chapman is Vice President of Marketing and Applications Engineering at GSI Technology. David is responsible for GSI's roadmap and new product definitions and has been heavily involved in the development of industry standards for high performance memory products since 1985 at Mostek, Motorola and since 1998, at GSI.

Chaowen Chung, Ph.D. is currently working for Unimicron Technology Corp. as Marketing Director in IC Substrate Strategy Business Unit. He has more than 15 years experience in Package Development/Assembly and Substrate Manufacturing domain. Chaowen received his MS and Ph.D. degrees in Systems Science and Industrial Engineering from State University of New York – Binghamton. Prior to joining Unimicron in 2007, he worked for LSI Logic and SPIL US.

Joseph Dang provides the technical support to the Kyocera Sales team for a broad range of customers that are using KST's HDBU/SLC laminates as well as promoting emerging technologies. For over the past 14 years, Joseph has worked for two Japanese substrate-manufacturing companies as a technical liaison for both companies. His focus has been on the manufacturing, reliability and design aspects of the organic buildup laminates that have been necessary to service the needs of semiconductor companies ranging from high volume MPU to small volume high-end ASIC applications. He received his B.S.E. in Chemical Engineering from Arizona State University.

Y.S. Kim has over 24 years of experience in the semiconductor assembly and test industry. Kim currently serves as Signetics' VP of Engineering and Research & Development. In this role he oversees all process engineering, package engineering, test engineering as well as R & D for a 300 million dollar provider of subcontract assembly and test services. Prior to his current role, Kim held several positions within the Signetics engineering team including process engineering for wire bonding development and package engineering, which included the development of new processes, packages and technologies as well as bringing them through qualification to production. Kim received his bachelor's degree in electronic engineering from Yeung Nam University in Korea.

Young Do Kweon is currently working for Samsung Electro-Mechanics Co. Ltd., as Vice President in Corporate R&D Center. He has been working in Semiconductor, Fiber Optics, Image Sensor, Wireless Component, System Module Packaging since 1988 with hands on experience in design, process, equipment and reliability, particularly between the R&D and mass production ramp-up. Currently, he is developing a next generation package substrates and PCB technologies for the mobile applications. He had worked for Micron Technology, Flip Chip Technology, and Samsung Semiconductor. Mr. Kweon received his BS degree in Metallurgical Engineering from Hanyang University in 1987, and his MS in Mechanical Engineering from University of Maryland at College Park in 1998. He had attended the several projects on CALCE Electronics Packaging Research Center in University of Maryland at College Park as well. He holds several patents in new packaging and its processes, and published papers.

Ray Niu is a Senior Component Engineer at Huawei Technology Research Center located in Santa Clara, California. He is responsible for developing memory solution for next generation Network products and he also serves as the Huawei representative at Jedec. Before coming to the US, Rui worked at the Huawei Technology Research Center in Beijing, interacting with cross-functional teams to source and qualify logic IC and memory components and in establishing component specifications for Router products. Ray has a degree from the Xidian University, majoring in Signal Processing and has authored multiple patents and presentations in the 2.5D technology arena.

E. Jan Vardaman is president and founder of TechSearch International, Inc., which has provided analysis on technology and market trends in semiconductor packaging since 1987. She is co-author of How to Make IC Packages (published in Japanese by Nikkan Kogyo Shinbunsha), a columnist with Circuits Assembly Magazine, and the author of numerous publications on emerging trends in semiconductor packaging and assembly. She served on the NSF-sponsored World Technology Evaluation Center study team involved in investigating electronics manufacturing in Asia and on the U.S. mission to study manufacturing in China. She is a member of IEEE CPMT, SMTA, IMAPS, MEPTEC, and SEMI. She received the "Die Products Industry Achievement Award," at the 14th Annual International KGD Packaging and Test Workshop in September 2007. She was elected to two terms on the IEEE CPMT Board of Governors. Before founding TechSearch International, she served on the corporate staff of Microelectronics and Computer Technology Corporation (MCC), the electronics industry's first precompetitive research consortium.

PANELISTS

Joseph Dang provides the technical support to the Kyocera Sales team for a broad range of customers that are using KST's HDBU/SLC laminates as well as promoting emerging technologies. For over the past 14 years, Joseph has worked for two Japanese substrate-manufacturing companies as a technical liaison for both companies. His focus has been on the manufacturing, reliability and design aspects of the organic buildup laminates that have been necessary to service the needs of semiconductor companies ranging from high volume MPU to small volume high-end ASIC applications. He received his B.S.E. in Chemical Engineering from Arizona State University.

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ROADMAPS FOR MULTI DIE INTEGRATION – STRATEGIES AND DRIVERS

Dave Love is a 30 year veteran of the Semiconductor Packaging industry, with stops at Intel, Fujitsu, and Sun Micro/ Oracle. Dave has authored 15 US Patents and over 30 published conference and journal papers. Dave received his BSc in Chemistry from the University of San Francisco. Currently, Dave is Director of Packaging and Technology Development at Genapsys.

Steve Smith is currently responsible for Synopsys' 3D-IC strategy and marketing. He has been with Synopsys for 15 years, having served in various functional verification and design implementation marketing roles. He has worked in the electronic design automation and computer industries for more than 30 years in a variety of senior positions including marketing, applications engineering and software development. Prior to Synopsys, Steve worked at Viewlogic, Teradyne, Unisys and ICL.

Alex Tsai is a Senior Program Manager at TSMC North America in Field Technical Support Division, specializing in Backend Technology. Alex has 28 years of semiconductor industry experiences in Process, Product, Test, Packaging, Operations and Sales Marketing fields. Prior to joining TSMC (2000), Mr. Tsai worked for WSMC (1998) and Texas Instruments (1984). Alex holds a M.S.E.E from Southern Methodist University (1987), and a B.S. Material Science and Engineering from National Tsing Hua University, Hsinchu, Taiwan (1980).

E. Jan Vardaman is president and founder of TechSearch International, Inc., which has provided analysis on technology and market trends in semiconductor packaging since 1987. She is co-author of How to Make IC Packages (published in Japanese by Nikkan Kogyo Shinbunsha), a columnist with Circuits Assembly Magazine, and the author of numerous publications on emerging trends in semiconductor packaging and assembly. She served on the NSF-sponsored World Technology Evaluation Center study team involved in investigating electronics manufacturing in Asia and on the U.S. mission to study manufacturing in China. She is a member of IEEE CPMT, SMTA, IMAPS, MEPTEC, and SEMI. She received the "Die Products Industry Achievement Award," at the 14th Annual International KGD Packaging and Test Workshop in September 2007. She was elected to two terms on the IEEE CPMT Board of Governors. Before founding TechSearch International, she served on the corporate staff of Microelectronics and Computer Technology Corporation (MCC), the electronics industry's first pre-competitive research consortium.

SESSION ONE

MULTI DIE INTEGRATION STRATEGIES

Session Chair:

Patrick Tang
Deputy Director, Business Development and Technology Marketing
STATSChipPAC

Tablet, smartphone, handheld, portable, and wireless products continue to be driven by the need for reduction in size and weight while at the same time meeting the demand for increased functionality, high density, speed, and performance. Component integration plays a key role in meeting these needs and demands. Multi-die integration, the combining of multiple components in a single package or on a single substrate, provides an effective solution for advanced integration. These multi-die integrations are not constrained by common wafer fabrication processes and can integrate passive components to create self-contained systems. The key attributes of multi-die integration strategies will reviewed, die interconnect technology selection issues and methods for assuring product quality will be addressed and what the multi-die integration landscape will look in 2013 and beyond.

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ROADMAPS FOR MULTI DIE INTEGRATION – STRATEGIES AND DRIVERS

MULTI-DIE INTEGRATION STRATEGIES AND SYSTEM PARTITIONS IN MOBILE WWAN DEVICES

Harrison Chang, Ph.D.
Vice President
Universal Scientific Industries, Co., Inc.

The hardware design of the smart phone has been evolving toward the trend of miniaturization aggressively in recent years. Tear down examples from various successful designs were given in the presentation. Nevertheless, the industry continues the drive for further miniaturization in order to allow for thinner and lighter design, as well as for more spaces for battery, antenna, and acoustic. In order to facilitate further miniaturization, utilizing of the electromagnetic design and simulation is essential. The technical rationale is two-fold. One is that the clock speed of the application processor already exceeded 1GHz, and will exceed 2GHz and further. Hence the design of the high speed digital circuitry involves in-depth understanding of the RF characteristics. The other is that the complexity of the multi-mode and multi-band RF front end design of the 3G to 4G modem calls for the considerations of the couplings and parasitic capacitance/inductance derived from the very compact structure. Examples of such SiP "System in Package" design were given in the presentations, including complete single SiP 2.5G data modem, and multi-band 3G + LTE RF frond-end modules. The process to design, simulate, and measure these SiPs are explained and discussed.

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ROADMAPS FOR MULTI DIE INTEGRATION – STRATEGIES AND DRIVERS

MULTI DIE INTEGRATION: A CASE STUDY

Y.S. Kim
VP of Engineering and R&D
Signetics Corporation

Case studies of Memory Multi Chip Packaging and eMMC (embedded Multi Media Card) will be discussed based on high volume manufacturing experience. Both MCP and eMMC are widely used for SmartPhones as a storage solution. MCP is the package level integration of heterogeneous memory chips, and eMMC is the further integration of NAND with Flash Card Controller and passives. The yield of Multi Chip packaging becomes a critical consideration, since the affected lot size at the assembly step becomes 2 to 5x larger than single chip package if the yield is found to be low at final test. The back grinding condition of NAND flash, Die Attach Film and its cure condition, filler damage during the mold process are identified as critical steps. Also, DC test yield feedback at the assembly site becomes an effective tool to closely monitor the yield.

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ROADMAPS FOR MULTI DIE INTEGRATION – STRATEGIES AND DRIVERS

ALTERNATIVES ON THE ROAD TO 3D TSV

E. Jan Vardaman
President
TechSearch International, Inc.

The demand for 3D TSV technology remains driven by performance such as high bandwidth between memory and processor and the need for lower power. While the drivers for 3D TSV remain constant but the time line for its adoption keeps shifting out. Several technical challenges and business logistics and infrastructure issues are delaying the full commercialization of 3D TSV. These issues include, design, the debonding step in wafer thinning, thermal dissipation, and test. Several companies are developing new materials that may improve yield and, improvements in equipment are expected in the future. EDA tool improvements to enable thermally aware designs are anticipated. The introduction of 3D TSV will also require new developments in test methodologies. Known good die is a requirement in order to provide sufficiently high yield to makes the process cost effective. Companies are still discussing issues such as whether to probe or not to probe wafers, the use of BIST, and required test methodologies. Supply chain issues are still under discussion.

While these issues are being resolved, companies will use alternative such as package-on-package (PoP) with fan-out WLP or embedded die in the bottom package, stacked die with wire bond, and interposers (also called 2.5D). This presentation describes various applications and the planned alternatives.

SESSION TWO

ENABLING MULTI DIE INTEGRATION

Session Chair:

Kumar Nagarajan
Director, Package Development & Assembly Engineering
Maxim Integrated

Multi die integration using 2.5D/3D IC is becoming the natural evolution of semiconductor technology since it enables integration of heterogeneous functionality and process technologies, complementing "Moore's Law" transistor scaling for different end market applications. It offers unique benefits such as increased capacity, improved performance, reduced power consumption, reduced footprints, faster time-to-market and lowered risk/cost. Various facets of the semiconductor industry such as Process/Package technology, Equipment technology, Material technology, EDA tools, Standards, Test, Metrology, Characterization, Reliability, FA have to come together to enable the transition into 2.5/3D IC. This session will discuss the enabling technologies and key trends that make multi die integration possible.

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ROADMAPS FOR MULTI DIE INTEGRATION – STRATEGIES AND DRIVERS

SILICON INTERPOSER DESIGN: ARCHITECTURE THROUGH IMPLEMENTATION

Bill Acito
Product Engineer
Cadence Design Systems Inc.

The buzz in the semiconductor industry over 3D-ICs and 2.5D integration continues to escalate. Today, many designs are implementing through-silicon-vias (TSVs) in passive silicon rather than active silicon; dies are being integrated side-by-side on a silicon-based substrate (interposer) and connected through silicon-process local interconnect.

While much of the discussion involving silicon interposers has been related to manufacturing, some are thinking broader and looking at the silicon interposer as a part of an overall system. This requires consideration of a silicon substrate as part of an integrated chip-interposer-package-PCB environment. There is great value in early system planning that includes the interposer so that cost of the system can be reduced and electrical performance maximized.

MULTI DIE INTEGRATION – CAN MATERIAL SUPPLIERS MEET THE CHALLENGE?

Jeff Calvert
Global R&D Director, Advanced Packaging Technologies
Dow Electronic Materials

A conundrum for materials suppliers relative to multi die integration is that with so many technical issues to address how can one be sure a material addresses the most important technical hurdle and know it is the right one? And, with so many players in the game setting different rules, how does one determine which design scheme will take hold? With so many applications and many potential integration options, it can be quite intimidating for material suppliers. Achieving economies of scale to meet cost targets is an enormous concern and there isn't a material supplier out there that doesn't want to take the gambling aspect out of the decision making. To manage this risk, one approach suppliers can take is to develop material platforms that are customizable and address common demands and requirements whenever possible. In the end, cost/performance trade-offs will be the determining factor for adoption of a material and it pays to embrace this certainty. This presentation will address these issues and challenges.

Presentation not available at time of printing.

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THE STRANGE WORLD OF NETWORKING MEMORY

David Chapman
VP Marketing & Applications Engineering
GSI Technology

The development of memory devices for the computer market continue to rely on increasing date bandwidth to improve performance...but the networking market has always needed something else...high transaction rate. As we move forward into a new age of fine pitch interconnect, the fundamental differences in the performance requirements of different markets will continue to drive demand for performance differentiated memory devices. In this presentation GSI will describe what makes networking different and describe what GSI is doing to drive a networking memory roadmap that will carry the industry into the next decade.

KEYNOTE

THE PROMISES AND PITFALLS OF 2.5D PACKAGING… A USER PERSPECTIVE

Anwar A. Mohammed
Senior Staff Scientist, Advanced Interconnect and Packaging
U.S. R&D Center, Huawei Technologies

There are very few technologies that are truly seminal and game changing; 2.5D appears to be one of them. There is a confluence of events that make this technology compelling. The inexorable demand in the market for escalating bandwidth is so potent that the present memory technologies cannot keep up with it. Wide I/O memories are fast becoming indispensable and their application is becoming feasible with powerful enablers like 2.5D technology. The integration of ASIC and memory, and other heterogeneous chipsets on a Silicon interposer, allow many benefits including miniaturization and enhanced performance. Next generation node scaling, our favorite pathway to keep up with Moore's law is becoming exorbitantly expensive. The technology landscape of the future will have fewer advanced semiconductor fabs, more companies going fabless and more companies leveraging opportunities offered by 2.5D packaging. Before we can materialize the promises of 2.5D technology there are significant hurdles and pitfalls the industry will have to overcome. Pre-competitive collaboration would be a very prudent approach to bring us all closer to the vision much faster.

Presentation not available at time of printing.

SESSION THREE

EMERGING TECHNOLOGIES FOR MULTI DIE PACKAGING

Session Chair:

John Xie, Ph.D.
Senior Manager, Packaging Technology Department
Altera Corporation

Multi-die packaging technology carries a new meaning today, with much increased system bandwidth requirements and fast progress in advanced interconnect technology and its integration with latest generation of silicon technology. It also fills the gap between high density and high cost 2.5D/3D integration solution and traditional 2D packaging solution. This session will include discussions covering advanced substrate technology, high density MCP assembly technology, design and performance consideration, possible business applications etc.

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ROADMAPS FOR MULTI DIE INTEGRATION – STRATEGIES AND DRIVERS

HIGH DENSITY ORGANIC INTERPOSERS FOR 2.5D/3D MULTI-CHIP PACKAGE

Chaowen Chung, Ph.D.
Marketing Director
Unimicron Technology Corp.

Due to the market demand, more functions and processing power are put into electronic packaging systems. Also reducing the over packaging and module dimensions becomes a continued effort in the electronic industry. Traditionally the most popular substrate is made of organic materials reinforced by glass fiber. However, due to requirement above, the substrate technology becomes more versatile. There are several organic substrate technologies are emerging that will be discussed.

- Low CTE substrate materials with CTE close to that of silicon.
- Substrate materials with a lower dielectric constant and dispassion factor for high frequency applications.
- Embedded technology, both embedded active and passive components into the substrate.
- Use thin core and even coreless technology for a better electrical performance with thin profile.
- Fine pillar substrate technology to support PoP structure.
- Organic interposer technology that requires 5/5 or even 3/3 μm fine line patterns in the organic substrate.

ORGANIC INTERPOSER ADVANCED PACKAGING BUILD-UP TECHNOLOGY

Joseph Dang
Field Applications Engineer
Kyocera America, Inc.

Kyocera has developed an advanced build-up substrate technology with a composite CTE of 10-13 ppm/C. This low CTE organic material reduces the thermal mismatch between chip and substrate that enables tighter flip chip pitches down to as low as 120um.

The technology is called APX (Advanced-SLC™Package X), which consists of core and build-up materials with copper circuitry. The new build-up film maintains both conductivity and dielectricity with 10/10μm line/space and 25μm via diameter. The core material has excellent reliability properties with 57μm through-hole diameter and 120μm through-hole pitch.

Substrates with these newly advanced design rules and material properties can enable smaller chip sizes, and lower thermal stress during the flip chip assembly. This presentation will discuss the key features and potential applications.

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ROADMAPS FOR MULTI DIE INTEGRATION – STRATEGIES AND DRIVERS

LOW COST SOLUTIONS FOR 2.5D PACKAGING

Young Do Kweon
Vice President
Samsung Electro-Mechanics Co., Ltd.

In order to achieve high density and high performance package, three dimensional chip integration has been desired. 3D chip integration may provide a path to miniaturization, high bandwidth, low power, high performance and system scaling. There are many approaches to 3D packaging. 3D ICs designed with TSV offers the ultimate in 3D integration, but currently it can be only adopted to high-end products because of cost issues such as known good die (KGD), expensive process cost, etc. 2.5D interposer stacking could offer alternate solutions. However, silicon interposers still have cost issues. If organic technology can replace silicon technology, it could be an innovative packaging solution.

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ROADMAPS FOR MULTI DIE INTEGRATION – STRATEGIES AND DRIVERS

MULTI DIE INTEGRATION FOR HIGH BANDWIDTH NETWORKING DEVICES: A USER PERSPECTIVE

Ray Niu
Sr. Component Engineer, U.S. R&D Center
Huawei Technologies

The demand on bandwidth for high end networking and computing applications escalates as high as ten times for every new generation of silicon, which results into serious challenges for the processor and memory device. The gap between system requirements and current memory technology is increasing at an alarming rate. Developing new solutions which can adequately respond to these needs, while concurrently mitigating the reliability, cost and manufacturability risks is becoming critical. 2.5D/3D IC integration with high density connection, high bandwidth and low power consumption appears to be a very promising solution. However there are serious hurdles to overcome first including thermal, test, cost and reliability before this becomes a reality.

SESSION FOUR

PANEL:
DRIVERS FOR MULTI-DIE PACKAGING

Moderators:

Ivor Barber
Director, Package Design and Characterization
LSI Corporation

Rich Rice
Senior Vice President of Sales
ASE (US) Inc.

During this symposium the speakers will explore multi die integration strategies, enabling technologies related to packaging and its infrastructure, as well as emerging technologies and approaches. In a panel session these speakers and other industry experts will interact with attendees to discuss and explore the new opportunities, barriers, and future work needed for packaging solutions in the era of 2.5D and 3D multi die integration.

Panelists:

Joseph Dang
Kyocera

Dave Love
GenapSys

Steve Smith
Synopses

Alex Tsai
TSMC North America

Jan Vardaman
TechSearch International

About MEPTEC

MEPTEC (MicroElectronics Packaging and Test Engineering Council) is a trade association of semiconductor suppliers, manufacturers, and vendors concerned exclusively with packaging, assembly, and testing, and is committed to enhancing the competitiveness of the back-end portion of the semiconductor industry. Since its inception over 30 years ago, MEPTEC has provided a forum for semiconductor packaging and test professionals to learn and exchange ideas that relate to packaging, assembly, test and handling. Through our monthly luncheons, and one-day symposiums, and an Advisory Board consisting of individuals from all segments of the semiconductor industry, MEPTEC continuously strives to improve and elevate the roles of assembly and test professionals in the industry. For more information about MEPTEC events and membership visit www.meptec.org.

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