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FPGA-forum 2014

The 9th FPGA-forum – where the Norwegian FPGA community meets

- **FPGA-forum and exhibition:** Wednesday 5th and Thursday 6th of February 2014
- **Tutorials/Workshops:** Tuesday 4th of February 2014

Britannia Hotel (Trondheim)

FPGA-forum er den årlige møteplassen for FPGA-miljøet i Norge. Her samles FPGA-designere, prosjektledere, tekniske ledere, forskere, siste års studenter og de største leverandørene på ett sted for 2 dagers praktisk fokus på FPGA.
Det blir foredrag fra norske bedrifter om utviklingsmetodikk og praktisk erfaring, universitetene presenterer nye og spennende prosjekter, og leverandørene stiller med aktuelle tekniske innlegg med et minimum av markedsføring. På utstillingen vil du kunne vurdere teknologi og verktøy fra de ledende leverandørene i bransjen.
FPGA-forum byr i tillegg på en ypperlig anledning til å møtes og utveksle erfaring innenfor FPGA-miljøet i Norge - både i pausene og under det sosiale arrangementet på kvelden.

In English:
FPGA-forum is a yearly event for the Norwegian FPGA community. FPGA-designers, project managers, technical managers, researchers, final year students and the major vendors gather for a two-day focus on FPGA.
There will be presentations from the Norwegian industry about methodology and practical experience, - the universities will present new and exciting projects, and the vendors will have technical presentations with a minimum of marketing. At the exhibition you can evaluate tools and technology from the leading vendors.
FPGA-forum also provides an excellent opportunity to meet and exchange experience with the Norwegian FPGA-community – in the breaks – and during the official dinner party on Wednesday.

Official website for FPGA-forum: www.fpga-forum.no

Hotel

A special discount price of NOK 1085 is available for conference participants at Hotel Britannia (Dronningens gate 5). For reservations call +47 73800800 and refer to Tekna's FPGA-forum ASAP.
Please note that the discount price or room availability can no longer be guaranteed.

Note: Minor programme changes may occur.

Programme Wednesday, February 5, 2014 (Note: See appendix for abstracts)

09.00	Registration and coffee	
Session 1	**Track AB -** Session chair: Atle Tangedal, Tekna, Jim Tørresen, UiO and Espen Tallaksen, Bitvis	
09.25	**Opening**	
09.30	**Keynote by Oliver Pell, VP of Engineering, Maxeler Technologies** From FPGAs to reconfigurable dataflow computers	
10.30	**Vendor presentations** (3 min. per exhibitor - in alphabetical order)	
11:10	**Coffee break (and exhibition)**	
Session 2	**Track A** Session chair: Knut Wold, Høgskolen I Gjøvik	**Track B** Session chair: Hans Jørgen Fosse, Mikrokrets
11.30	**A practical introduction to High Level Synthesis (HLS) using Vivado HLS** Jan Anders Mathisen, AvnetSilica (Xilinx)	**SmartFusion2 – Embedded system "Root-of-Trust". Secure Boot Demonstration** Peter Trott , Avnet Memec (MicroSemi)
12.00		**Ruby for digital design** Audun Wilhelmsen , OmniVision Technologies
12:30	**Scaling your design environment with less pain** Petter Gustad, Cisco	**10 Ways to Effectively Debug your FPGA Design** Antti Innamaa, Synopsys
13.00	**Lunch and Exhibition**	
Session 3	**Track A** Session chair: Håvard P.Alstad, Data Respons	**Track B** Session chair: John Aasen, Kongsberg
14:15	**Erfaringer fra å fornye ett «parkert» produkt og ta fram et nytt i samme slengen** Atle Haga , HDD	**RCU2 - The ALICE TPC Readout Electronics Consolidation for Run 2** Johan Alme , HiB (Høyskolen I Bergen)
14:45	**Implementation of Level-Shifted PWM Control for Modular Multilevel Converter Utilizing Xilinx ZC702 Evaluation Board** Chuen Ling , NTNU	**HW/SW Co-Design and Verification Made Easier** Jonas Rutström , Mathworks
15:15	**Hybrid Memory Cube - Next generation SDRAM** Nikolay Rognlien , Arrow (Altera)	**A practical guidance towards more advanced verification using Coverage and OVL** Rick Stroot , InnoFour (Mentor Graphics)
15.45	**Exhibition and Coffee**	
Session 4	**Track A** Session chair: Jim Tørresen, Universitetet I Oslo	**Track B** Session chair: Roar Skogstrøm, Kongsberg
16.15	**Presentation of the 2 Master's theses nominated for the FPGA-forum award** *(see page 4)* *(Note: The award is given during the dinner party)*	**Timing analysis "crash course"** Nikolay Rognlien , Arrow (Altera)
16:45		**Distribuert versjonkontrollsystem – himmel eller helvete?** Tore Fleten, Cisco
Session 4x	**Track AB -** Session chair: Espen Tallaksen, Bitvis	
17.15	**Closing Keynote: VHDL: past, present & future** Jim Lewis, VHDL Training Expert, SynthWorks	
18.00	**End of today's presentations**	
19.30	Aperitif in the 'Lobby Lounge' outside 'Speilsalen', Britannia Hotel	
20.00	Dinner party in 'Speilsalen', Britannia Hotell. Entertainment: Pirum (Student choir)	

Programme Thursday, February 6, 2014 (Note: See appendix for abstracts)

Session 5	**Track A** Session chair: Johan Alme, Høgskolen I Bergen	**Track B** Session chair: Arild Kjerstad, Kongsberg
09.00	**VUnit - An Automated Testing Framework for VHDL** Lars Asplund , Synective Labs	**Linux på FPGA – himmel eller helvete?** Tore Fleten , Cisco
09.30	**Designing with Vivado in real life projects** Frode Eskelund , Prevas	**Development of a 10G Ethernet UDT Server in FPGA** Steinn Gustafsson , Chevin Technology
10.00	**Learning FPGA Design Through Internet and Remote Labs** Jim Tørresen, UiO (Universitetet I Oslo)	**Verification practices for FPGAs with embedded processors** Alex Grove, FirstEDA (Aldec)
10.30	**Posters, Exhibition and Coffee**	
Session 6	**Track A.** Session chair: Bjørn B. Larsen, NTNU	**Track B** Session chair: Frode Eskelund, Prevas
11.30	**RESET (og andre myter) i FPGA** Rune Bæverud , Thales	**Maximising Serial Bandwidth and Signal Integrity in High Speed FPGAs" and "Measuring & Characterising low power Energy Efficient Devices"** Thomas Göransson, 4Test Instruments (Agilent)
12.00	**The good, the bad and the ugly** Espen Tallaksen, Bitvis	
12.30	**Lunch and Exhibition**	
Session 7	**Track A** Session chair: Anne Elisabeth Vallestad, ABB	**Track B** Session chair: Ian Ringheim, WesternGeco
13.45	**KRYPTO og SAFETY i FPGA** Rune Bæverud, Thales	**Choosing the right SoC FPGA for Your Application** Amar Abid-Ali , EBV (Altera)
14.15	**User experiences from the FPGA development of T-9, the next generation reverse vending machine** Atle Holter, Tomra	**Exhibition**
14.45	**Coffee break**	
Session 8	**Track AB: Closing Keynotes** Session chair: Atle Tangedal, Tekna	
15.00	**Closing Keynote: Seismic Acquisitions Systems – with ASIC and FPGA as enabling technologies in past, presence and future** Vidar Husom, Chief Electrical Engineer, WesternGeco	
15.35	**Closing Keynote: I have a product! Now let's build the market!** Torstein Dybdahl, Product Management Director, FXI Technologies	
16.10	Closing words	
16.15	The end	

Keynotes:

- Opening keynote: Oliver Pell, VP of Engineering, Maxeler Technologies
  From FPGAs to reconfigurable dataflow computers
- Closing keynote D1: Jim Lewis, VHDL Training Expert, SynthWorks
  VHDL: past, present & future
- Closing keynote D2: Vidar Husom, Chief Electrical Engineer, WesternGeco
  Seismic Acquisitions Systems – with ASIC and FPGA as enabling technologies in past, presence and future
- Closing keynote D2: Torstein Dybdahl, Product Management Director, FXI Technologies
  I have a product! Now let's build the market!

Workshops/Tutorials Day 0, Tuesday 4th:

Note that workshops have limited seating. There are also limitations on min. number of participants.
There are 5 workshops in parallel. Workshops 5a and 5b run in series.
Some workshops are free; others have a small registration fee.
More info in the Workshop overview (pages 6-11)

- 1: MathWorks
  - HDL Coder Workshop
- 2: Avnet Memec (MicroSemi)
  - SmartFusion2 FPGA Hands-on workshop
- 3: Cancelled
- 4: Silica (Xilinx)
  - Introduction to Vivado
- 5a: Bitvis
  - Making good VHDL testbenches
- 5b: FirstEDA (Aldec)
  - Simplify Design Validation with VHDL Transaction Level Modelling

List of exhibitors (for Wedn. 5th and Thur. 6th):

- 4Test www.4test.no
- Arrow Norway (Altera) www.arrowne.com
- Avnet Memec (Microsemi/Actel) www.microsemi.com
- Avnet Silica (Xilinx) www.silica.no
- Bitvis www.bitvis.no
- EBV (Altera) www.ebv.com
- FirstEDA (Aldec) www.firsteda.com
- Innofour (Mentor) www.innofour.com
- MathWorks www.mathworks.com
- Prevas www.prevas.no
- Synective www.synective.se
- Synopsys www.synopsys.com

Price award for Best FPGA related Master thesis in Norway:

FPGA-Forum's price is given to the best FPGA related Master thesis in Norway.

The award committee:

- Knut Wold, Høgskolen i Gjøvik (Gjøvik University College)
- Kjetil Ullaland, Universitetet i Bergen (University of Bergen)
- Hans Jørgen Fosse, Mikrokrets

The nominees in alphabetical order:

- Cecilie Bjelbøle, Universitetet i Oslo (University of Oslo)
  "An Attitude Determination and Control System for CubeSTAR",
- Andre Firing, NTNU (Norwegian University of Science and Technology)
  "FPGA Filter Design and Measurements with Emphasis on a Filter with Steep Transition Bands"

Both nominees will present their Master thesis in the last session on day 1.
The winner will be announced during the dinner party.

Entertainment (during the dinner party):

Pirum (Student choir)

Poster Presentation (Day 2):

Context Switching on FPGAs with State Save and Restore
by Sindre Georgsen, University of Oslo

FPGA-forum Program-committee:

- Arild Kjerstad, Kongsberg
- Hans Jørgen Fosse, Mikrokrets
- Jan Anders Mathisen, Silica/Xilinx
- Jim Tørresen, Universitetet i Oslo
- Atle Tangedal, Tekna
- Espen Tallaksen, Bitvis

Workshops (day 0) details for FPGA-forum 2014

(In company alphabetical order)

Workshop 1	**HDL Coder Workshop**	
Company	**MathWorks**	Engineers are using MATLAB and Simulink to design and verify complex algorithms for applications such as signal processing, communications, image processing, and control design. When these algorithms are implemented in FPGAs and ASICs using hand-coded Verilog and VHDL, design errors creep in and lead to increased costs, lower quality designs, and delayed or cancelled projects. In today's session, we will demonstrate how you can leverage automatic HDL code generation and verification on different levels of abstraction to accelerate your FPGA design and ASIC prototyping workflow. We will also illustrate how these technologies can be integrated into your existing design workflows. You will get hands-on experience with: • MATLAB to HDL workflow: - Start with floating point model - Conversion to the fixed-point model - Generate optimized HDL code and test bench - Verify HDL vs. MATLAB (stand-alone and HDL co-simulation) • Simulink to HDL workflow: - Optimize fixed-point models - Generate optimized HDL code and test benches - Various verification techniques for models, HDL code and FPGAs - Integrating legacy HDL, vendor specific HDL and peripheral interfaces - Rapidly prototype algorithms on FPGA evaluation boards
Presenter	Jonas Rutström	
Start time	9:15	
End time	17:00	
Registration fee	Free	
Lunch & coffee?	Included	
Min. no. of participants	5	
Max. no. of participants	12	
Prerequisites	Participants will use their own laptops.	
Important notices		

Workshop 2	**SmartFusion2 FPGA Hands-on workshop**	
Company	**Avnet Memec (Microsemi)**	The class demonstrates the techniques and tools used to create a basic SmartFusion2 SoC FPGA design that integrates an inherently reliable flash-based FPGA fabric, a 166 megahertz (MHz) ARM® Cortex™-M3 processor, DSP blocks, SERDES transceivers, DDR controllers, eSRAM, eNVM, and advanced security processing accelerators. During the workshop, you will learn about the capabilities, features and usage of SmartFusion2 SoC FPGAs, including: • Understanding the capabilities of the flash-based FPGA fabric including DSP and integrated memory blocks • Introduction to the ARM Cortex-M3 based microcontroller subsystem (MSS) • Details of the MSS peripherals and integration techniques • Low power design techniques • Design and data security features of the SmartFusion2 • Overview of the 5Gbps SERDES, PCIe, XAUI / XGXS+ Native SERDES capabilities • Debug capabilities of the device and software tools Hands on labs will utilize the SmartFusion2 Starter Kit, which supports: • Introduction to the FPGA design flow including timing and power analysis • Firmware development for ARM Cortex-M3 design • System Builder session for SoC system configuration • USB design implementation demo
Presenter	Peter Trott	
Start time	9:00	
End time	17:00	
Registration fee	NOK 750 (*1)	
Lunch & coffee?	Included	
Min. no. of participants	6	
Max. no. of participants	20	
Prerequisites	None	
Important notices	*1: Registration fee includes free SmartFusion2 Starter kit worth $299 More information may be found under: http://www.avnet-memec.eu/seminar/smartfusion2-fpga-hands-on-workshop-at-the-fpga-forum.html?L=0&cHash=299be19ca082265a5d1259436cd81a4a	

Workshop 4	**Introduction to Vivado**	
Company	**Avnet Silica (Xilinx)**	This entry level course provides a foundational understanding of the Xilinx® Vivado® Integrated Development Environment (IDE) and demonstrates its use in taking a design from RTL through implementation. Short presentations and hands-on labs show attendees how to create a new project, create and import IP cores, set basic clocking and I/O timing constraints, synthesize and implement a design, and analyze the results through Vivado Analysis features and the various design reports.
Presenter	Jan Anders Mathisen	
Start time	9:00	
End time	16:00	
Registration fee	Free	
Lunch & coffee?	Included	
Min. no. of participants	6	
Max. no. of participants	14	
Prerequisites	Laptop required. Basic FPGA design experience is helpful.	
Important notices		

Workshop 5a	**Making good VHDL testbenches**	
Company	**Bitvis**	1) Making a simple and structured TB, using Bitvis Utility Library; - including concepts and usage 2) DEMO: How to debug your design in a very efficient manner - using Bitvis Utility Library 3) Making good BFMs. a) Using Bitvis Utility Library b) General overview of a good BFM and what it should do b) Handling normalisation of vectors for procedures c) Including sanity checks d) Configuring behaviour - to allow single BFM for multiple targets e) Looking into the VHDL code in more detail 4) Making a testbench with concurrent execution of multiple BFMs. (TLM-based approach) a) The "normal" approach b) A structured process-oriented approach c) A structured component oriented approach
Presenter	Espen Tallaksen	
Start time	10:00	
End time	13:00 (*1)	
Registration fee	Free	
Lunch & coffee?	Included (*2)	
Min. no. of participants	6	
Max. no. of participants	20	
Prerequisites	VHDL knowledge	
Important notices	*1: In series with 5b, but separate registration *2: Common lunch at 13:00 for workshops 5A and 5B	

Workshop 5b	**Simplify Design Validation with VHDL Transaction Level Modelling**	
Company	**FirstEDA (Aldec)**	Thoroughly testing a design takes time, particularly when one considers that we must first do RTL testing, then Core-level testing, and then Chip/System-level testing. Many would prefer to skip to the lab and test their FPGAs there. However, as FPGAs have grown, so has the complexity of lab based debugging, simulation based environments on the other hand give easy access to all internal logic and simplify debug. This workshop explores the use of a Transaction Level Modelling (TLM) test environment to simplify test creation in that simulation environment. ---------- TLM is just a fancy way of saying let's represent the bus interface operations (such as CPU Read and CPU Write) as VHDL procedure calls. These subprogram calls replace wiggling interface signals directly. As a result, the test is easier to create and to read, as the design and interfaces evolve, a small change to the interface signalling in a TLM environment results in minor changes to the TLM procedures. On the other hand, when using the alternative approach, an interface change is a significant change to the test environment. What you will learn: • How to create TLM tests. • Transitioning from RTL to Core to Chip level testing. • Use of the Open Source VHDL Verification Methodology (OS-VVM) to add constrained random and intelligent coverage test generation. • Use of coverage to validate that all items in the testplan have been completed.
Presenter	Jim Lewis and David Clift	
Start time	14:00 (*1)	
End time	17:30	
Registration fee	Free	
Lunch & coffee?	Included (*2)	
Min. no. of participants	6	
Max. no. of participants	20	
Prerequisites		
Important notices	*1: In series with 5a, but separate registration *2: Common lunch at 13:00 for workshops 5A and 5B	

Titles and Abstracts for presentations at FPGA-forum 2014

(In company alphabetical order)

Company & Presenter	Title & Abstract
4Test Instruments (Agilent) Thomas Göransson	**Maximising Serial Bandwidth and Signal Integrity in High Speed FPGAs" and "Measuring & Characterising low power Energy Efficient Devices"** Maximising Serial Bandwidth and Signal Integrity in High Speed FPGAs: Consumers demand more performance and throughput in the increased use of data in our connected world– as a result engineers must design, develop and validate boards and systems that have multiple high speed transceiver SERDES channels. The entire serial transmission and measurement eco-system must be considered to accurately characterize the throughput, waveform and jitter performance of such lanes. For example, accurate de-embedding requires measurement of the calibration structures which plays an important part in the ability of an oscilloscope to recover the undistorted waveform from such fast transmitters. This paper will describe some of these challenges and offers possible solutions with the latest innovations. Measuring & Characterising low power Energy Efficient Devices: The proliferation of mobile devices and "green" products has created a growing need to make low-power, high-dynamic-range measurements. As products get smarter and more feature rich, all components need to be more energy efficient to consume less and preserve battery life. Designers who work with power-consumption measurements need solutions to make accurate current-consumption measurements at an affordable cost. This paper discusses how a high resolution 9000 H-Series oscilloscope and new current probes combine low noise and high sensitivity to give engineers the high-accuracy measurements they need for creating energy-efficient products."
Aldec	See FirstEDA
Altera	See Arrow and EBV
Arrow (Altera) Nikolay Rognlien	**Hybrid Memory Cube - Next generation SDRAM** External DDR3/DDR4 SDRAM interfaces has reached some physical challenges that are hard to overcome. Hybrid Memory Cube is a groundbreaking new way forward. This session introduce you to HMC concepts and architectures.
Arrow (Altera) Nikolay Rognlien	**Timing analysis "crash course"** This session will give you an introduction to "Static Timing Analysis" concepts and SDC(Synopsys Design Constraint) language. Helpful to both fresh fpga designers as well as experienced ones that could use some reminders.
Avnet Memec (MicroSemi) Peter Trott	**SmartFusion2 – Embedded system "Root-of-Trust". Secure Boot Demonstration** Content: With the enhanced security that has been added to SmartFusion2, the family can not only be programmed in an "un-trusted" location but can also be used as a system root of trust device. Using secure cryptography techniques SmartFusion2 can be used to boot and validate code belonging to any processor within the system. If tampering is detected then action can be taken which far exceed any other security device that might be used within a system. This paper will show a possible implementation of secure boot and demonstrate the process on a hardware platform.

AvnetSilica (Xilinx) Jan Anders Mathisen	**A practical introduction to High Level Synthesis (HLS) using Vivado HLS** The idea of using higher abstraction levels in designing digital systems and bridging SW/HW development for FPGAs with hard processor systems has been the theme for several presentations at FPGA-Forum over the last few years. This presentation takes a practical look at the use of HLS through examples and demos with Vivado HLS.
Bitvis Espen Tallaksen	**The good, the bad and the ugly** The way you implement your FPGA design and write your code has a huge impact on your development efficiency and product quality. The strange thing is that even many experienced designers tend to write both bad and ugly code. Does it matter if the code is ugly if it works in the lab? Yes – definitely, and for several reasons. First of all – the probability that ugly code has serious bugs is far higher than for good code. Also any change made to ugly code has a far higher risk of introducing bugs. And of course – ugly code makes it far more difficult to do a proper review. More time consuming, often frustrating, and with a far worse review quality. Bad and ugly code often results in errors that may be difficult to find and terrible to correct. This presentation will show some examples of bad and ugly code, how they result in inefficiency or bugs, and also suggest some remedies and suggestions for improvements – in order to write good code. (Examples will be in VHDL, but apply equally well for other languages)
Chevin Technology Steinn Gustafsson	**Development of a 10G Ethernet UDT Server in FPGA** This presentation describes development of a 10G Ethernet UDT server on a Virtex6 FPGA for a high-speed, high-reliability data recording application. We will look at architecture choices and selection of protocol, architecture for processor and data offload mechanism in FPGA. Lower layers from SFP+ wire to PHY chip and XAUI, XGMII require use of Xilinx Multi Gigabit Transceivers at relatively high clock rates. The protocols Ethernet, ARP, ICMP, IP, UDP and their implementation in FPGA are all a requirement for an efficient and high-performance UDT server implementation. We will see how these layers are handled by hardware and software functions, and look at the verification strategy, simulation, test vectors and other tools such as Wireshark. The presentation will also cover figures for FPGA resource usage, data transfer rate performance, latency and reliability. Extensive and continuous use over long time demonstrates that FPGAs today are capable of sustained high speed data transfer, using protocols that ensure zero errors using standard off the shelf hardware. The presentation will show how high performance Ethernet connectivity can be quickly and easily embedded through the use of standardized interfaces, widely used tools and test harnesses, which greatly shorten integration time and reduces development effort.
Cisco Tore Fleten	**Linux på FPGA – himmel eller helvete?** Vi har lenge brukt Linux, som operativ system, på ARM prosessorer. Jeg vil gå igjennom noen av de system valgene vi gjorde på et ARM/FPGA design, hvor vi valgte å bruke Linux som operativ system. Dette medførte noen overraskinger: • Avhengighet mellom FPGA releaser og OS releaser • Program størrelse • Power forbruk • Oppstart tid
Cisco Tore Fleten	**Distribuert versjonkontrollsystem – himmel eller helvete?** En presentasjon over hvilke fordeler og ulemper vi hadde med å gå fra subversion til git, som versjonkontrolsystem. Subversion er det siste «sentraliserte» versjonkontrollsystem, mens git (og Mercurial) er de ledende distribuerte versjonskontrollsystemer.
Cisco Petter Gustad	**Scaling your design environment with less pain** How to make the transition from a design environment consisting of one designer, one design, single vendor, and one PC to multiple designers, multiple designs, and multiple vendors and utilizing a simulation and build farm less painful.

EBV (Altera) Amar Abid-Ali	**Choosing the right SoC FPGA for Your Application** We will analyze various metrics to help system architects, engineers and managers decide if SoC FPGAs are a fit for their application and what the advantages of an Altera SoC solution are. SoC FPGA devices integrate both processor and FPGA architectures into a single device. Melding the two technologies provides a variety of benefits including higher integration, lower power, smaller board size, and higher bandwidth communication between the processor and FPGA. Best-in-class devices exploit the unique advantages of a merged processor and FPGA system while retaining the benefits of a stand-alone processor and FPGA approach. But which SoC FPGA is right for your application?
FirstEDA (Aldec) Alex Grove	**Verification practices for FPGAs with embedded processors** Most FPGAs will have an embedded processor large or small. In this presentation we will look at a number of techniques that can be employed to verify embedded systems. We will look at the use of virtual prototypes, RTL simulation, hardware assisted verification, and finally hardware development boards. For each use case we will explore the benefits and costs and provide practical examples of their use.
FXI Technologies Torstein Dybdahl	***** CLOSING KEYNOTE Day 2: I have a product! Now let's build the market!** First you have a good idea, then you develop the product at get rich:-) What if you take it backwards, you have a fantastic new product and nobody understands your product and there is no market. I will walk you through the story how we created the Cotton Candy microcomputer and how we changed an industry.
HDD Atle Haga	**Erfaringer fra å fornye ett «parkert» produkt og ta fram et nytt i samme slengen** HDD lager krypteringsløsninger for lagrede data, framfor alt disker til laptop'er. Det er en stor utfordring å forholde seg til alle standarder og legacy som ligger i en PC-plattform og finne løsninger som fungerer på «all» hardware. HDD har tatt fram en ny generasjon produkter og vi vil fortelle om gode og noen dårlige erfaringer gjort underveis.
HiB (Høyskolen I Bergen) Johan Alme	**RCU2 - The ALICE TPC Readout Electronics Consolidation for Run 2** This presentation focuses the solution for optimization of the ALICE TPC readout for running at full energy in the Run 2 period after 2014. During these three years an event readout rate of 400 Hz with a low dead time is envisaged for the ALICE central barrel detectors. A new component, the Readout Control Unit 2 (RCU2), is being designed to increase the present readout rate by a factor of about 2.6. The immunity to radiation induced errors will also be significantly improved by the new design. The project is driven from the Norwegian groups within the ALICE experiment at CERN, and includes contributions from UiB, UiO, HiB and HiVe in addition to international partners.
InnoFour (Mentor Graphics) Rick Stroot	**A practical guidance towards more advanced verification using Coverage and OVL** Many FPGA designs are being verified using traditional methods by providing stimulus and debugging the output results to find any possible errors in the design. Although there are more advanced methods to verify designs, the hurdle to adopt these complex techniques is often too high or the time to invest in learning these methodologies is simply lacking. This presentation will give you a more practical approach into adopting methodologies such as Coverage and OVL, that form a first step towards advanced verification. These methodologies are easy to adopted without having to invest time and effort in learning new languages or complex methodologies. Live demonstrations will clarify the methodologies discussed in the presentation, and tutorials based on these demonstrations will be made available to the audience for a quick start in deploying these methodologies in your own organization.

Mathworks Jonas Rutström	**HW/SW Co-Design and Verification Made Easier** During this presentation you will learn how you can accelerate your HW/SW co-design process, speed up your verification workflow, and increase confidence in your final implementation targeting FPGAs, ASICs, MCUs or DSPs. We will focus on MATLAB and Simulink as an integrated environment that can be used during the entire development process of a product including both hardware and software – from idea to implementation. We hope to inspire you to investigate new powerful solutions that take you and your colleagues into the next level of product development using MATLAB/Simulink in combination with other tools from leading FPGA vendors. Highlights include the following: - Integrated workflow for HW/SW co-design - Fixed-point conversion and analysis - Platform independent HDL code generation - Area, speed and power optimization techniques - Verification and validation using co-simulation and FPGA-in-the-Loop with FPGAs from Xilinx and Altera.
Maxeler Technologies, Oliver Pell	***** OPENING KEYNOTE: From FPGAs to reconfigurable dataflow computers** High performance computing systems are increasingly constrained by power consumption, and it will not be possible to achieve exascale performance by simply scaling existing HPC architectures. At the same time, parallelism scaling and reliability are increasingly problematic. Inherently many of these issues arise from the intrinsic compromises and limitations of the general-purpose control-flow computer architecture. One solution is dataflow computing - a completely different method of computing to control-flow processors, focusing on optimizing the movement of data in an application and utilizing massive parallelism between thousands of tiny OEdataflow cores[1]. Modern FPGAs are increasingly capable and can be used as reconfigurable compute units in dataflow computers. However, enabling end-users to create dataflow configurations pushes FPGA chips firmly outside their common use case as 'ASIC replacements' and brings its own significant challenges. This talk will discuss some of the benefits of dataflow computing, the challenges in building and programming dataflow computers with FPGAs, and cover a few application case studies.
Mentor Graphics	See Innofour
MicroSemi	See Avnet Memec

NTNU Chuen Ling	**Implementation of Level-Shifted PWM Control for Modular Multilevel Converter Utilizing Xilinx ZC702 Evaluation Board** Abstract – Modular Multilevel Converter (MMC) is an advanced power electronics multilevel converter. It is modular with identical power cells. A unit of power cell consists of a minimum of two power semiconductors together with capacitor voltage sources. Therefore, the output voltage may easily be scalable by adding in new power cells. With this flexible structure, MMC has been proposed for HVDC applications. MMC manage to enable higher voltage operation by using low voltage power semiconductors. However, the complexity of the design and control in these converters will increase proportionally to the expansion of voltage steps. This type of converter requires hard real time control with short cycle time (in less than hundred microseconds range). DSP and FPGA have been widely used in this application. Complex control algorithms which involve mathematical functions are normally programmed in DSP. Since, DSP has limited number of IO ports; FPGA is normally used to distribute the obtained PWM pulses for driving each of the power semiconductors. In some implementation, FPGA may also use to execute part of the algorithms to minimize the processing time in DSP. Therefore, the handshake between DSP and FPGA must be coordinate properly to avoid noise problems. The Xilinx newly invented ZC702 is predicted as a new embedded processing platform for future development in power electronics converter control. It combines processing system with programmable logic in a single component (System-on-Chip) which eases designers to test their proposed algorithms freely. This presentation will share an implementation experience of MMC control using ZC702 board. An overview of the Level-Shifted PWM modulation scheme will first be presented. Then, implementation of two LogiCORE IP, i.e. Xilinx Analog-to-Digital Converter Wizard and Direct Digital Synthesizer Compiler core, will be discussed in details.
OmniVision Technologies Audun Wilhelmsen	**Ruby for digital design** Ruby is a modern scripting language that has gained popularity in recent time. It is well suited for various tasks within digital design, e.g. text processing, workflows for compiling and simulation, controlling simulation through VPI, high level modelling and domain specific languages. The presentation begins with an introduction to Ruby, and continues with examples of how the language can be used to solve various tasks within digital design
Prevas Frode Eskelund	**Designing with Vivado in real life projects** Vivado is Xilinx' newest design tool, and in several ways it is quite different from the classic and well established ISE design suite. Based on first-hand experience, this presentation will give an overview of how Vivado can be used in real life projects and highlight some of the new features and differences with respect to the older ISE. Practical examples based on experience gained in the use of Vivado alone and in combination with other tools will be presented.
Synective Labs Lars Asplund	**VUnit - An Automated Testing Framework for VHDL** Research suggests that iterative and incremental development (IID) is a key factor in increasing the success rate of projects. IID is not a new idea but has gained in popularity as agile software development methods are getting commonplace. This increased use of IID has also driven the development of tools to support iterative practices, for example unit testing frameworks for efficient, structured, and automated testing and continuous integration tools to enable many and short iterations. These tools are readily available for software practitioners, but are lacking for VHDL developers. VUnit was developed to close this gap and enable VHDL developers to make better use of known good practices. This presentation will show how VUnit can support development in a number of common use cases, from the creation of your test bench until it's a fully automated and continuously running regression test.
Synopsys Antti Innamaa	**10 Ways to Effectively Debug your FPGA Design** Today's FPGAs implement the equivalent of millions of ASIC gates. When the design fails to synthesize or fails to operate as expected on the board, the designer is faced with the daunting task of determining the source of the failure among potentially thousands of input files. Given how lengthy design iteration runtimes have become, designers have an enormous need for better ways to find errors early, incrementally and en masse. This paper is an elaboration of state of the art debug tools and techniques that avail today's high-end FPGA designers.

SynthWorks Jim Lewis	***** CLOSING KEYNOTE Day 1: VHDL: past, present & future** VHDL is an evolving language. It started as VHSIC (Very High Speed Integrated Circuits) Hardware Description language and has evolved into a modern Verification and Hardware Design Language. VHDL has been through revisions in 1993, 2000/2002, 2008, and is currently going through another revision. This presentation will take a look at some significant changes from the past, present (VHDL-2008), and some insight into the current on going work.
Thales Rune Bæverud	**KRYPTO og SAFETY i FPGA** I ethvert system kan det oppstå feiltilstander, vanligvis som en følge av ytre påvirkning. Dersom kravet til sikkerhet er høyt, hvordan kan vi håndtere og redusere effekten av en slik feiltilstand? I et sikkerhetskritisk system bygger man gjerne inn redundans og isolasjon av kritisk funksjonalitet for å kunne detektere og håndtere feiltilstander. Dette realiseres vanligvis med separate, fysiske kretser på et kretskort, noe som kan bli komplekst, dyrt, energikrevende og plasskrevende. KRYPTO og SAFETY bygger i utgangspunktet på ulike funksjonsmessige forutsetninger, men de deler likevel mange av prinsippene for oppbygningen av et sikkerhetskritisk system. Er det mulig å implementere et slikt system i en enkelt krets, f.eks. en FPGA?
Thales Rune Bæverud	**RESET (og andre myter) i FPGA** Har du noen gang REFLEKTERT over om og hvordan man bør implementere RESET i en FPGA? Bedrifter med egen avdeling for FPGA-utvikling har gjerne utviklet egne retningslinjer for "FPGA Best Practices", og der kan det f.eks. stå krav som: "Alle registre skal ha en RESET inngang med asynkron assert og synkron de-assert." Dette fungerer selvsagt. Vanligvis. Men dersom man glemmer å ha et kritisk og reflektert forhold til "Best Practices", så etablerer man samtidig et klima der MYTER lett kan slå rot. I grensetilfellene kan slike regler få store konsekvenser for mulig utnyttelsesgrad av en FPGA. I dette foredraget skal jeg ta for meg grensetilfellene for implementasjon av RESET i FPGA. Når trenger vi RESET? Når trenger vi ikke RESET? Hvordan bør vi eventuelt implementere RESET?
Tomra Atle Holter	**User experiences from the FPGA development of T-9, the next generation reverse vending machine.** In September 2013 Tomra released the new state-of-the-art reverse vending machine (RVM) named T-9. The T-9 is the result of 4 years of development and is the first of a new generation of RVMs from Tomra. T-9 features the first ever 360 degree recognition system applied inside an RVM and enables faster and cleaner collection of beverage containers, even odd shape containers that until now could not be collected in RVMs. The T-9 is built around the quite unique 'OneRing' mainboard. Experiences from the FPGA development will be presented.
UiO (Universitetet I Oslo) Jim Tørresen	**Learning FPGA Design Through Internet and Remote Labs, Jim Tørresen, Universitetet i Oslo** Teaching FPGA has typically required both dedicated FPGA-boards and special software. However, in the ERASMUS project European Digital Virtual Design Lab (eDiViDe, www.edivide.eu, 2011-2014) University of Oslo is together with three European partners developing remote FPGA-labs that students can access through the Internet. These are intended for learning development with programmable logic. We have in addition to hardware platforms, some tasks with simple setups with motion involved (traffic light control and robot control). The task for students is to develop control functions in programmable logic. Students can observe what happens both through video and electronic readings on the remote lab. The talk would introduce the lab environment and tell about the experience we have made so far. Other institutions are welcome to use the systems and/or connect their own setups to the framework.
WesternGeco Vidar Husom	***** CLOSING KEYNOTE Day 2: Seismic Acquisitions Systems – with ASIC and FPGA as enabling technologies in past, presence and future**
Xilinx	See Avnet Silica