From Spin Torque Random Access Memory to Spintronic Memristor

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Contents

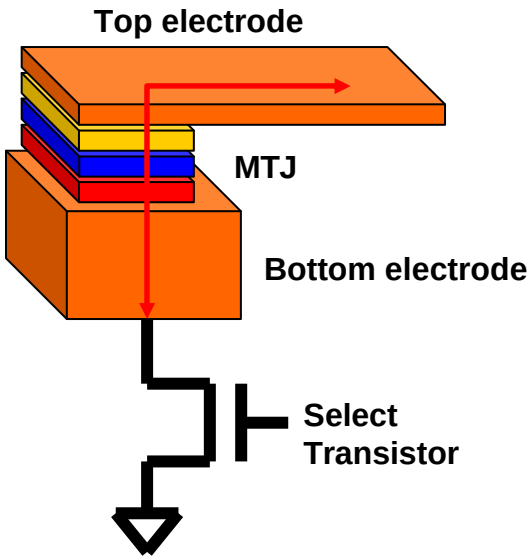
- Spin Torque Random Access Memory:

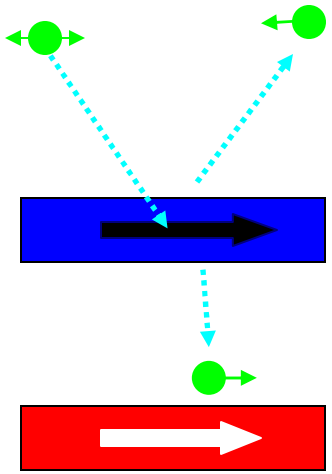
  dynamics characterization, device scale down challenges and opportunities

- Spin Torque Memristor:

  concept, device and application examples

Spin Torque Random Access Memory (SPRAM) Working Principle





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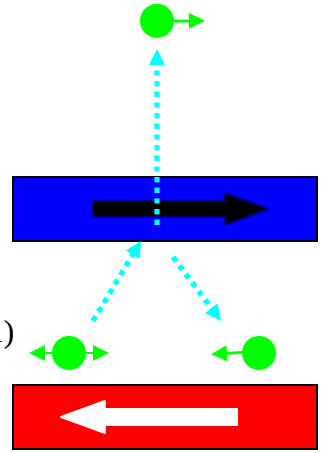


Magnetic tunneling junction (MTJ)

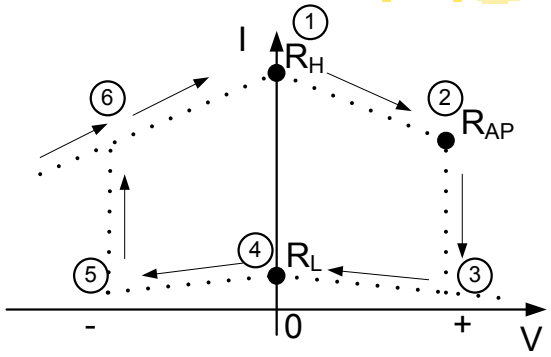
Reference layer

Tunneling insulating barrier

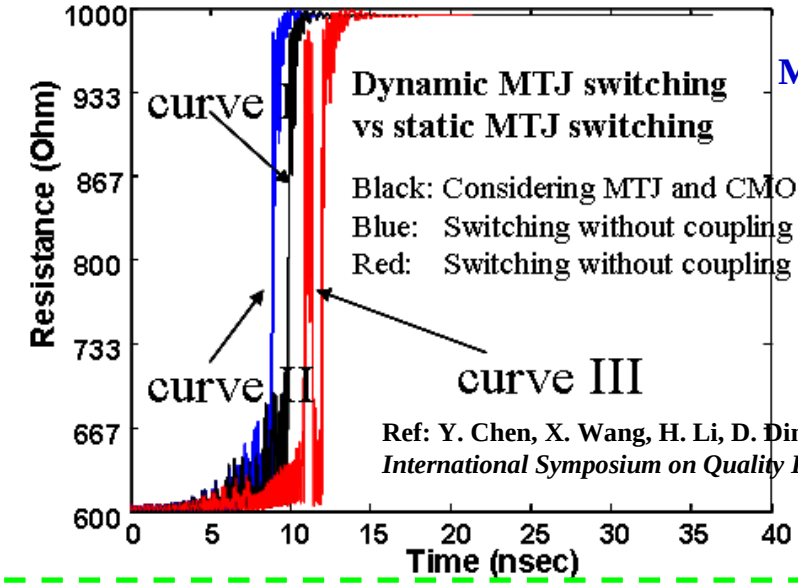
Free layer

Integrate magnetic tunneling junction (MTJ) with CMOS
Reading through magneto-resistance principle
Writing through spin torque excitation

SPRAM Switching Behavior

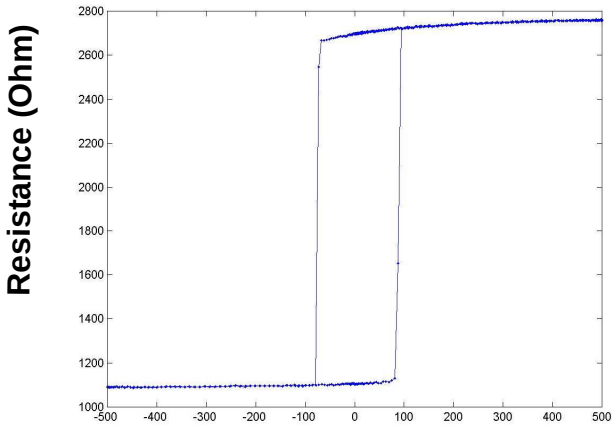


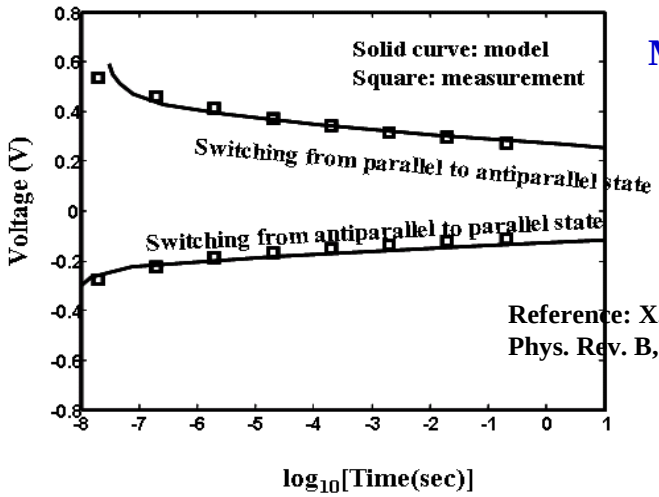
MTJ static picture



MTJ coupled with CMOS

Ref: Y. Chen, X. Wang, H. Li, D. Dimitar, H. Liu,
***International Symposium on Quality Electronic Design*, 2008.**



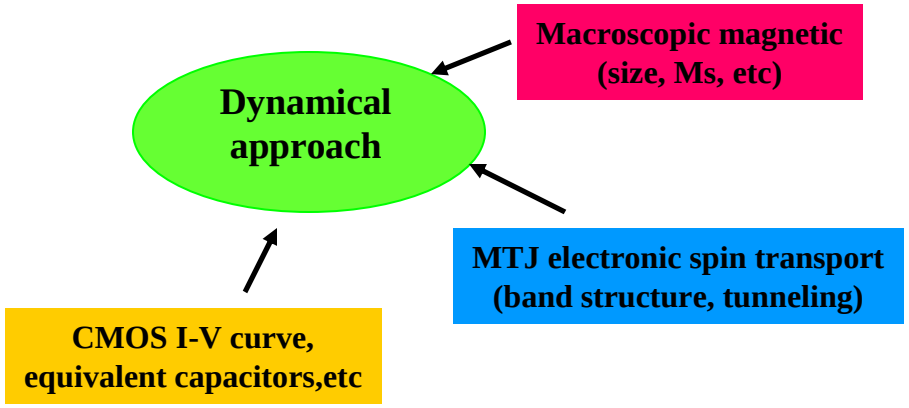


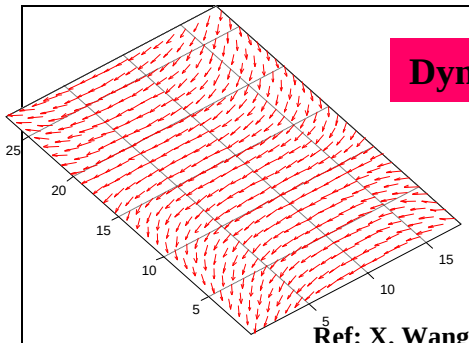
MTJ switching asymmetry

Spin torque switching asymmetry for a field balanced MTJ stack

Reference: X. Wang, W. Zhu, D. Dimitrov, Phys. Rev. B, 79, 104408, 2009.

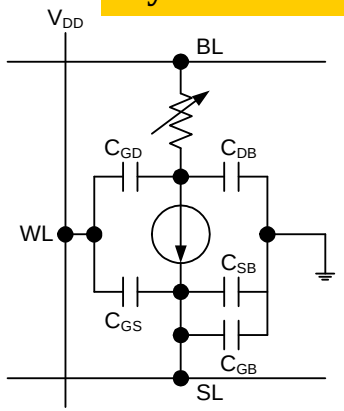
SPRAM System Dynamical Approach: Quantum-Micromagnetic-SPICE





Ref: X. Wang, Y. Chen, H. Li, D. Dimitar, H. Liu, IEEE Tran. On Magn., 44(11), 2470, 2008

Dynamic CMOS circuit



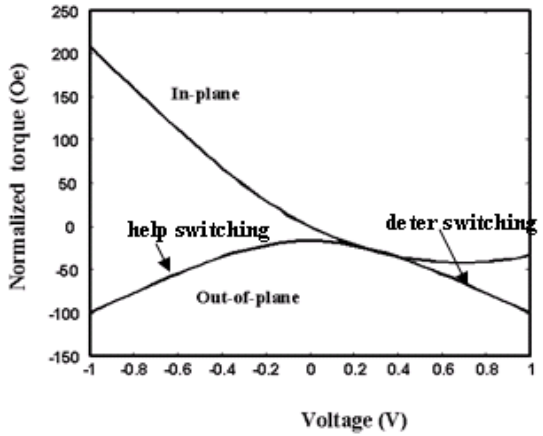
$$I_M + I_{GD} = I_{DB} + I_T$$

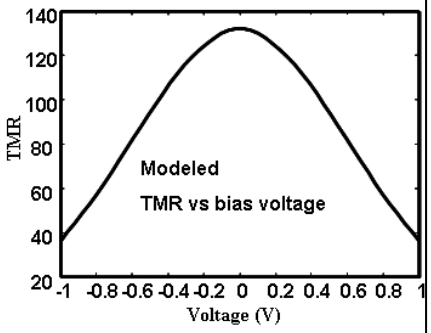
$$I_{GD} = C_{GD} \cdot \left(-\frac{dV}{dt}\right)$$

$$I_{DB} = C_{DB} \cdot \left(\frac{dV}{dt}\right)$$

$$I_M \cdot R(t) = V_{DD} - V \quad (BL \rightarrow SL) \text{or}$$

$$I_M \cdot R(t) = -V \quad (SL \rightarrow BL)$$

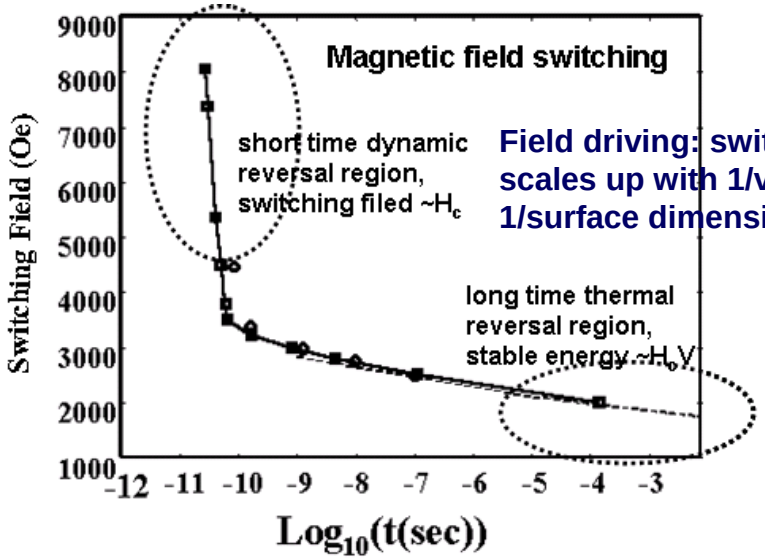




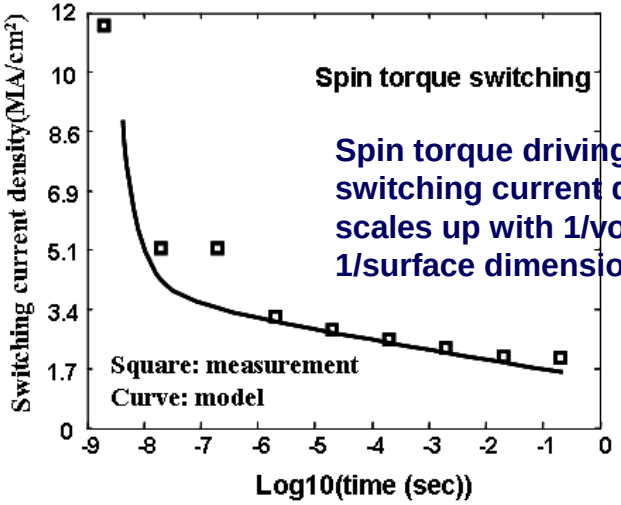
Quantum electronic spin transport

Reference: X. Wang, W. Zhu, D. Dimitrov, Phys. Rev. B, 79, 104408, 2009.

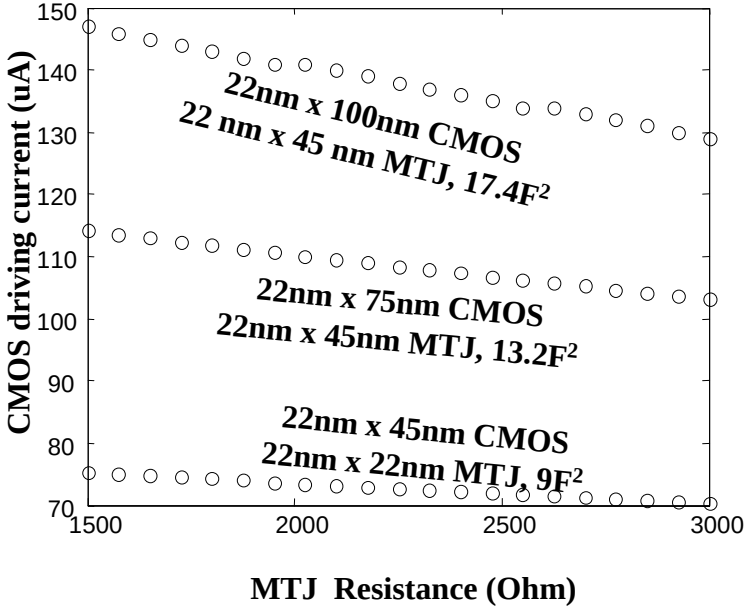
Challenge for SPRAM to Scale Down



Field driving: switching field scales up with 1/volume or 1/surface dimension

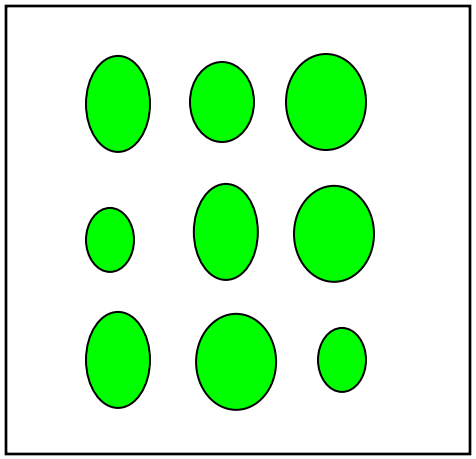


Spin torque driving: switching current density scales up with 1/volume or 1/surface dimension

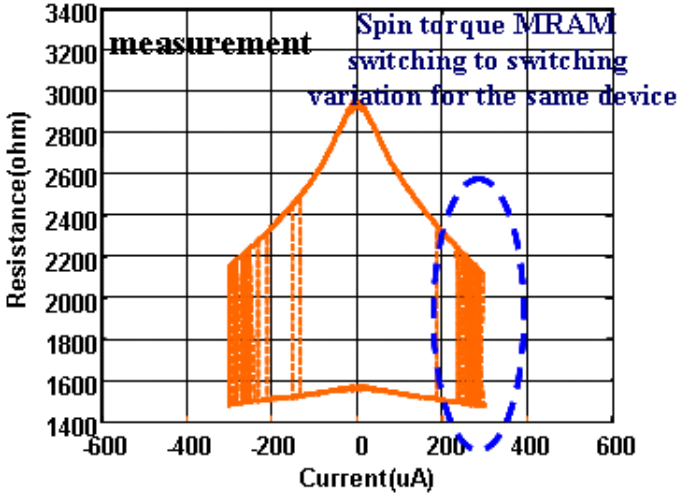


As magnetic device scales down, with CMOS driving stength decreasing, achieving fast nanosecond time scale magnetization switching and maintaining thermal stability at years time scale become a challenge.

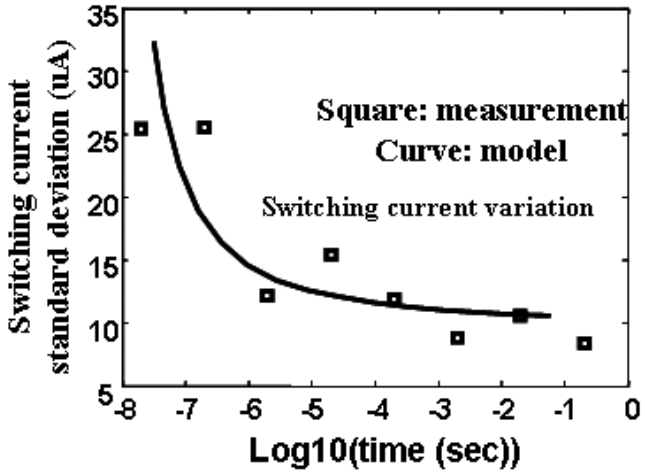
Challenge for SPRAM to Scale Down



Spin torque MRAM device to device variations reduce sensing and writing margins

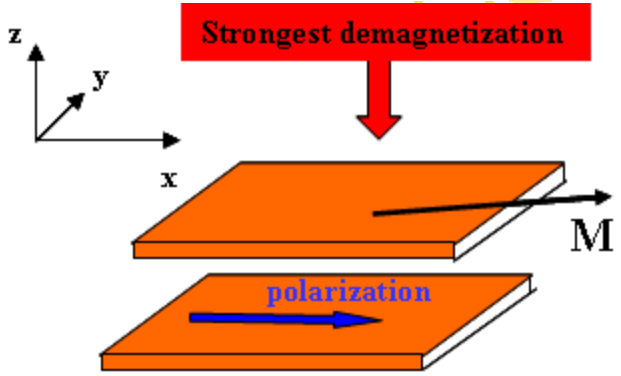


Variation of single device different switching



As device scales down, increased variability is another challenge.

Current Reduction Through Magnetization Dynamics

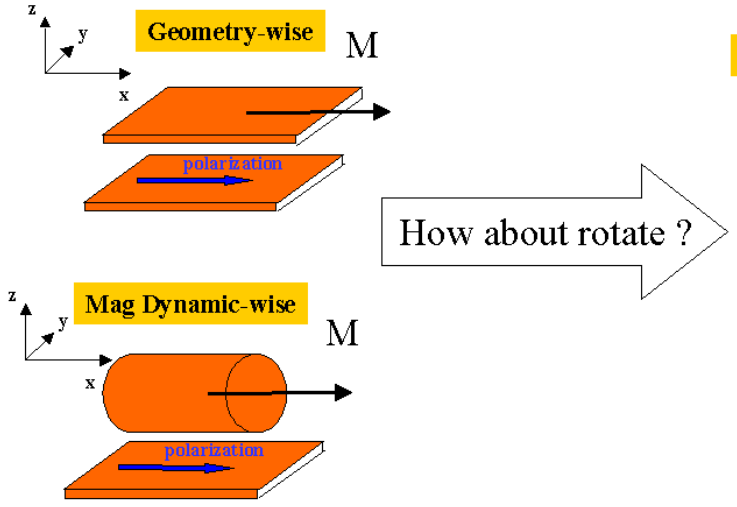


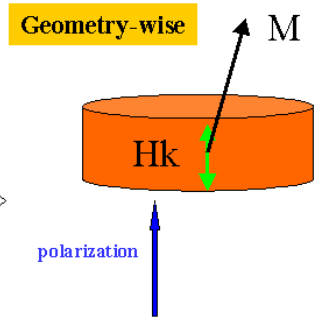
$$\text{critical switching current} \propto \frac{M_s^2 V \alpha}{\eta}\sqrt{(D_z - D_y)(D_z - D_x)}$$

D_x, D_y : demag factors in - plane, D_z : demag factor out - plane

Stable energy in equilibrium : $M_s^2 V (D_y - D_x)$

D_z >> D_x, D_y, different scaling behavior of MTJ writing current magnitude and thermal stability energy



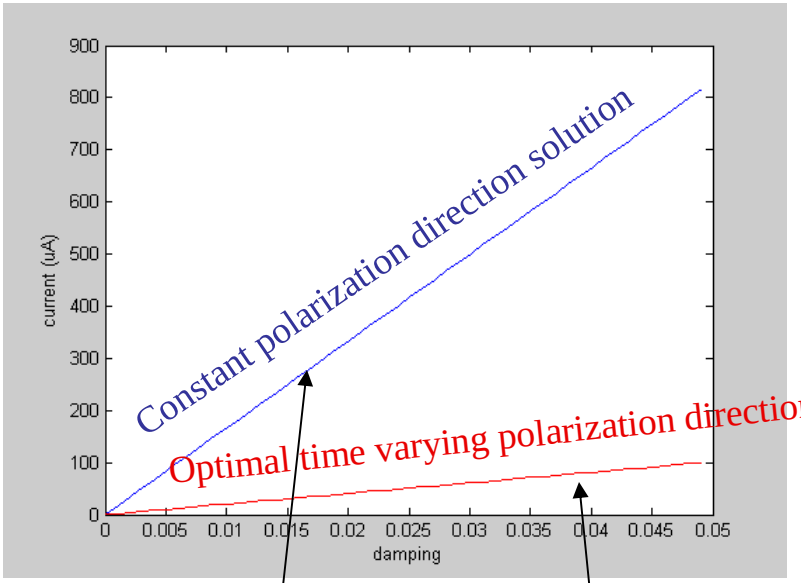


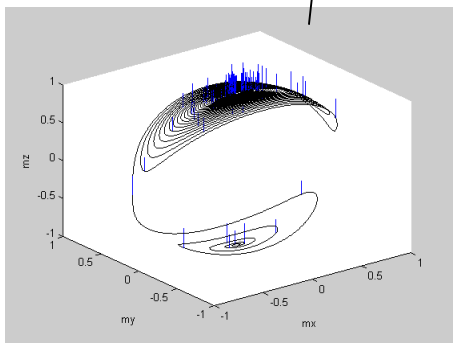
Geometric wise: thin film for TMR etc.
Magnetization dynamics wise: Symmetric magnetization motion: $D_z = D_y$

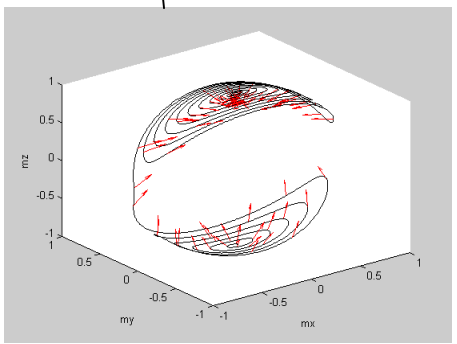
Road leads to same scaling of switching current and thermal stability energy

Current Reduction Through Magnetization Dynamics

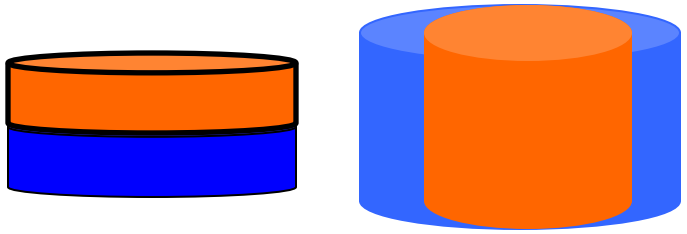
RF frequency time varying polarization angle





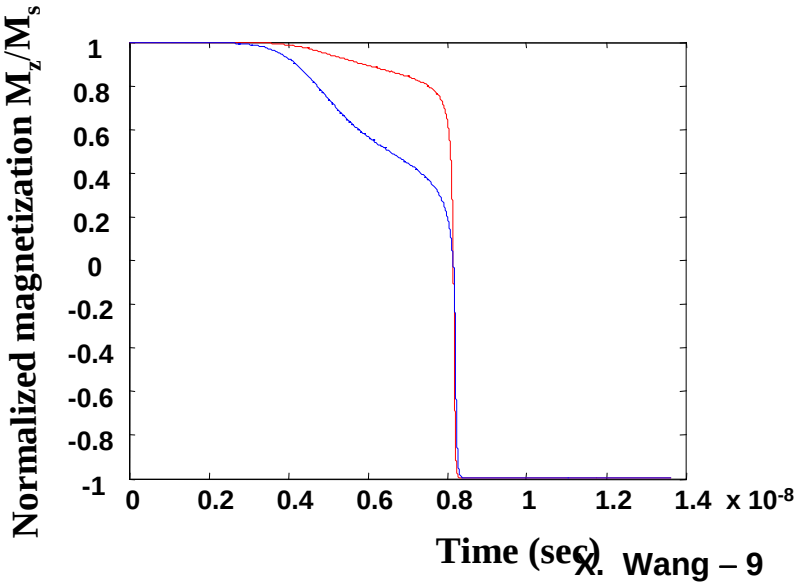


Composite material stack

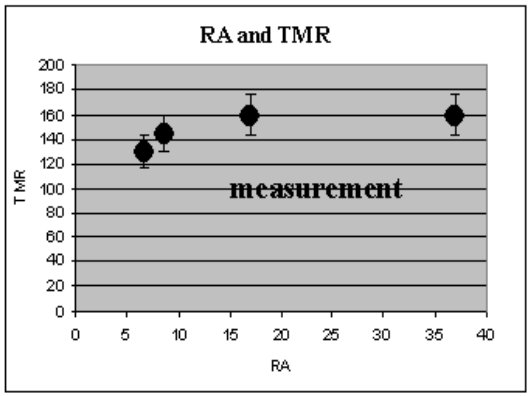


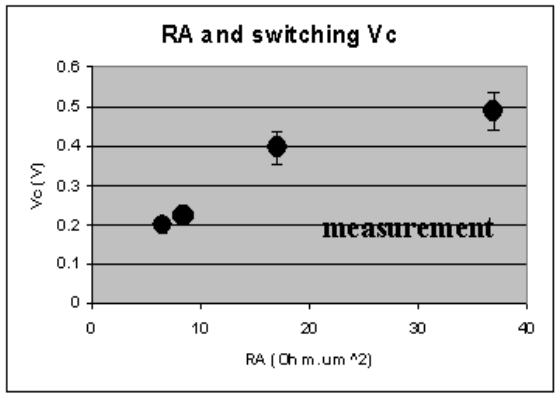
Hard magnetic layer to keep thermal stability

Soft magnetic layer to decrease switching field/current magnitude

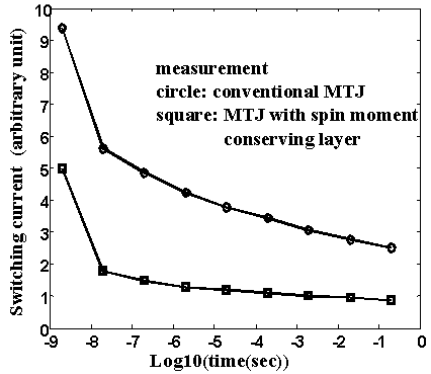


Current Reduction Through Electronic and Spin Transport Across Interface





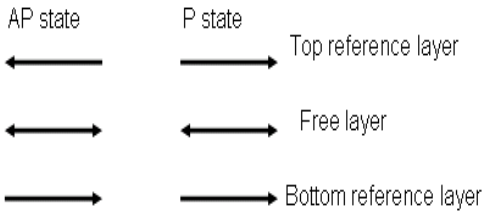
Increase insulating layer thickness only, RA increases 5 times, critical switching voltage only increases 2.5 times

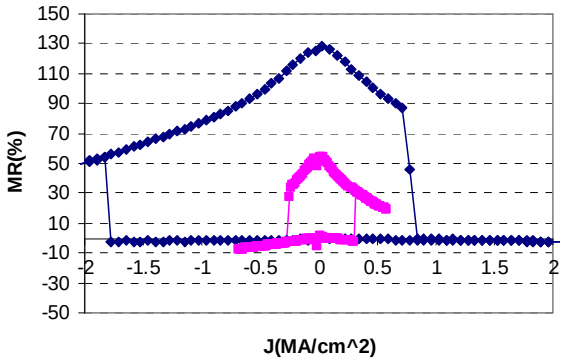


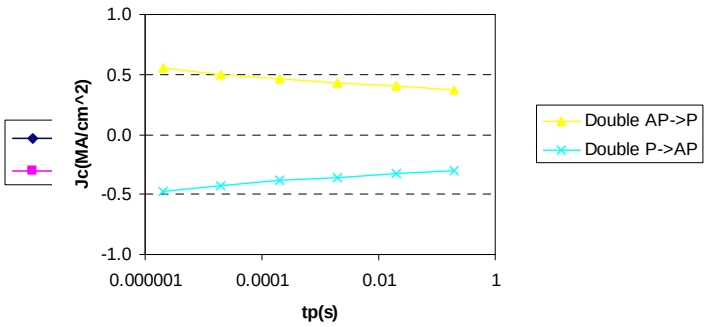
MTJ with spin moment conservation layer between free layer and top cap layer

More opaque barrier, less magnetization precessing induced spin pumping, effective damping reduction

Ref: X. Wang, W. Zhu, Y. Zheng, Z. Gao, H. Xi, INTERMAG 2009





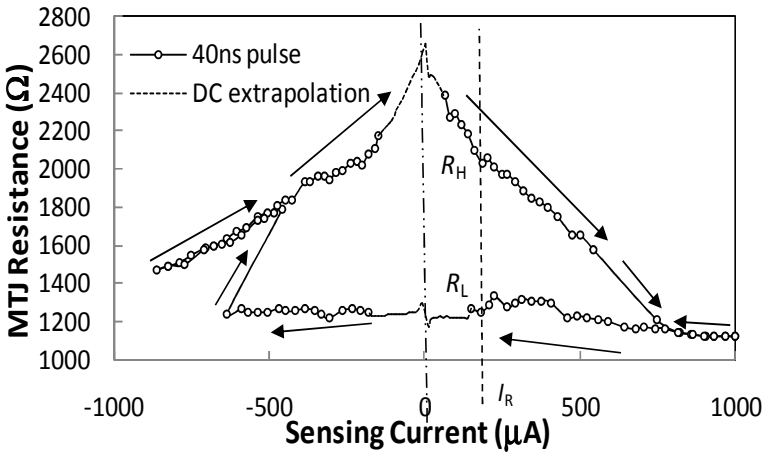


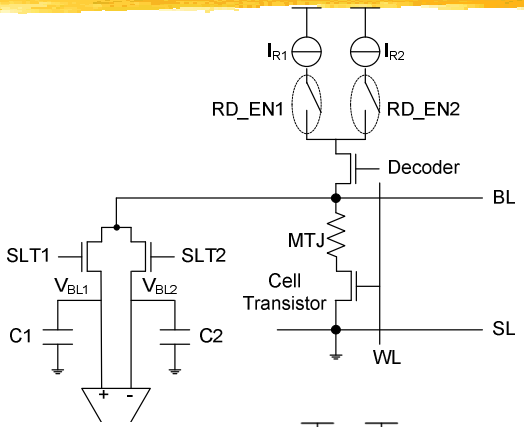
Dual tunneling barrier, critical switching current down to 0.6MA/cm2, quantum confinement effects ?

X. Wang – 10

Ref: Y. Zheng, W. Zhu, X. Wang, Z. Gao, D. Wang, D. Dimitrov et. al. submitted to Appli. Phys. Letters

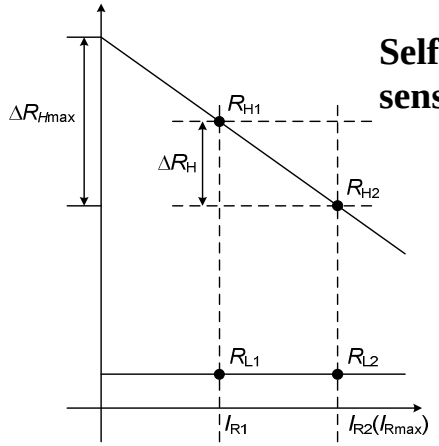
Variation Controlling at Device Level



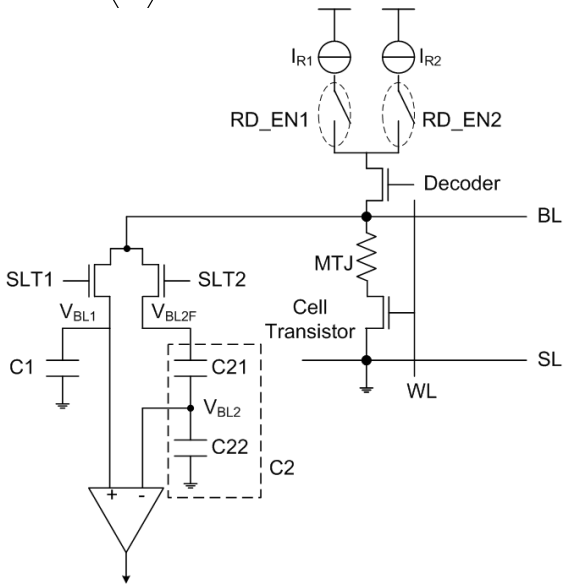


destructive

Unique Device characters leads to new sensing scheme



Self-reference sensing



non-destructive

Ref. Y. Chen, H. Li, X. Wang, W. Zhu, W. Xu and T. Zhang, Design, Automation & Test in Europe Conference and Exhibition, 2010.

Variation Controlling at System Level

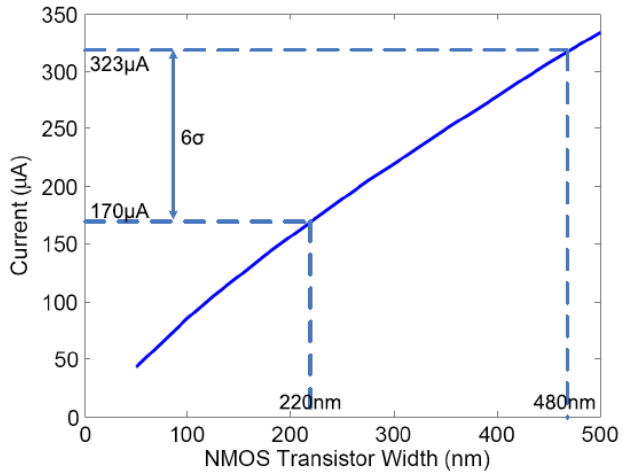


Fig. 3. The current driving strength of the nMOS transistor in STT MRAM cell at 45nm technology node.

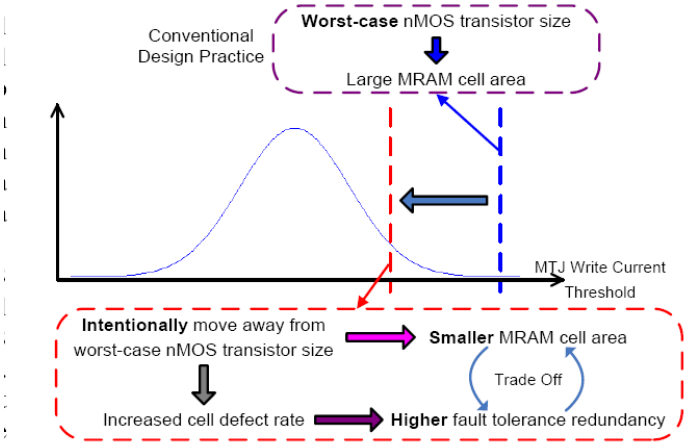


Fig. 4. The proposed area efficient STT MRAM design methodology.

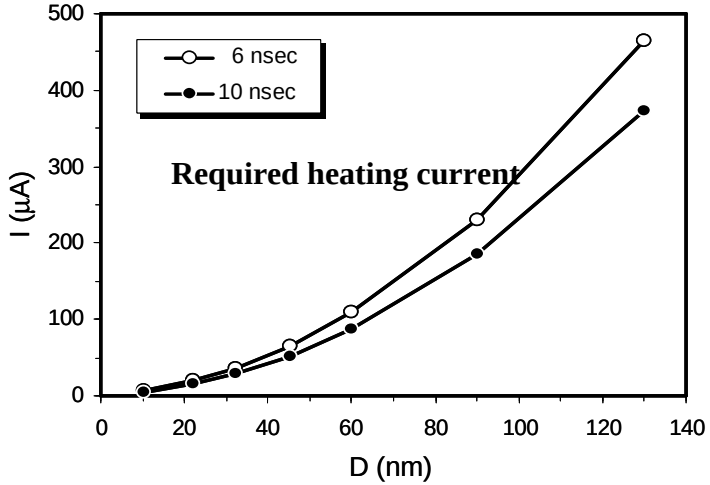
Reduce switching current requirement by intentionally move away from worst case scenario design

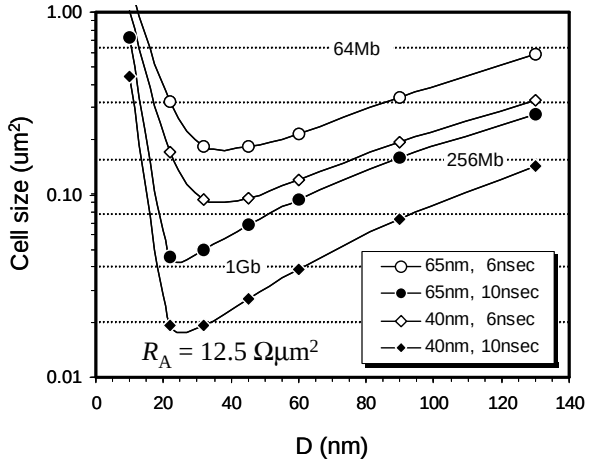
a smaller-than-worst-case transistor sizing approach. For 256Mb SPRAM design at 45nm node, under a normalized write current threshold deviation of 20%, the overall memory die size can be reduced by more than 20% compared with the conventional worst-case transistor sizing design.

Ref: W. Xu, Y. Chen, X. Wang, and T. Zhang, 46th Design Automation Conference, 2009.

Heat Asssited Solutions

Surface anti-ferromagnetic coupled (AFC) magnetic layer with relatively low Curier temperature:
At room temperature, the AFC coupling provides surface anisotropy to maintain thermal stability of the square magnetic element.
During the writing process, the joule heating of spin torque current raises temperature of AFC surface magnetic layer above Curier temperature and the AFC induced surface anisotropy disappears. The element can be switched at low threshold current.

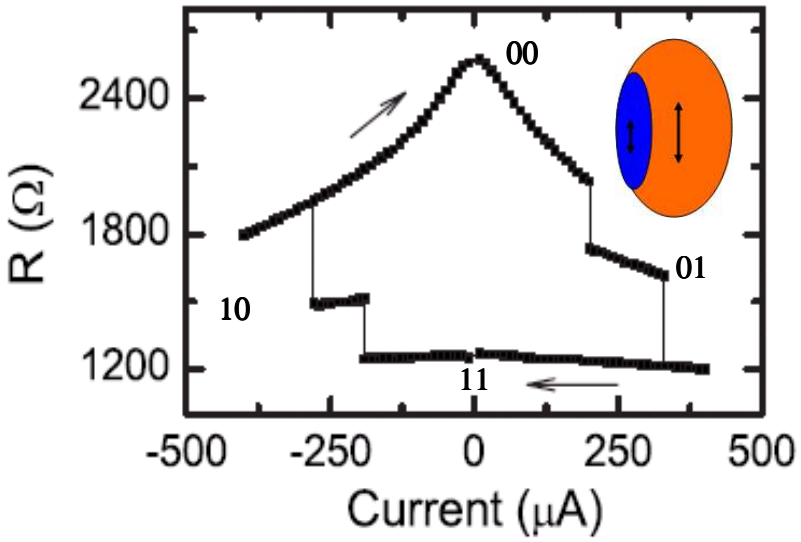




Write current decreases with decreasing memory element dimension D. Meanwhile, the MTJ resistance increases with decreasing memory element dimension. For a given technology node, an optimal memory cell size can be found due to the tradeoff between critical switching current and MTJ resistance

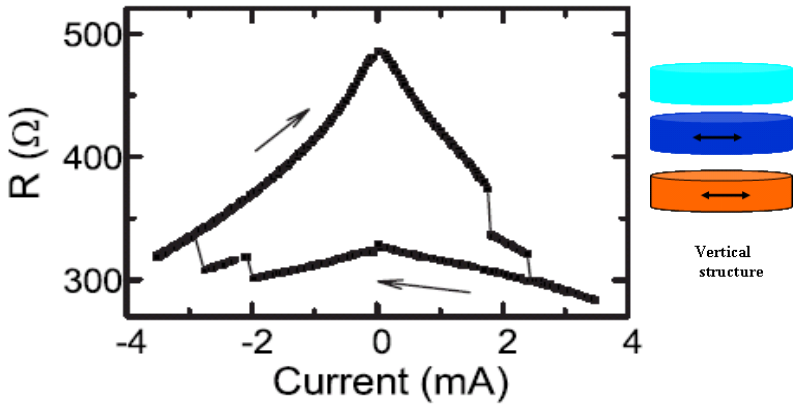
Ref: H. Xi, J. Sreicklin, H. Li, Y. Chen, X. Wang, and Y. Zheng, Z. Gao, M. Tang, IEEE Trans. Magn, 46,no. 3, 860, 2010

MTJ Memristor and Mutibit Data Storage and Logic



demonstrated multi-bit MTJ devices

Ref: X. Lou, Z. Gao, D. Dimitrov, and M. Tang, Appli. Phys. Letters, 93, 242502, 2008



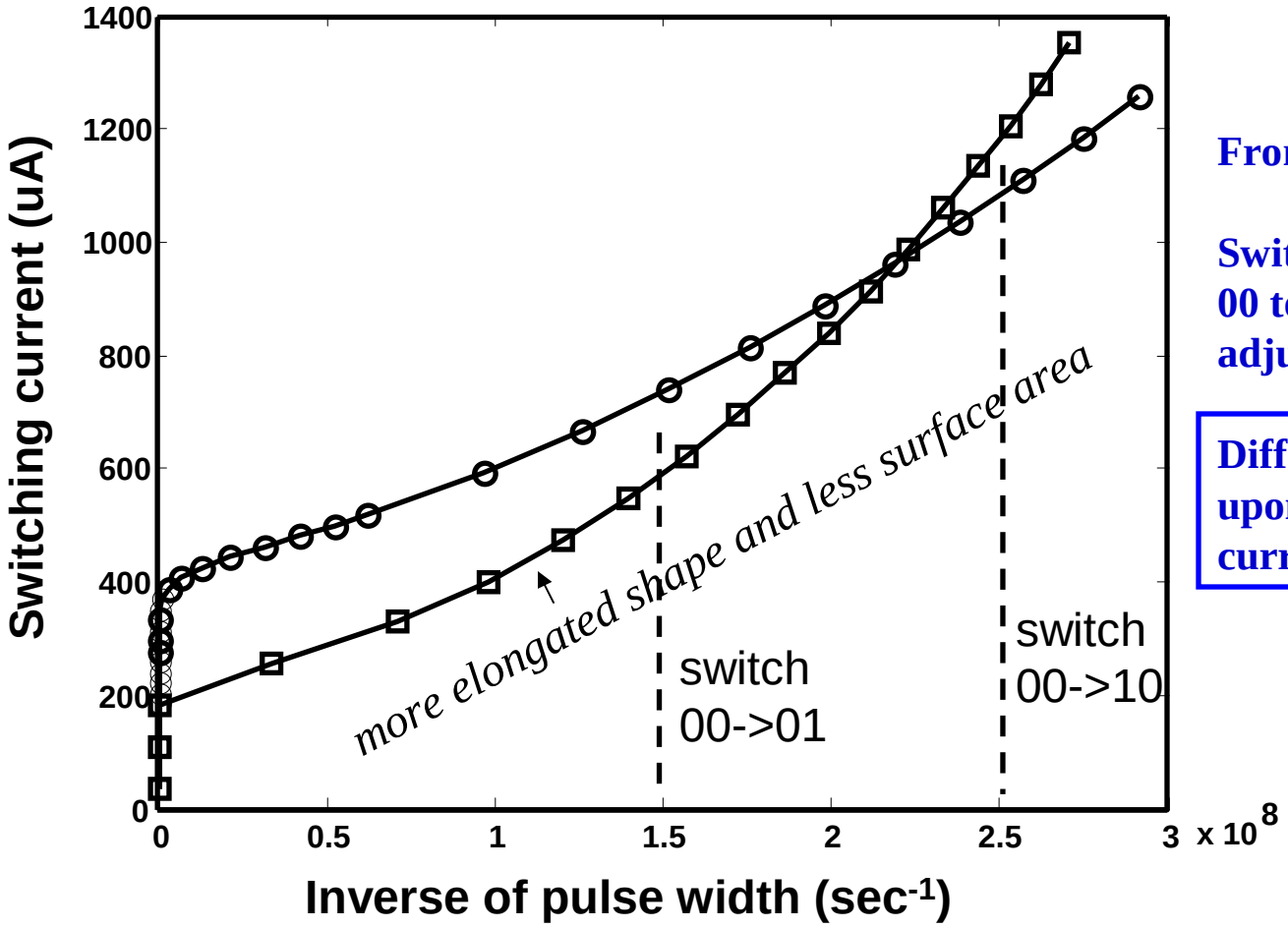
Vertical structure

From nonlinear resistor point of view:

reversible branch: 11 to 10, 00 to 01

Irreversible branch: 00 to 10

MTJ Memristor and Mutibit Data Storage and Logic



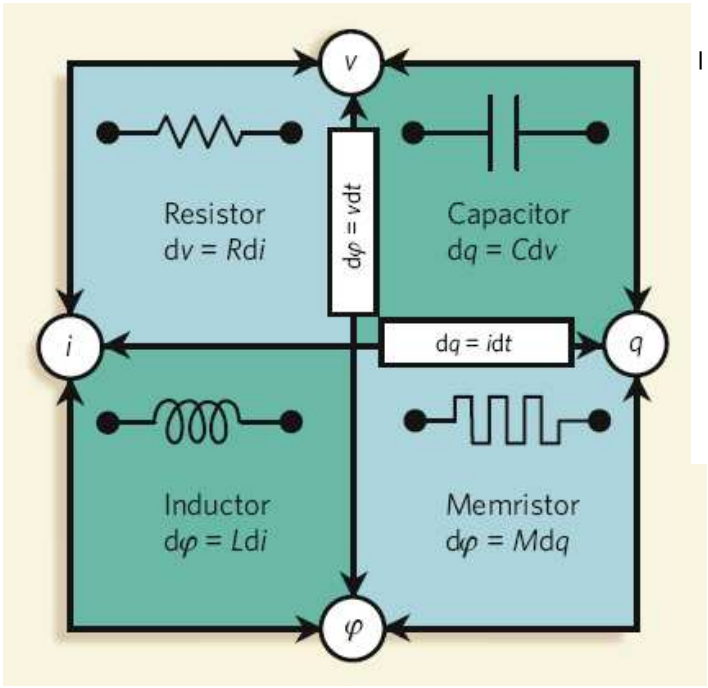
From memristor point of view:

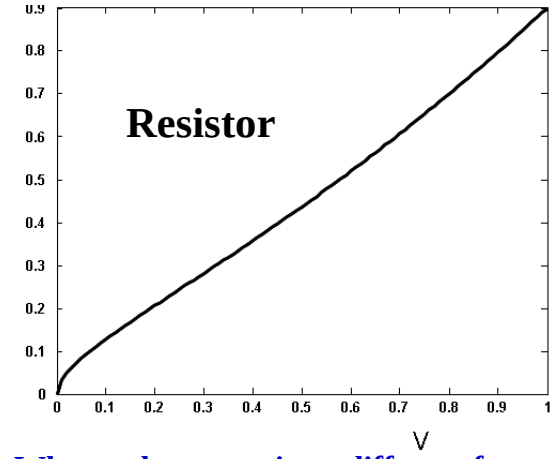
Switching from 00 to 10 and from 00 to 01 are all possible by adjusting pulse width

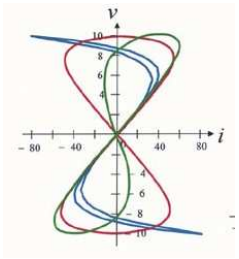
Different slope, switching depends upon integration of current, not current magnitude !

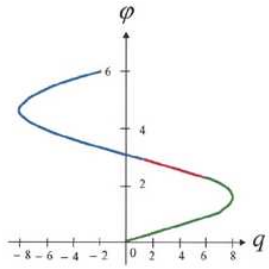
Ref. X. Wang, Y. Chen,
Design, Automation & Test in Europe Conference and Exhibition, 2010.

Memristor as Fourth Circuit Element







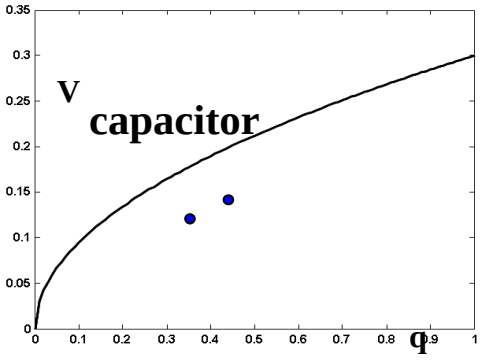


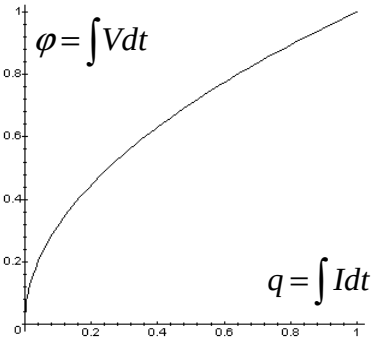
Memristor

What makes memristor different from an ordinary constant resistor or even a curre or voltage dependent nonlinear resistor: memristance is a function of charge, which depends upon the hysteretic behavior of the current (or voltage) profile.

Leon O. Chua, Memristor-the missing circuit element, IEEE Trans. Circuit Theory, vol. 18, no. 5, 1971

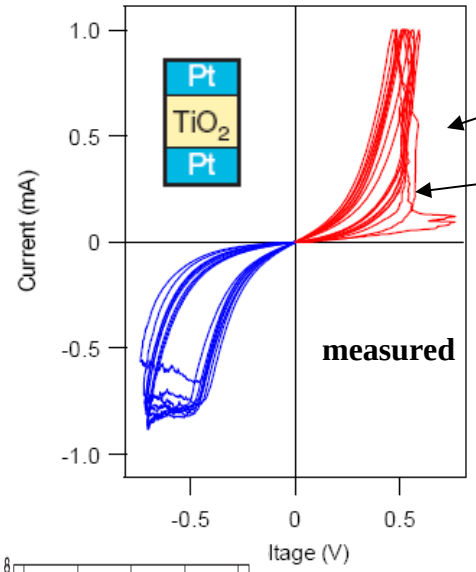
Chua (1971) proposed memristor for logic completeness of circuit element





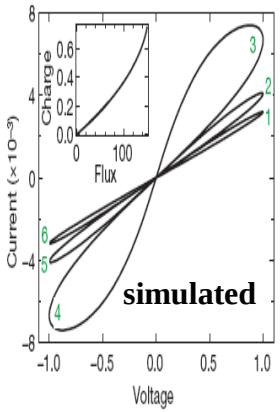
What makes memristor different from a capacitor or inductor is the ability to accumulate current or voltage information at constant voltage or current.

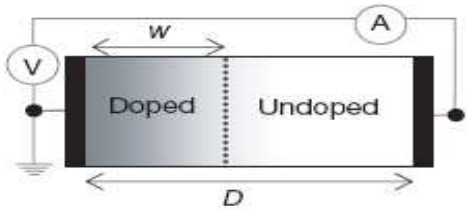
Memristance in Resistive Memory Stack

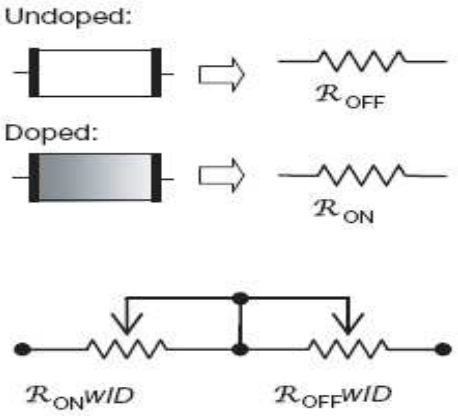


low resistance state

high resistance state







1) Nano-scale two terminal device as two connecting resistors (doped region and undoped region)

2) Bias electric current drives the front of the doped region

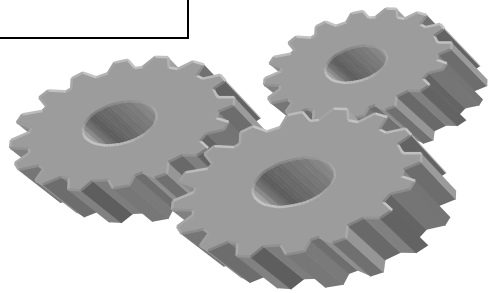
1) J. M. Tour and T. He, Nature 453, 42, (2008).

2) D. B. Strukov; G. S. Snider; D. R. Stewart and R. S. Williams, Nature, 453, 80, (2008)

Spintronic Memristor Through Spin Torque Induced Magnetization Motion

GMR/TMR device: resistance depends upon magnetization state

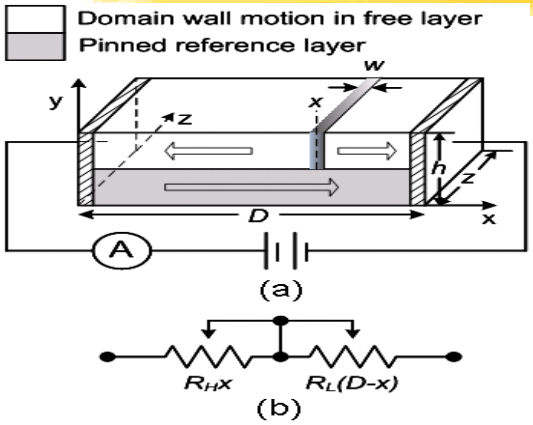
Spin Torque device: current electronic spin changes the magnetization state of the device. The magnetization state of the device depends upon the cumulative effects of electron spin excitations.



Spintronic memristor: resistance depends upon the integral effects of its current profile.

X. Wang, Y. Chen. H. Xi, H. Li, D. Dimitrov: IEEE electronic device letters vol. 30, no. 3, pp.294, 2009.

Domain Wall Memristor and Temperature Sensor

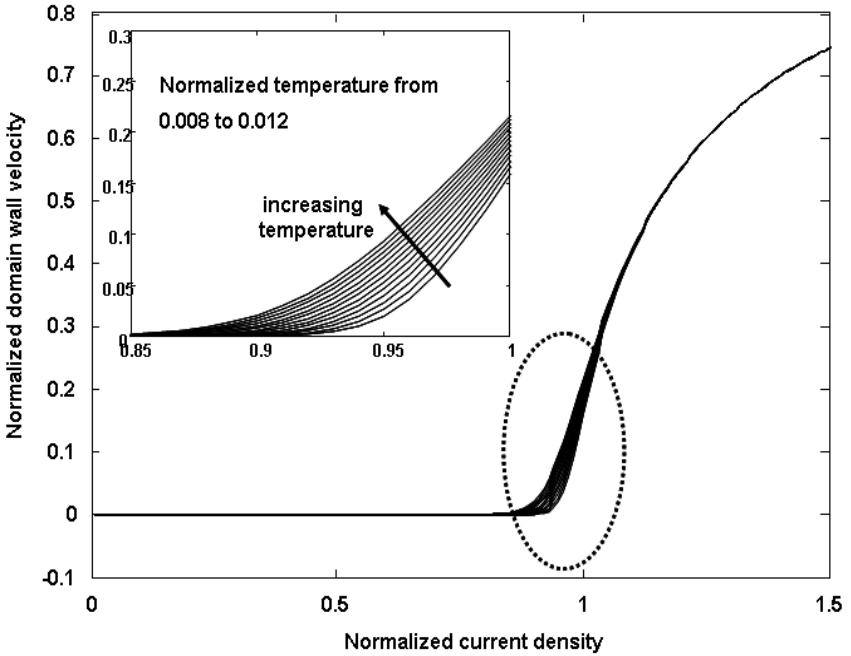


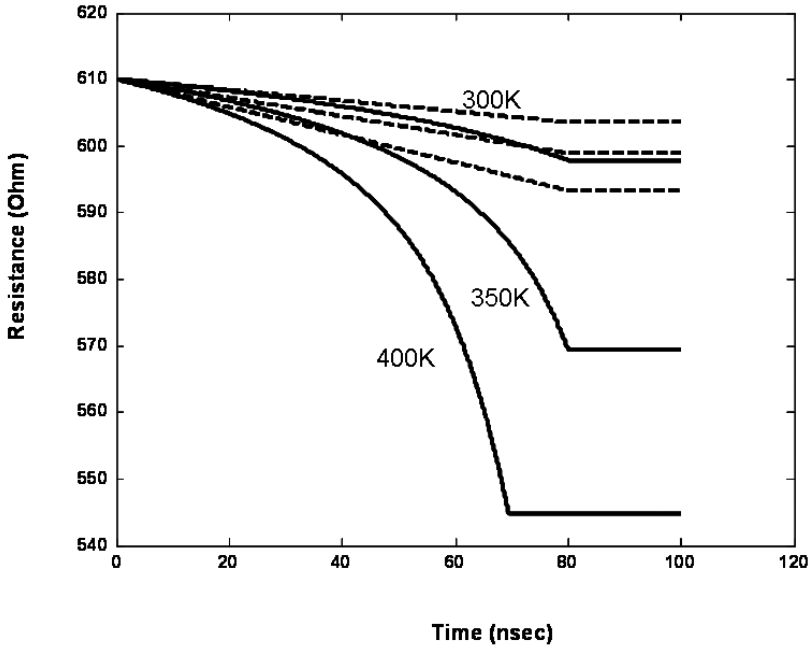
interactions between macroscopic coherent magnetic structures and random fluctuations

Nano-scale feature size, low cost, and mature integration technology with the CMOS process.

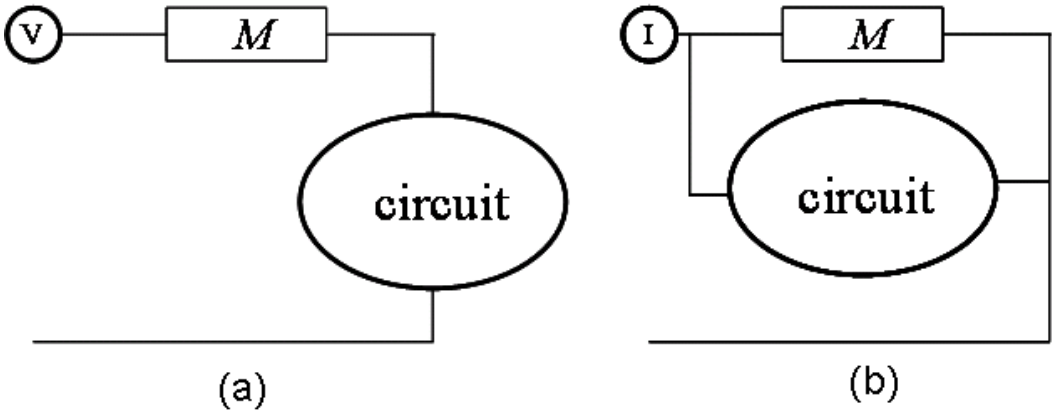
Targeting the highly integrated on-chip thermal detection applications

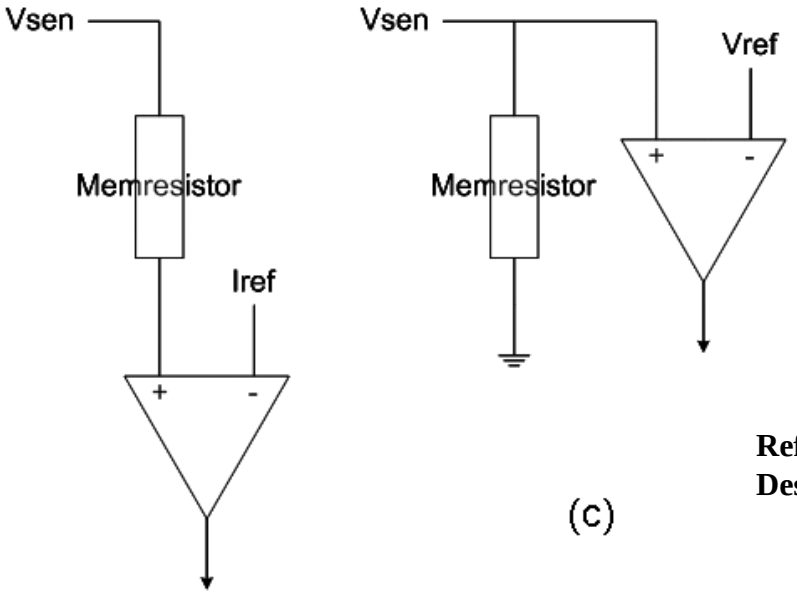
X. Wang, Y. Chen, Y. Gu, H. Li: IEEE electronic device letters vol. 31, no. 1, pp.20, 2010.





Memristor for Power Management





The ability to accumulate current/voltage through constant current and/or voltage driving strength: power monitor device

$$E = \int VIdt = V\int Idt$$

Negative feedback: power control device

Ref. X. Wang, Y. Chen,
Design, Automation & Test in Europe Conference and Exhibition, 2010.

Memristor for Data Security

Question: Administrator and user. Design a scheme to fight against following action: after reading the stored data information, the user tries to restore the device state to the same state as before reading, so that administrator could not find whether the data has been accessed.

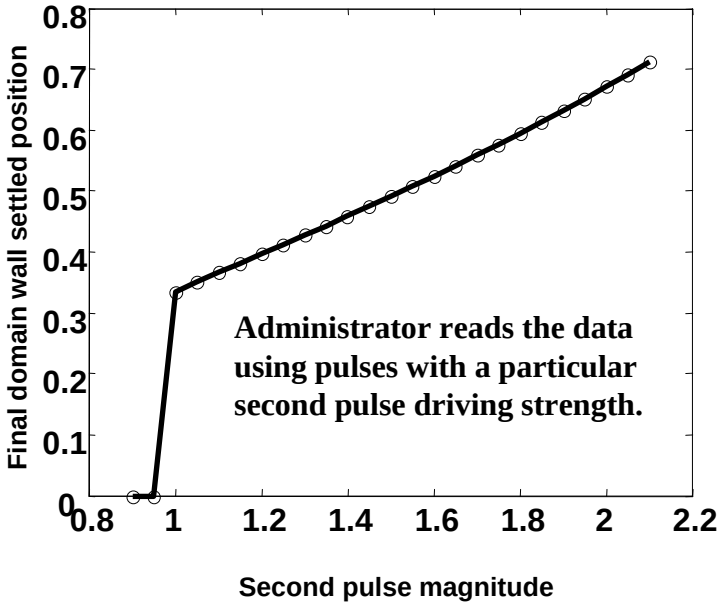
Solution depends upon whether the user is given the limited or the same authority on device writing and reading compared to that of the administrator. For the case of user with limited reading and/or writing authority, data information security task can be achieved more easily. For limited writing authority case, user may not be able to restore the device to the state set by the administrator before. For reading limited case, the user may not know the state of the device set by the administrator.

A solution giving user and administrator the same authority on reading and writing:

1) Writing process: administrator sets high resistance state (0) fully saturated and low resistance state (1) partially saturated.

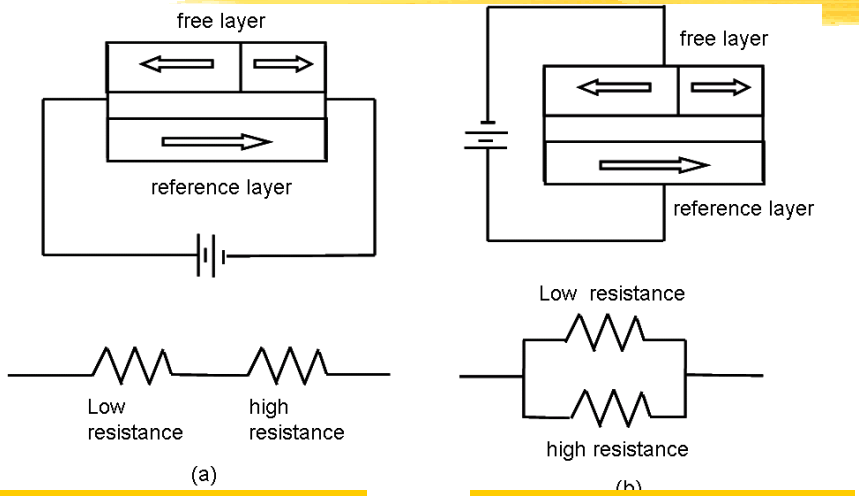
2) Reading process: two constant voltage pulses excite device a few times (order of 10). One pulse pushes domain wall toward high resistance end and the other pulse tries to push domain wall toward low resistance end.

3) The device reports two values for reading: 1) final state of the device close to high or low resistance state (High or Low) and 2) whether the device resistance has been significantly changed during reading (Yes or No).



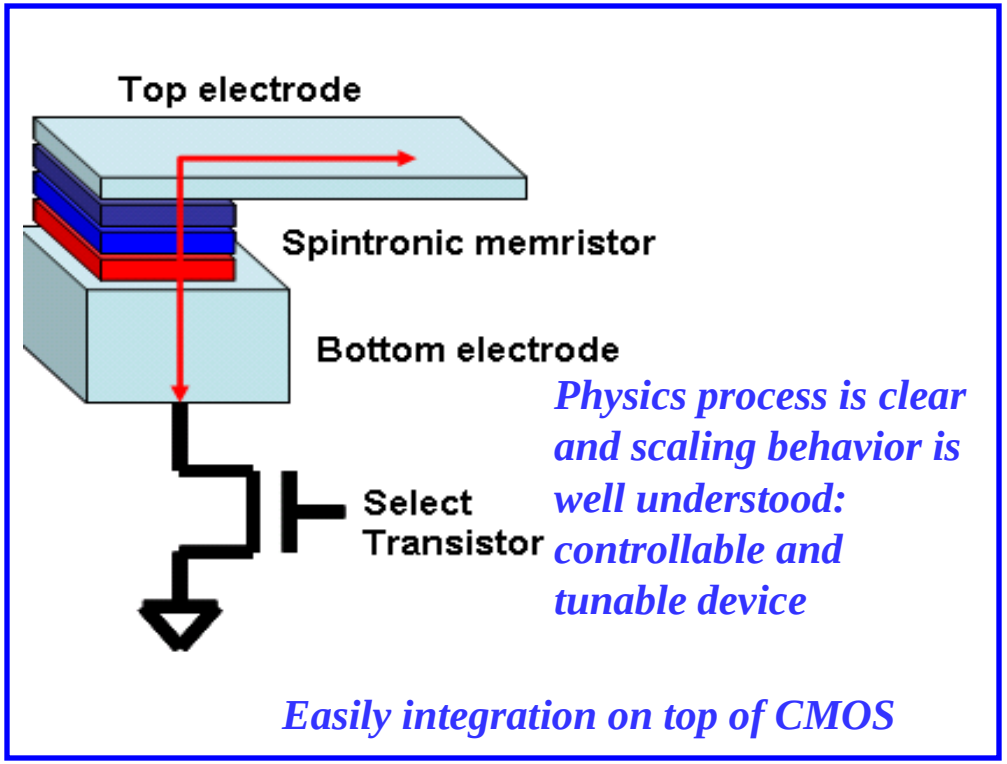
Ref. X. Wang, Y. Chen, Design, Automation & Test in Europe Conference and Exhibition, 2010.

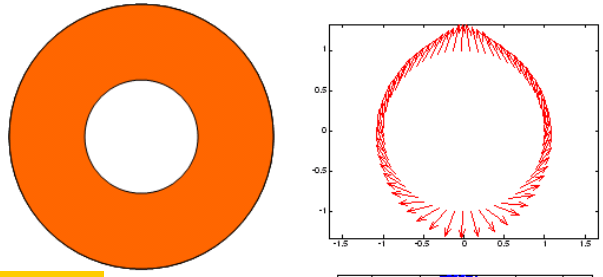
Path to Future: Potentials



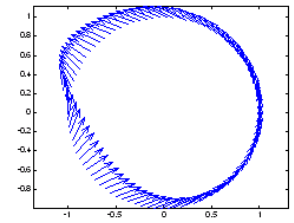
GMR with spin valve structure

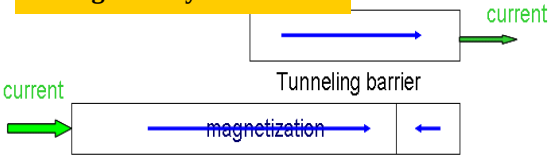
TMR with tunneling structure





New geometry structures





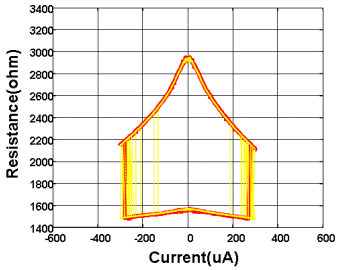
New material

Y. V. Pershin and M. Di Ventra, Phys. Rev. B, 78, 113309, 2008

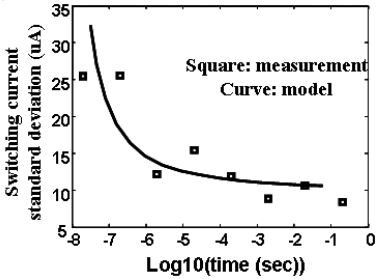
Spin blockade, half-metallic material

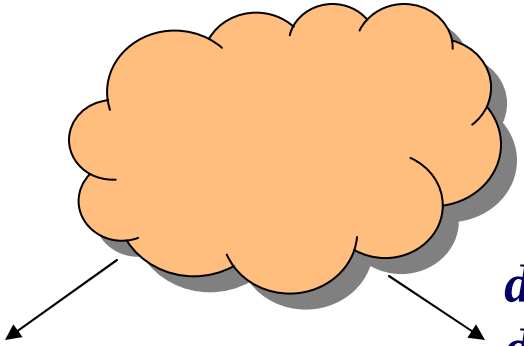
Path to Future…….

nano-scale, ultra-fast…….



variability,
memory effects…….





analogue/digit mixture
fuzzy,
neural system
……

deterministic, precise
digital
control
……..