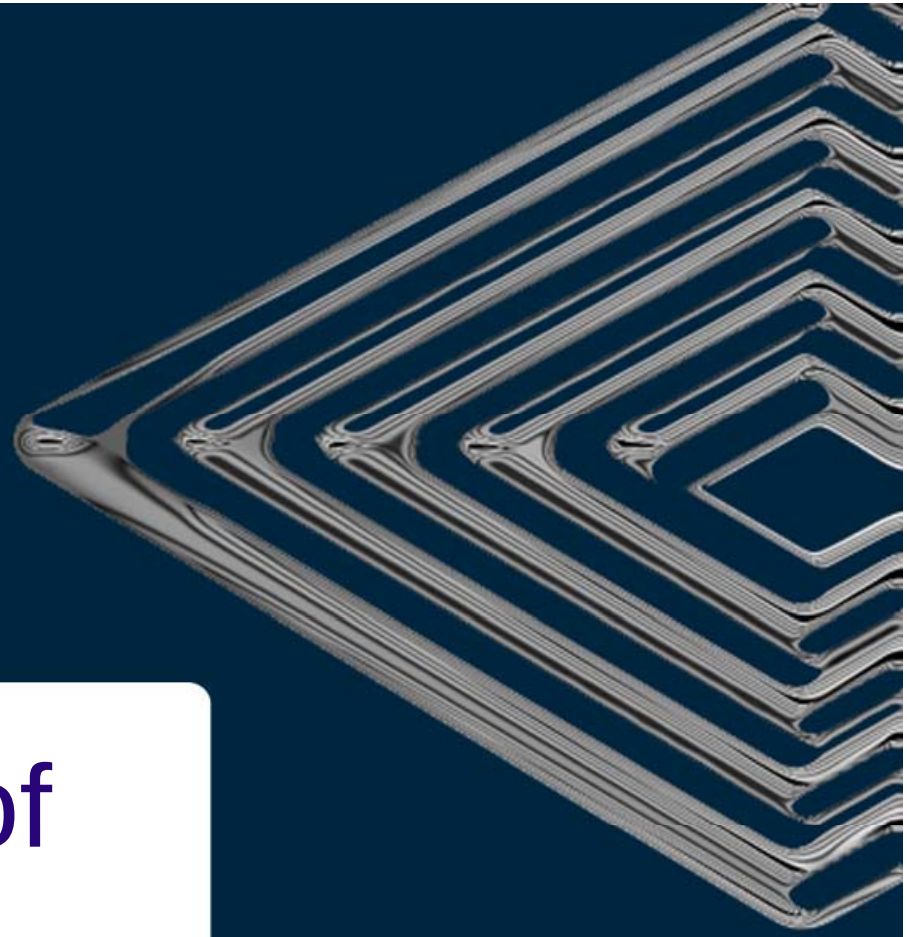


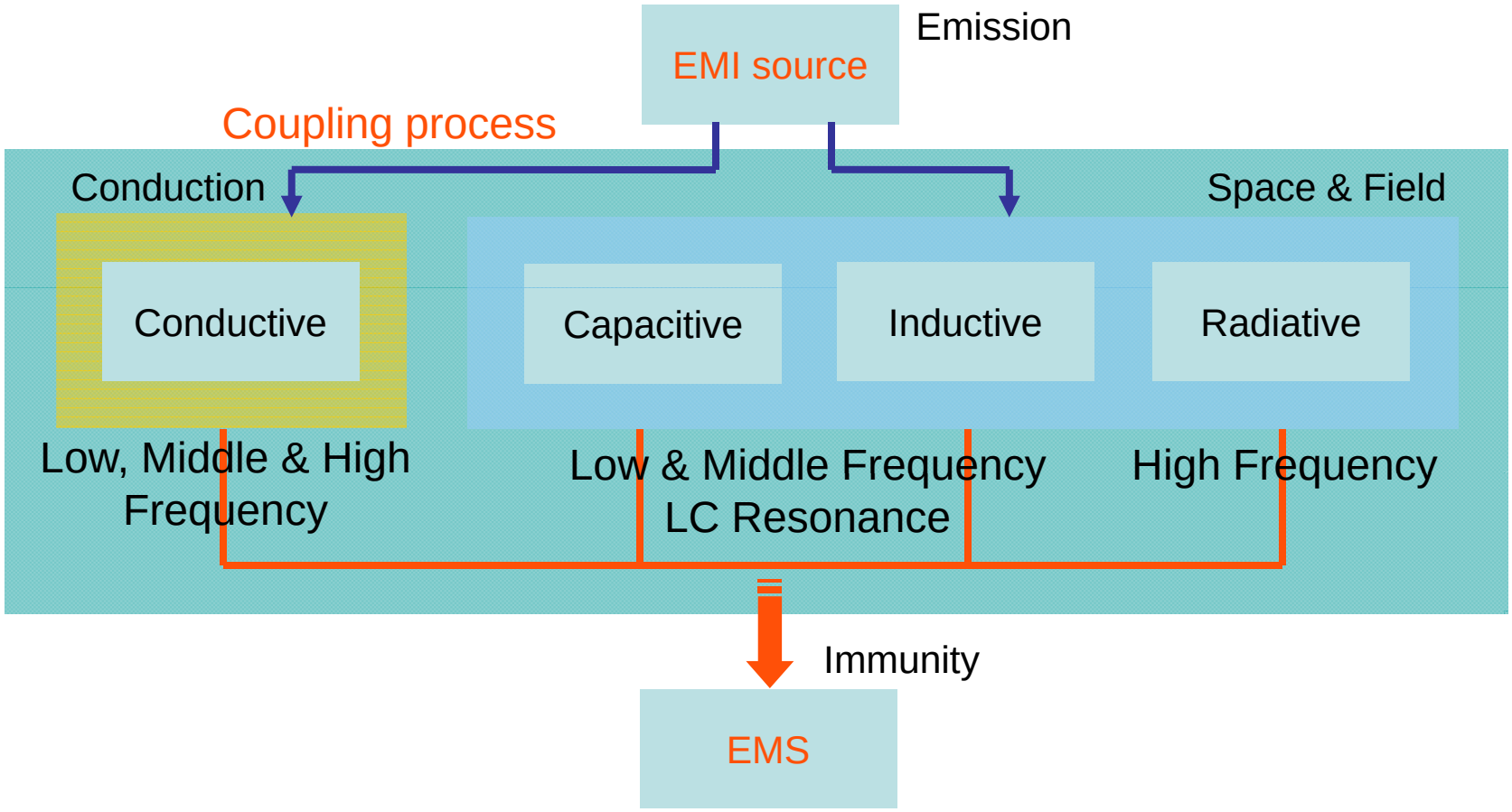
Fundamentals of EMI

Chris Herrick

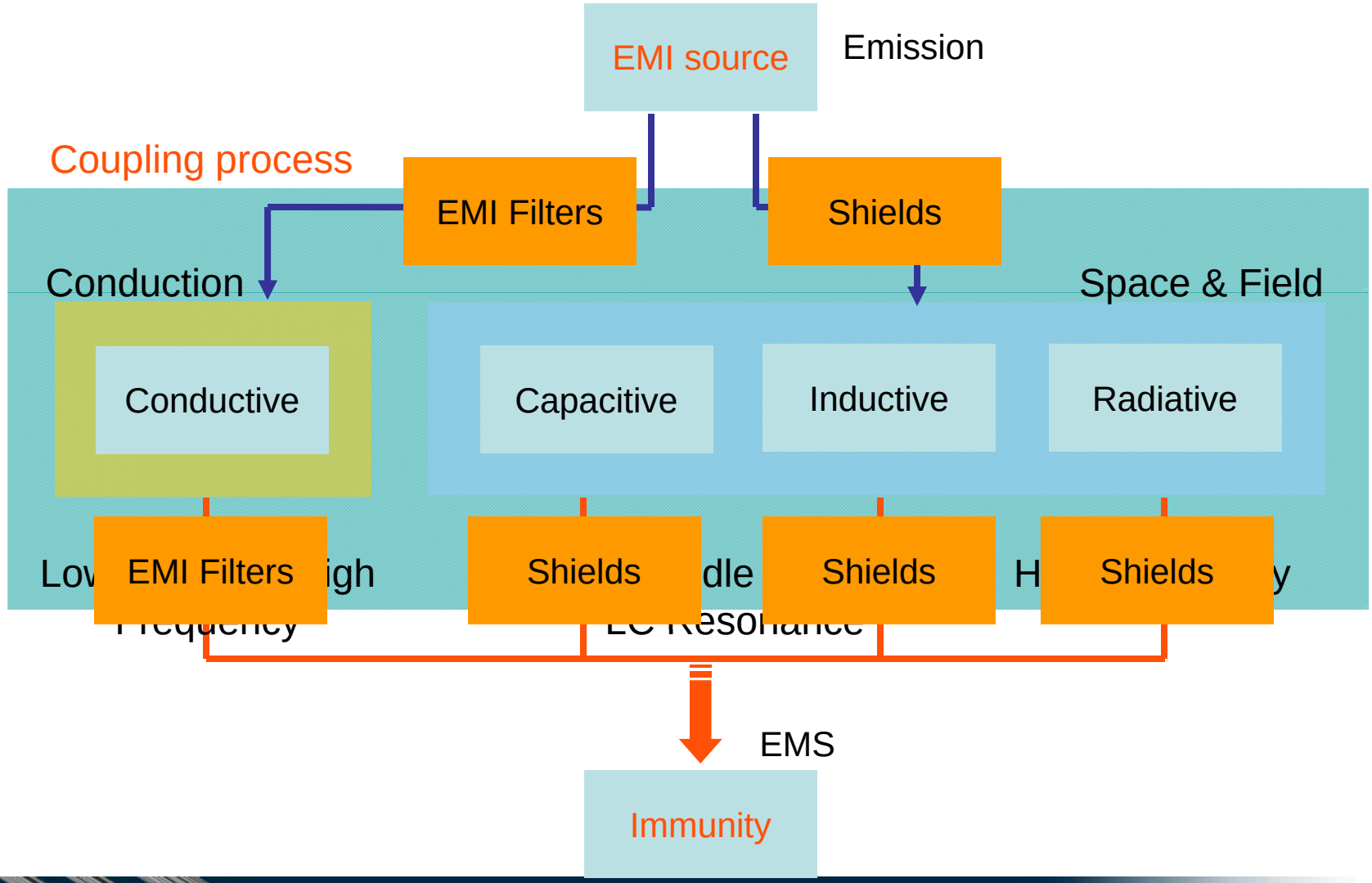
Ansoft

Applications Engineer

Three Basic Elements of EMC



Controlling EMI



PCB Noise Sources

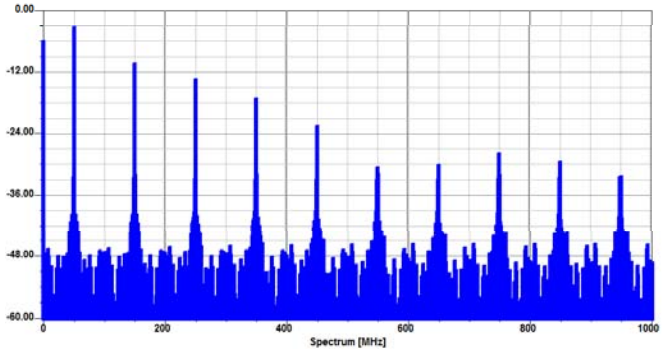
- **Intentional Signals**
  - Emissions from intentional signals include loop-mode and common-mode sources.

- **Unintentional Signals** (more than 90% of EMI)
  - Emissions from unintentional signals include common-mode, crosstalk coupling to I/O traces (both PCB and IC level), power planes, and above board structures.

*Reference from "*PCB Design for Real-World EMI Control,"* Bruce Archambeault

Intentional Signals

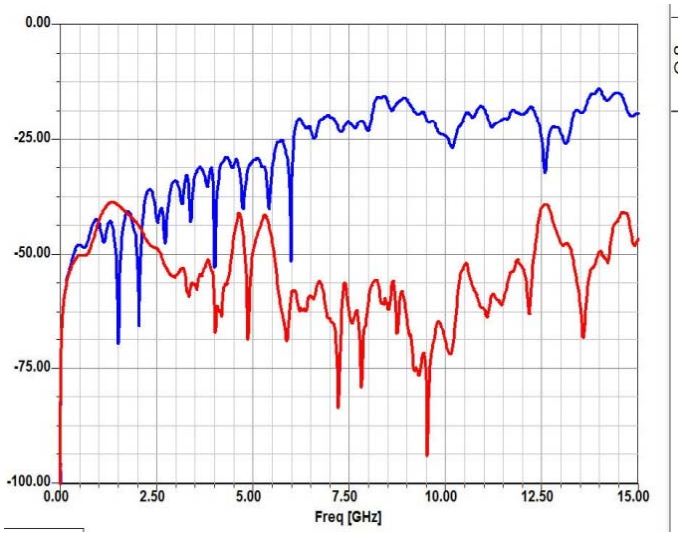
- Focus on Clock and High Speed Signals
  - Stripline not necessarily better than Microstrip
  - Examine Clock Harmonics



  - Common Mode Conversion

    SCD11=0.5*(S11-S13+S31-S33)

    SCD21=0.5*(S21-S23+S41-S43)

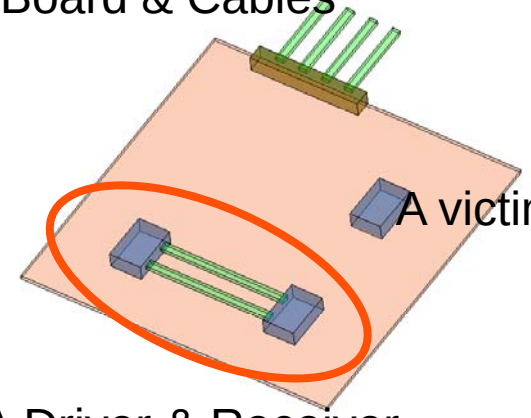


Unintentional Signals

- Crosstalk is a big concern
  - Beware the low speed nets; use post-layout analysis to scan for unintended coupling
  - Coupling may be direct, through intermediate metal or even from plane cavities
- Common mode will always exist
  - Don’t neglect the overall plane impedance

Loop Mode & Common Mode Noise

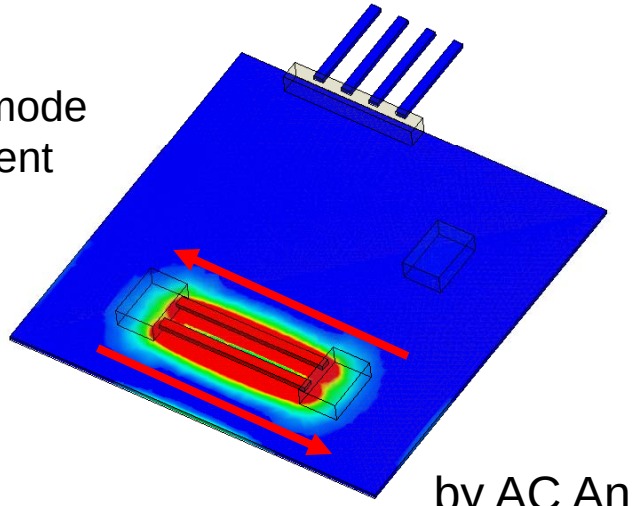
A PC Board & Cables



A victim device

A Driver & Receiver

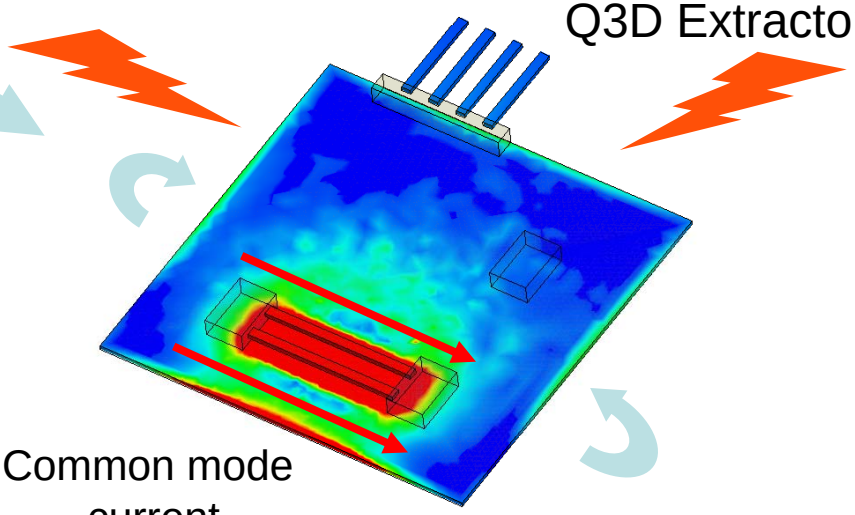
Loop mode current



by AC Analysis of Q3D Extractor

Differential mode current flows --- Loop
Common mode current flows --- Open

We can see Common mode current is more serious than Normal mode.



Common mode current

Antenna theory

-A Differential mode current flow → Loop antenna theory
-A Common mode current flow → Dipole antenna theory

$$E = \frac{131.6 \times 10^{-16} (f^2 AI) \sin\theta}{r}$$

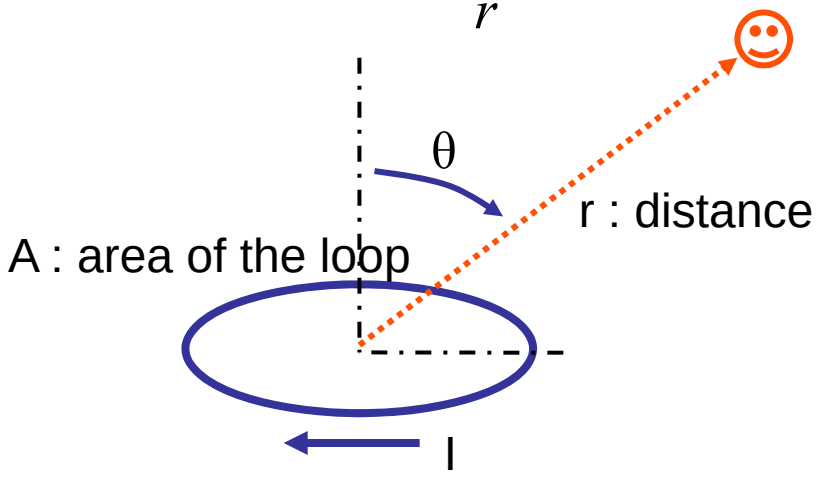


Illustration of a loop antenna

$$E = \frac{4\pi \times 10^{-7} (fIl) \sin\theta}{r}$$

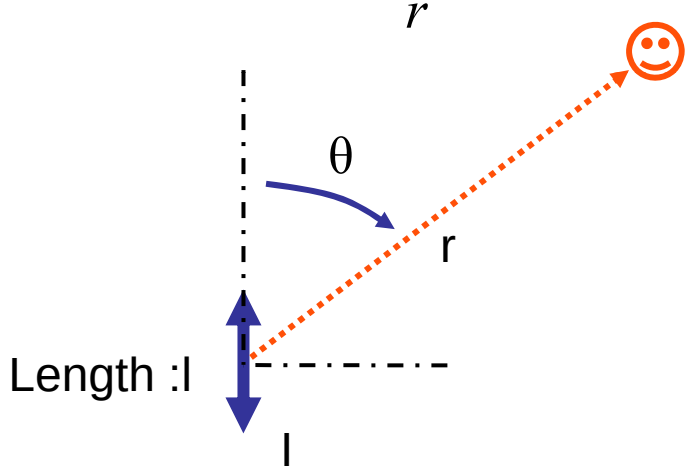


Illustration of a dipole antenna

FCC B level Mag. E limit :40dBuV/m @ 3m
Mag. E(Loop antenna) : 20mA
Mag. E(Dipole antenna) : 8uA

EMC Design Flow

Impedance Analysis

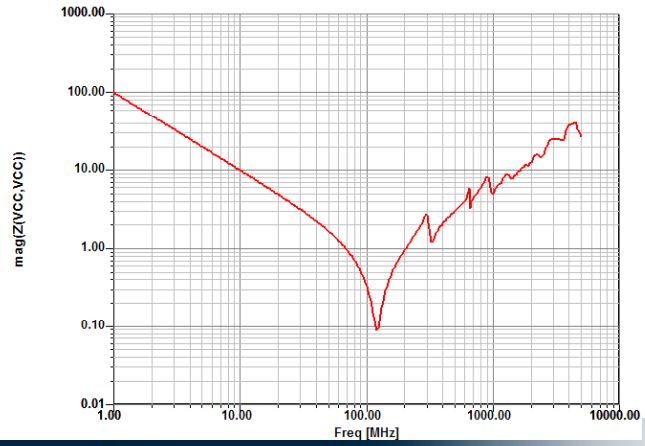
Ensure a low impedance as seen by active parts

Resonance Analysis

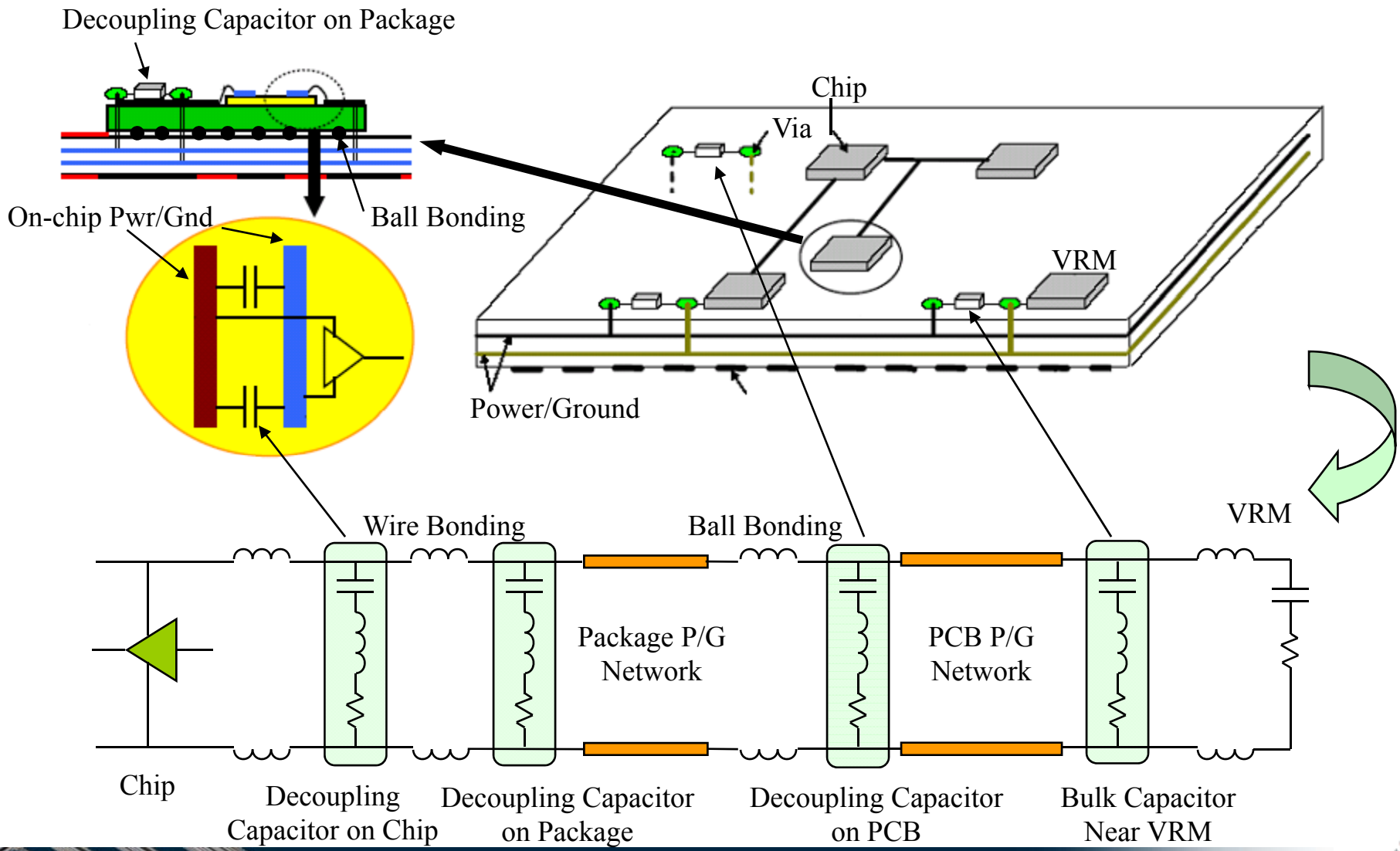
Change stackup, plane cutouts and decoupling as necessary

Signal Extraction

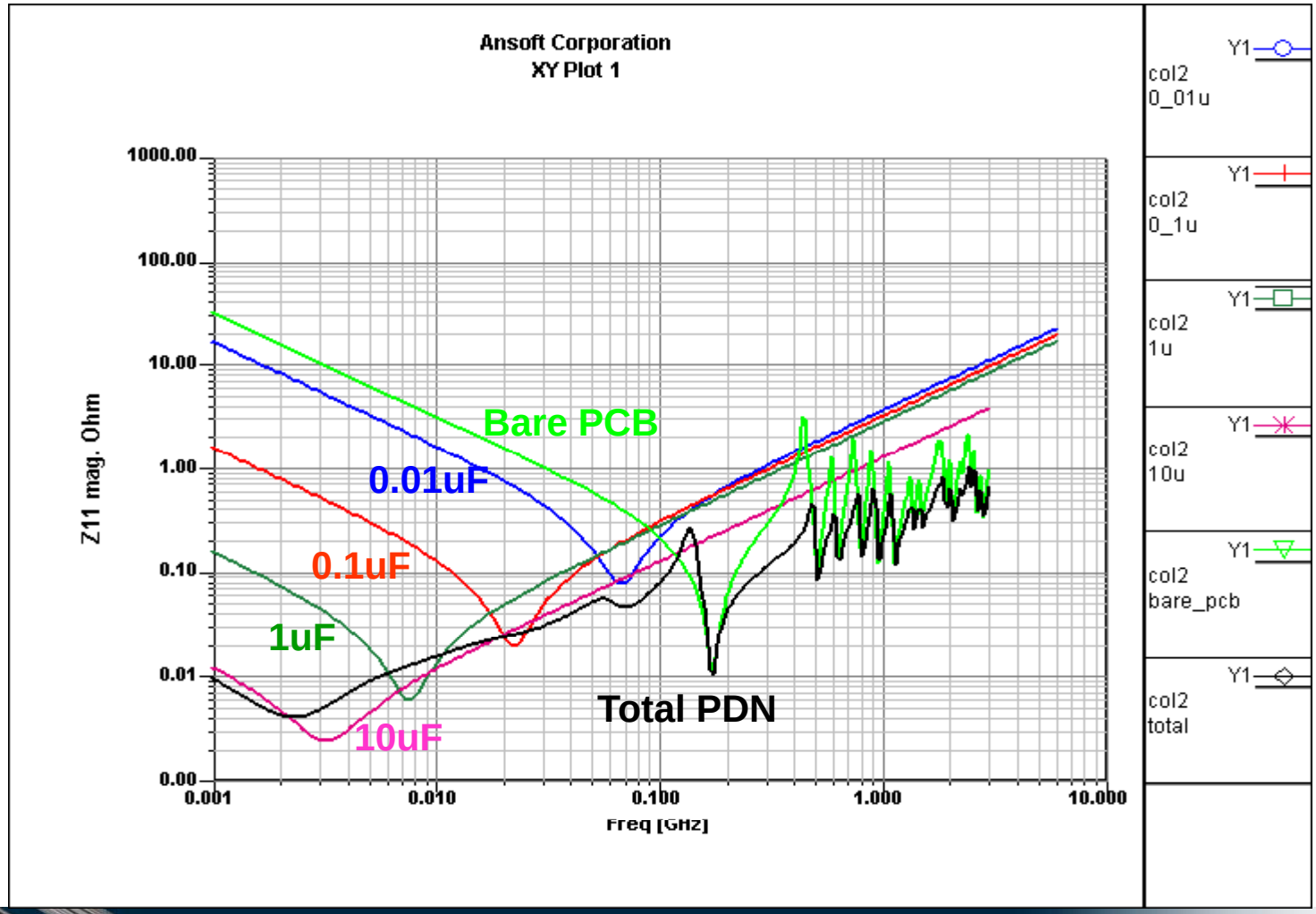
Emissions Analysis



Decoupling Capacitor



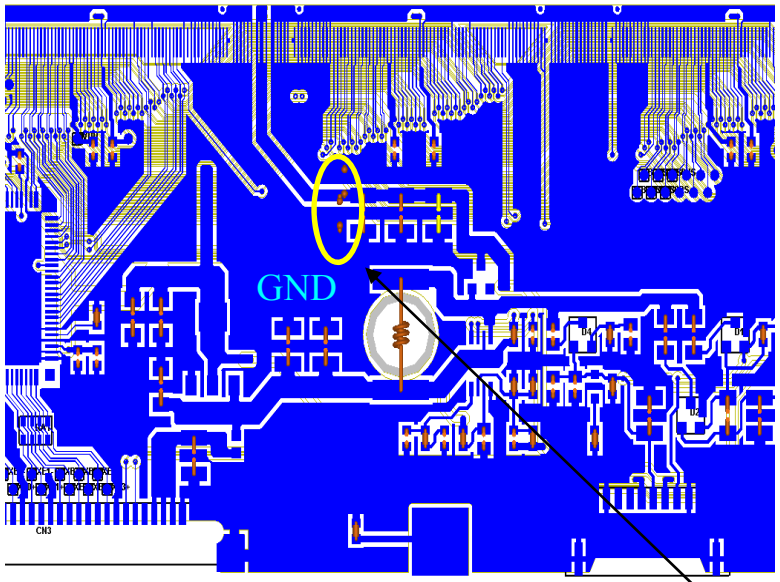
Decoupling Impedance of PDN



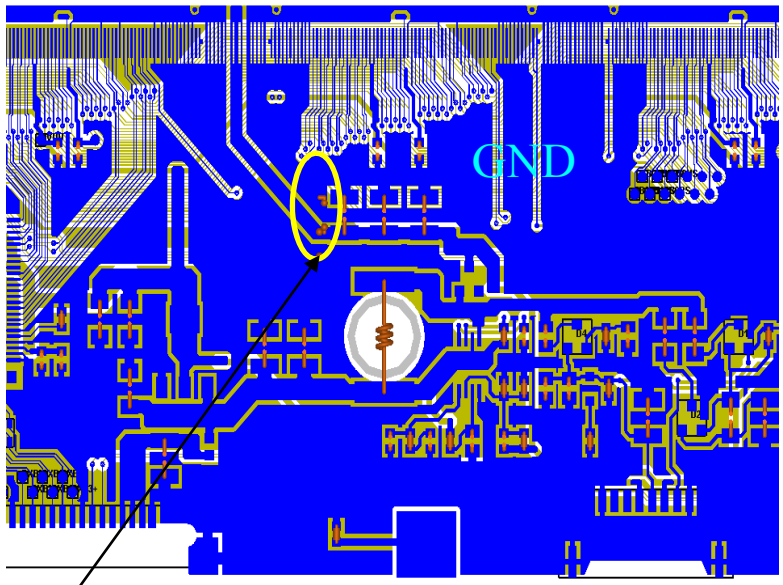
Plasma Screen Example

Changed Return Path

- Widened section of GND plane
- Added decoupling Capacitors



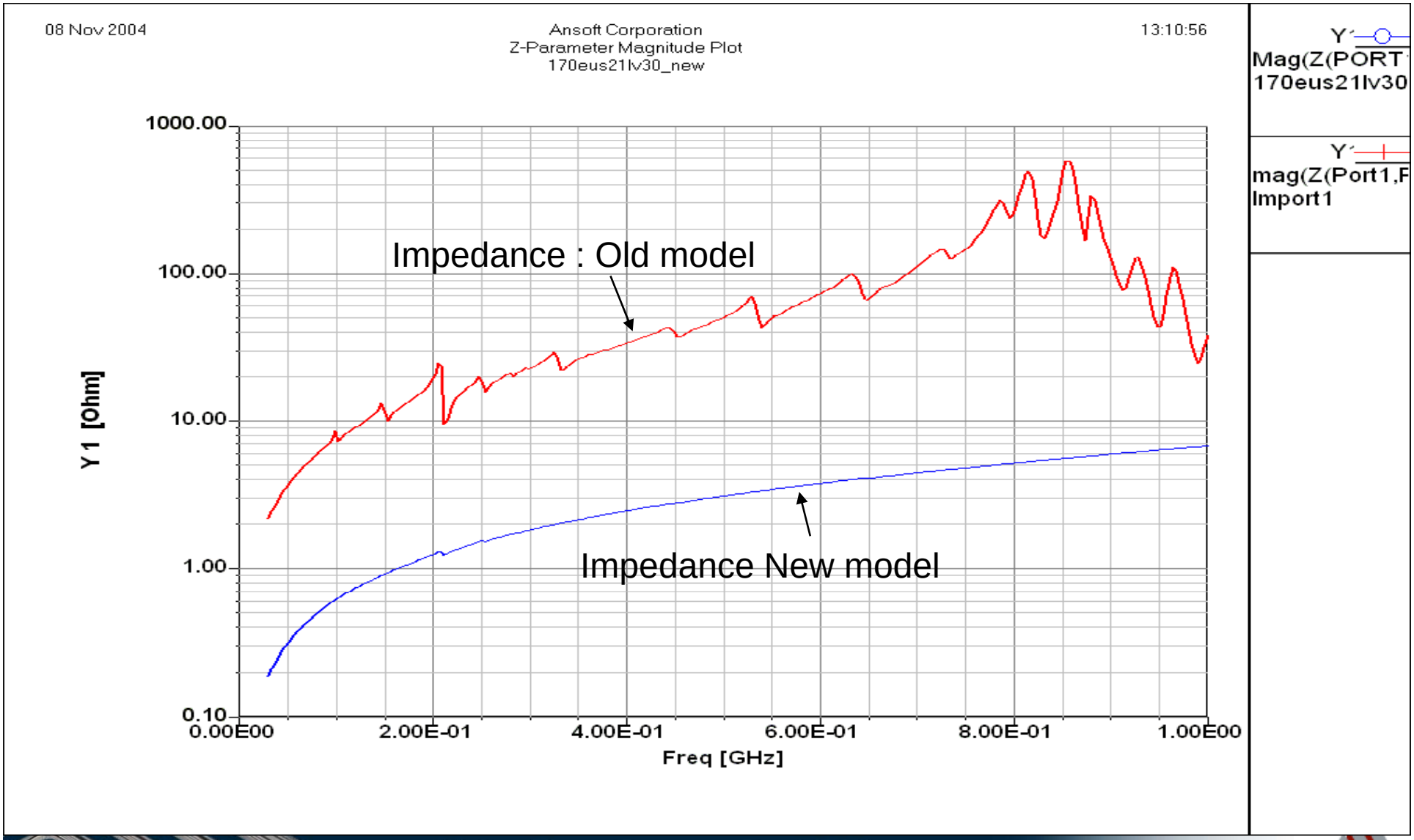
Old model



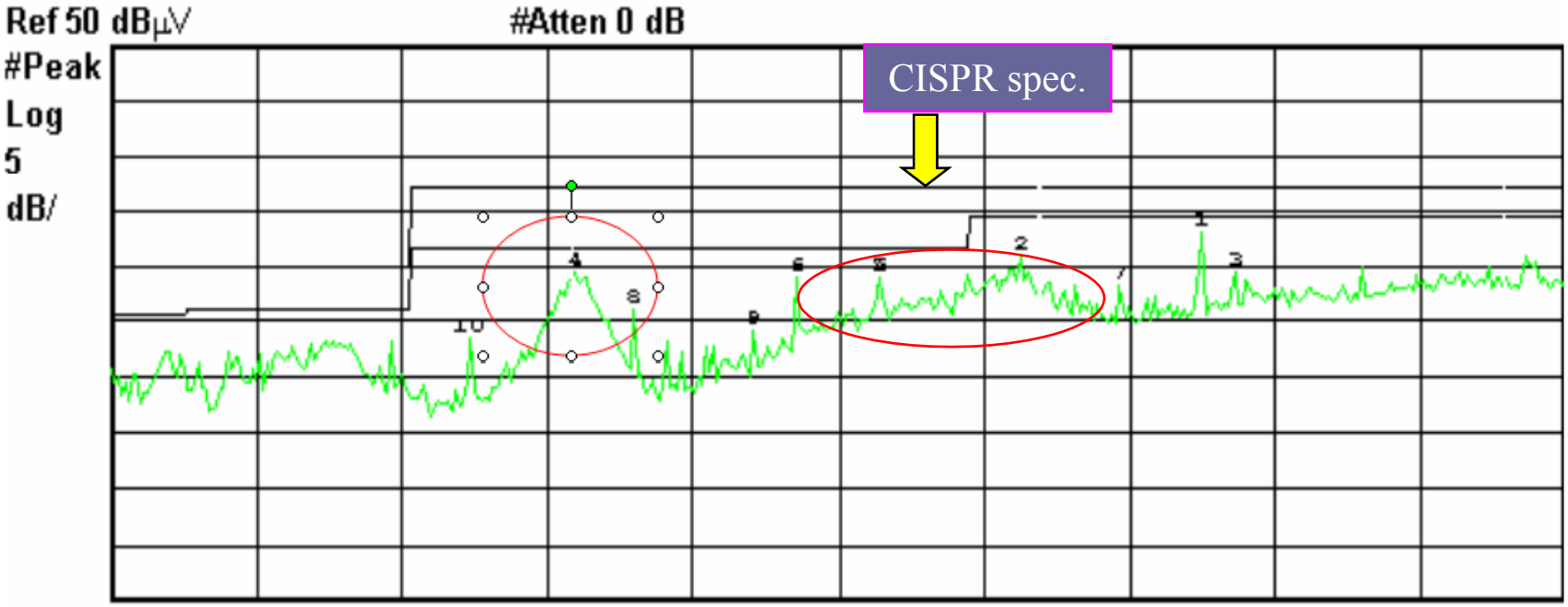
New model

Impedance test port near C3,4,5

Impedance Plot

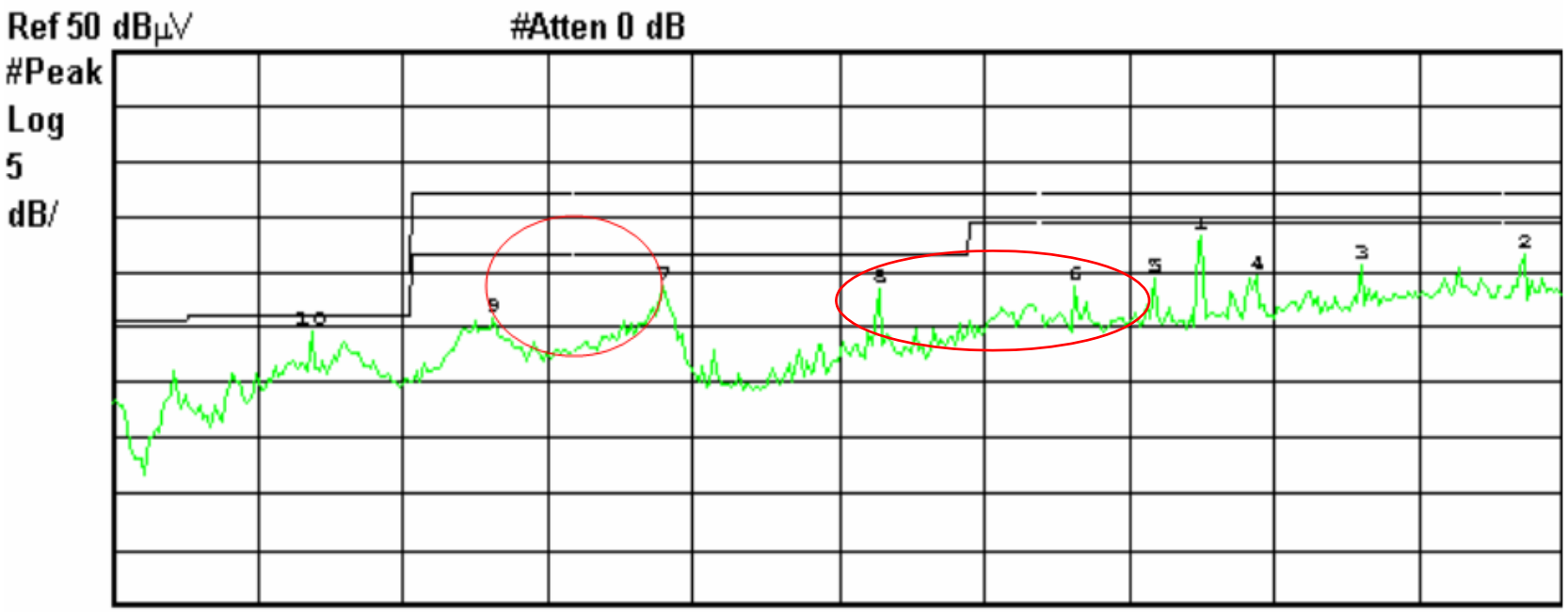


EMI Test Results : Old model



Pk	X Axis	Amplitude	Pk	X Axis	Amplitude
1	758 MHz	32.95 dBµV	6	486 MHz	28.91 dBµV
2	636 MHz	30.87 dBµV	7	702 MHz	28.17 dBµV
3	779 MHz	29.51 dBµV	8	379 MHz	25.97 dBµV
4	340 MHz	29.36 dBµV	9	459 MHz	24.25 dBµV
5	542 MHz	28.94 dBµV	10	270 MHz	23.49 dBµV

EMI Test Results : New model



Pk	X Axis	Amplitude	Pk	X Axis	Amplitude
1	758 MHz	33.28 dBµV	6	673 MHz	28.83 dBµV
2	973 MHz	31.52 dBµV	7	399 MHz	28.7 dBµV
3	864 MHz	30.66 dBµV	8	542 MHz	28.58 dBµV
4	794 MHz	29.76 dBµV	9	285 MHz	25.82 dBµV
5	726 MHz	29.52 dBµV	10	163 MHz	24.62 dBµV

EMC Design Flow

Impedance Analysis

Ensure power planes do not resonant in critical locations

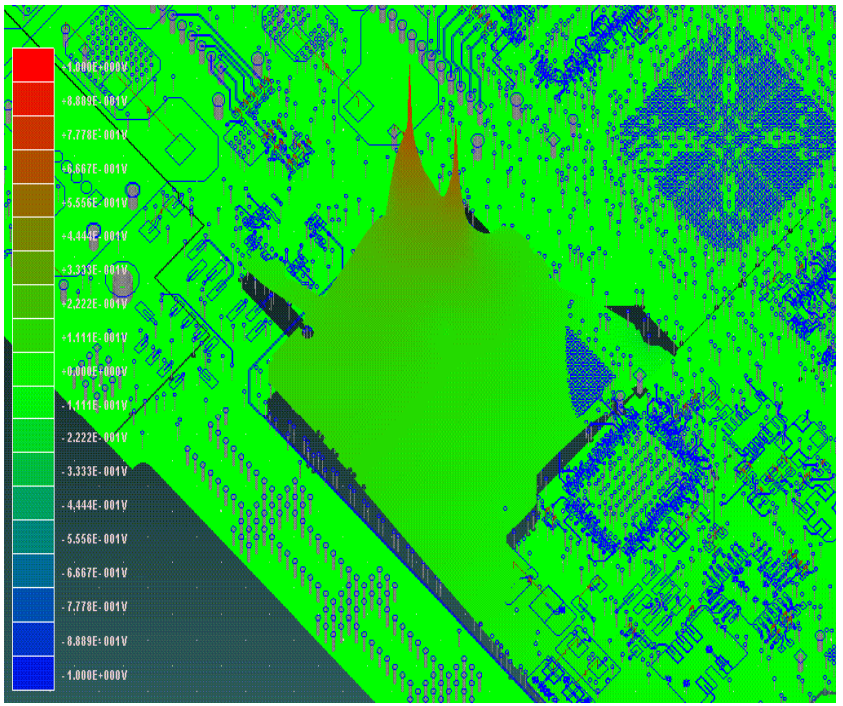
Resonance Analysis

Change stackup, plane cutouts and decoupling as necessary

Signal Extraction

Emissions Analysis

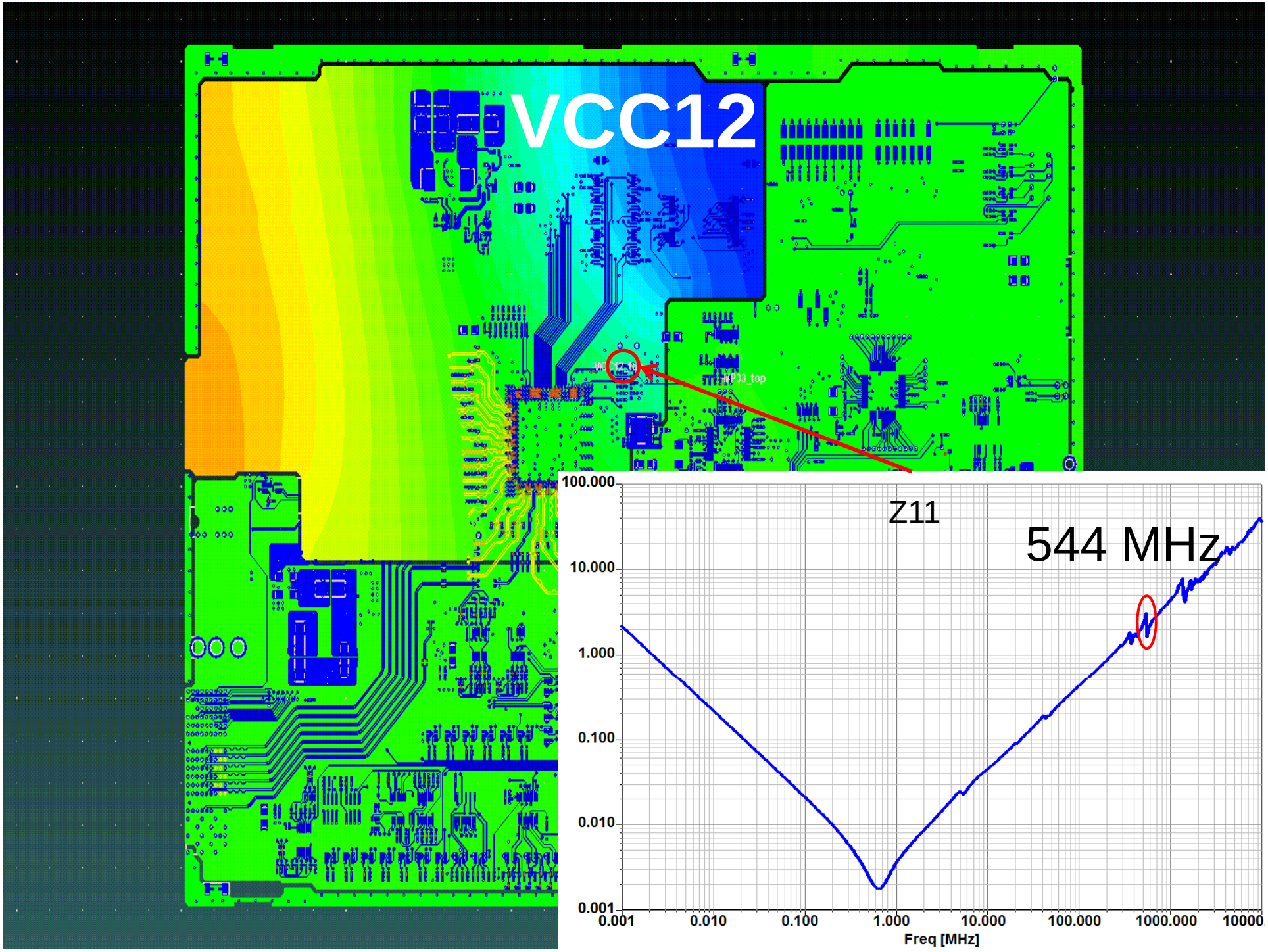
Enclosure Simulation



Managing Resonances

Even though resonances ALWAYS exist, you don't need to excite them:

- Keep them away from Clock harmonics
- Examine Via Transitions
- Avoid routing near splits
- Move discrete parts


VCC12
Z11
544 MHz
100.000
10.000
1.000
0.100
0.010
0.001
0.001
0.010
0.100
1.000
10.000
100.000
1000.000
10000.
Freq [MHz]

EMC Design Flow

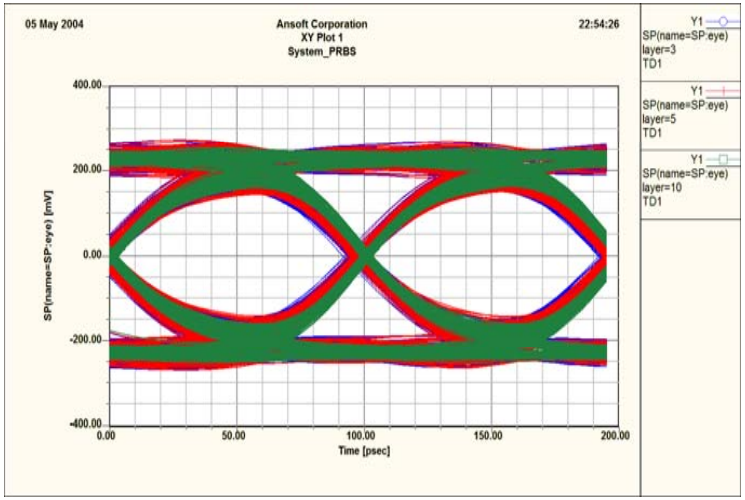
Impedance Analysis

Resonance Analysis

Signal Extraction

Emissions Analysis

Enclosure Simulation

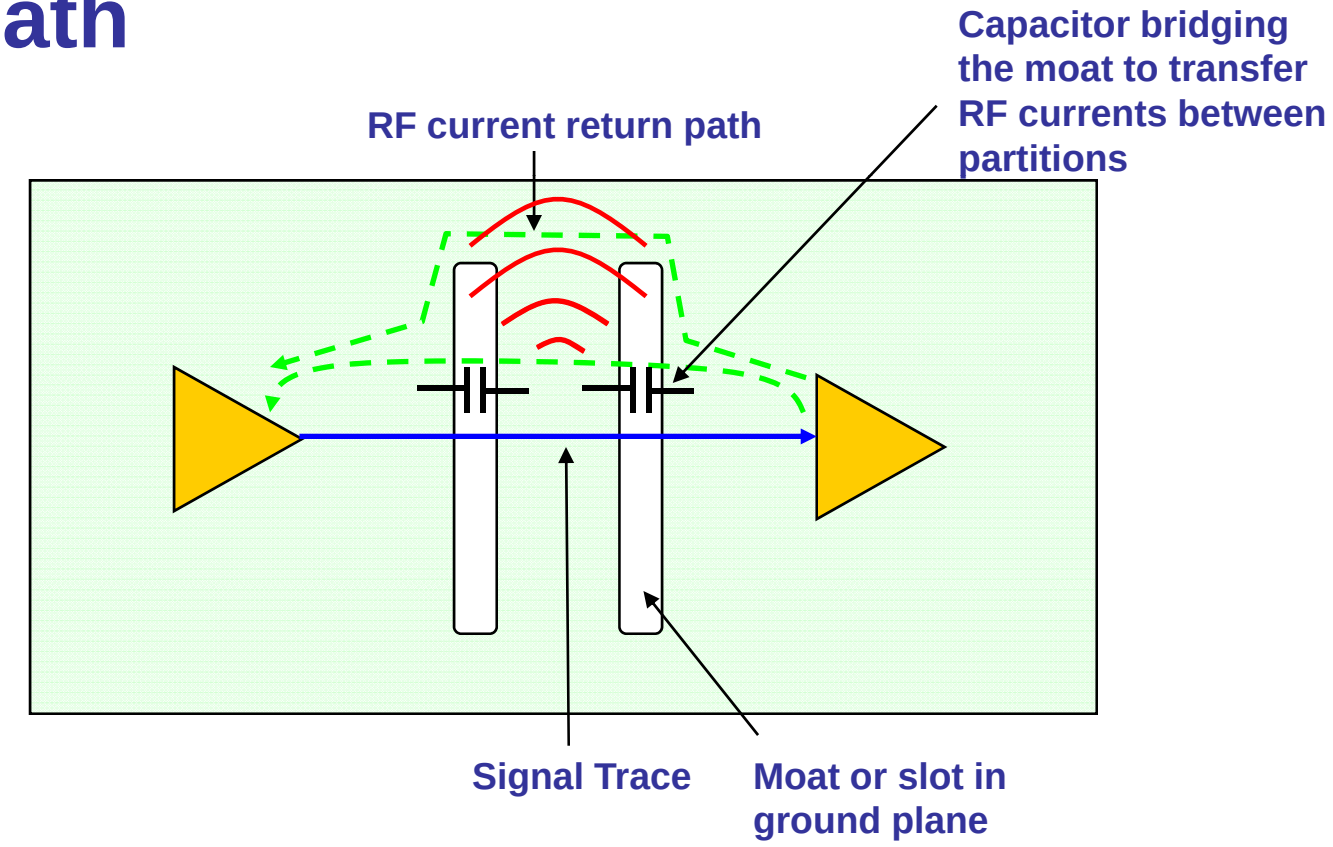


Ensure signals meet required bandwidth

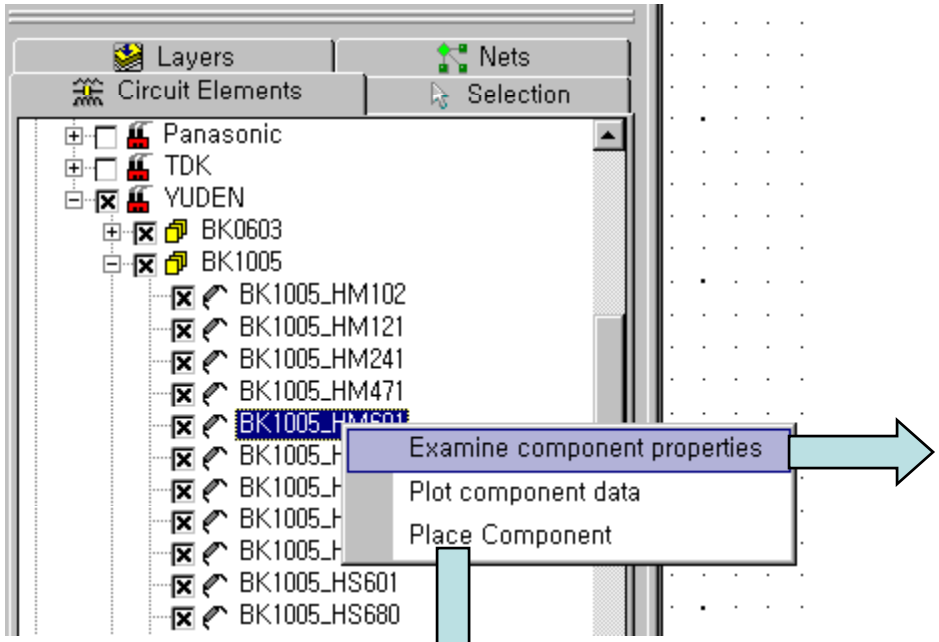
Change routing as necessary

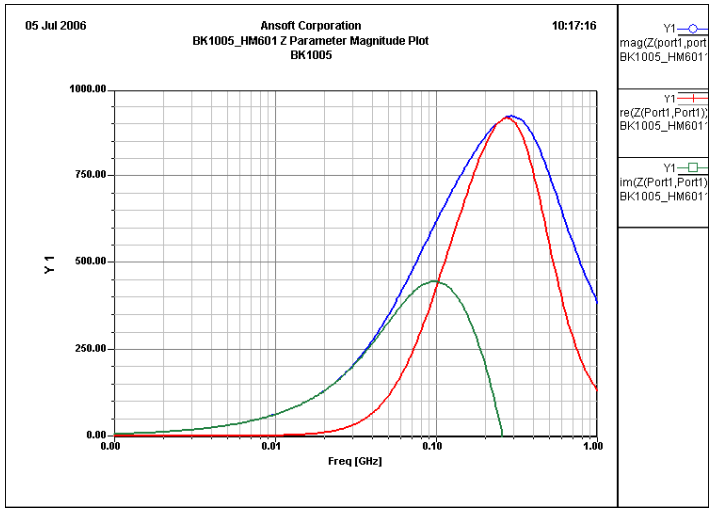
Image Plane Violations

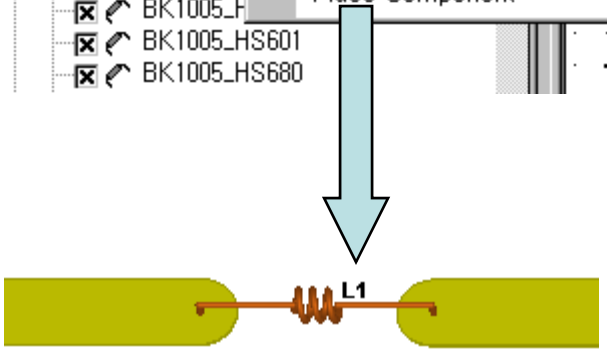
- **Always Consider Return Current Path**



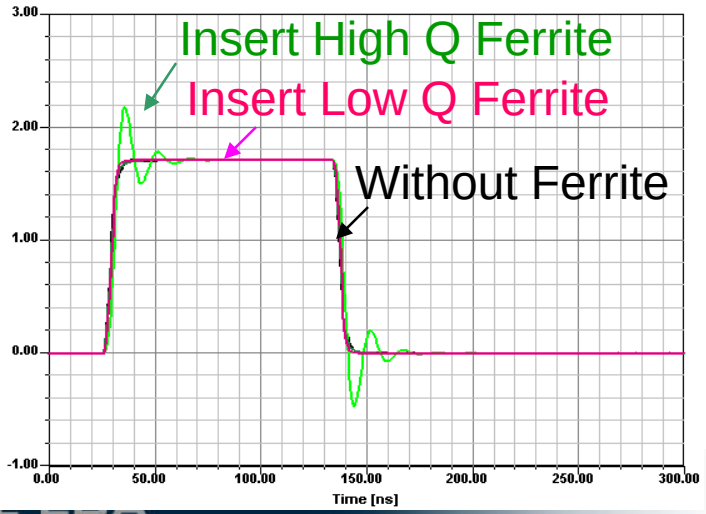
EMI Reduction using Ferrites



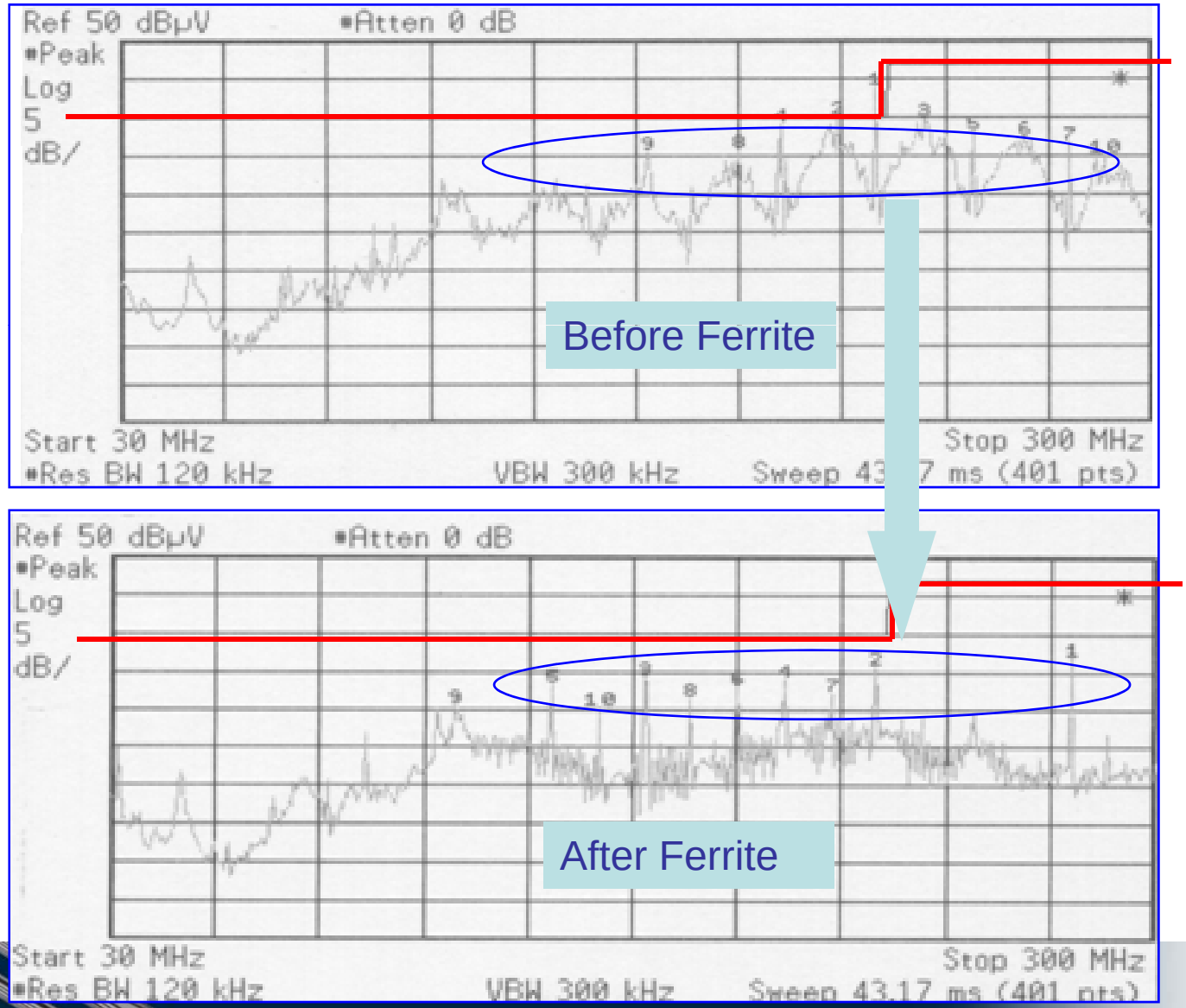




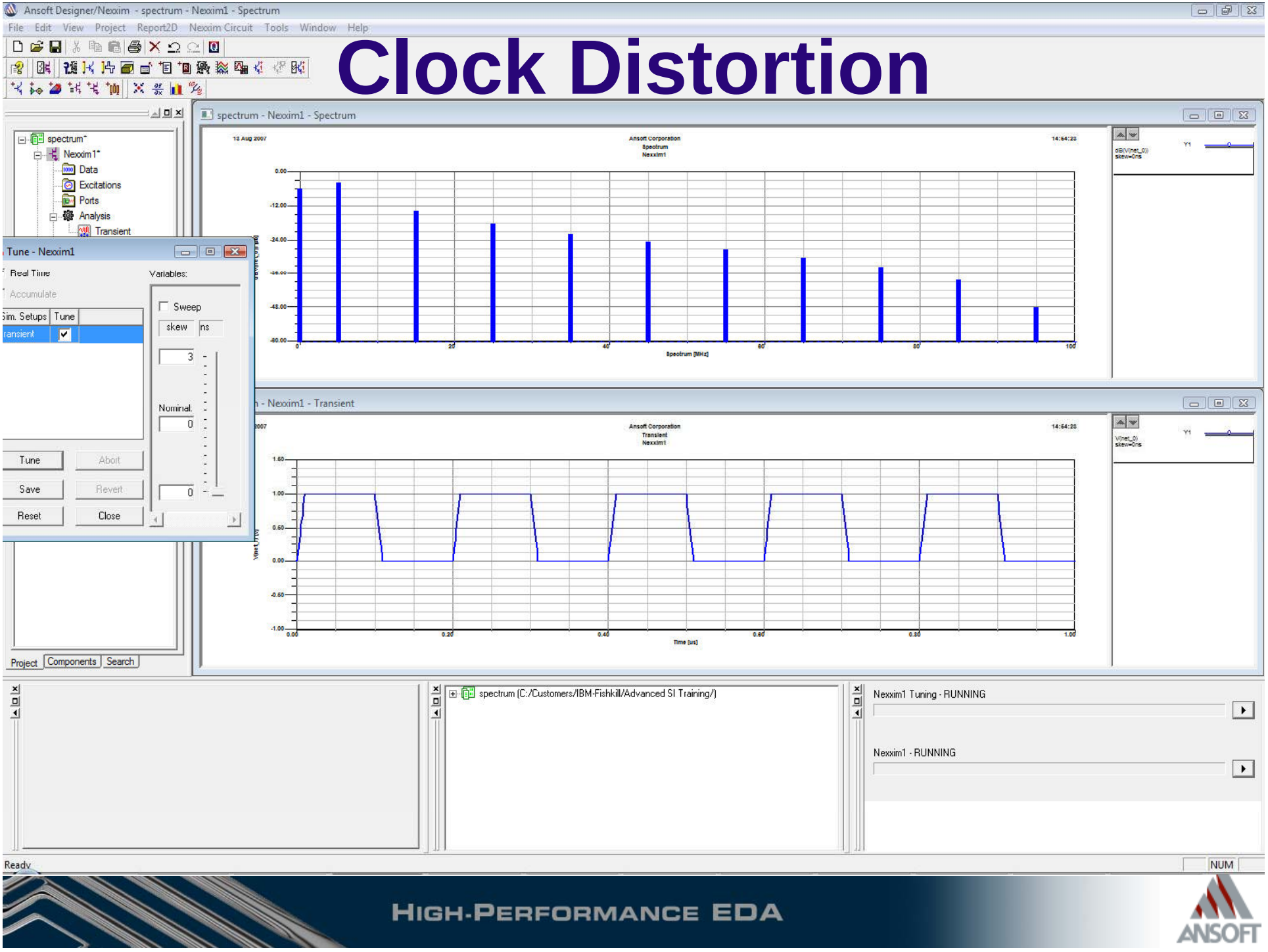
Internal Clock Line



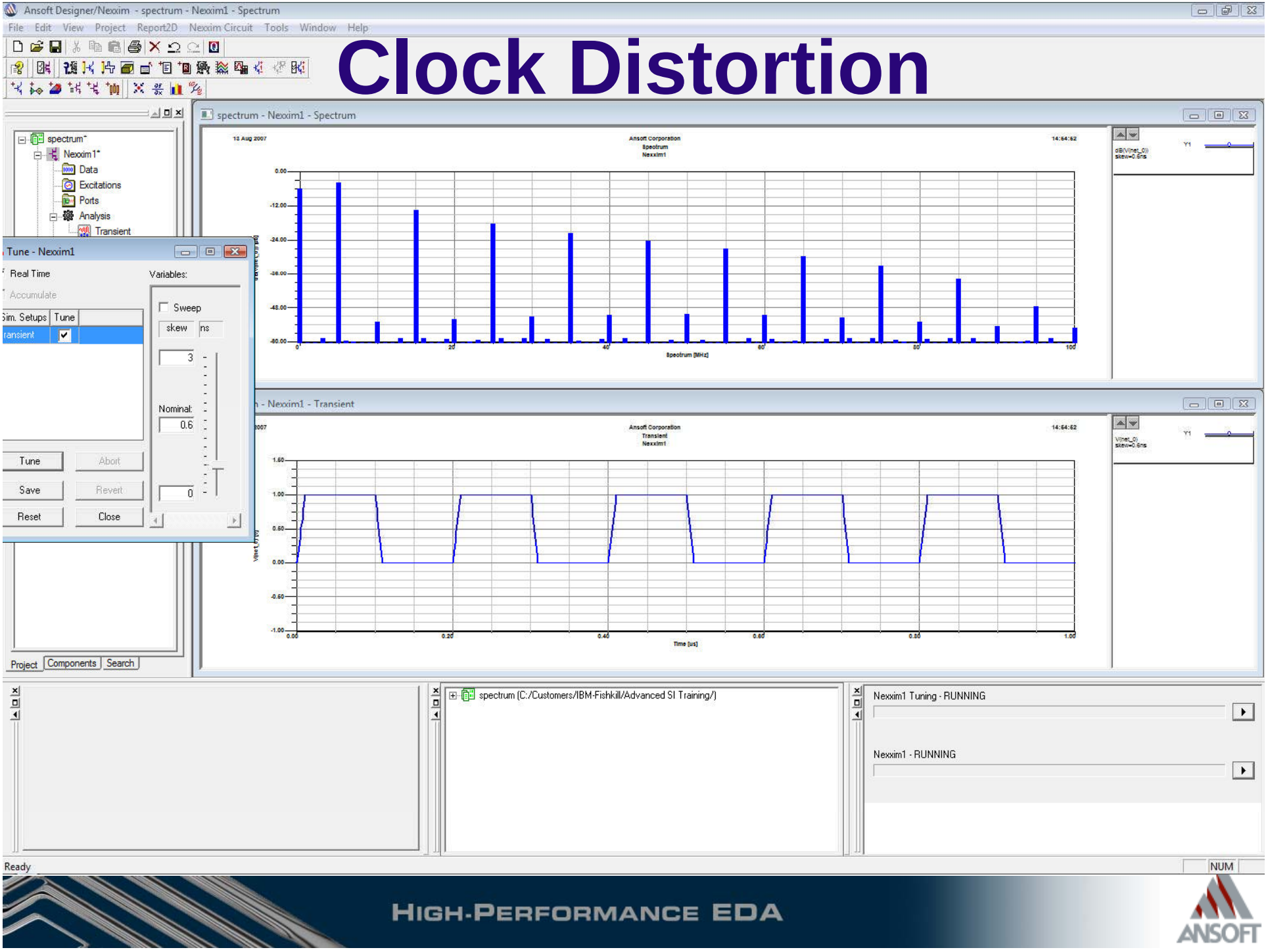
EMI Test Results



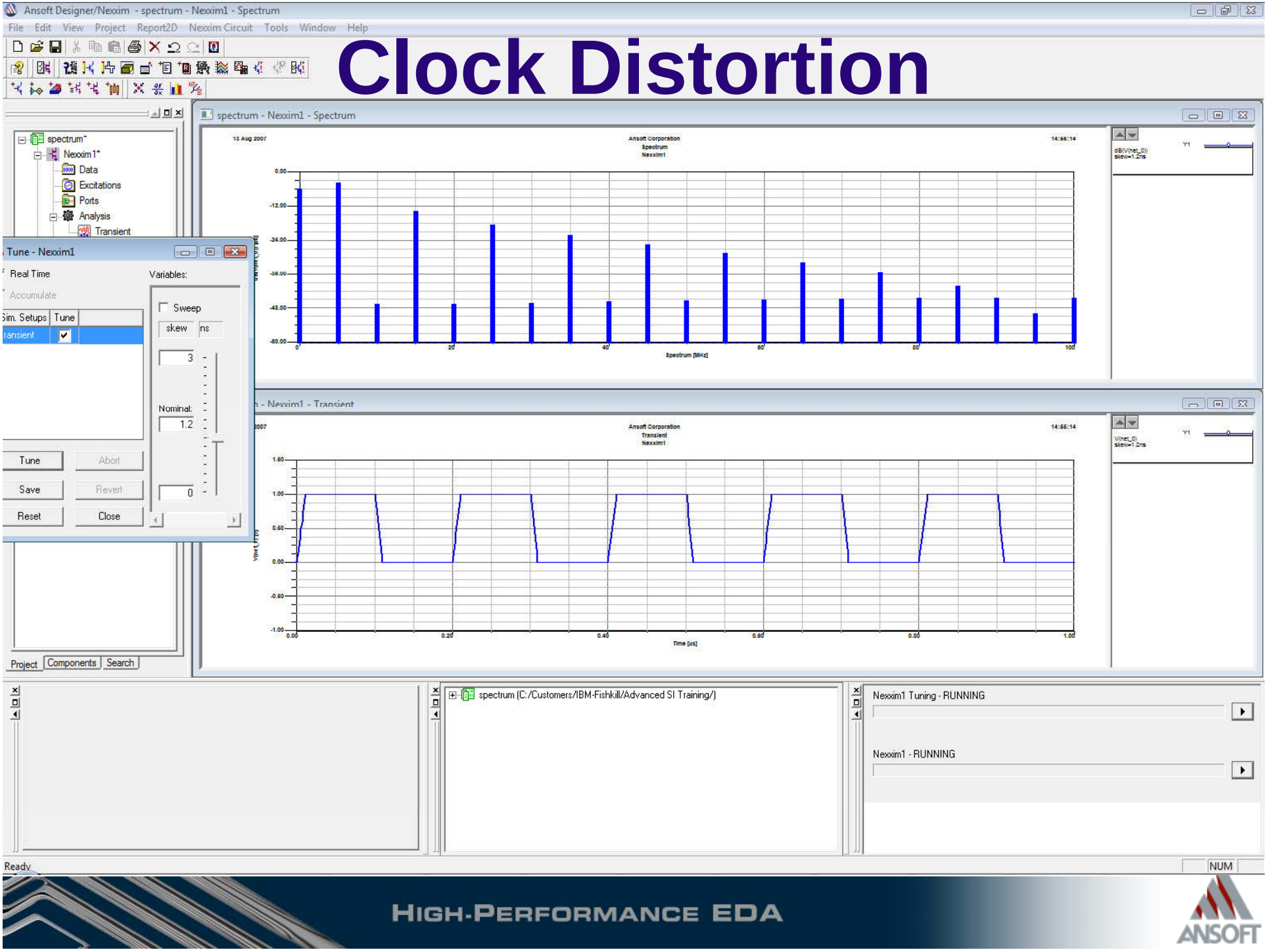
Clock Distortion



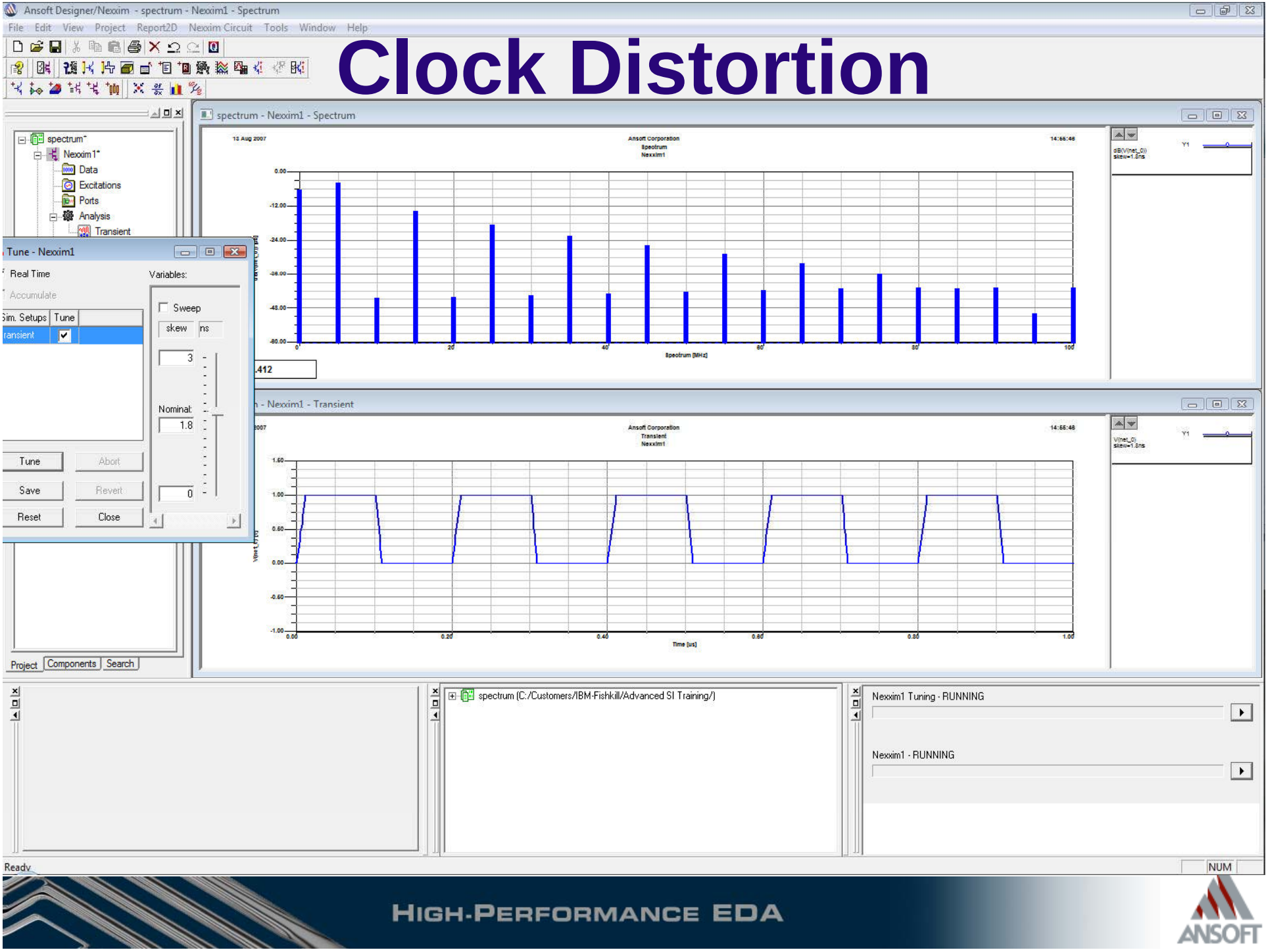
Clock Distortion



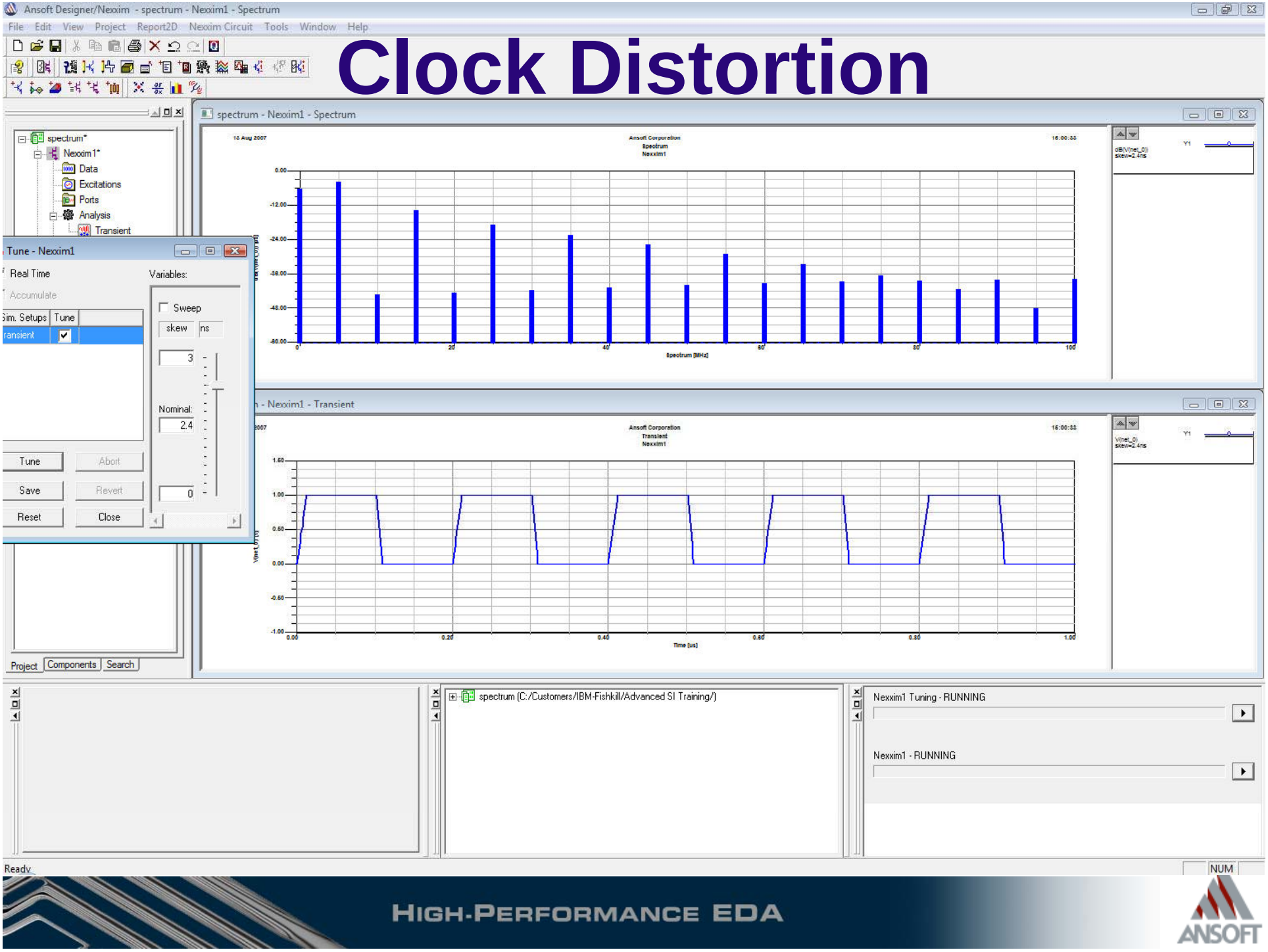
Clock Distortion



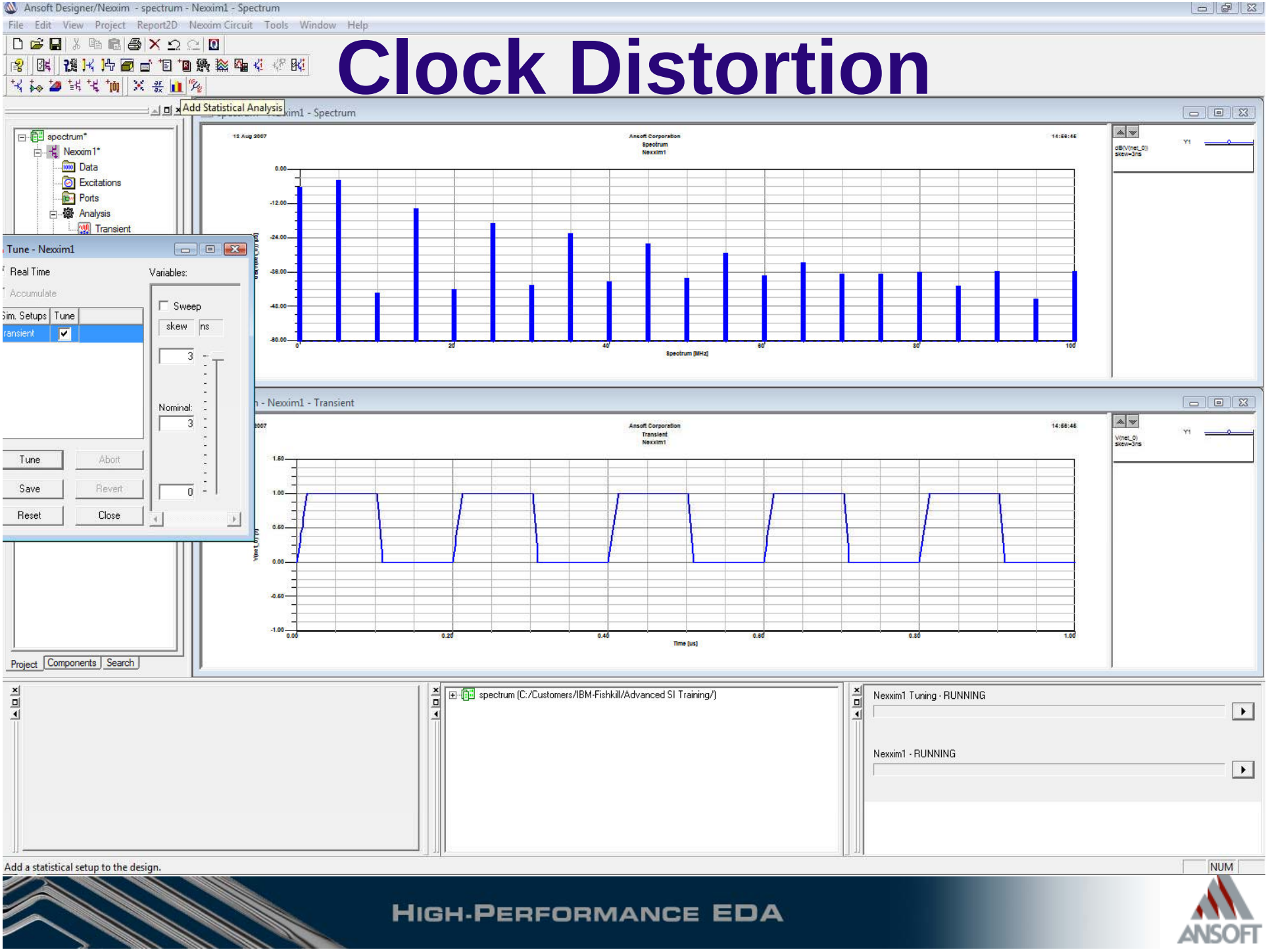
Clock Distortion



Clock Distortion



Clock Distortion



EMC Design Flow

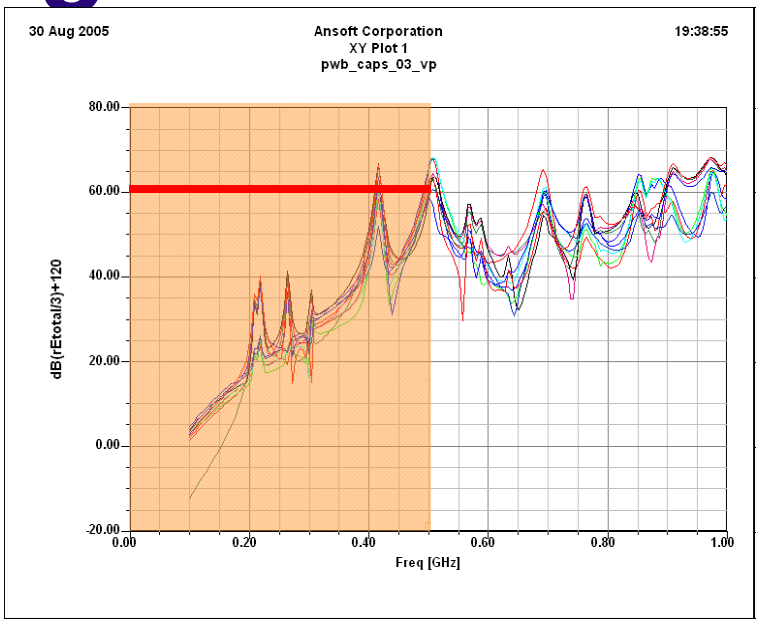
Impedance Analysis

Resonance Analysis

Signal Extraction

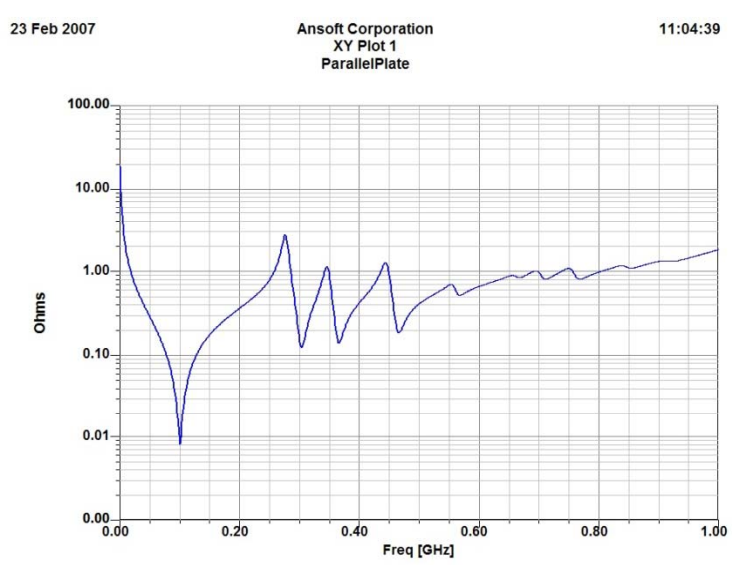
Emissions Analysis

Enclosure Simulation

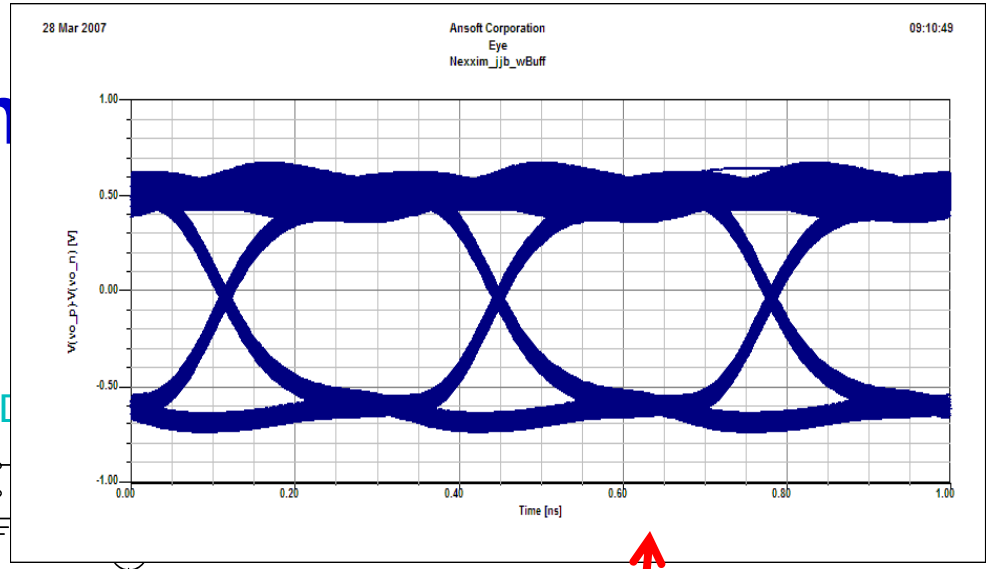


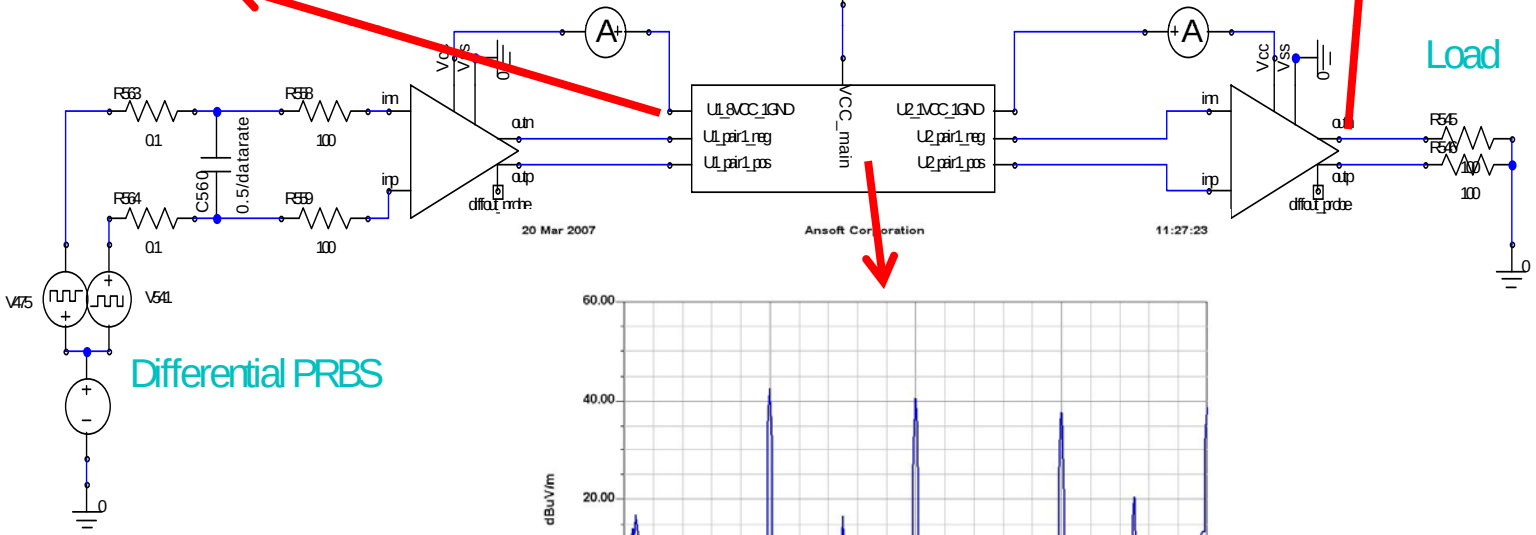
Ensure EMI is at acceptable level

Optimize previous three simulations


23 Feb 2007
Ansoft Corporation
XY Plot 1
ParallelPlate
11:04:39
Ohms
Freq [GHz]

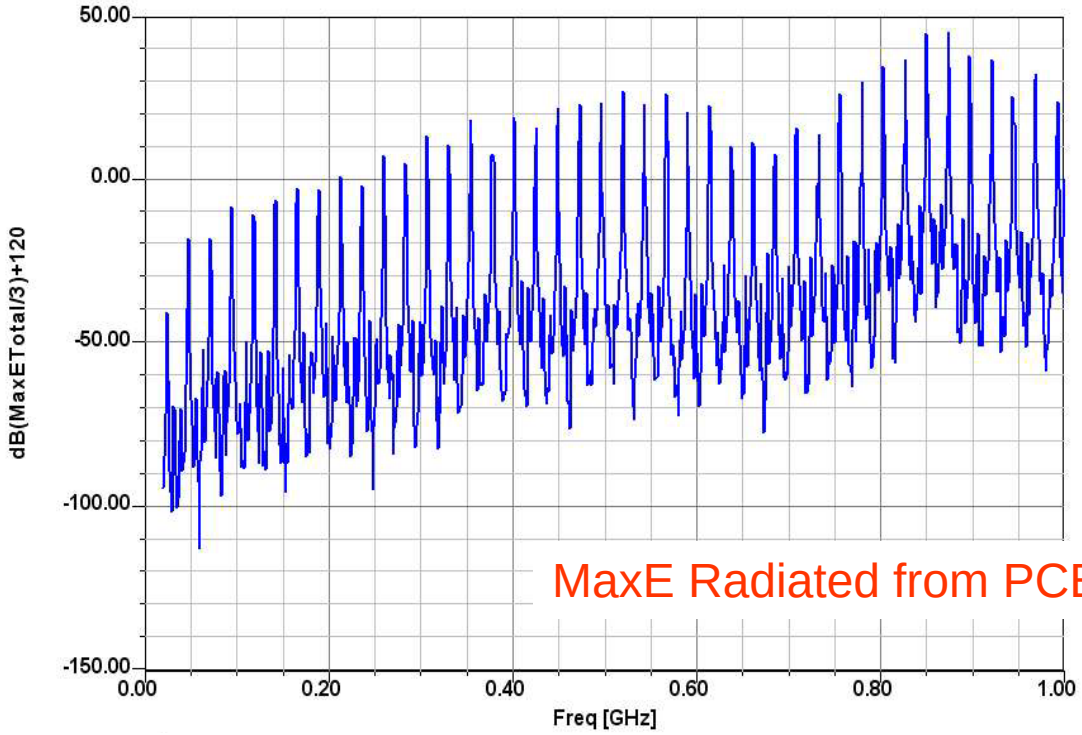
hann


28 Mar 2007
Ansoft Corporation
Eye
Nexxim_jjb_wBuff
09:10:49
Time [ns]

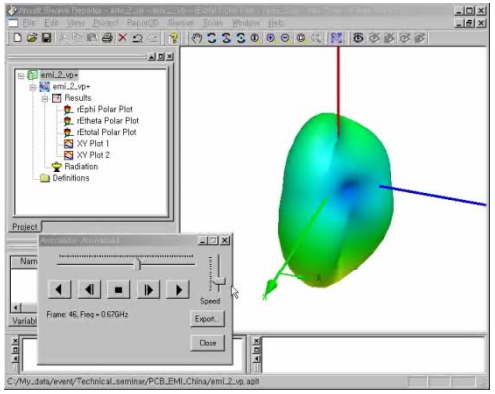

Load
Differential PRBS
U1_8VCC_1GND
U1_pair1_neg
U1_pair1_pos
VCC_main
U2_1VCC_1GND
U2_pair1_neg
U2_pair1_pos
20 Mar 2007
Ansoft Corporation
11:27:23

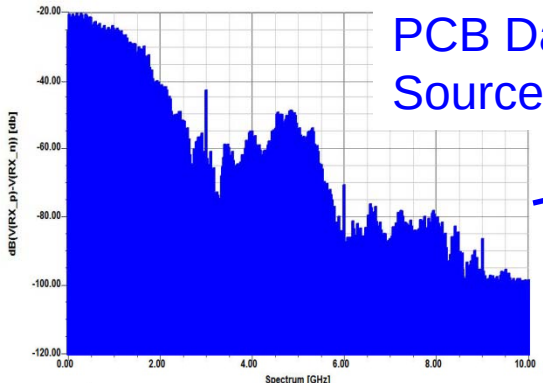
dBuV/m
Freq [GHz]

Real Drivers as Noise Source

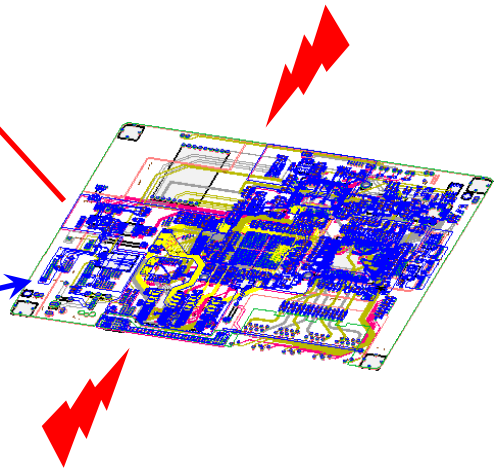


MaxE Radiated from PCB

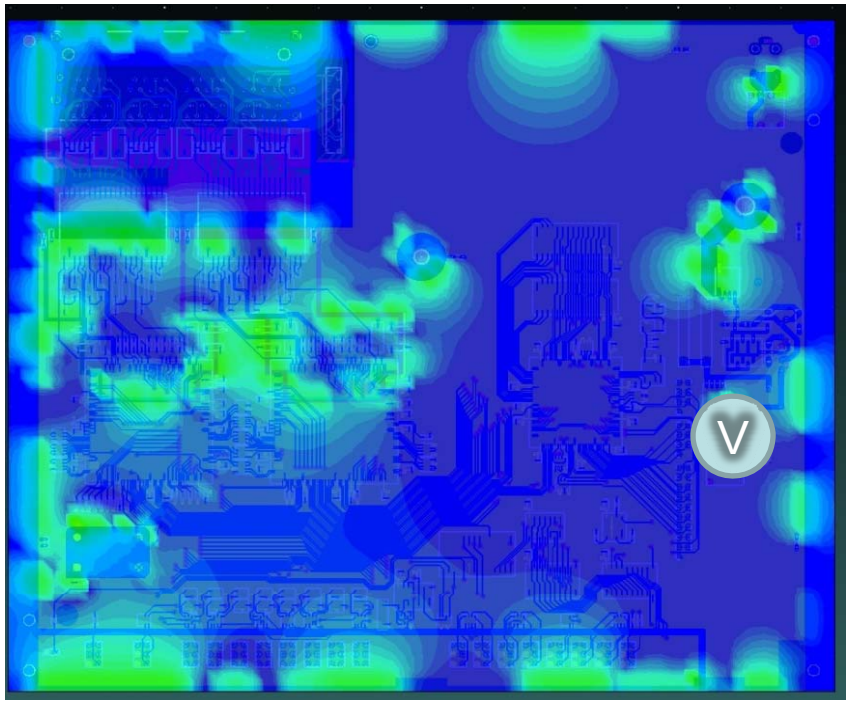


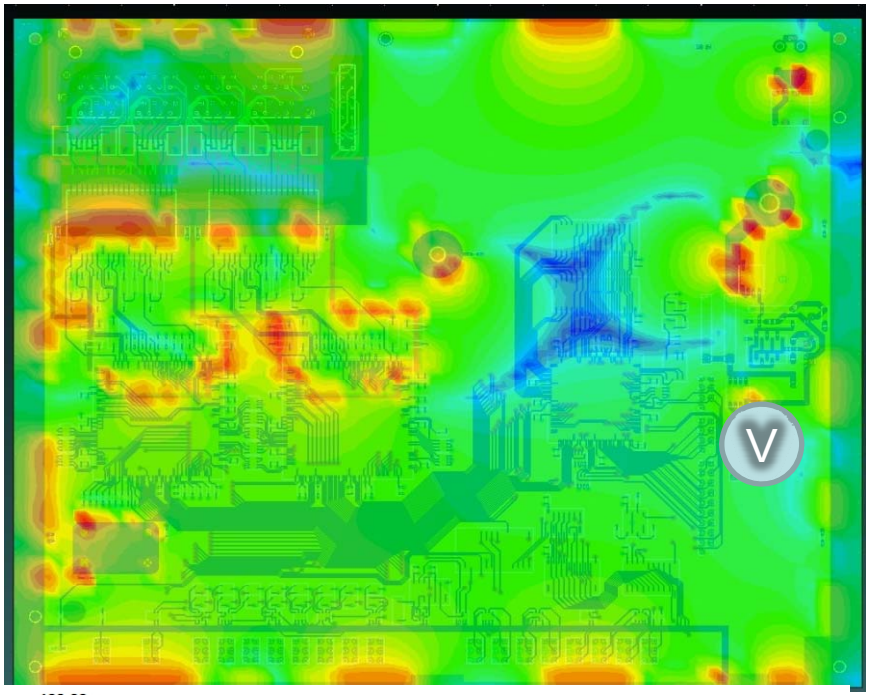


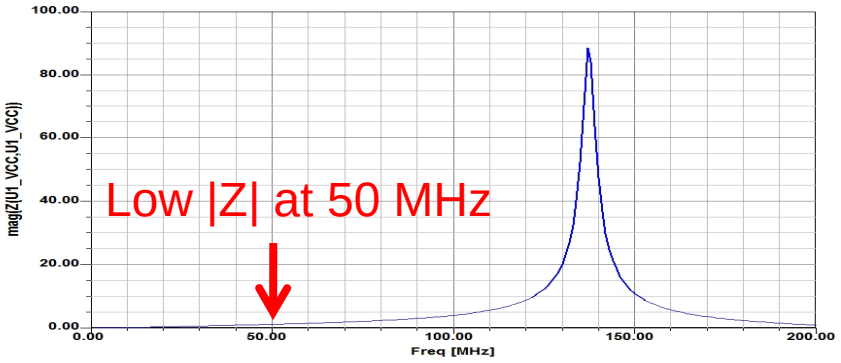
PCB Data-Line
Source spectrum

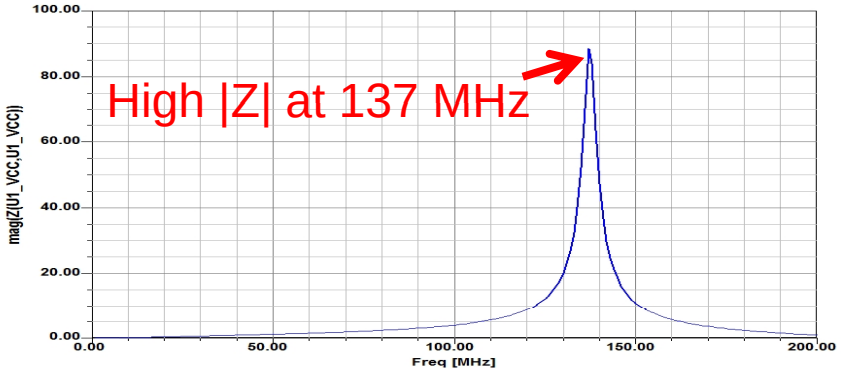


Near-Fields


V


V


Low |Z| at 50 MHz
mag(Z(U1_VCC,U1_VCC))
Freq [MHz]
100.00
80.00
60.00
40.00
20.00
0.00
0.00
50.00
100.00
150.00
200.00


High |Z| at 137 MHz
mag(Z(U1_VCC,U1_VCC))
Freq [MHz]
100.00
80.00
60.00
40.00
20.00
0.00
0.00
50.00
100.00
150.00
200.00

EMC Design Flow

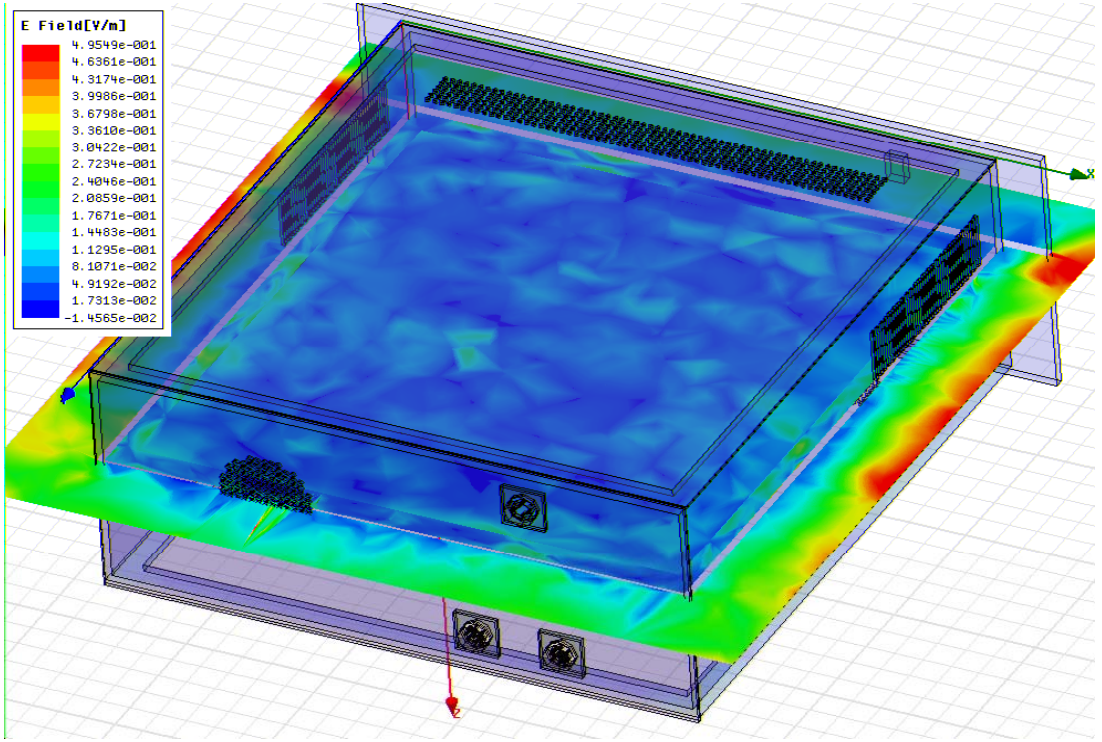
Impedance Analysis

Resonance Analysis

Signal Extraction

Emissions Analysis

Enclosure Simulation

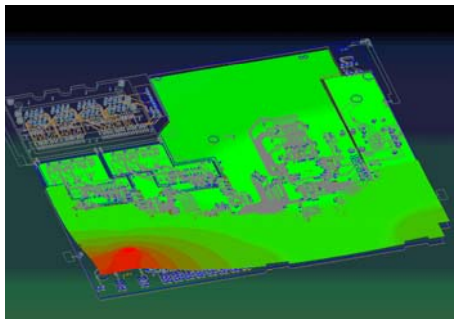


Test performance of different enclosures

Iterate design as necessary

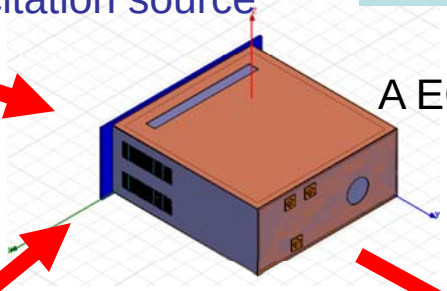
Linking EMI Source with Shield

A noise analysis by SIwave

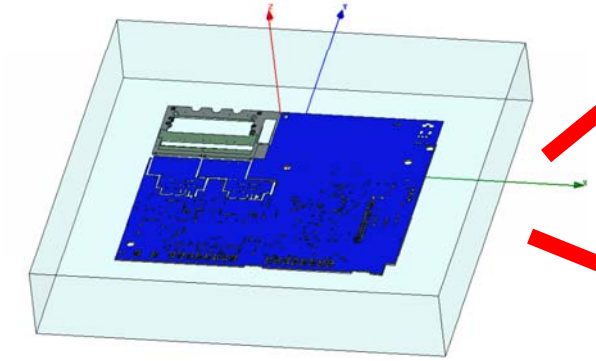


SIwave to HFSS
HFSS to HFSS

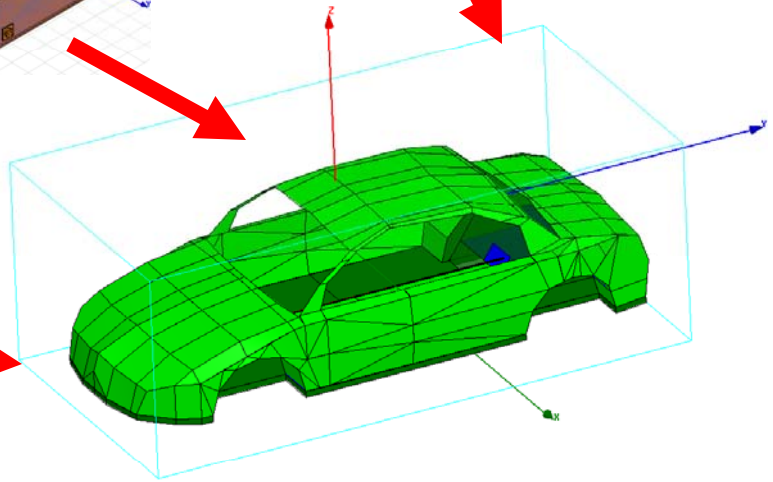
A excitation source



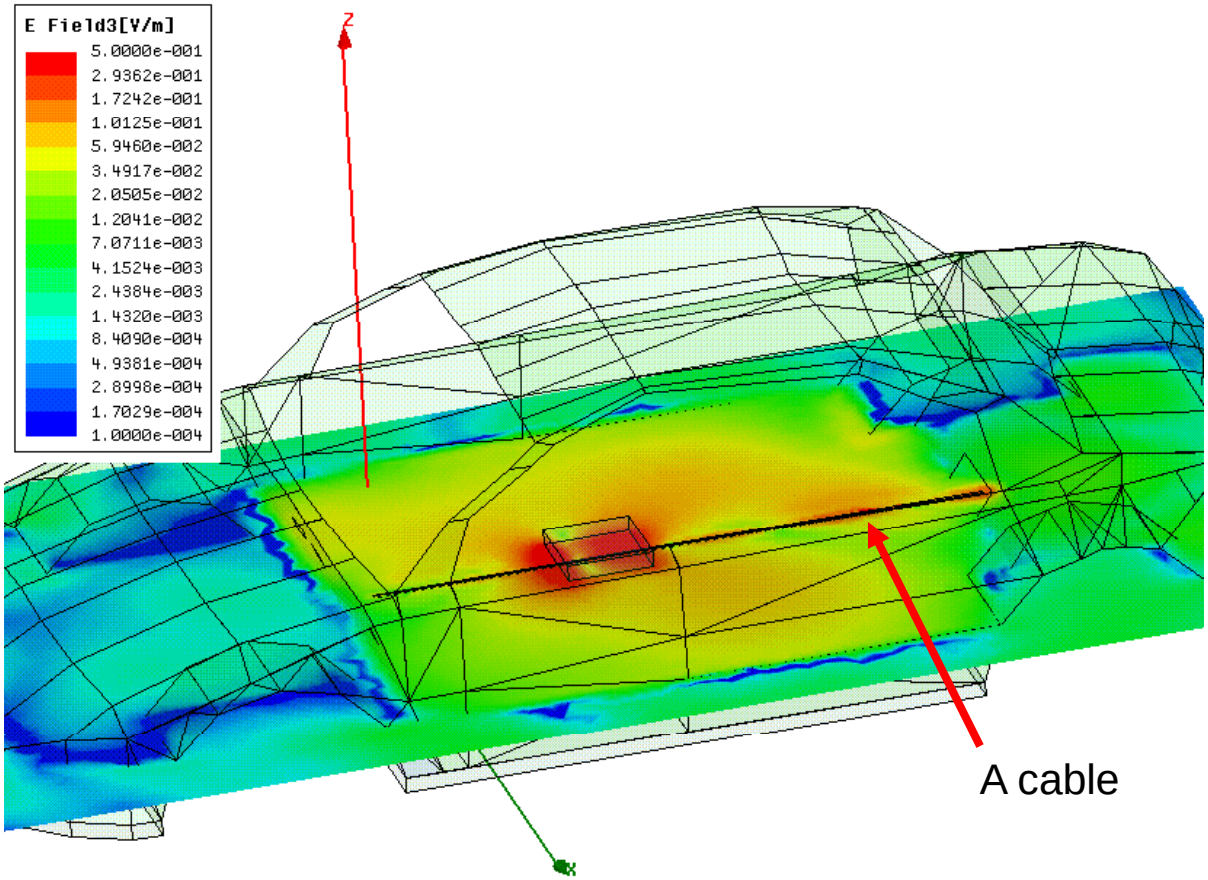
A ECU analysis by HFSS



A EM analysis by HFSS



A noise source and a cable



310 MHz
Impedance
Peak on PCB

Conclusions

- It’s easiest to control EMI at it’s source
  - Prevents Emission and Self Interference
- EMC is comprised of good PI and SI
- Simulating throughout the design cycle can help you avoid trouble in the chamber