# Gate Drive Card for High Power Three Phase PWM Converters

Anil Kumar Adapa
Engineer R&D
Medha Servo Drive Pvt. Ltd., India
Email: anilkumaradapa@gmail.com

Vinod John
Department of Electrical Engineering
Indian Institute of Science, India
Email: vjohn@ee.iisc.ernet.in

***Abstract*—Gate driver is an integral part of every power converter, drives the power semiconductor devices and also provides protection for the switches against short-circuit events and over-voltages during shut down. Gate drive card for IGBTs and MOSFETs with basic features can be designed easily by making use of discrete electronic components. Gate driver ICs provides attractive features in a single package, which improves reliability and reduces effort of design engineers. Either case needs one or more isolated power supplies to drive each power semiconductor devices and provide isolation to the control circuitry from the power circuit. The primary emphasis is then to provide simplified and compact isolated power supplies to the gate drive card with the requisite isolation strength and which consumes less space, and for providing thermal protection to the power semiconductor modules for 3-$\phi$ 3 wire or 4 wire inverters.**

***Index Terms*—Gate drive, multi-channel isolated power supply, thermal protection.**

## I. Introduction

Gate drive card converts logic level turn on/off commands from the PWM converter to proper power level signals for reliable control of the power semiconductor devices. These gate drive cards should protect power semiconductor switches against short circuit events [1]. In applications, short circuit can happen due to bad wiring/load, turning on complementary devices in a leg and cross conduction due to insufficient dead time. By monitoring $V_{CE(sat)}$ of the IGBT, it is possible to prevent destruction of the device due to desaturation. Very high currents through the device results in raise of $V_{CE(sat)}$ and the device dissipates excessive power and fails due to thermal break down. Insufficient gate drive voltage also leads to desaturation of the device which is undesirable [2]. Rapid turn off of an IGBT under fault leads to failure of the device because of higher voltage stresses due to large $di/dt$ induced voltages, soft turn-off will prevent such failure.

Commercial gate drive cards provide attractive features like soft turn off after desaturation fault detection, under voltage lockout, fault indication with isolation etc. [3]. Gate driver ICs also provide such features in a single package which reduces the effort of design engineers to develop gate drive cards. Power semiconductor devices of a converter will have different potential reference nodes and the reference potential of these nodes can vary depending on the switch state, which demands and isolated power supply per device connected to the different reference nodes. A primary challenge in a practical implementation of a gate drive card is powering of the gate driver with floating potential references [4]. An additional requirement in designing a gate drive card is to provide isolated power supplies in a small area and with high reliability. This paper presents a simple power supply configuration for the design of gate drive cards for poly-phase inverters and for providing semiconductor thermal protection by making use of a thermistor based temperature sensor.

## II. Gate Drive Card

Basic requirements to design a gate drive card are:

1) Number of channels and selection of driver IC.
2) Requirement of isolated power supplies and their rating.
   -Gate voltage levels
   -Gate charge estimation
   -Peak current requirement
3) Provision for isolated power supplies.

A gate drive card has been designed with 6 driver channels, which can be extended upto 8 channels. The gate drive card makes use of AVAGO technologies HCPL-316J gate driver IC [5]. Block diagram of the designed gate drive card, shown in Fig. 2, indicates the arrangement of the gate drive channels, power supply and temperature sensing sections. Each channel requires two isolated power supplies and one non-isolated power supply whose ground is same as that of the system control ground reference. Each channel is designed to deliver at least 2 $W$ of average power to the gate circuit

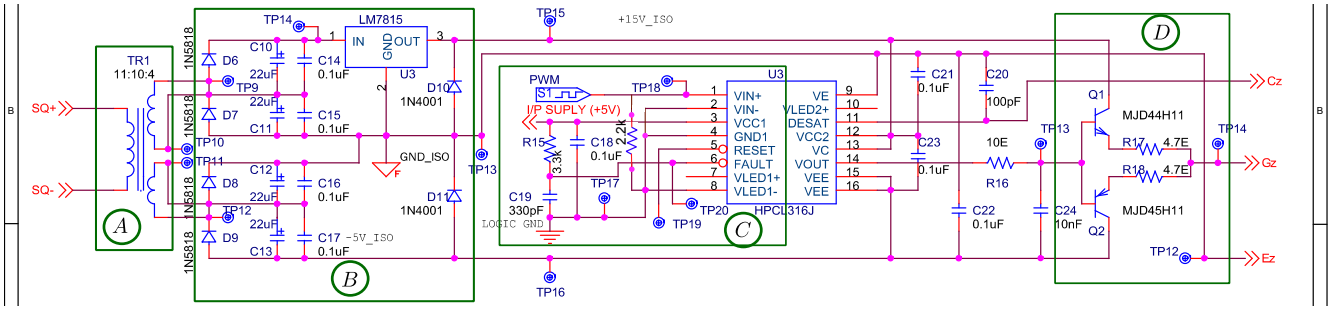



Fig. 1. Schematic of one channel of the gate drive. The sections identified are: (A) High frequency transformer for isolation; (B) Isolated power supplies for the gate drive card; (C) Primary side of the gate driver powered with +5V non-isolated supply with signal or controller ground; and (D) output peak current boosters.

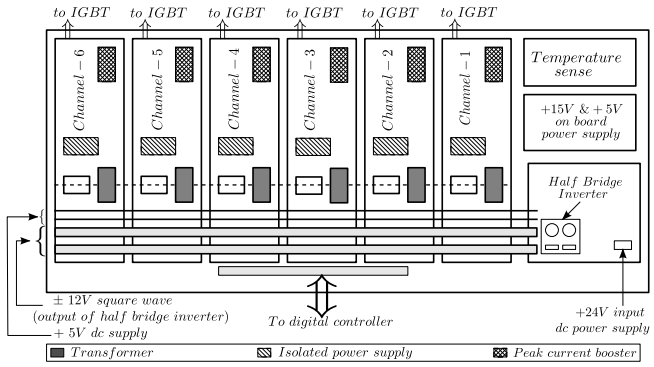



Fig. 2. Block diagram of the gate drive card for a $3-\phi$ 3 leg inverter.

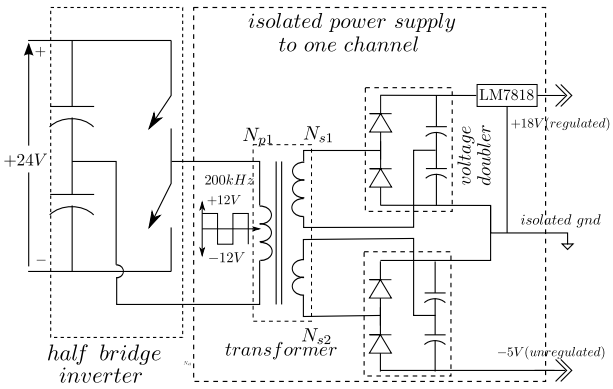



Fig. 3. Schematic showing the isolated power supply for a channel of the gate drive card.

including the gate resistor, with a peak current capacity of 8 $A$. To increase peak gate current of 8 $A$ npn/pnp switching transistor buffer is used. This allows the gate drive card to be used in the design of high power inverters. Schematic of one channel of the designed gate drive card is shown in Fig. 1.

## III. Power Supply

Isolated power supplies can be provided using switched mode power converters. With increasing converter switching frequency, the size of the magnetic circuit and output charge reserve capacitor comes down. Though wide varieties of switched mode power converters are possible each has its own merits and limitations. Fly back converter is simple and has less number of components compared other types of converters. Such converters are used in many cases where the requirement is for low power of less than 10 $W$, with isolation. It suffers from inevitable higher voltage stresses across the switches and produces switching noise because of ringing across the diodes. Providing many power supplies using fly back converters is not advisable. Such need exists in poly-phase inverters for 3 wire and 4 wire applications. Another option, that is investigated in this paper, is to generate many isolated power supply channels with in a small area is using high frequency AC square wave voltage source and small toroidal ferrite transformers.

*1) High frequency inverter:* For the designed gate drive card, a 200 $kHz$ half bridge inverter has been designed to power all the gate drive channels. The use of the half bridge topology ensures that there is no chance of saturation in the core of transformers as there is no path for circulating DC current. Using a small toroidal transformer of less than 16 $mm$ outer diameter, with one primary and two secondary windings has been designed to supply dual voltages at 4 $W$ power level. A high level schematic of the isolated power supply based on a half-bridge inverter is shown in Fig. 3. The secondary low voltage side of the power supply consists of a voltage doubler circuit, which requires fewer turns and with a single diode drop in the circuit path. Gate turn on and turn off voltage levels can be adjusted easily by changing number of secondary turns of the transformer. For additional isolated power supply channels only the high frequency transformer and the diodes on the secondary are duplicated. Hence, only two active switches are required for generating isolated supplies for all the channels of a poly-phase inverter.

### A. Design of the Transformer

The high frequency transformer core selection has been done based on area product calculation [6],

$$A_c A_w = \frac{VA}{4 f B_m k_w J} \quad (in\ mm^4) \tag{1}$$

where

| | | |
|---|---|---|
| $VA$ | : | transformer volt ampere rating ($8\ VA$) |
| $f$ | : | frequency of operation ($200\ kHz$) |
| $B_m$ | : | peak operating flux density ($0.1\ T$) |
| $k_w$ | : | window factor ($0.05$) |
| $J$ | : | current density of ($2.2\ A/mm^2$) |

A low value of window factor, with $k_w$ taken to be $0.3$ is used in this case because PVC coated stranded conductors are for achieving high voltage isolation levels. These conductors area is approximately $4$ times the bare copper conductor area. A small plastic partition of width $0.5\ mm$ is used to physically separate the primary and secondary windings, again to obtain adequate creepage distance between the windings. This partition also occupies an area of window that is comparable to the windings because of very small core size used in this application. Isolation voltage between primary and secondary is greater than $1.55\ kV$ peak with a minimum air gap of $0.5\ mm$ at all points along the isolation barrier in the power supply channels. Calculated transformer area product is $909\ mm^4$, EPCOS $R15{\times}10.4{\times}5.3$ ferrite core is selected. It has an area product of $1023\ mm^4$ and area of cross-section of $12.05\ mm^2$.

To select the primary winding turns, $N_{p1}$, a $10\%$ drop in $V_1$ has been considered assuming that the leakage inductance of primary winding is be around $10\%$. Two isolated dc supplies are derived using voltage doublers. A linear regulator has been used for positive supply of $+15\ V$ in each channel. An unregulated negative supply from the second voltage doubler has been used for the negative bias of $-5\ V$ for each gate drive channel. Unregulated input voltage to the linear regulator should be at least $3V$ higher than that of its output. This is used to obtain the turns requirement of the secondary windings.

$$\begin{aligned} V_s &= \frac{dc\ output, V_{dc}}{2} + Diode\ drop, V_D \\ V_{s1} &= \frac{18V}{2} + 0.5V = 9.5\ V \\ V_{s2} &= \frac{5V}{2} + 0.5V = 3\ V \end{aligned} \tag{2}$$

Number of turns are,

$$\begin{aligned} N_{p1} &= \frac{V_{p1}}{4 f B_m A_c} \approx 11 \\ N_{s1} &= \frac{V_{s1}}{4 f B_m A_c} \approx 10 \\ N_{s2} &= \frac{V_{s2}}{4 f B_m A_c} \approx 3 \end{aligned} \tag{3}$$

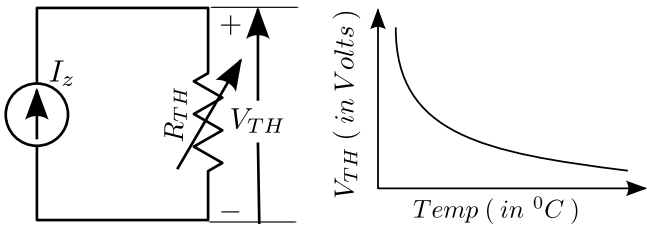



Fig. 4. Principle of thermistor based temperature sensor, with a look up table used for the dependence of the resistance with temperature.

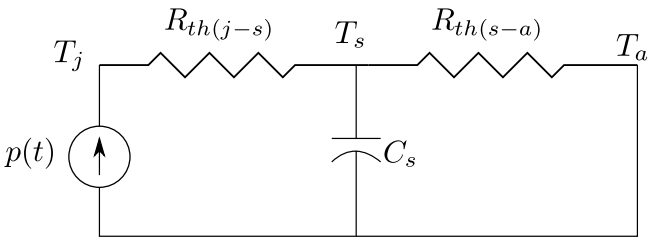



Fig. 5. Modelling of the semiconductor module and heat sink of a power converter to obtain the junction temperature.

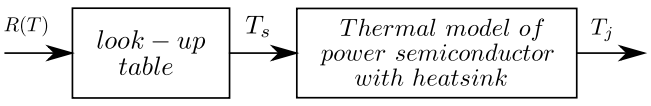



Fig. 6. Thermistor based thermal protection. The voltage $V_{TH}$ is used to calculate the power device junction temperature.

## IV. Thermal Protection

In addition to over-current protection, the power converter needs to shut down in case the junction temperature exceeds the semiconductors rated maximum level of $150^0C$. It is common to sense the heat-sink temperature, or power semiconductor device case temperature when such as option is available, and to use it as a scaled estimate of the junction temperature and to initiate converter shut down.

If temperature sensors such as thermocouples and RTD are used, the noise generated during the switching operation of the power converter will corrupt the small voltage levels of these sensors easily. Hence, for satisfactorily temperature sensing in such inverter environments,

a sensor with high signal level is advantageous. In spite of non-linear resistance variation with temperature, thermistor based temperature sensors can serve well in this situation because of its high sensitivity to temperature. Modern power semiconductor modules available today are having thermistors embedded inside the module with double bonded copper insulation [7], [8]. A constant current source and thermistor based temperature sense circuit, as shown in Fig. 4, has been used in the gate drive circuit. By driving small current of the order of 1 $mA$ through the thermistor and monitoring the voltage across its terminals, it is possible to extract the temperature information at the base plate of the power semiconductor module. This can be considered to be the case temperature, $T_c$, of the module. Temperature of the heat sink of the inverter can be found using external thermistor mounted on the heat sink. Once this information is made available to the processor, from the heat sink modelling and resistance-temperature profile of the thermistor, fast temperature information can be obtained, which can be used on a sub-cycle basis for thermal protection.

Referring to the thermal model of the semiconductor device and heat sink arrangement shown in Fig. 5, $T_j$ is the junction temperature of the device and $T_s$ is the heat sink temperature. $R_{th(j-s)}$ is junction to heat sink thermal resistance. $R_{th(s-a)}$ is heat sink to ambient thermal resistance. From the resistance information of the thermistor $R(T)$ and using a look-up table, temperature of the case $T_c$, or heat sink $T_s$, can be obtained. From the thermal model of the heat sink, the junction temperature of the module is as given in eq.(5).

The resistance of the thermistor can be modelled as,

$$R(T) = R_0 e^{B(\frac{1}{T} - \frac{1}{T_0})} \tag{4}$$

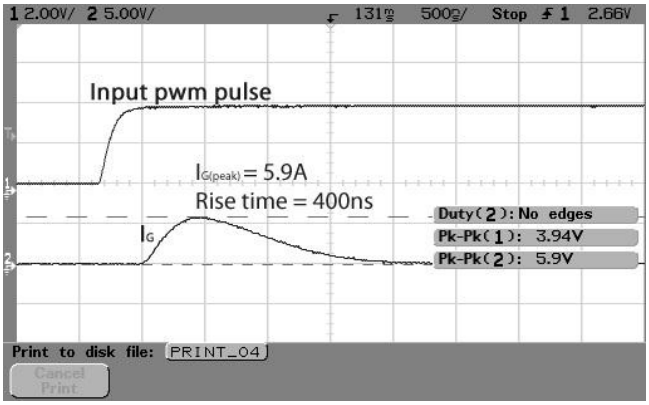
Where $R(T)$ is resistance of the thermistor at a temperature of $T$ degrees $K$, $R_0$ is resistance of the thermistor at a temperature of $T_0 K$, and $B$ is a constant specified in datasheet [8].

$$T_j(t) = T_s(t)\left(1 + \frac{R_{th(j-s)}}{R_{th(s-a)}}\right) + C_s R_{th(j-s)} \frac{dT_s}{dt} \tag{5}$$

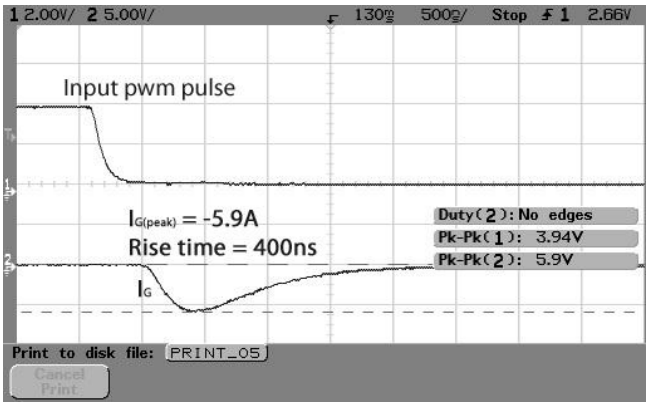
For a given thermistor current bias, the terminal voltage $V_{TH}$ is used with a lookup table to provide a readout of the case temperature as shown in Fig. 6.

## V. Results

The designed gate drive card has been tested for its peak current delivery. With $+15$ $V$ gate turn on voltage and $-5$ $V$ gate turn off voltage, 2 $\Omega$ turn on and turn off gate resistors and with a capacitive load of 470 $nF$ connected to the gate and emitter terminal of the gate drive card by a 10 $cm$ long twisted pair of wires, gate currents have been captured. These results are shown in Fig. 7. The wire impedance prevented the peak gate




(a) Turn-on gate current




(b) Turn-off gate current

Fig. 7. Peak current test on gate drive card. CH1 : Input PWM pulse (2V/div) and CH2 : Gate current, $I_G$ (5A/div) and time: 500 ns/div.

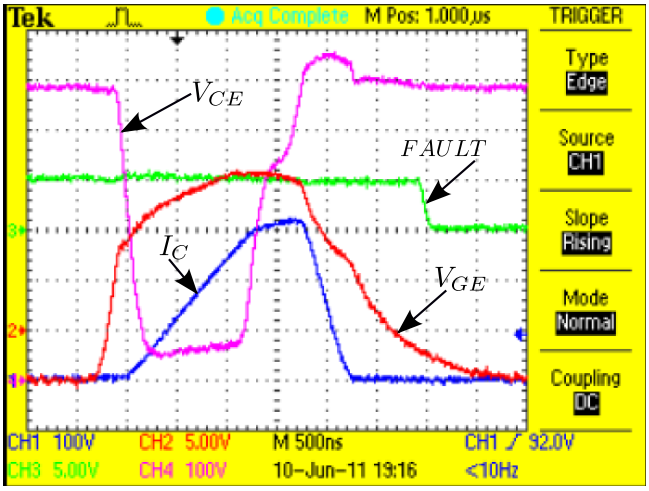
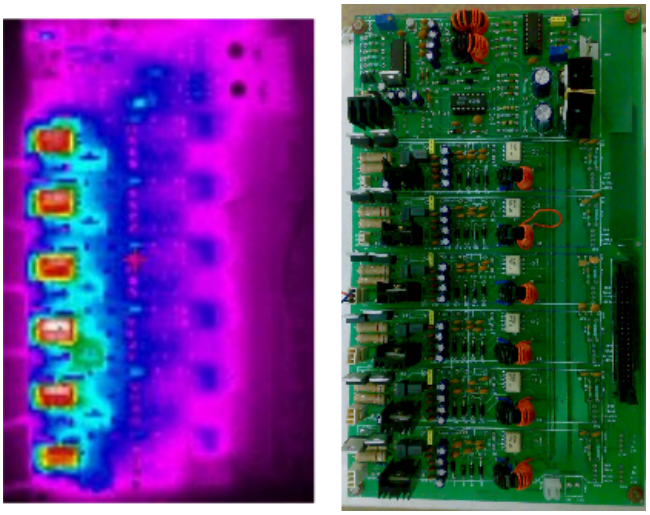
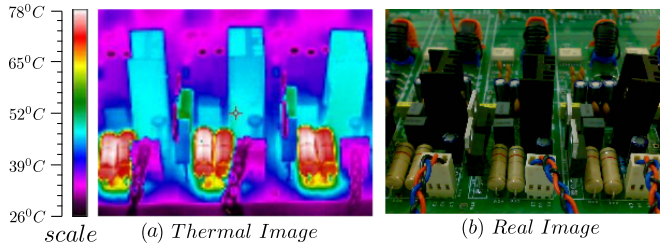



Fig. 8. Short circuit test on a gate drive channel of the designed gated drive card. $V_{CE}$:100V/div, $I_C$:100A/div, $V_{GE}$:5V/div, FAULT:5V/div and time:500 ns/div.



$(a)Thermal\ Image$ $(b)\ Real\ Image$

Fig. 9. Thermal image of the gate drive card during long term endurance tests.




$(a)\ Thermal\ Image$ $(b)\ Real\ Image$

Fig. 10. Thermal image of output booster stage and gate resistor stage of the designed gate drive card during long term endurance tests.

current from reaching $8\ A$. This effect of the lead length is also expected in the practical laboratory packaging of the inverter.

Short circuit test has been performed on the designed gate drive card to test for its functionalities such as desat fault detection, soft turn off during fault shut down. The results of the short circuit test are shown in Fig. 8. To perform this test one leg of the inverter has been operated as a chopper with light RL-load and then it is shorted using mechanical contactor. Duty ratio of the pulses are very low for this case with $T_{on} = 400\ \mu s$ and $T_{off} = 4\ ms$. In Fig. 8 the IGBT on which this test is performed shows the condition where it has been turned on during short circuit conditions. The waveforms indicate that the gate drive card detected the fault after a short blanking time and then cut-off the gate pulse using soft turn off feature. The fault is then notified to the controller using $FAULT$ status by taking the fault output from logic high to low state. The fault and switching tests has been performed with different gate resistors and it is observed that the gate resistor values have a major influence on the turn on and turn off process of the IGBT in terms of

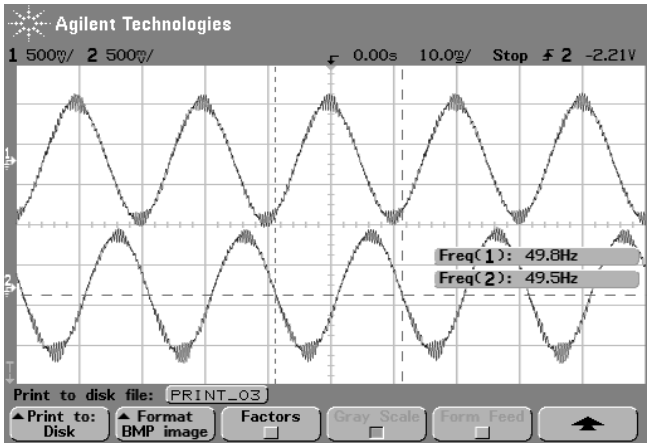



Fig. 11. No-load line current waveforms of a $2.3kW$, $415V$, $4.5A$, $1440rpm$ $\Delta$-connected induction machine used in a $10kW$ inverter with the gate drive card. CH1 and CH2 : $1.735A/div.$, time: $10ms/div.$

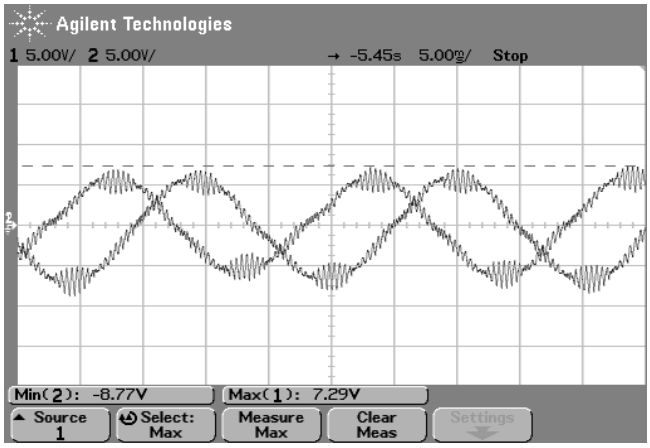



Fig. 12. Line current waveforms of a $22kW$, $415V$, $4.5A$, $1475rpm$ $\Delta$-connected induction machine at $10kVA$ input used in a inverter with the gate drive card. CH1 and CH2 : $17.35A/div.$, time: $10ms/div.$

losses, diode recovery etc. [9].

After continuous operation of the gate drive card for 5 hours while delivering rated power, its thermal image has been captured and the maximum temperature on the card is observed as $76^0C$ at the output stage gate resistors as shown in Fig. 9 and Fig. 10. The remaining parts of the gate drive circuit are at less than $45^0C$ with an ambient temperature of $26^0C$. All other semiconductor ICs junction temperature will be within limits for continuous operation of the designed gate drive card. Test conditions are, $R_{g(on)} = R_{g(off)} = 8.2\ \Omega$ and $300\ nF$ capacitive load was connected using a $10\ cm$ long twisted pair of lead wires. The switching frequency of $21\ kHz$ input is applied to dissipate $2\ W$ power in the gate resistors for the thermal endurance test of the gate drive card.

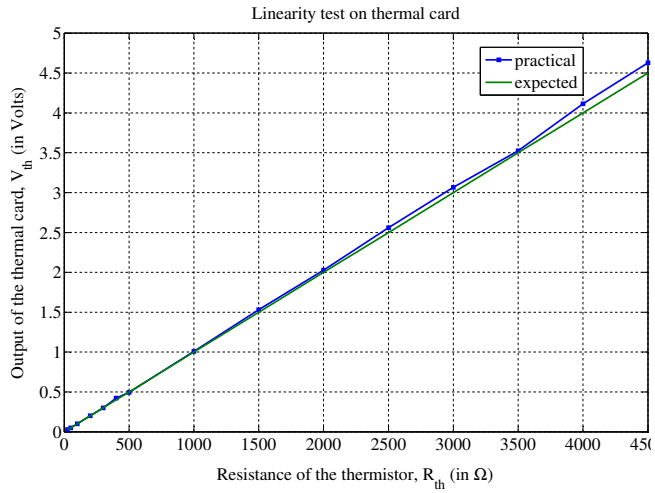



Fig. 13. Linearity test on temperature sensing circuit.

To test the operation of the gate drive card in an inverter circuit, the designed gate drive card has been assembled in a 10 $kVA$ $3-\phi$ 3 leg induction motor drive inverter and the drive is operated in $V/f$ mode to run a 2.3 $kW$ induction machine at no load. Another test was also carried out with a $22kW$ induction machine at 10 $kVA$ power level and switching using conventional space vector PWM technique. The motor current waveforms for the tests are shown in Fig. 11 and Fig. 12 respectively.

Linearity test on temperature sensing circuit has been carried out by connecting an external resistance and output of the temperature sense circuit has been noted. Experimentally measured values of the thermal card are matching with the expected analytical values with a minimum error. A plot of resistance versus output voltage of the temperature sense circuit is shown in Fig. 13.

## VI. Conclusions

A simple and compact isolated power supply has been designed to develop a gate drive card for high power converters using commercially available gate driver optocoupler ICs. The features of the gate driver IC makes it is possible to design the gate drive cards which can compete with the commercially available high performance gate drivers. To provide multiple isolated power supplies in a single PCB within a small area, a high frequency half bridge inverter, small toroidal ferrite transformers, and voltage doublers at the output is seen to be a good choice. The laboratory PCB prototype gate drive card made used of through hole components. The size of the 6 channel gate drive card with thermal monitoring is 32.8 $cm \times 15.5$ $cm$. The size can be further reduced by using surface mounted components. Sensing temperature information of the heat sink and with proper modelling of the heat sink it is possible to estimate the junction temperature of the device with adequate accuracy. Experimental tests on the prototype gate drive card shows that its performance meets the design objectives and it can be used for high frequency high power applications.

## References

[1] A. K. Jain and V. T. Ranganathan, "$v_{CE}$ sensing for igbt protection in npc three level converterscauses for spurious trippings and their elimination," *IEEE Trans. Power Electron.*, 2011.

[2] SEMIKRON, "Gate resistor - principles and applications," Tech. Rep., nov 2007.

[3] "Advanced igbt driver application manual," MICROSEMI Power Products Group, Tech. Rep., jul 2006.

[4] J. C. Crebier and B. D. Nguyen, "Gate driver supplies and dead time management circuits for ac to ac converters," *IEEE Trans. Power Electron.*, 2010.

[5] "Datasheet and application note of hcpl-316j," Tech. Rep.

[6] V. Ramanarayanan, " SMPC E-book," http://www.peg.iisc.ernet.in/people/faculty/vram/.

[7] SEMIKRON, "Application manual for power semiconductor devices."

[8] "Datasheet of semix101gd128ds," Tech. Rep.

[9] R. S. Chokhawala, J. Catt, and B. R. Pelly, "Gate drive considerations for igbt modules," *IEEE Trans. Appl. Ind.*, vol. 31, pp. 603–611, May/Jun. 1995.

[10] PEG, "Document of 10kva converter," Indian Institute of Science, Tech. Rep., 2003.