GDI Technique : A Power-Efficient Method for Digital Circuits

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***Abstract* - Since there is many advancement in VLSI technology and there are many efficient styles of designing VLSI circuits. Some of the styles are CMOS, PTL, GDI (Gate Diffusion Input) techniques. GDI technique helps in designing low-power digital combinatorial circuit by which we can eradicate demerits of CMOS, PTL techniques. This technique allows reducing power consumption, propagation delay, and area of digital circuits while maintaining low complexity of logic design. The different methods are compared with respect to the layout area; transistor count, delay, and power dissipation are discussed here in this paper showing advantages and drawbacks of GDI compared to CMOS style.**

Keywords - ***CMOS, Gate Diffusion Input (GDI), Pass Transistor Logic (PTL), Propagation delay, low-power.***

I. INTRODUCTION

With the intensified research in low power, high speed embedded systems such as mobiles, laptops, etc has led the VLSI technology to scale down to nano regimes, allowing more functionality to be integrated on a single chip. The wish to improve the performance of logic circuits, once based on traditional CMOS technology [6], resulted in the development of many logic design techniques during the last two decades [2, 3]. One form of logic that is popular in low-power digital circuits is pass-transistor logic (PTL). Formal methods for deriving pass-transistor logic have been presented for nMOS. They are based on the model, where a set of control signals is applied to the gates of nMOS transistors. Another set of data signals are applied to the sources of the n-transistors. The PTL (Pass Transistor Logic) is most popular for low power digital circuits. Some of the main advantages of PTL over standard CMOS design are 1) high speed, due to the small node capacitances; 2) low power dissipation, as a result of the reduced number of transistors; and 3) lower interconnection effects due to a small area. But the implementation of PTL has two basic problems: 1) slow operation at reduced power supply as the threshold voltage drop across the single channel pass transistor results in low drive current, 2) the high input voltage level at the regenerative inverter is not Vdd, the PMOS device in the inverter is not fully turned OFF and hence direct path static power dissipation is significant. GDI is a technique which is suitable for design of fast, low power circuits using reduced number of transistors compared to traditional CMOS design and existing PTL techniques.

II. BASIC GDI CELL

The GDI method is based on the use of a simple cell as shown in Fig. 1.

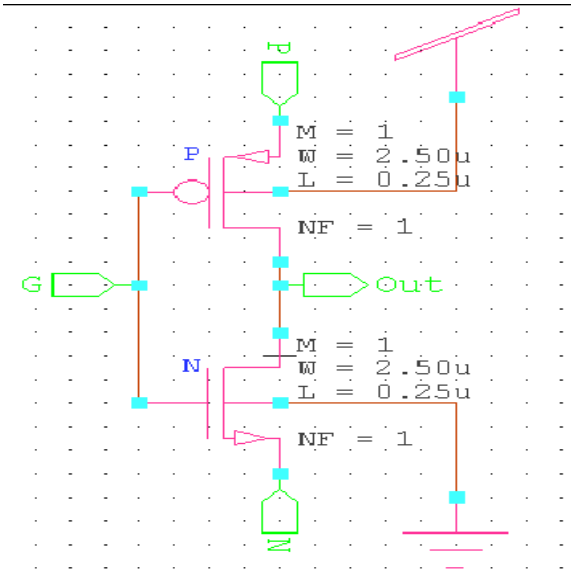


Fig. 1 : Basic GDI Cell

At first glance, the basic cell reminds one of the standard CMOS inverter, but there are some important differences [1].1) The GDI cell contains three inputs: G (common gate input of nMOS and pMOS), P (input to the source/drain of pMOS), and N (input to the source/drain of nMOS). 2) Bulks of both nMOS and pMOS are connected to N or P (respectively), so it can be arbitrarily biased at contrast with a CMOS inverter. The GDI cell structure is different from the existing PTL techniques. It must be remarked that not all of the functions are possible in standard p-well CMOS process but can be successfully implemented in twin-well CMOS or silicon on insulator (SOI) technologies.

TABLE I

BASIC FUNCTIONS USING GDI CELL

N	P	G	OUTPUT	FUNCTION
0	1	A	A’	INVERTER
0	B	A	A’B	F1
B	1	A	A’+B	F2
1	B	A	A+B	OR
B	0	A	AB	AND
C	B	A	A’B+AC	MUX
B’	B	A	A’B+B’A	XOR
B	B’	A	AB+A’B’	XNOR

III. ADVANTAGES OF GDI

It can be seen that large number of functions can be implemented using the basic GDI cell. MUX design is the most complex design that can be implemented with GDI, which requires only 2 transistors, which requires 8-12 transistors with the traditional CMOS or PTL design. Many functions can be implemented efficiently by GDI by means of transistor count. Table 2 shows the comparison between GDI and the static CMOS design in terms of transistors count. It can be seen from table II that using GDI technique AND, OR, Function1, Function2, XOR, XNOR can be implemented more efficiently. However to implement NAND, NOR it requires 4 transistors as that in Static CMOS design. NAND and NOR the universal logic gates, any Boolean Function can be implemented using these gates, are most very efficient and popular with static design style. Function1 and Function2 are universal set for GDI, and consists of only two transistors, compared to NAND and NOR. These functions can be used synthesize other functions more effectively than NAND and NOR gates.

TABLE II

COMPARISON OF TRANSISTOR COUNT OF GDI AND STATIC CMOS

FUNCTION	GDI	CMOS
INVERTER	2	2
F1	2	6
F2	2	6
OR	2	6
AND	2	6
MUX	2	12
XOR	4	16
XNOR	4	16
NAND	4	4
NOR	4	4

IV. COMPARISON WITH OTHER LOGIC STYLES

A. Digital Circuits

Some of the digital circuits are implemented using 0.35µm CMOS process and the comparison of carried out between the standard CMOS logic and GDI Technique. The percentage of power consumed with respect to standard CMOS and transistor count are mentioned in table III.

TABLE III

B. 8-bit Comparator

Digital circuit	Power consumed by GDI with respect To CMOS	Transistor Count GDI	Transistor Count CMOS
Ripple Carry Adder	70.4	72	168
Carry Bypass Adder	83.11	88	230
Carry Look Ahead Adder	73.02	80	208
Carry Select Adder	78.61	122	294
Binary Array Multiplier	81.67	296	600

The 8-bit Comparator is implemented using 1.6µm CMOS process [4]. The comparison is carried for GDI technique, Standard CMOS process and NMOS pass gate. It is seen that GDI provides the best performance among the all, as it can be seen in Table, all 3 circuits are implemented 96 transistors.

TABLE IV

COMPARISON OF GDI, CMOS AND N-PG 8-BIT COMPARATOR

Logic Style	CMOS	GDI	N-PG
Power(in mW)	1.82	1.4	13.87
Number of transistor	96	96	96

C. 4-bit Multiplier

The multiplier is implemented using 0.5µm CMOS technology with 3.3V supply voltage. Comparison results are shown in table V. 26 transistors are used in GDI technique while 44 Transistors are used in standard CMOS.

TABLE V

COMPARISON OF GDI, CMOS 4-BIT MULTIPLIER

Logic Style	CMOS	GDI
Power(in mW)	1.265	0.3079
Number of Transistors	44	26

D. XOR Gate

XOR Gate is implemented using 180nm technology and the comparison is done among Complementary Pass Transistor Logic (CPL), Dual Pass Transistors (DPL), standard CMOS and GDI Techniques and results are mentioned in table. Among all the implemented techniques GDI consumes least power and the least number of transistors. 23.93 micro Watts is consumed by standard CMOS, power consumed by different techniques is mentioned with respect to standard CMOS technique.

TABLE VI

COMPARISON OF GDI, CMOS, CPL AND DPL XOR GATE

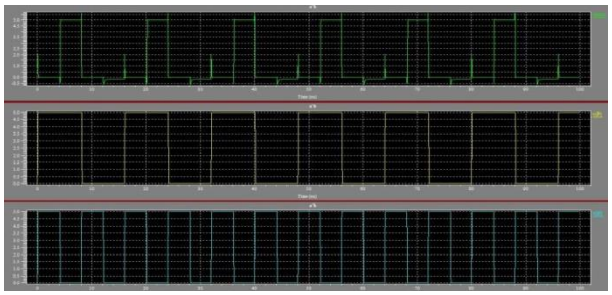
Logic Style	CMOS	CPL	DPL	GDI
Percentage Power Consumed with respect to CMOS	100	107.35	43.96	27.12
Number of Transistor	16	8	10	4

V. SIMULATION AND RESULTS

Basic GDI Functions have been simulated using SPICE and the simulated outputs are show in below. These are the outputs of Basic GDI Cell without employing any level restoring circuits at their outputs. It can be seen that the outputs are within the range of noise margin to predict the correct output of the logic implemented by the Basic GDI cell. The simulation results of few functions as listed in Table are shown in figure 2. Figure 3 denotes logic circuit comparison based on CMOS and GDI implementation.

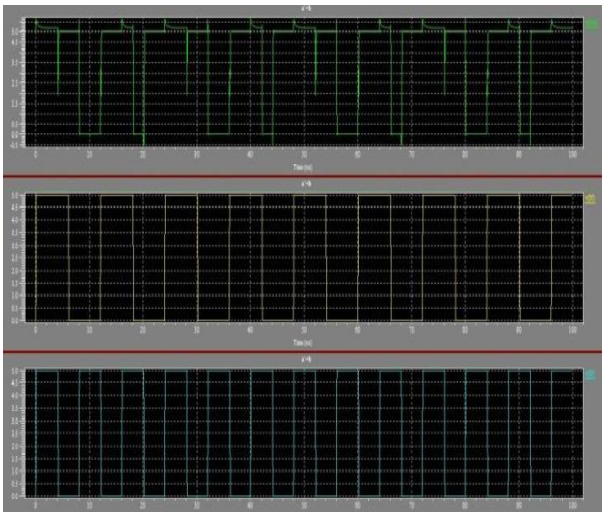
VI. CONCLUSION

A novel GDI technique for low-power design was presented. Comparisons with existing TG and N-PG techniques were carried out, showing an up to 45% reduction of power-delay [7] product in the test chip in GDI over CMOS and significant improvements in performance. GDI will allow high density of Fabrication as now a day's chip area is very important parameter [3, 6]. The GDI technique allows use of a simple and efficient design algorithm, based on the Shannon expansion. It makes GDI suitable for synthesis and realization of combinatorial logic in real LSI chips, while using a single-cell library. This proves to be an additional advantage of GDI over CMOS and PTL. Implementations of GDI circuits in SOI or twin-well CMOS processes are expected to supply more power-delay efficient design, due to the use of a complete cell library with reduced transistor count.

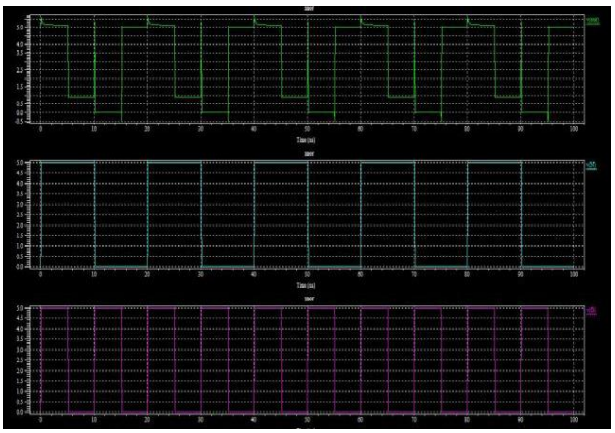


(A) OUTPUT OF F1

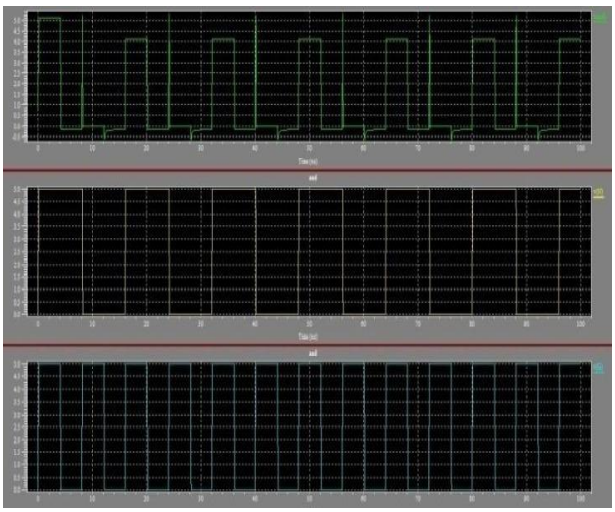
(B) OUTPUT OF GDI OR



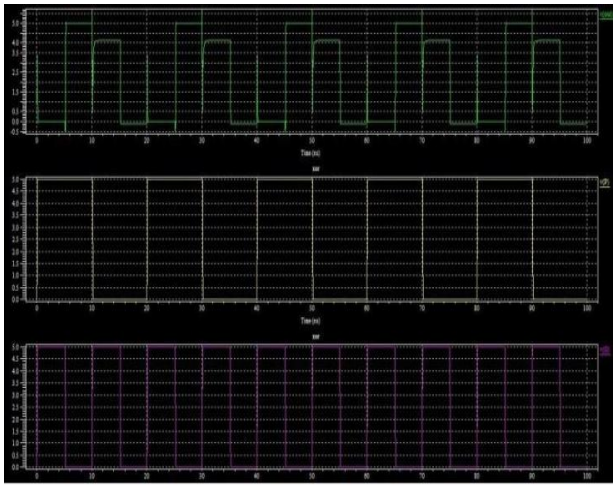
(C) OUTPUT OF F2



(D) OUTPUT OF GDI XNOR



(E) OUTPUT OF GDI AND



(F) OUTPUT OF GDI XOR

FIG. 2: GDI IMPLEMENTATION OF DIFFERENT GATES

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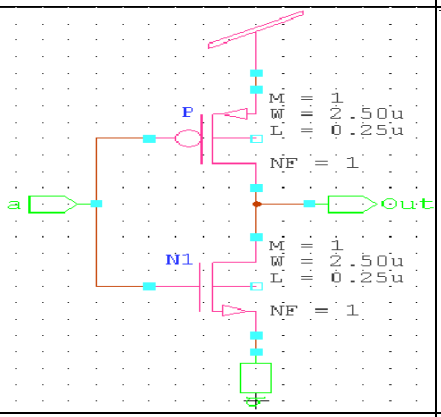
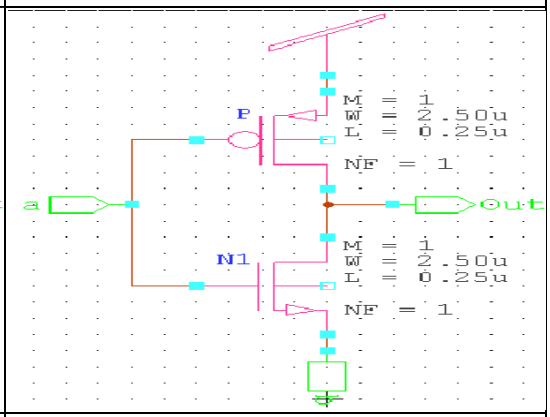
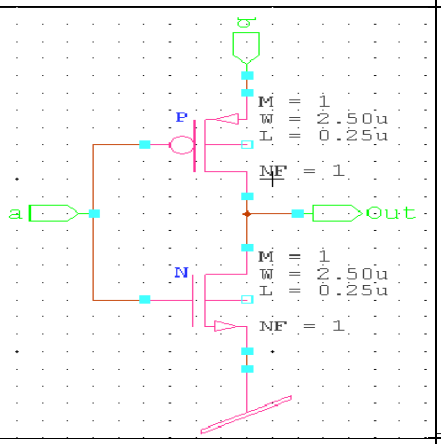
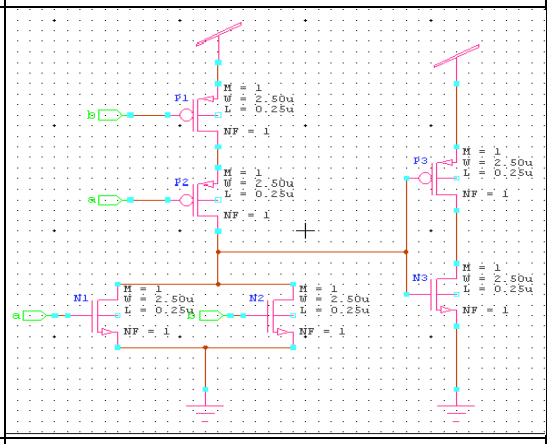
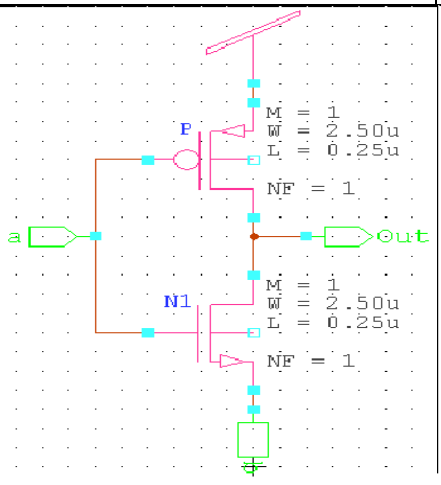
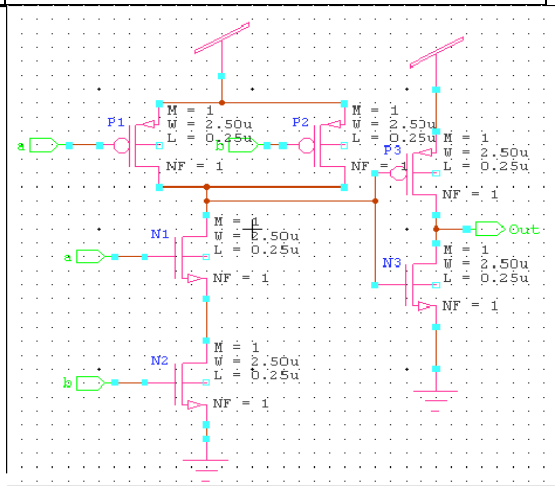
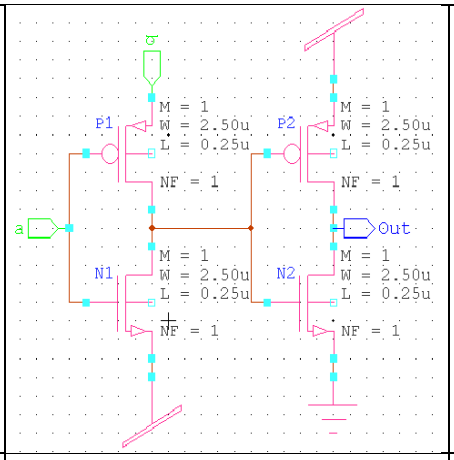
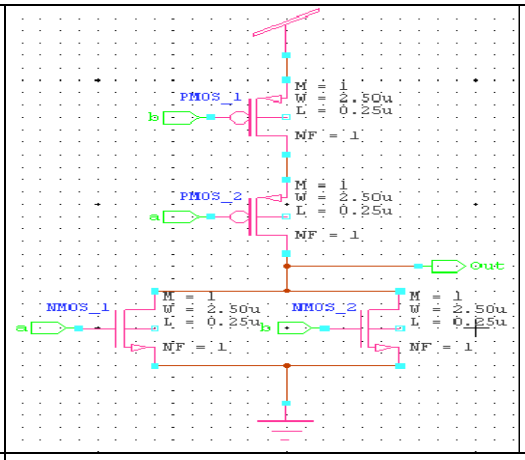
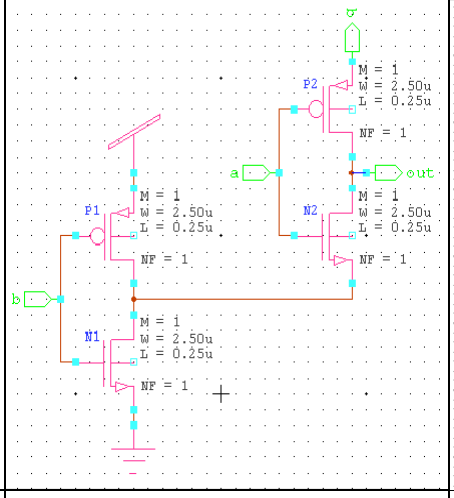
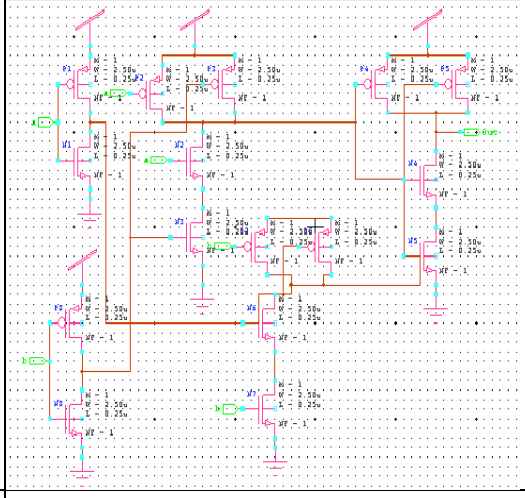
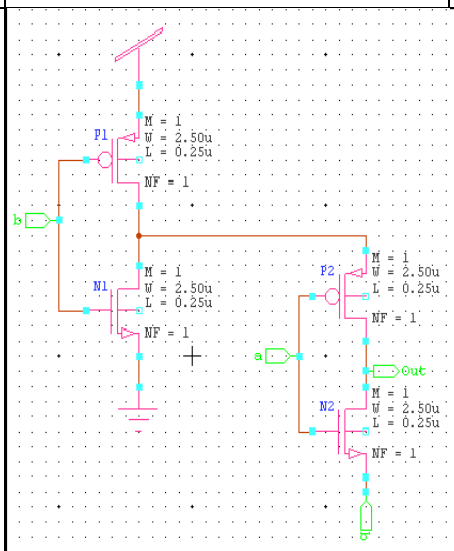
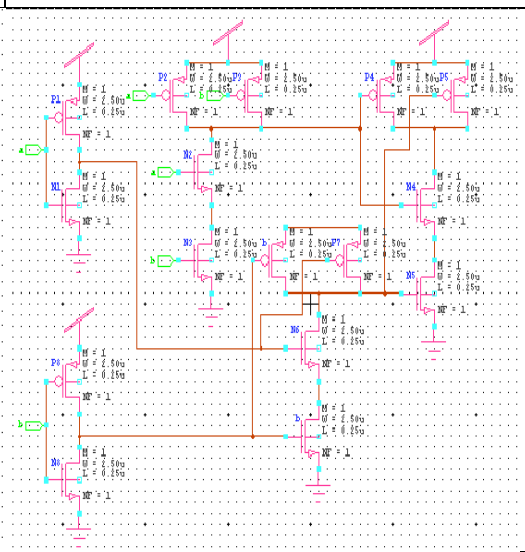
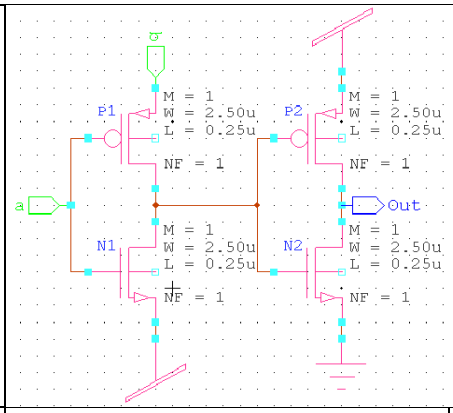
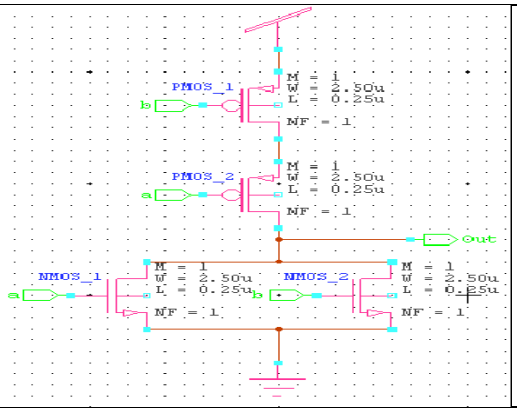
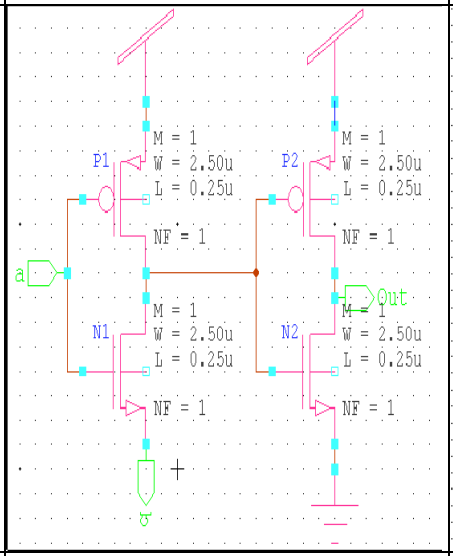
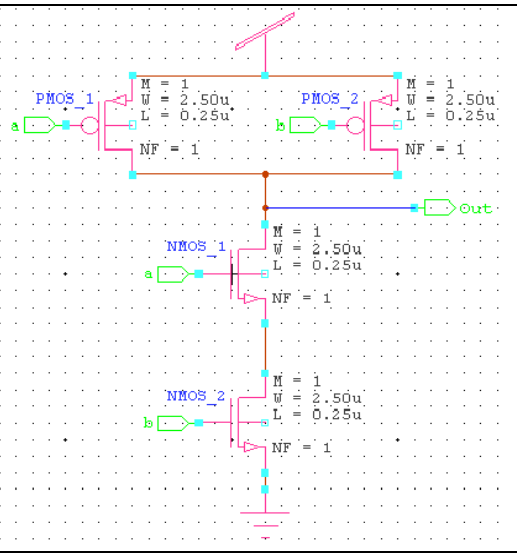
	GDI	CMOS
INVERTER		
	FIG. 3(A)	FIG. 3(B)
OR		
	FIG. 3(C)	FIG. 3(D)
AND		
	FIG. 3(E)	FIG. 3(F)

NOR		
	FIG.3(G)	FIG.3(H)
XOR		
	FIG.3(I)	FIG.3(J)
XNOR		
	FIG.3(K)	FIG.3(L)

NOR		
	FIG.3(M)	FIG.3(N)
NAND		
	FIG.3(O)	FIG.3(P)

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