Generating a Voltage-Dependent Sinusoidal Signal from a Linear Ramp Input using a Folding Amplifier for IEEE Design Challenge

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Abstract

A folding amplifier can be used to generate a voltage-dependent sinusoid from a linear ramp input for 0 [V] to 1 [V]. The output of the system will result in a sinusoid with a peak-to-peak voltage of, in this case, 2 [V]. The circuit consists of 4 major stages, the folding amplifier, the level-shifter, the differential amplifier, and the current sources. Each stage was built using only ALD1101 and ALD1102 transistors, as requested in the IEEE challenge, but not required by the MSD class. The circuit written about in this paper produces an output with a peak-to-peak voltage of 1 [V] centered around 0.5 [V] instead of a peak-to-peak voltage of 2 [V] centered around 0 [V].

I. Theory

The IEEE design challenge instructed students to build a circuit that would create the following output, shown in figure 1, given a linear ramp input. Figure 1 appears to be a sinusoid with a peak-to-peak voltage of $2V_0$, that crosses the x-axis at V_1, $2V_1$, $3V_1$, and $4V_1$. In the case of circuit I will be designing under the idea that V_1 is equal to 0.25 [*V*]. This means that the circuit will use an input ramp that goes from 0 [V] to 1 [V].

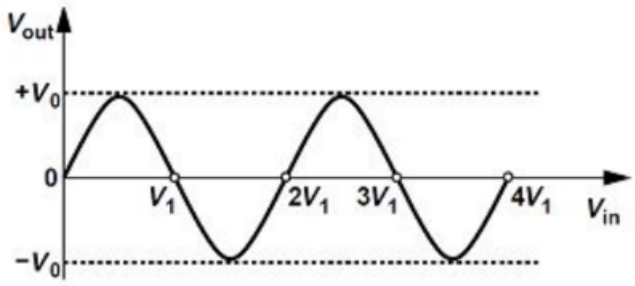

Figure 1: *IEEE Design Challenge Desired Output Waveform*

This can be created using a folding amplifier utilizing 5 MOS differential pairs. A differential pair exists when the sources and substrates of 2 NMOS or PMOS are tied together, their gates are receiving 2 separate inputs and their drains produce different outputs depending on the input at their gates. These are often seen in differential amplifiers and operational amplifiers, in order to amplify differential AC signals or sinusoidal DC signals.

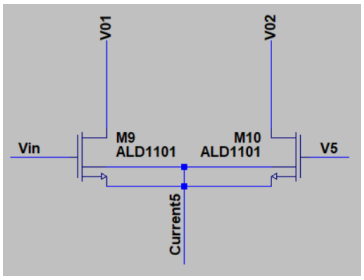

Figure 2: *NMOS differential pair used in Folding Amplifier*

In our case, our differential pairs will have our input voltage ramp going into the gate of one NMOS and a static DC value going into the other gate. This will ensure that the output voltages will switch once the ramp reaches a DC Value equal to the static DC value of the other NMOS. In our cases, we want the values to switch at 0, ¼, ½, ¾, and 1 [V]. We pick these values because the point at which both inputs are equal will become the point where the amplifier will cross the V_{in} axis shown in Figure 1. In our case, the components will be shifted to 0.5 [V].

The folding amplifier shown below in figure 4 shows the general form of the folding amplifier. The drain of the output of every odd numbered MOSFET (M1, M3, M5, M7) will always be falling from a higher potential to a lower potential and thus, every even numbered MOSFET (M2, M4, M6, M8) will be rising from a lower potential to the higher potential. In order to create a sinusoidal signal as a result, the drains of M1, M4, M5, and M8 need to be combined to form one sinusoid and M2, M3, M6, and M7 need to be combined to form the other. The differences of each sinusoidal signal is that they have reversed polarity. M1 will begin to increase as V_{in} gets closer to V_{ref1} until it has reached saturation. That same signal will begin to decrease as V_{in} gets closer to V_{ref2}, as it is connected to the drain of M4. This will be the same for M5 and M8. The exact opposite is true for M2 and M3, as well as M6 and M7.

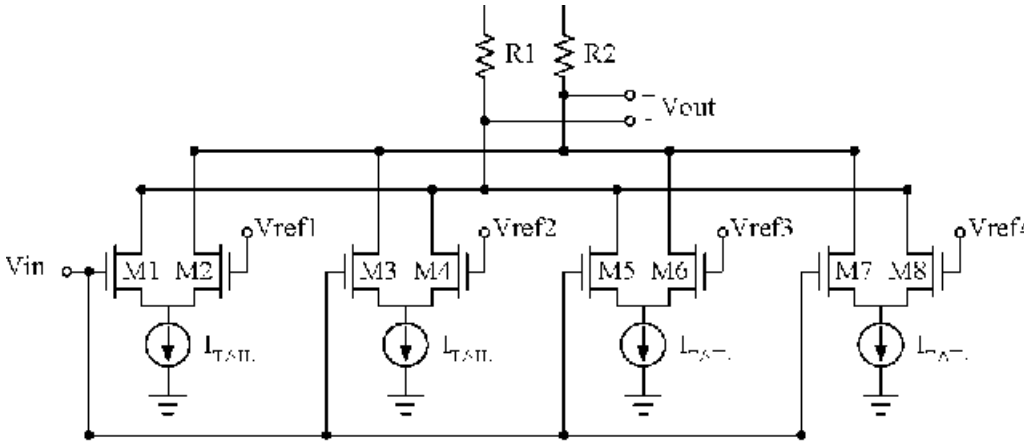

Figure 3: *Generic Folding Amplifier using 4 Differential Pairs* [1]

If MOSFETs were completely ideal, the output would look like a triangle wave as opposed to a sinusoid, as each MOSFET would perfectly linearly increase and linearly decrease. Due to properties of the MOSFET, this is not the case and the MOSFET will produce a signal that looks similar to a sinusoidal signal, as shown below in Figure 4.

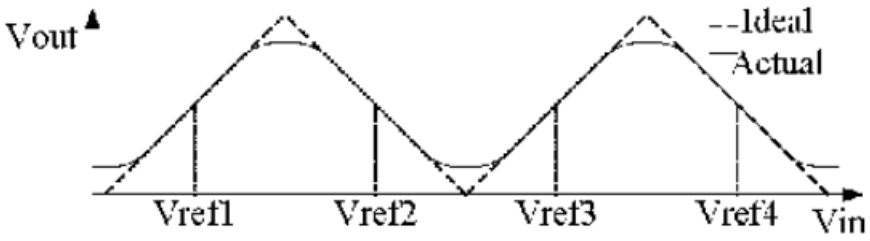

Figure 4: *Ideal and Actual output of Folding Amplifier shown in Figure 3* [1]

The reason we need 5 MOS pairs instead of 4 is because we want the input and output of our amplifier to being centered as opposed to beginning at the lowest potential and ending at the lowest potential. The 5 MOS differential pairs are shown below as simulated using LTSpice.

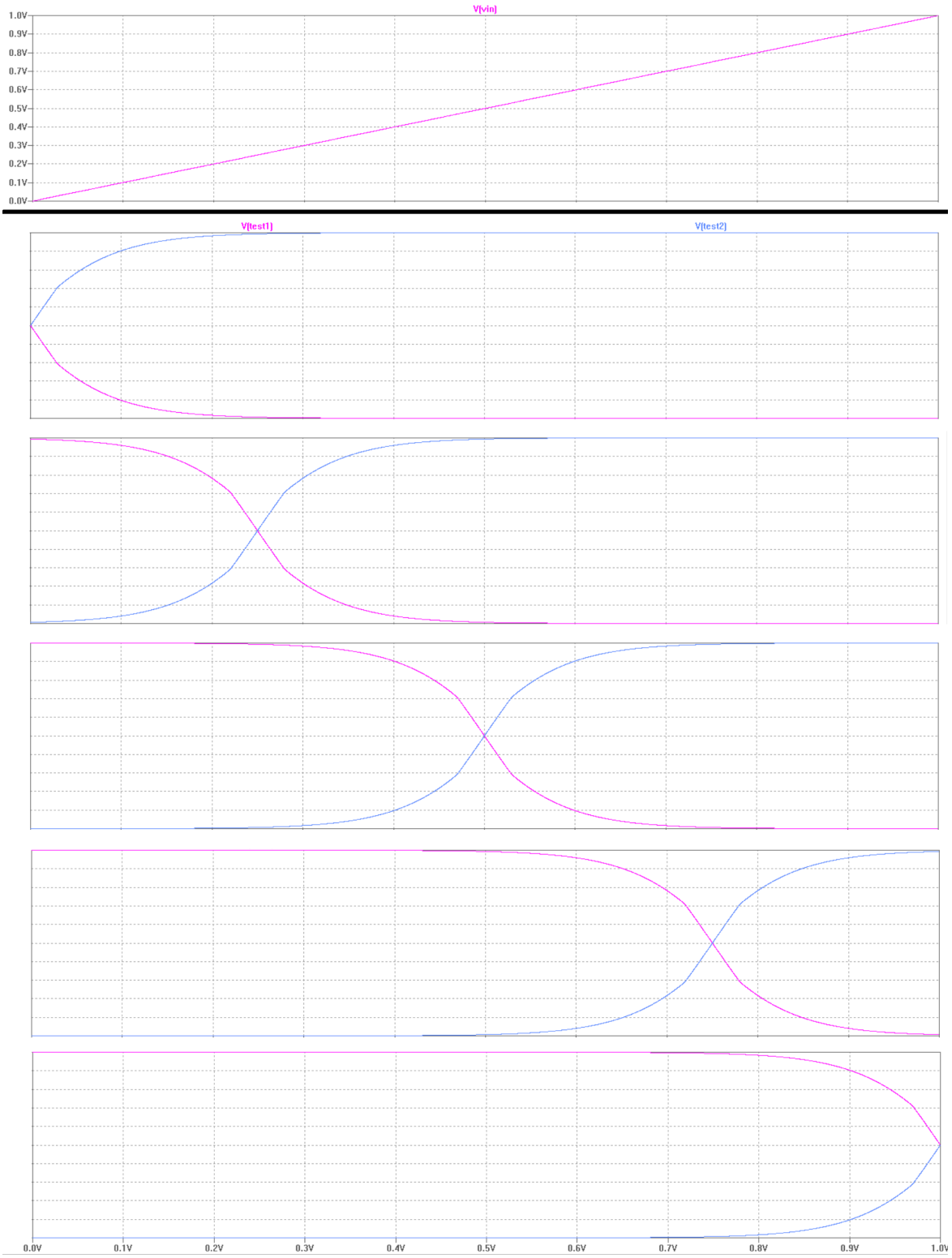

Figure 5: *The Outputs of 5 NMOS Differential Pairs*

The static DC reference voltages that are used and easily generated by putting 4 resistors in series between V_{dd} and ground. Each node created between the resistors will create a reference voltage that is equal to the previous node minus ¼ [V]. This means we can generate reference voltages of ¼, ½, and ¾ [V] with no issues, as shown in figure 6 below.

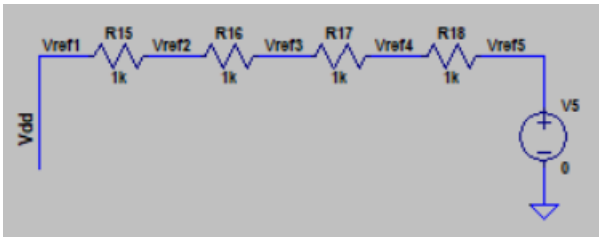

Figure 6: *Generating Reference Voltages using resistors in series, Vref1 =1 [V], Vref2 = 0.75 [V], Vref3 = 0.5 [V], Vref4 = 0.25[V], Vref5 = 0 [V]*

After using 5 differential pairs, we should have 2 sinusoidal signals on each of the output drain connections. The sinusoidal signals should have the same peak-to-peak voltage and should have opposite polarity. These signals will then be level shifted such that they are centered around, ideally 0 [V], but in the case of my circuit they should be centered around 0.5 [V] or 500 [mV]. This was done because I did not originally have a negative voltage rail to begin with, so the circuit was tested from 0 [V] to 1 [V] instead of -1 [V] to +1 [V]. After I acquired a negative voltage rail, I didn't level shift to 0 [V] and kept it level shifted at 0.5 [V].

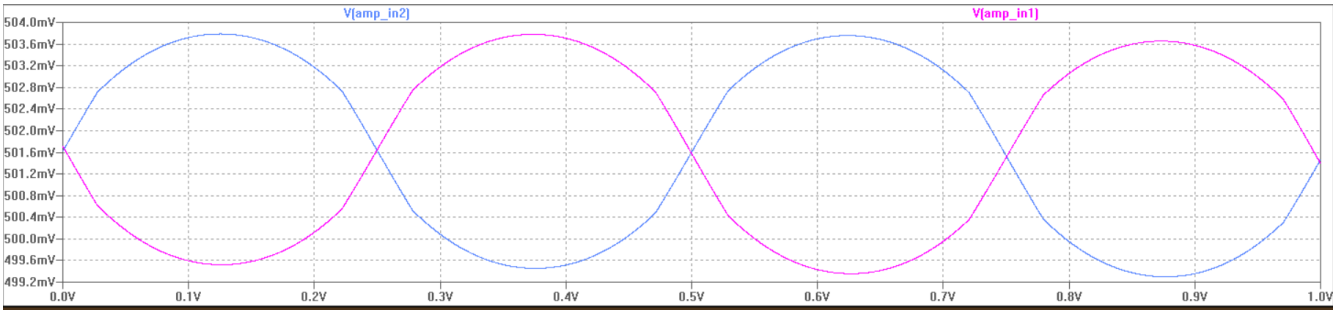

Figure 7: *Differential Output Signal of Folding Amplifier level shifted to around 502 [mV]*

The only thing left is to amplify the 2 signals generated from the folding amplifier using a differential amplifier or an operational amplifier. As we were only working using 1 [V] originally, there was no need for a 2nd stage to the differential amplifier or the use of an operational amplifier. My goal was to use only the ALD1101 and ALD1102 parts that were allowed in the challenge, despite the class allowing us to use other parts.

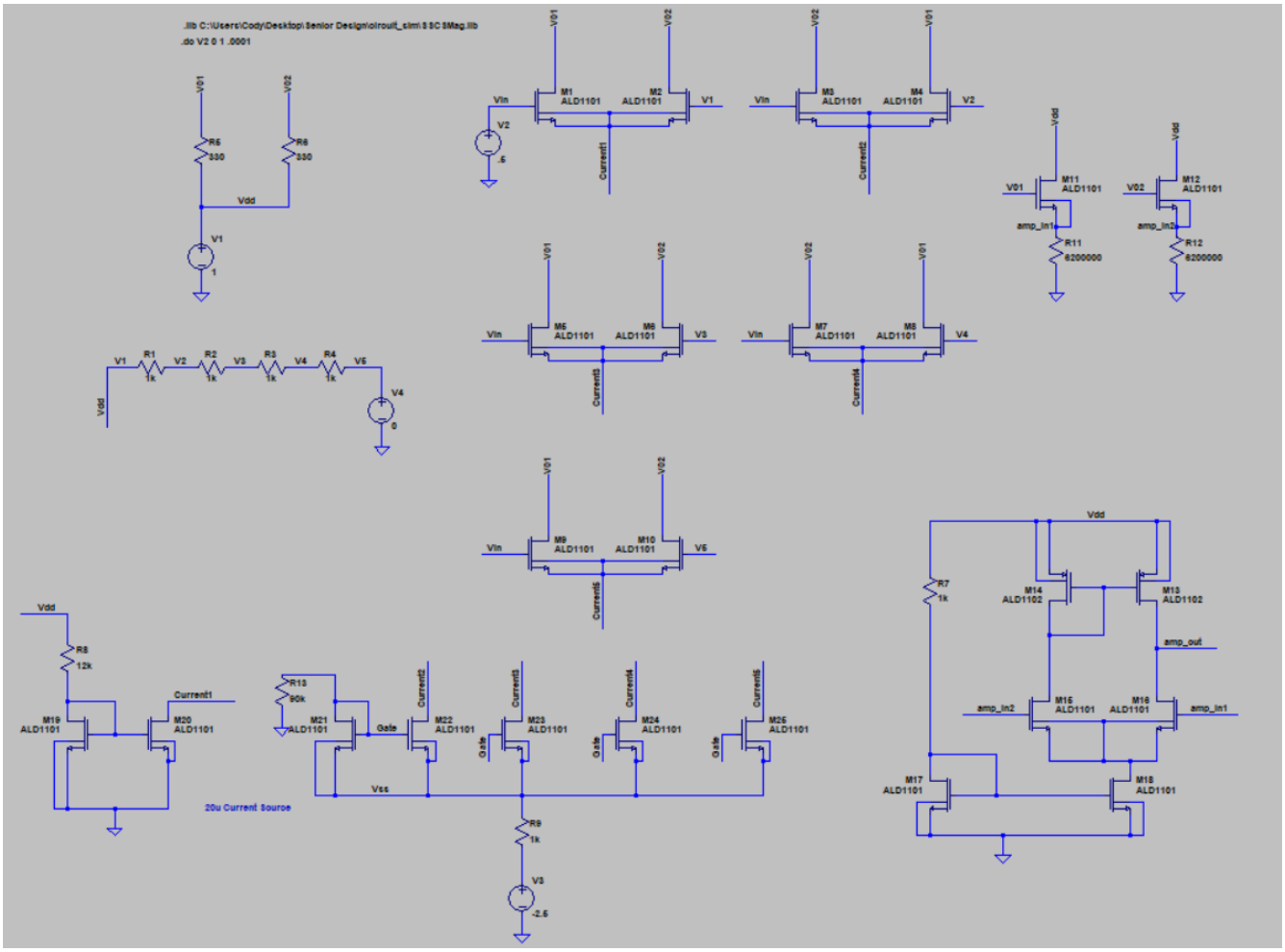

Figure 8: *The Final Circuit of the Folding Amplifier*

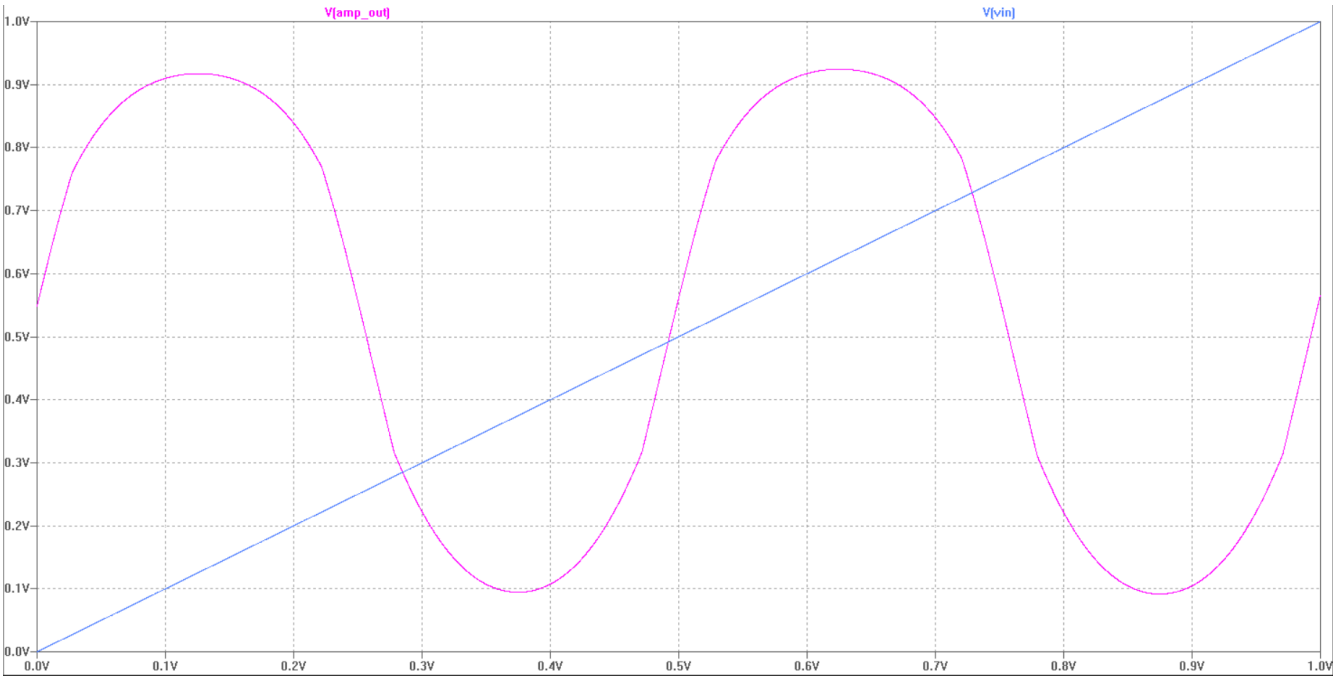

Figure 9: *The Output (purple) and Input (blue) of the Circuit*

As shown above, the circuit has an output swing of about 100mV from Vdd to ground and is centered around around 550 [mV], due to needing a very specific resistor for the level shifter. Unlike the requirement of a $2V_0$ peak-to-peak output voltage, this circuit only has a V_0 peak-to-peak voltage, but has a relatively clean sinusoidal output.

The -2.5 [V] source shown in Figure 8 was generated using the LT1617 – 1, which takes our Vdd input and generates a negative voltage using an internal clock and external capacitors and inductors. This circuit is shown in figure 10 below.

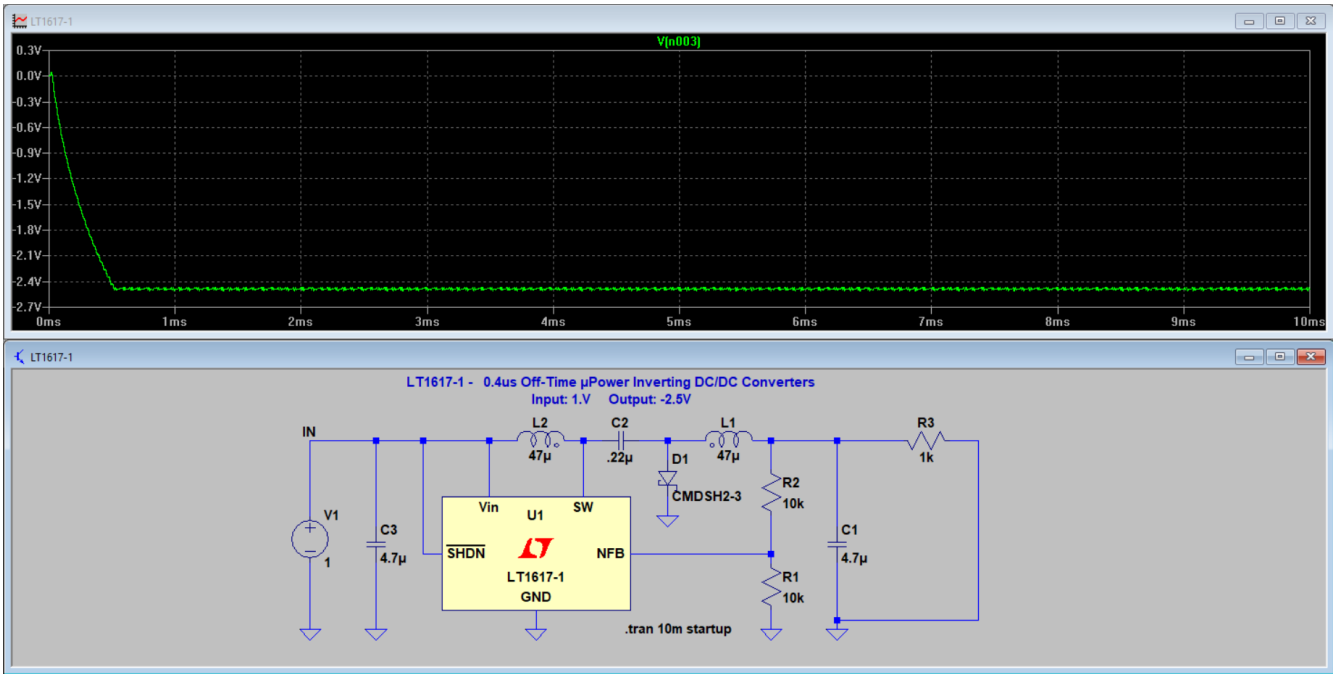

Figure 10: *Using LT1617-1 to generate a negative voltage reference*

The two circuits shown in Figure 8 and Figure 10 should create a sinusoidal output shown in Figure 9.

The circuit needs to be built and tested on a Printed Circuit Board. Using EAGLE's free software I was able to replicate the schematics in Figures 8 and 10 only the EAGLE tools. The Schematic is used to create a netlist for the layout, which will help place and route the part on the EAGLE layout tools.

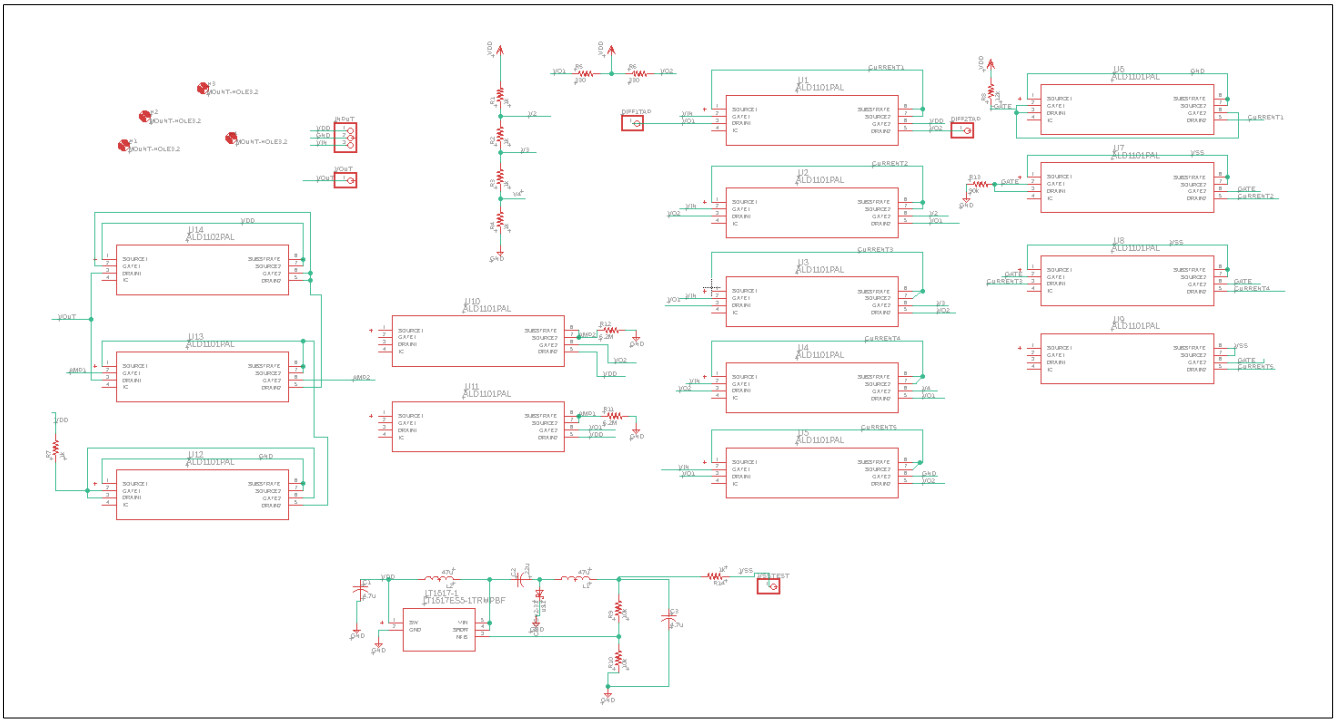

Figure 11: *Schematic Replicated in EAGLE PCB tools*

The PCB itself was constructed using the EAGLE PCB Layout tools. I used a 2-layer board with the bottom layer consisting of primarily a ground plane. I ensured that each wire width was larger than the minimum required to ensure that no wires would have too much parasitic resistance and to ensure that no wires would risk damage due to high current. The Vdd rail was much thicker than needed to be for the same reason. I attempted to place the parts such that most of the routing would be able to be on the top layer, as I didn't want to break up the ground plane on the bottom layer. The board is broken up into sections with test points at the folding amplifier outputs and to look at my -2.5 [V] rail. The board is relatively small at 3.35" x 2.79". The inputs and output are placed at the top of the PCB.

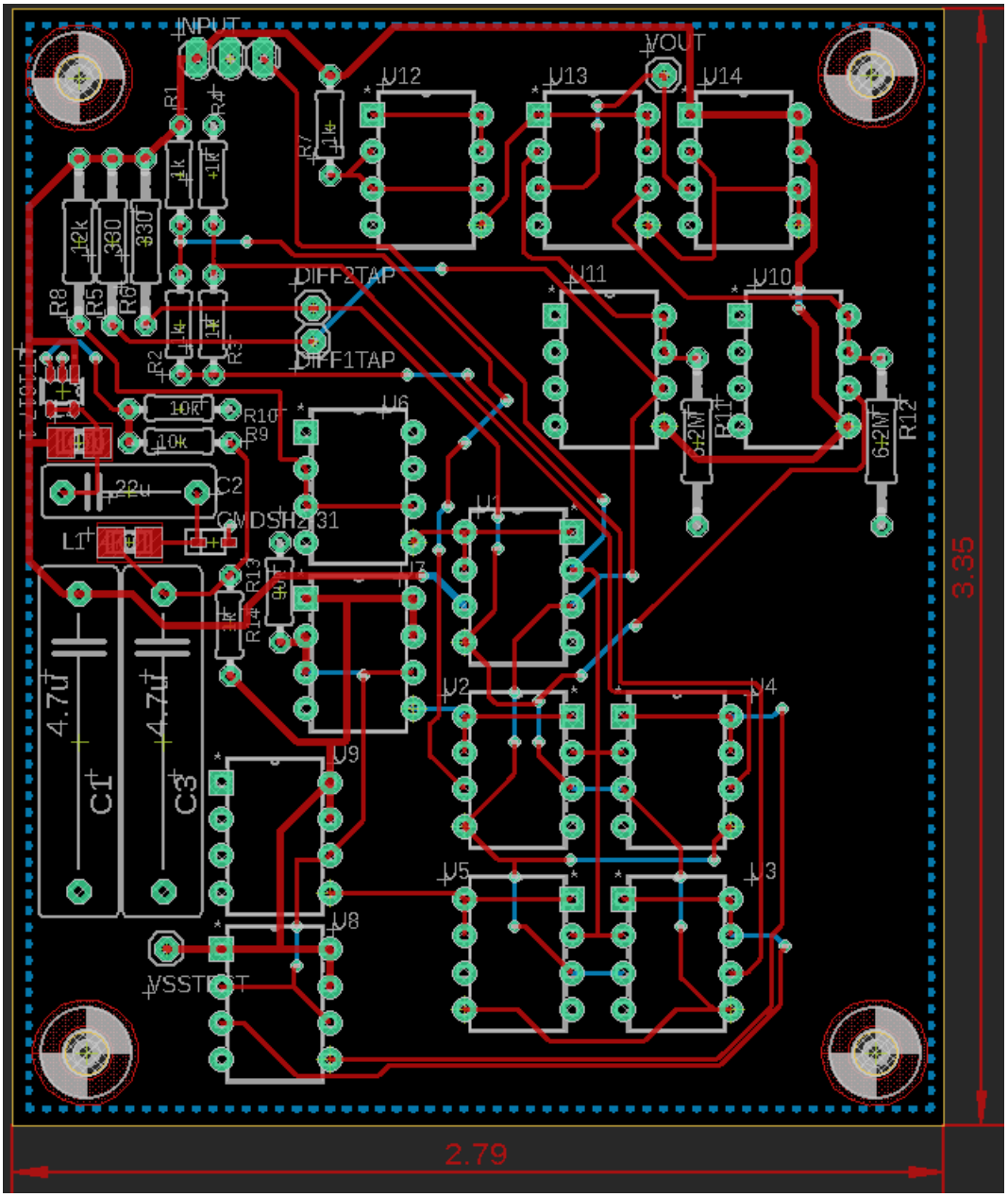

Figure 12: *Custom PCB of the Circuit*

II. Results and Discussion

	Ideal	Actual
R1 [ohm]	1k	998
R2 [ohm]	1k	998
R3 [ohm]	1k	999
R4 [ohm]	1k	999
R5 [ohm]	330	328
R6 [ohm]	330	328
R7 [ohm]	1k	999
R8 [ohm]	12k	11.99k
R9 [ohm]	10k	9.99k
R10 [ohm]	10k	9.99k
R11 [ohm]	6.2M	6.16M
R12 [ohm]	6.2M	6.06M
R13 [ohm]	90k	84.5k
R14 [ohm]	1k	998
Vss [V]	-2.5	-2.373

Figure 13: *Table of actual resistors vs ideal resistors used in schematic*

There is current a short-circuit between one of the critical nets that leads into the differential amplifier and Vdd. This will continue to be tested and looked at. Currently the output only ranges from 0 [V] to .4 [V], which is due to one of the inputs to the differential amplifier being tied to power. This is then being level shifted such that the amplifier is in common-mode state as opposed to differential state.

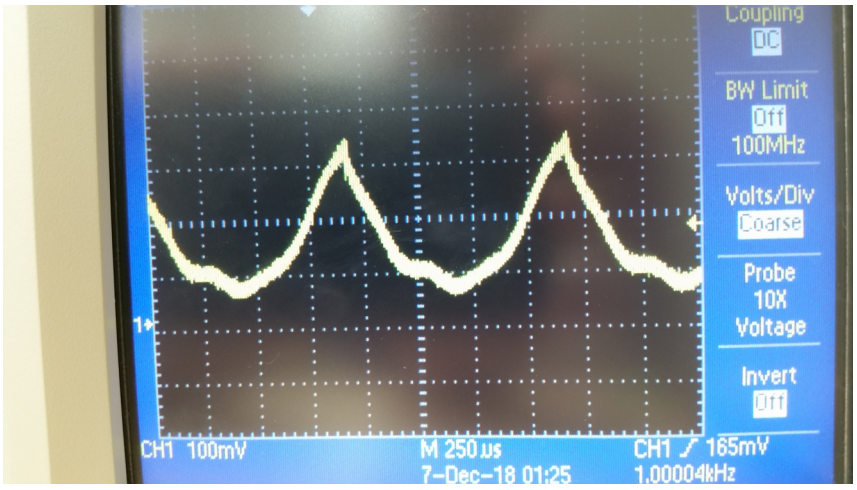

Figure 14: *Output of the Circuit before testing*

There was also an issue with the board where I had wrong connections on one of the parts. In order to fix this issue I had to physically cut the wire connections and attach wires on top of the board. This was an issue because these connections determined my negative reference voltages, which needed to be very specific in order to supply the correct voltage to the folding amplifer.

Figure 15: *Custom wire fix with cut on-board wire*

III. Conclusion

I had multiple issues while attempting to create the sinusoid both in simulation and with the PCB. I made a few errors when soldering the parts on the board as well as with the placement of the board. I will continue to work on the circuit during finals week and meet with Mark to see my final circuit. The circuit technically does work but not to the extent that the requirements need them to be.

[1] Weng, Ro-Min and Chi-Cheng Chao. "A 1.5 V high folding rate current-mode folding amplifier for folding and interpolating ADC." *2006 IEEE International Symposium on Circuits and Systems* (2006): 4 pp.-.