Generating Common Waveforms Using the LM555, Operational Amplifiers, and Transistors

Kenneth Young
November 16, 2012

I. Abstract

The generation of precise waveforms may be needed within any circuit design. This application note describes in detail how to generate precise pulse, square, and ramp waveforms as well as clipping and adding DC offsets to generated waveforms. Circuit schematics and relevant design equations will be covered while discussing waveform generator design.

II. Keywords

Waveform Generation, Linear Ramp, Pulse, Square Wave, Duty Cycle, Clipping, DC Offset

Table of Contents

III. Introduction

This application note discusses how to create circuits which will generate precise pulse, square, and ramp waveforms using entirely the LM555, Operational Amplifiers, common BJT Transistors, and passive circuit elements. Discussion is also presented on how to precisely clip the positive and negative peaks of generated waveforms and how to precisely add positive and negative offsets to generated waveforms.

IV. Objective

After reading this application note a circuit designer should have all the knowledge necessary to generate precision pulse, ramp, and square waveforms. A designer will also learn relevant equations for calculating values of circuit passive elements and be capable of explaining the operation of pulse, ramp, and square wave generating circuits.

V. Pulse Generator with Greater Than 50% Duty Cycle

The LM555 Timer can be used to generate a pulse train of greater than a 50% duty cycle by using the standard astable operation schematic seen below in Figure 1. The astable operation schematic can be found in most LM555 datasheets. The schematic in Figure 1 was taken from the Fairchild Semiconductor LM555 datasheet.

The pulse train output is taken from terminal 3 and varies from approximately ground to +Vcc-1 volts from output low to high. The pulse train will look like Figure 2 with the output high time, t1, equal to the length of time required to charge capacitor C from (1/3)Vcc to (2/3)Vcc through resistors Ra and Rb and the output low time, t2, is equal to the time required to discharge capacitor C from (2/3)Vcc to (1/3)Vcc.

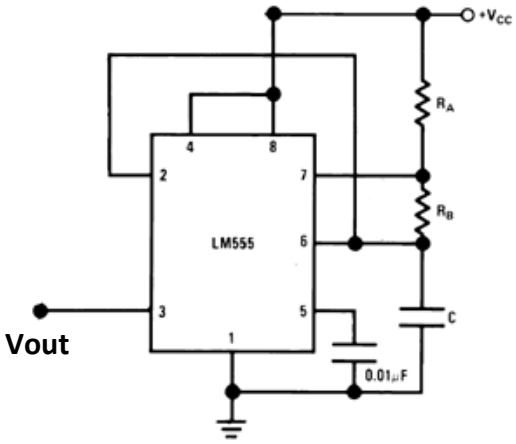


Figure 1

The Fairchild Semiconductor LM555 Datasheet gives the following equations for determining resistor and capacitor values in the design of a greater than 50% duty cycles pulse generator.

The charge time (output high) is given by:
t1 = 0.693 (Ra + Rb) C
Discharge time (output low) by:
t2 = 0.693 (Rb) C
Thus the total period is:
T = t1 + t2 = 0.693 (Ra +2Rb) C

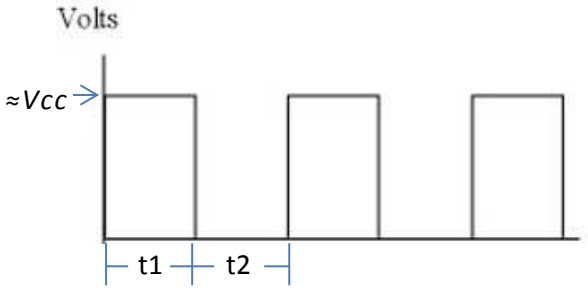


Figure 2

A problem however does arise with the circuit in Figure 1 with the range of duty cycle capable of being produced. The time t1 is determined by the charge time of the capacitor C through both resistors Ra and Rb and the time t2 is determined by the capacitor discharge time through only Rb. In comparing the above equations for t1 and t2 it can be seen that since both Ra and Rb are positive real values it is impossible for t1 to be less than t2. Thus only duty cycles of >50% can be obtained.

VI. Pulse Generator with Less Than 50% Duty Cycle

An LM555 Pulse generator with less than 50% duty cycle can easily be made by simply inserting a small signal diode such as the 1N4148 between pins 6 and 7 of the grater than 50% duty cycle pulse generator from Figure 1. The less than 50% duty cycle pulse generator is shown in Figure 3. The high time, t1, is equal to the length of time required to charge capacitor C from (1/3)Vcc to (2/3)Vcc through only resistor Ra. The diode acts to bypass resistor Rb when charging C. The output low time, t2, is equal to the time required to discharge capacitor C from (2/3)Vcc to (1/3)Vcc through only Rb. When C is discharging the diode is reversed biased and will not allow current to pass through.

The equations for the less than 50% duty cycle pulse generator are as follows:

The charge time (output high) is given by:
t1 = 0.693 (Ra) C
Discharge time (output low) by:
t2 = 0.693 (Rb) C
Thus the total period is:
T = t1 + t2 = 0.693 (Ra + Rb) C

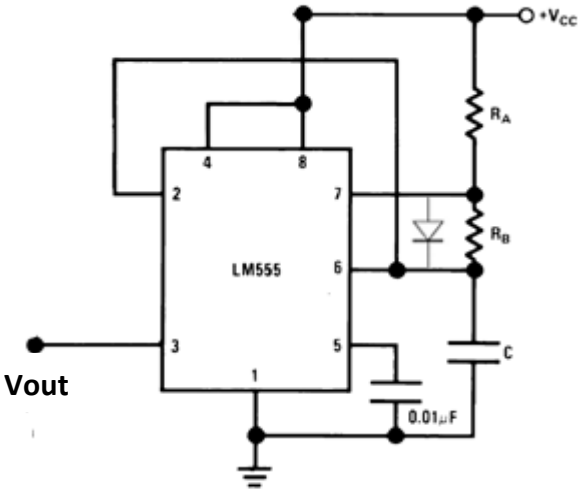
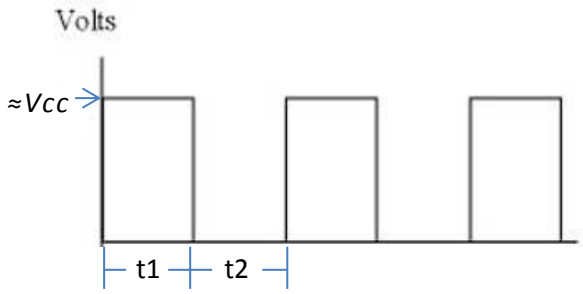


Figure 3



Repeat of Figure 2

VII. Linear Ramp Generator

A linear Ramp waveform generator can be created by combining a <50% duty cycle pulse generator along with the attached circuit containing two transistors seen in Figure 4. Components Ra, Rb, and C are chosen to produce a pulse train at the output pin 3 of the LM555 with the desired period of the ramp wave T, as seen in Figure 5, and with a duty cycle preferably less than 1%.

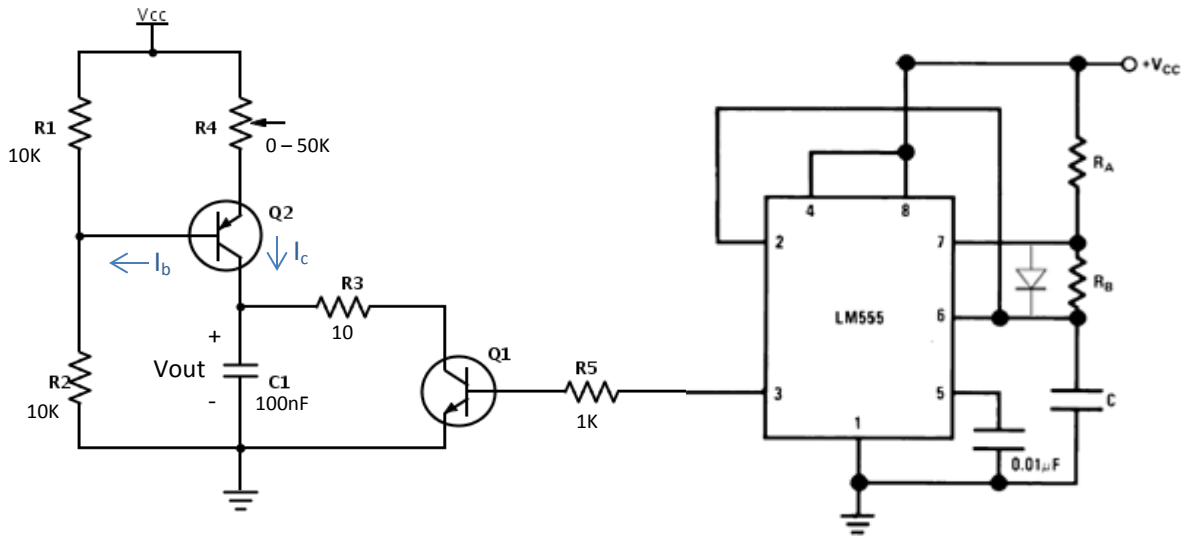


Figure 4

Transistor Q2 is set up as a constant current source. Q2 has a constant fixed base current, I_b, between the emitter to base junction through R4 and to the voltage divider formed between R1 and R2. If Q2 is operating in active mode with a constant base current the collector current through Q2 must also be constant and will equal to βI_b, with β being the DC gain of the transistor. In other words, because the transistor has a fixed bias current it must also have a fixed collector current in the active mode.

The current flowing though the collector of Q2 can then go in two directions depending on the state of the LM555 output at pin 3. If the LM555 output is low transistor Q1 is in cutoff and appears like an open circuit between the collector to emitter. With Q2 cutoff the collector current of Q2 can only flow into the capacitor C1 and begin charging the capacitor and increasing Vout. When a constant current is charging a capacitor there must be a constant +dV/dt across the capacitor equal to the current divided by the capacitor capacitance, thus there is a linear ramp voltage present across the capacitor. The amount of current flowing through the collector of Q2 and thus the maximum ramp voltage Vp can be adjusted by varying potentiometer R4. Lowering the resistance of R4 allows more current to flow from the collector of Q2 during the duration between pulses from the LM555 and increases Vp. Alternatively, raising the resistance of R4 lowers the collector current of Q2 and reduces Vp.

During the brief time in which the output of the LM555 at pin 3 is high the transistor Q1 becomes saturated. When Q1 becomes saturated it appears almost like a short circuit between the collector to emitter. C1 then discharges very quickly through R3 and the saturated Q1 because essentially only R3, a very small resistance, is between the capacitor and ground. However the capacitor voltage Vout cannot discharge all the way to zero volts because of the small transistor saturation voltage present between

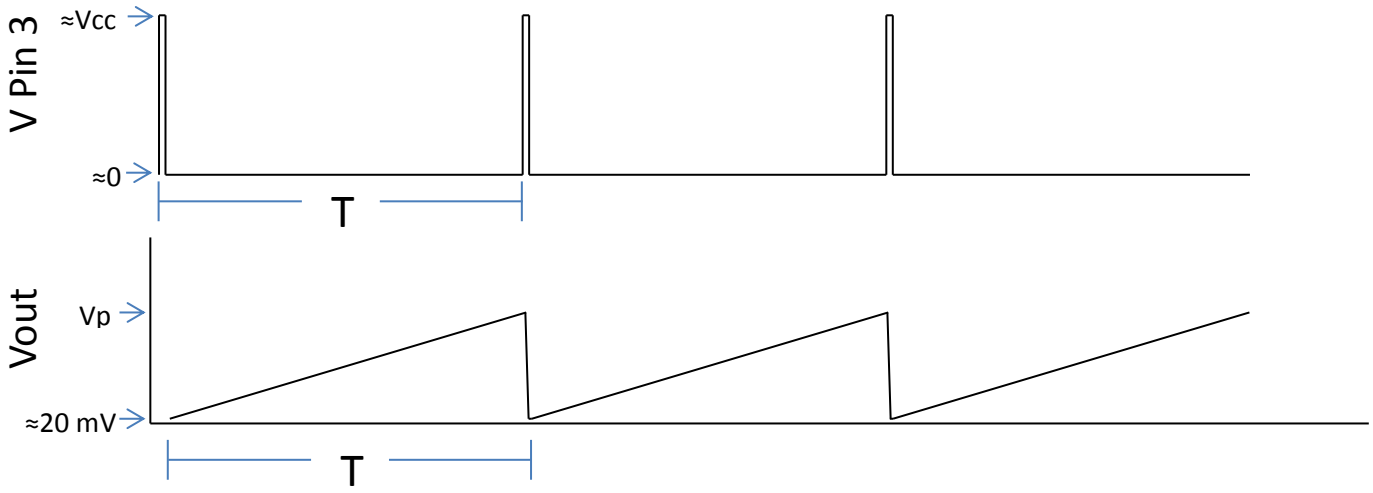


Figure 5

the collector and emitter of Q1. Once the output of the LM555 at pin 3 returns to a low state Q1 again goes into cutoff and the charging process of C1 starts again until the output of the LM555 returns high.

Note- In the lab the author has observed that the minimum voltage of the ramp wave, Vout, is approximately 20mV when using Q2N3904 and Q2N3906 transistors for Q1 and Q2 respectively over a range of Vcc and Vp voltages and LM555 pulse duty cycles.

The resistor R3 is not always needed in the ramp generator circuit and could be removed. R3 is present only to limit the current spike through Q1 when it saturates, however if R3 is too large C1 will not have enough time to completely discharge during the brief period in which the LM555 output is high and thus the minimum voltage of the ramp wave, Vout, could increase. The Resistor R4 is needed to prevent the base current of Q1 form exceeding its maximum allowed value when the output of the LM555 is high. Vcc should be at least twice the desired Vp of the ramp waveform to ensure linearity of the ramp over the entire range of ramp voltage.

The relevant equations for the ramp wave generator circuit are as follows:
Assuming the diode drop voltage between the Q2 emitter to base junction is 0.65V and β is the DC gain of Q1:

$$I_b = \frac{Vcc - Vcc * \frac{R2}{R1 + R2} - 0.65}{(\beta + 1) * R4}$$

$$Ic = \beta * I_b$$

For the Capacitor C1 when charging:

$$Ic = C1 * \frac{dVout}{dt}$$

$$\frac{dVout}{dt} = \frac{Ic}{C1}$$

For a linear ramp wave across C1 with pulse period of T from the LM555 output with duty cycle <1%:

$$Vp \approx \frac{dVout}{dt} * T$$

VIII. Square Wave Generator

Sections V and VI covered how to generate pulse waveforms using only an LM555 timer. However the pulse waveform produced by an LM555 only varies between 0 volts and +Vcc. There may be applications in which a square wave having peaks of +Vcc and –Vcc is desired.

50% Duty Cycle Square Wave Generator

A simple square wave generator with a 50% duty cycle can be produced using one dual supply Op Amp as show in Figure 6**Error! Reference source not found.**. The output of the Op Amp is always either at +Vcc or –Vcc. To simply explain the action of the circuit say that C1 is initially uncharged and the output or the Op Amp is at +Vcc.

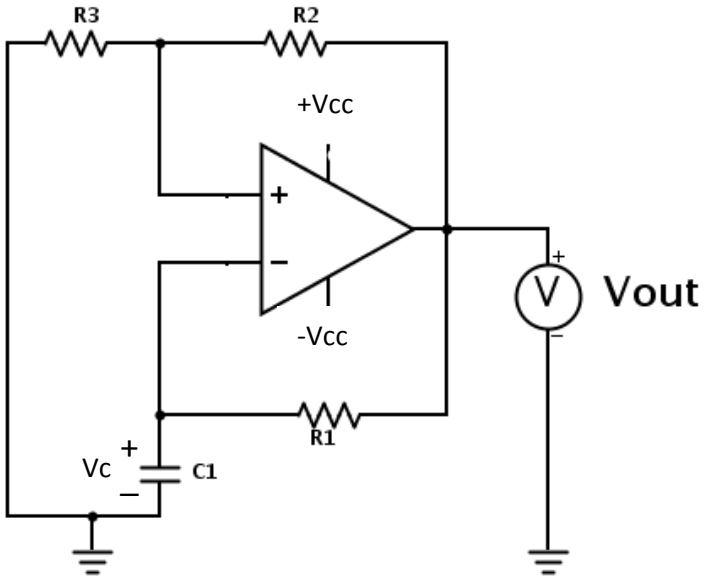


Figure 6

R2 and R3 will form a voltage divider which creates a voltage at the non-inverting input of:

$$V_+ = \left(\frac{R3}{R2+R3}\right)(+V_{CC})$$

The positive voltage on the non-inverting input will keep the output of the Op Amp high so long as $V_+ > Vc$. At the same time C is charging through R1 and the voltage across the capacitor V_C is increasing. The voltage Vc is also the voltage on the V_- input, thus it is always true that:

$$V_- = V_C$$

C1 will continue to charge through R1 until $Vc = V_+$ at which point the output of the Op Amp will transition to –Vcc. Upon transition the voltage at V_+ switches negative to

$$V_+ = \left(\frac{R3}{R2+R3}\right)(-V_{CC})$$

which will keep the output at the Op Amp low. C1 will then discharge through R1 and Vc will begin to go negative. Again the output of the Op Amp will stay at -Vcc until $Vc = V_+$ at which point the Op Amp will transition back to +Vcc.

Without going through the full derivation the frequency of the square wave output can be solved for using the RC charge time constant of R1 and C1 and is equal to:

$$f_o = \frac{1}{2(R1)(C1)\ln\left(\frac{2(R3)}{R2}+1\right)}$$

To manually change the frequency of the output it is recommended that R2 and R3 bee chosen to be equal resistors of 100K ohms and R1 be replaced with a potentiometer. R1 can then be adjusted until the output is the desired frequency by changing the RC charge constant between R1 and C1. Also, note that the square wave generator in Figure 6 will only produce a 50% duty cycle square. This is due to the fact that C1 both charges and discharges through the same resistor R1, thus the RC time constant during the positive and negative output swings is identical and the output is a 50% duty cycle wave.

Variable Duty Cycle Square Wave Generator

A variable duty cycle square wave generator can be created by combining an astable LM555 pulse generator and a dual supply Op Amp as shown in Figure 7.

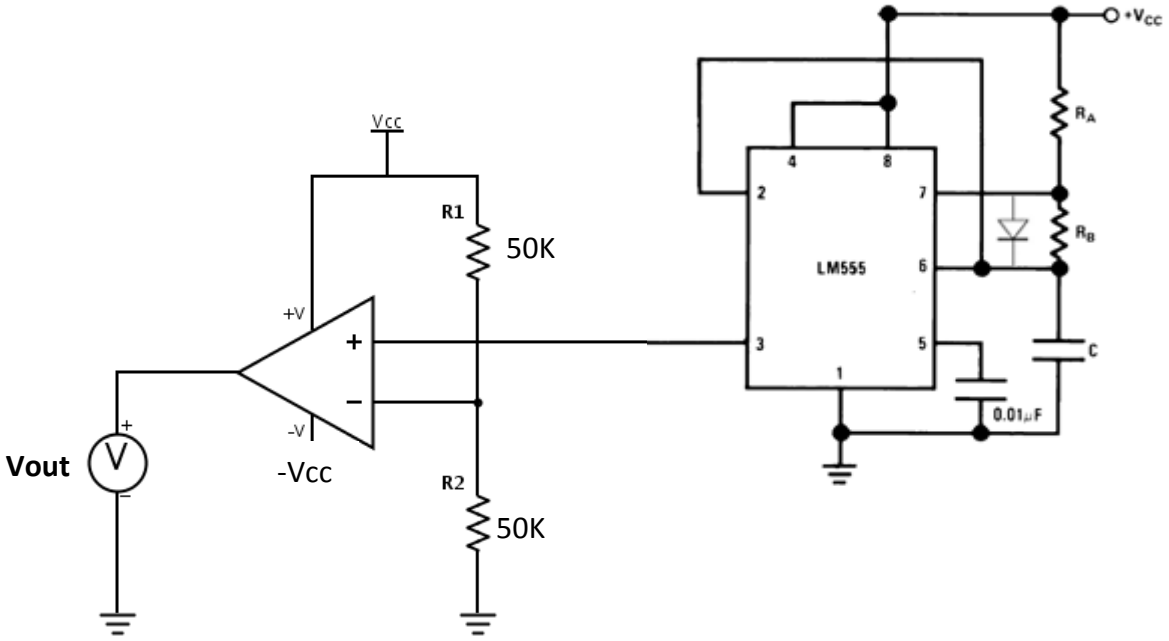


Figure 7

The duty cycle and frequency of the LM555 timer should be set to the duty cycle and frequency of the desired square wave. Setting the duty cycle and frequency of the LM555 is discussed in sections V and VI. The voltage on the V_- input to the Op Amp is referenced at $V_{C\,C}/2$ and the output from the LM555 will either be $+V_{CC}$ or approximately zero volts. When the output from the LM555 is high $V_+ > V_-$ and the output from the Op Amp is +Vcc. When the output from the LM555 is low $V_+ < V_-$ and the output from the Op Amp is $-V_{CC}$.

Note- Obviously the design for the variable duty cycle square wave generator is much more versatile than the fixed 50% duty cycle square wave generator discussed previously. However the variable duty cycle design requires more components than the 50% duty cycle design and an additional Integrated Circuit chip. Thus, the 50% duty cycle design is less costly and less prone to failure due to greater simplicity. If a designer only needed to generate a 50% duty cycle square wave the fixed type design might be more advantageous.

IX. Clipping Waveforms

The ability to precisely clip waveforms may be needed when creating pulse train waveforms or square waves. Sections V and VI discuss how to generate pulse trains of specific frequency and duty cycle however the peak value of the pulse train will be at Vcc minus some small voltage drop from the LM555. A circuit designer might desire to have the peak of the pulse train to be at some specific value between Vcc and zero volts. To set a specific peak value of a pulse train an Op Amp positive clipper circuit can be used as show in Figure 8.

Vin is where a pulse train is input into the positive clipper and Vout is the clipped output. The level of voltage at which the waveform will be clipped is determined by potentiometer R2. The wiper on R2 should be adjusted so that the voltage, Vref, at the wiper is equal to the desired clipping voltage. Example Vin and Vout waveforms are shown in Figure 9. The dotted line at Vref on the input waveform represents the level at which positive clipping will occur. Vout shows the waveform with positive clipping at Vref at the output.

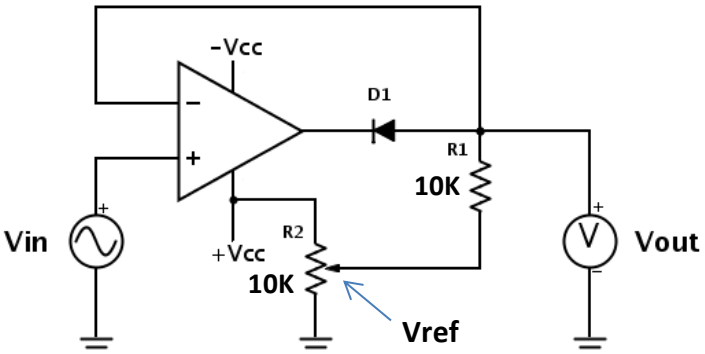


Figure 8

Vref can be a positive or negative voltage depending on the waveform design needs. In Figure 8 Vref is a positive value because R2 is attached between +Vcc and ground. R2 could also be attacked between-Vcc and ground, in which case a negative Vref can be achieved.

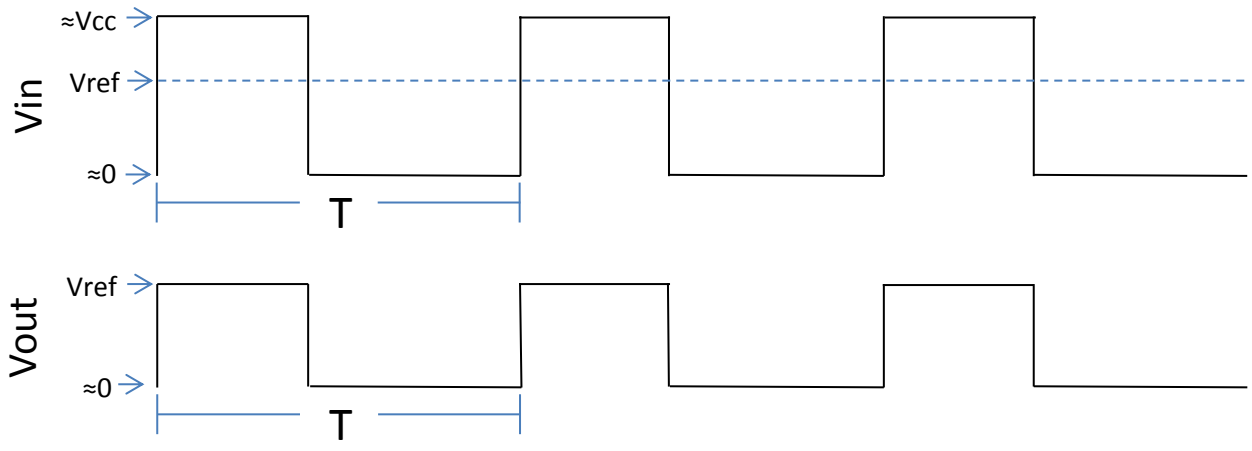


Figure 9

The output of the positive clipper should be attached to a high impedance load to avoid changes in output voltage due to the effects of loading. It is recommended that the load should contain an Op Amp voltage buffer if any significant current is needed from the output waveform.

A circuit designer may also want to utilize a negative precision clipping circuit to set the negative peaks of a square wave or other waveform. Figure 10 shows a negative clipping Op Amp circuit. The voltage level at which negative clipping will occur is Vref, which can be adjusted via potentiometer R2. Just as in the positive clipping circuit Vref can be positioned between either +Vcc or –Vcc depending on if the desired clipping voltage is positive of negative. As displayed in Figure 10 negative clipping will occur at a negative voltage because R2 is connected between –Vcc and ground, thus Vref must be negative. Also, an Op Amp voltage buffer should be used in the output of the negative clipper if any loading is expected, just as with the positive clipper.

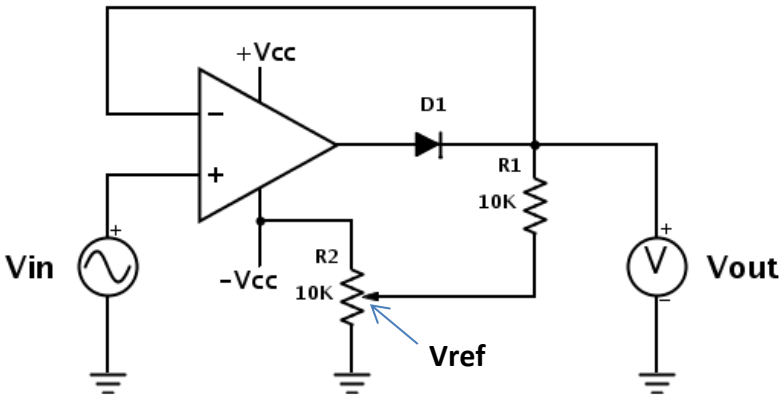


Figure 10

X. Adding a Positive or Negative Offset

A circuit designer may desire to add a precise positive of negative offset to a generated waveform. A positive of negative offset can be added to a waveform by utilizing a non-inverting or inverting summer.

Non-Inverting Summer

A non-inverting summer is shown in Figure 11. A DC offset can be added to a waveforms simply by applying the waveform to R1 as voltage V1 and applying the DC offset voltage to R2 as voltage V2.

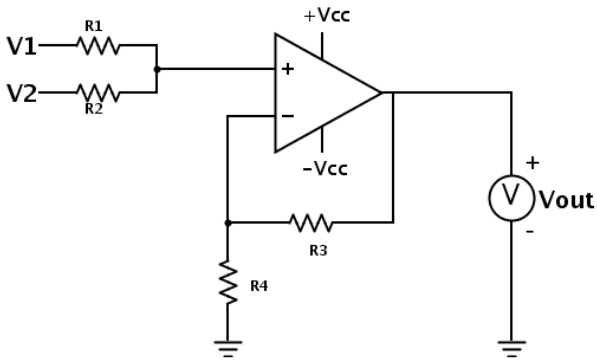


Figure 11

For a non-inverting summer with two input voltages the transfer function can be derived as follows

$$V_+ = (V_2 - V_1)\left(\frac{R1}{R1+R2}\right) + V_1$$

$$V_- = V_{out}\left(\frac{R4}{R3+R4}\right)$$

Since a non-inverting summer has negative feedback $V_+ = V_-$

$$(V_2 - V_1)\left(\frac{R1}{R1+R2}\right) + V_1 = V_{out}\left(\frac{R4}{R3+R4}\right)$$

$$V_{out} = \left[(V_2 - V_1)\left(\frac{R1}{R1+R2}\right) + V_1\right]\left(\frac{R3+R4}{R4}\right)$$

$$V_{out} = \left[V_2\left(\frac{R1}{R1+R2}\right) + V_1\left(\frac{R2}{R1+R2}\right)\right]\left(1+\frac{R3}{R4}\right)$$

For the non-inverting summer in Figure 11 with two inputs if R1=R2=R3=R4

$$V_{out} = V_1 + V_2$$

An example of the output of a non-inverting summer with a 0 to 5v pulse signal on V_1 and +2v DC on V_2 can be seen in Figure 12. The output waveform will be the sum of $V_1 + V_2$ which is a 2 to 7v pulse.

More than two inputs can be added together by adding additional resistors to the node at V_+. A non-inverting summer with more than two inputs would have a different transfer function than that which was previously derived for the two input design. The transfer function for a design with more than two inputs can be derived by solving for the voltage at the V_+ input at any time using the superposition theorem and equating to the voltage at the V_- input in terms of Vout.

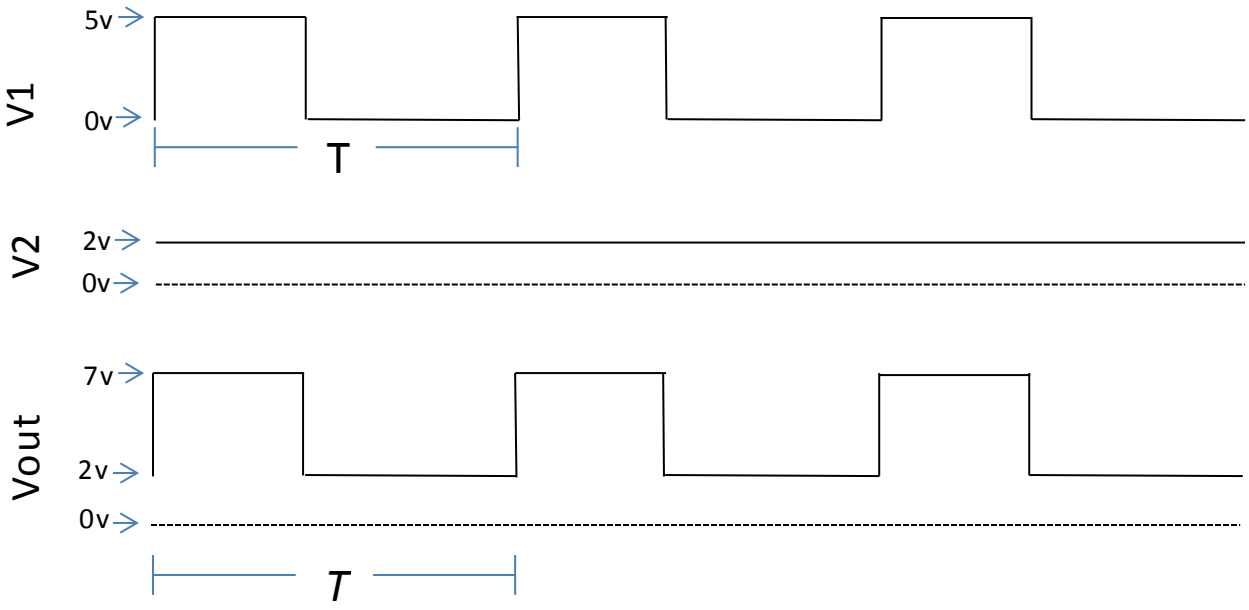


Figure 12

Inverting Summer

The inverting summer performs the same function as the non-inverting summer except the output of an inverting summer is, as the name implies, inverted in polarity. There are slight advantages and disadvantages to using an inverting summer or non-inverting summer. An Inverting summer is shown in **Error! Reference source not found.**.

One of the most apparent advantages to designing an inverting summer is that its transfer function is much simpler than the transfer function of a non-inverting summer, as will be shown, however a disadvantage which the inverting summer can be seen with a hypothetical example. If a circuit designer desires to add together multiple positive signals there will be a positive sum. If an inverting summer is chosen for the design the output will be the opposite polarity of the desired signal summation, thus an inverter must be used to change the output polarity back to a positive value. Also, because an inverting summer is used a dual supply Op Amp must also be used with ostensibly means that a dual power supply must be available. If a non-inverting summer was chosen for the design instead of an inverting summer an inverter on the output would not be necessary and a signal supply Op Amp could be used, thus allowing the circuit to function with only a single supply.

The transfer function for an inverting summer is much simply than the transfer function for a non-inverting summer, but will not be derived here. Suppose that an inverting summer has n different inputs and thus n different input resistors, the output voltage will then be:

$$V_{out} = -Rf\left(\frac{V_1}{R1} * \frac{V_2}{R2} * \dots * \frac{V_n}{Rn}\right)$$

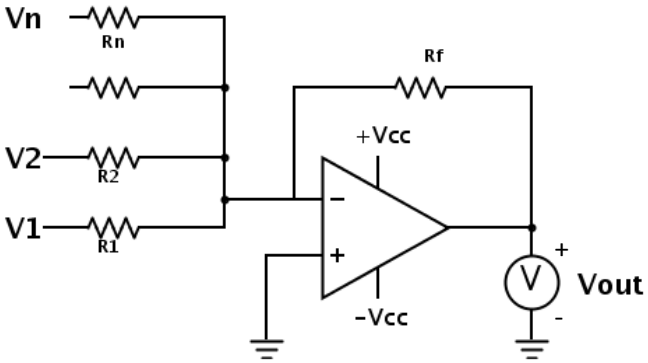


Figure 13

XI. Final Notes

1. All equations and circuit explanations involving Op Amps in this application note are on the assumption that the Op Amp output has complete rail-to-rail capability. In reality no Op Amp has complete rail-to-rail capability. Even Op Amps which are rated as rail-to-rail have some small amount of offset from the rail voltage. Thus the designer should take into account the output swing of the specific Op Amps, found in an Op Amp's datasheet, chosen to create the wave generating circuits in this application note.

2. All waveform figures shown in this application note assume that the LM555 timer and all Op Amps used has infinite slew rate. In reality the LM555 and all Op Amps have a finite slew rate which will distort a pulse train waveform. The effect of slew rate distortion will be greater with higher signal frequencies. All Op Amp datasheets contain specifications on the slew rate of a particular Op Amp. Op Amps can have slew rates ranging anywhere between .3 to over 100 Volts/µs.

3. All schematics used in this application note except for the LM555 astable operation schematic were created using the online Digikey Scheme-it software, which can be found at: http://www.digikey.com/schemeit

4. References to refer to for more information on the topics discussed in this application note are as follows, reiterated in section XII:
   - V, VI, VII (LM555)
   - VIII (Ali and Kazimierczuk)
   - IX (Bakshi)
   - X (Leach)

XII. References

. "LM555." . Fairchild Semiconductor, 25 Sep 2012. Web. 10 Nov 2012. <http://www.fairchildsemi.com/ds/LM/LM555.pdf>.

Ali, Aminian, and Kazimierczuk Marian. *Electronic Decices: a design approach*. 1st. Prentice Hall, 2004. Web. <http://www.cs.wright.edu/~dkender/bme460/RectangularWaveGenerators.pdf>.

Bakshi, U. A. *Linear Intigrated Circuits*. 1st. Pune: Technical Publications Pune, 2010. 4-147- 4-149. Print. <http://books.google.com/books?id=-zAe0P33BAcC&printsec=frontcover

Leach, Marshall. "ECE3050 Analog Electronics." *Georgia Tech School of Electrical and Computer Engineering*. Georgia Tech . Web. 12 Nov 2012. <http://users.ece.gatech.edu/mleach/ece3050/sp04/OpAmps01.pdf>.