GN001 Application Guide

Design with GaN Enhancement mode HEMT

Updated on Oct-7-2016

GaN Systems Inc.

Overview

- GaN has extremely fast switching speed and excellent reverse recovery performance.
- GaN Systems offers high performance and easy to use GaN true Enhancement mode HEMT (E-HEMT) in embedded package.

Very high switching speed combined with some unique characteristics of GaN requires special attention to the gate drive circuit and layout design.

Abstract:

- This application guide highlights the basic characteristics of GaN Systems GaN E-HEMTs, then the key design consideration of gate drive circuit and layout will be discussed followed by design examples.
- Most of the discussion will be focused on 650V GaN, though many basic design principles apply to 100V GaN design as well.

Agenda

- ❑ Basics
- ❑ Gate Drive Design considerations
- ❑ Design examples
- ❑ PCB Layout
- ❑ Switching Testing results

Latest update OCT-07-2016

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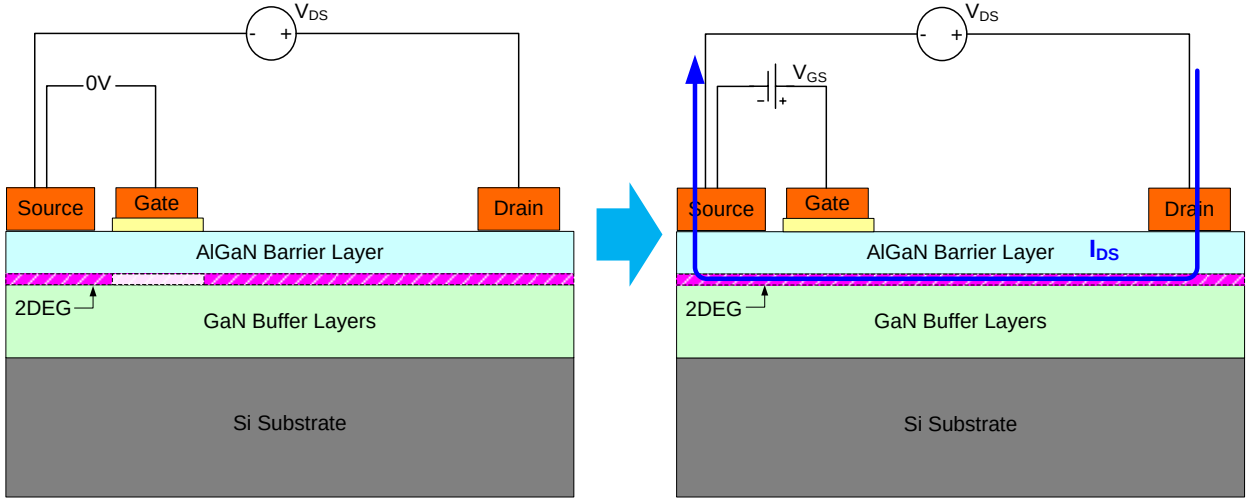
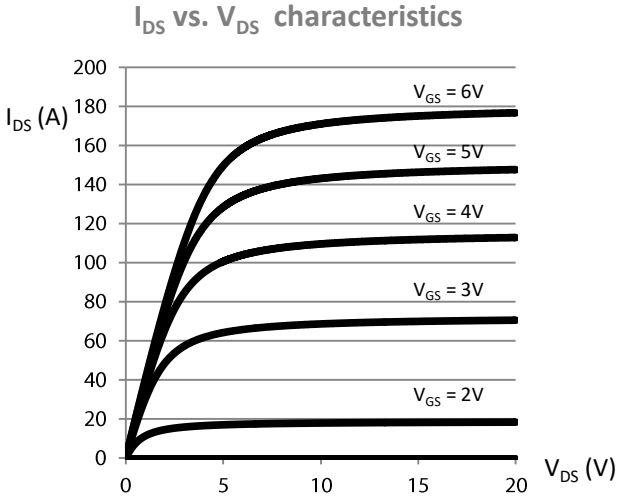
GaN Enhancement mode High Electron Mobility Transistor (E-HEMT)

- Lateral 2-dimensional electron gas (2DEG) channel formed on AlGaN/GaN hetero-epitaxy structure provides very high charge density and mobility
- For enhancement mode operation, a gate is implemented to deplete the 2DEG underneath at 0V or negative bias. A positive gate bias turns on the 2DEG channel

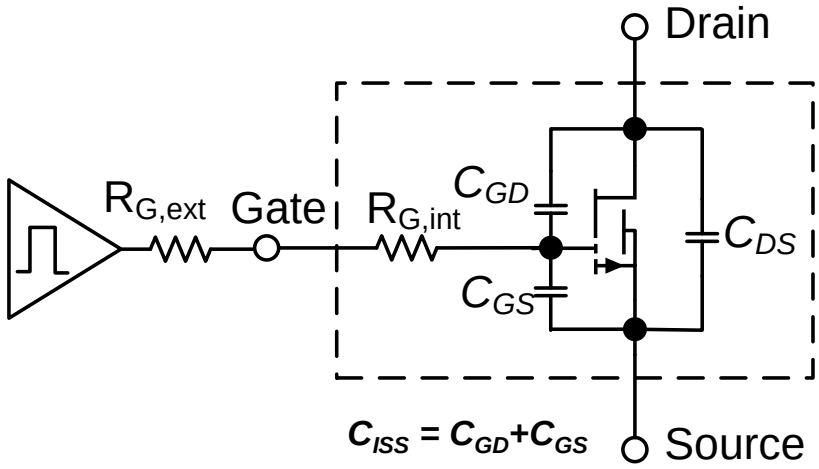




E-HEMT Gate characteristics

Common with Si MOSFET

- True e-mode normally off
- Voltage driven - driver charges/discharges C_{ISS}
- Supply Gate leakage I_{GSS} only
- Easy slew rate control by R_G



Differences

- Much Lower Q_G : Lower drive loss; faster switching
- Higher gain and lower V_{GS} : +5-6V gate bias to turn on
- Lower $V_{G(th)}$: typ. 1.5V

Vs other e-mode GaN

- More robust gate: +7/-10V DC max rating
- No DC gate drive current required
- No complicated gate diode / PN junction

Gate Bias Level	GaN Systems GaN E-HEMT	Si MOSFET	IGBT	SIC MOSFET
Maximum rating	-10/+7V	+/-20V	+/-20V	-8/+20V
Typical gate bias values	0 or-3/+5-6V	0/+10-12V	0 or -9/+15V	-4/+15-20V

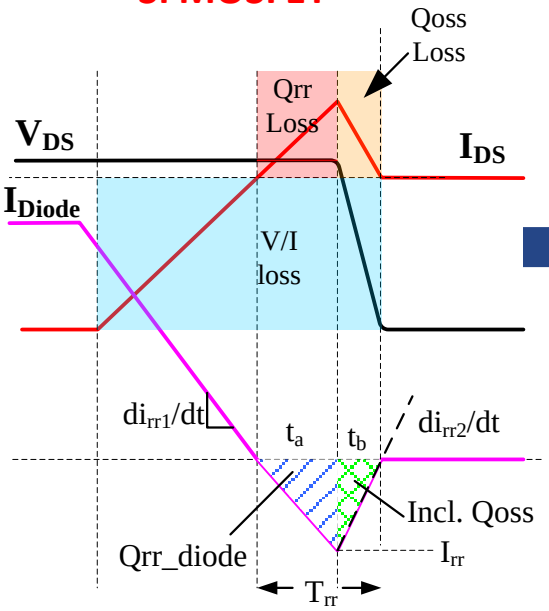
Reverse recovery performance

GaN E-HEMT does not have parasitic body diode, thus ***No Q_{RR}, only Q_{OSS} loss***

But it is naturally capable of reverse conduction ***without external anti-parallel diode***

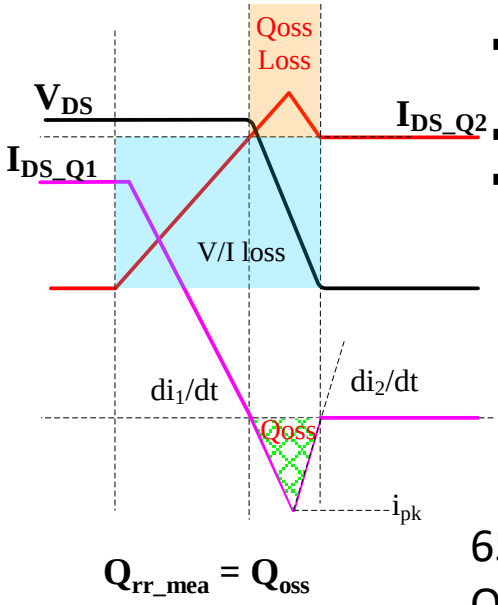
GaN is good fit for half bridge hard switching application

Si MOSFET



$Q_{rr\_mea} = Q_{rr\_diode} + Q_{OSS}$

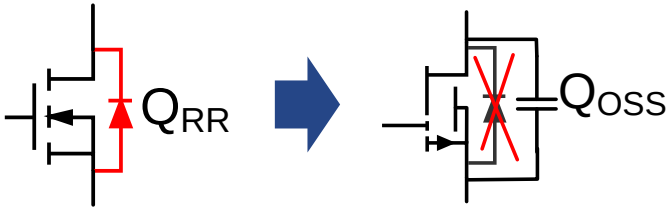
GaN E-HEMT



$Q_{rr\_mea} = Q_{oss}$

GaN Q_{OSS} vs Si MOSFET Q_{RR}:

- Order of magnitude smaller than Q_{OSS}
- Q_{RR} changes with di/dt and T_J while Q_{OSS} is a fixed value
- Similar I_{DS} overshoot caused by charging high side C_{OSS}
- No Q_{RR} loss period
- di_2/dt can be controlled (turn-on di/dt and LC resonance), *No uncontrolled snappy recovery issue*



650V SJ MOSFET

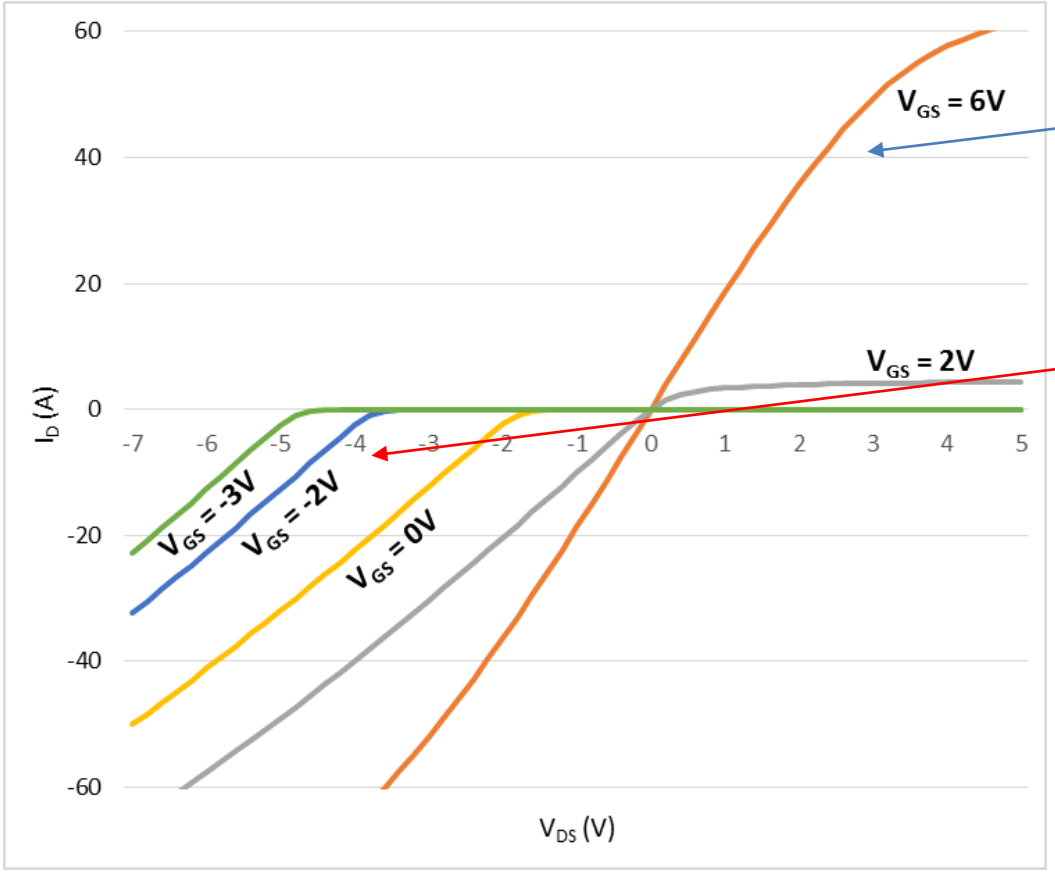
Q_{RR} = **1000 – 10000nC!**

650V GaN

Q_{OSS} = **60nC**

Reverse Conduction Loss

GS66508 I/V curve (T_J=25°C)



GaN E-HEMT reverse conduction has a 'diode' like characteristics and it is V_{GS} dependent

V_{GS} = 6V (on-state):

- 2-quadrant bidirectional current flow
- $P_{rev} = I_{SD}^2 x\ R_{DS(ON),\ Tj}$

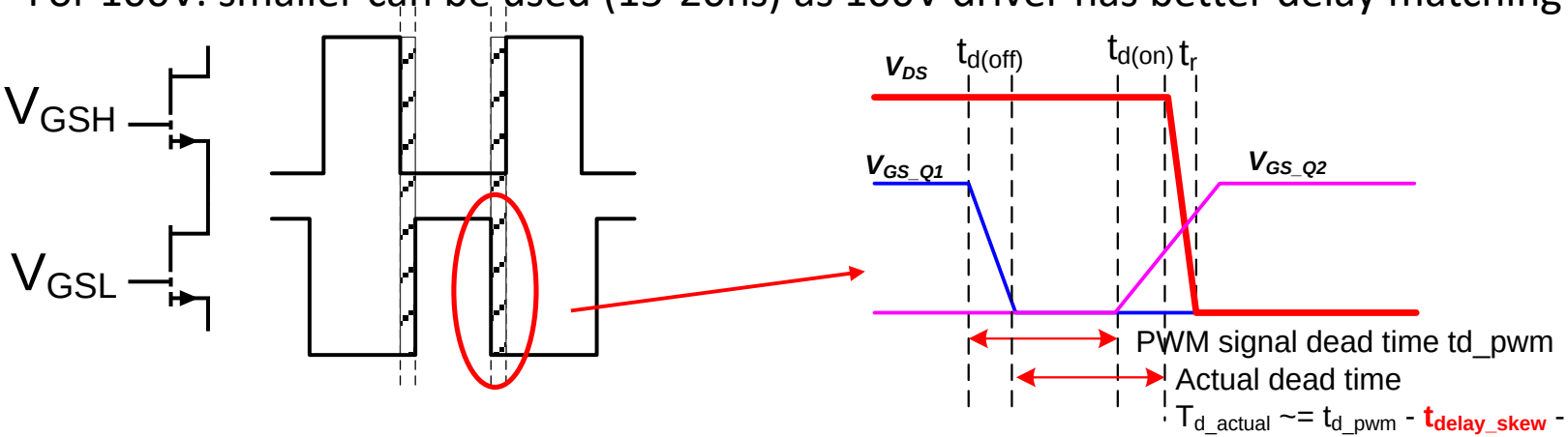
$V_{GS} \leq$ 0V (off-state):

- "diode" with V_F + channel resistance R_{rev_on}
- Negative gate bias adds to the V_{SD}
- $P_{rev} = I_{SD}^2\ X\ R_{REV(ON)} + I_{SD} x\ (V_{GTH} + V_{GS\_OFF})$
- $R_{REV(on)}$ increases with TJ while $V_{G(th)}$ remains stable over the temperature range

- **Unlike MOSFET/IGBT, current always flows in same 2DEG regardless of V_{GS}**
- No need for external anti-parallel diode
- Excellent reverse recovery performance (No Q_{RR}) for high efficiency hard switching
- V_{SD} higher than typical diode – minimize dead time and use synchronous drive

Setting up dead time

- For hard switching: t_{d_pwm} must be > t_{delay_skew} + ($t_{d(off)}$ - $t_{d(on)}$):
- Gate turn-on/off delay difference varies with R_G: typical +/-5ns range (GS66508)
- High/low side gate driver delay skew (worst case delay mismatch) usually dominates:
  - Example Silab Si8261 isolated gate driver $t_{delay\_skew\_max}$ = 25ns. In this case the dead time must be set > **30ns** as minimum
  - However in practical circuit safety margin must be considered: for GS66508 typical **50-100ns** is chosen for dead time
- For soft switching dead time needs to be chosen for achieving ZVS transition
- For 100V: smaller can be used (15-20ns) as 100V driver has better delay matching



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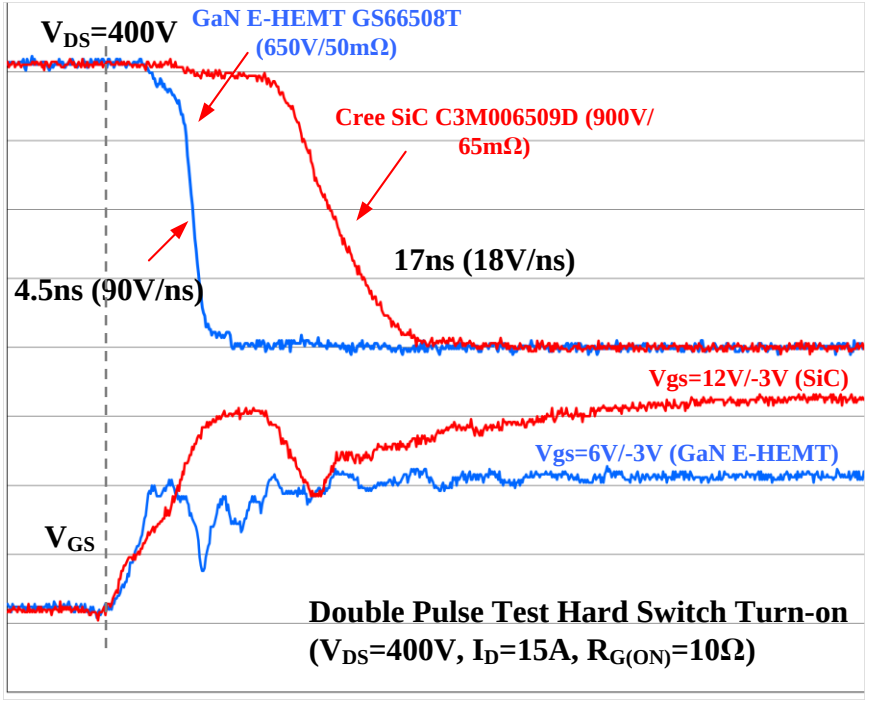
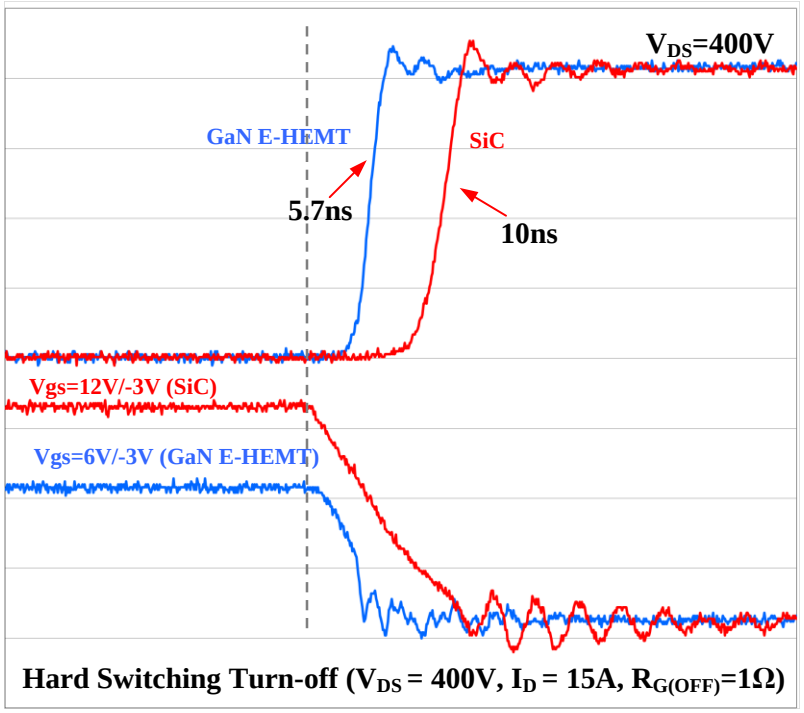
Design Considerations – fast switching

GaN can switch faster than Si/SiC MOSFETs with dv/dt > **100V/ns**

- GaN shows 4x faster turn-on and ~2x faster off time than state of art SiC MOSFET with similar Rds(on)
- ***Care should be taken when designing with such a high switching speed and dv/dt***





Design considerations for driving high speed GaN E-HEMTs:

Controlling noise coupling from power to gate drive loop should be the first priority:

- High dv/dt and di/dt combined with low C_{ISS} and $V_{G(th)}$ → Need to protect gate spikes from going above threshold or maximum rating under miller effect for safe operation
- Gate ringing or sustained oscillation may occur if the design is not done properly and may lead to device failure. We will discuss how to mitigate that in this section
- On the other hand, the switching performance of GaN should not be compromised too much
- This is more critical for 650V hard switching half bridge application as very high dv/dt could occur at hard turn-on.
- Single end topology has less concern with miller effect, and for resonant ZVS topology the dv/dt and di/dt are lower so their design requirement may be relaxed.

In this section we will walk through the design tips on how to control miller effect and mitigate gate ringing/oscillation, followed by gate driver recommendations

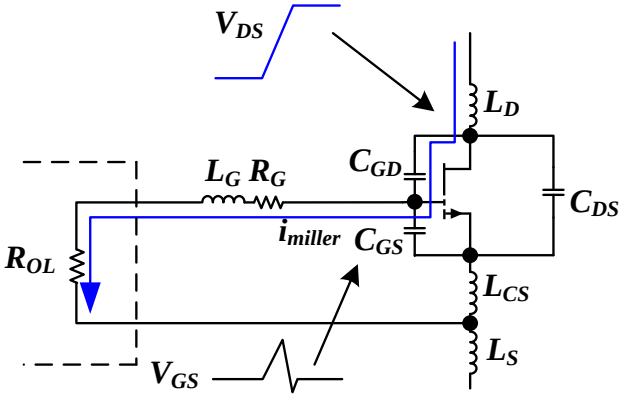
Control miller effect

Gate drive impedance (Rg and Lg) is critical for turn-off, but less at turn-on

Basic rule: the gate needs to be held down as strong as possible with minimum impedance

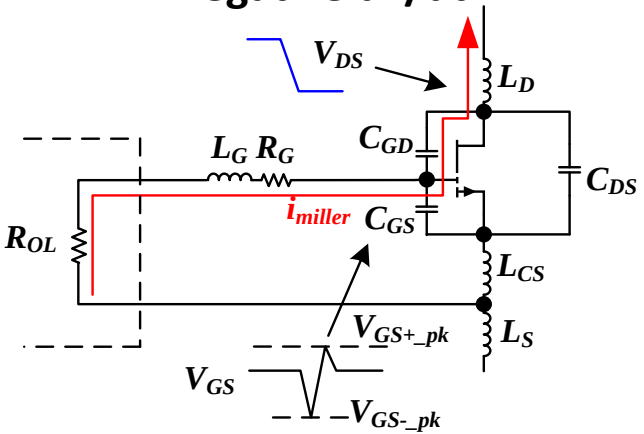
Miller effect is more prominent at 650V than 100V design due to the higher dv/dt

Positive dv/dt



- Prevent false turn-on
- Strong pull-down (low R_G/R_{OL})
- Low L_G to avoid ringing
- Use negative gate bias, -2 to -3V is recommended

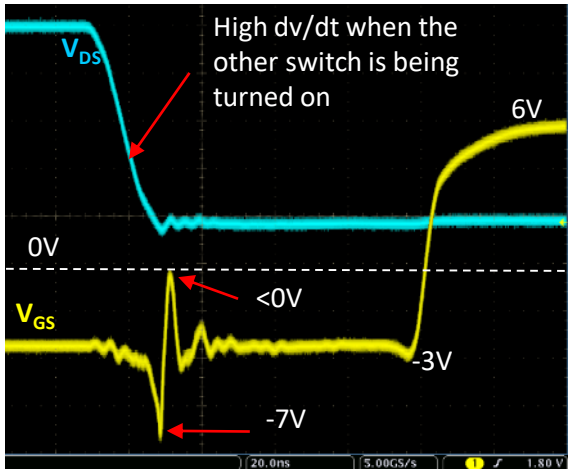
Negative dv/dt

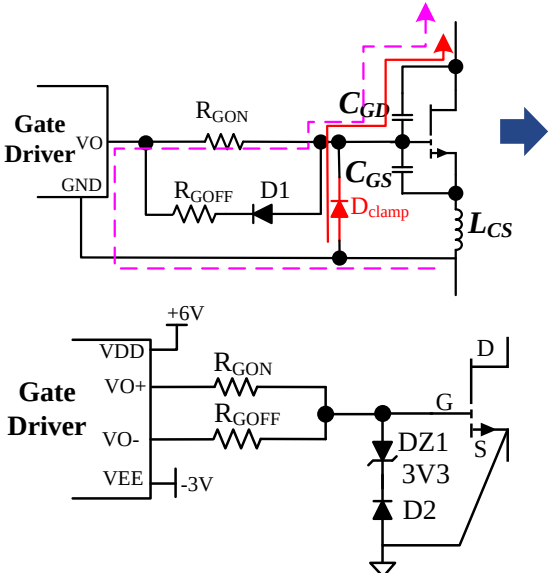


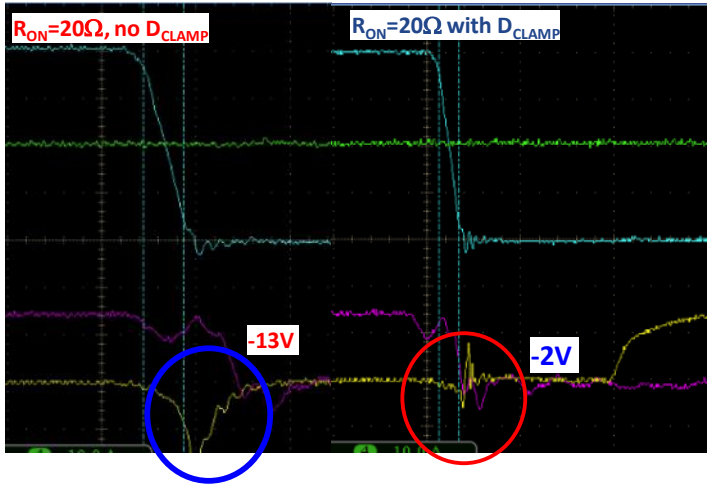
- Occurs at turn-on of the complementary switch in half bridge
- Keep V_{GS-_pk} within -10V
- Strong pull-down (low R_G/R_{OL}) and low L_G for lower ringing
- V_{GS} may bounce back >0V (LC ringing): ensure $V_{GS+\_pk} < V_{G(TH}$ to avoid false turn-on or gate oscillation

Control miller effect

- For negative dv/dt, it is important to have a low-Z path for the reverse miller current to reduce the negative V_{GS} spike (and the ringing afterwards caused by LC resonance)
  - Pay attention to the V_{GS} spike around V_{DS} <50V due to the change of non-linear C_{ISS}/C_{RSS} ratio
  - A clamping diode is recommended for gate drive with single output. For gate drive with separate sink output the diode may not be needed depending on the R_G and L_G in the circuit
  - For bipolar gate bias, use a TVS diode in series with the clamping diode (or two back to back)
  - *C_{GS} may not help in some cases, be careful! (induce LC resonance with L_{gate} and L_{CS})*
  - Negative gate bias can help to prevent false turn-on, but ensure worst case Vgs-_pk within -10V



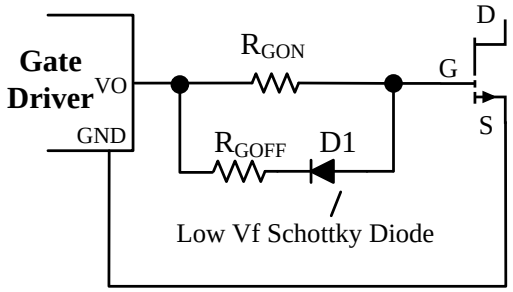




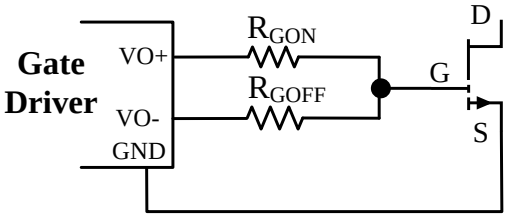
Control miller effect

Select right gate resistor

- GaN E-HEMT speed can be easily controlled by gate resistors
- Critical to choose the right $R_{G(ON)}/R_{G(OFF)}$ ratio for performance and drive stability
- Separate R_G for turn-on and off is recommended
- Recommend $R_{G(ON)}/R_{G(OFF)} \geq$ **5-10** ratio for controlling the miller effect
- GaN has extremely low Qg and drive loss: most cases 0402/0603 SMD resistors can be used
- Turn on $R_{G(ON)}$:
  - Control the turn-on dv/dt slew rate
  - Too high $R_{G(ON)}$ slows down switching and increases loss
  - Too small R_{GON}: High dv/dt -> Higher switching loss due to the miller turn-on and potential gate oscillation
  - For GS66508: recommend to start with $R_{G(ON)}$ = **10-20Ω**
- Turn off $R_{G(OFF)}$:
  - Typical starting value range is **1-2Ω**
  - Provide strong and fast pull-down for robust gate drive



Gate driver w/ single output



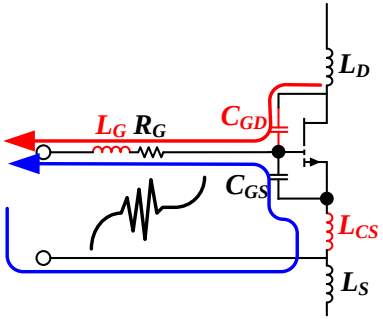
Gate driver w/ separate outputs

(Preferred)

Mitigate gate ringing/oscillations

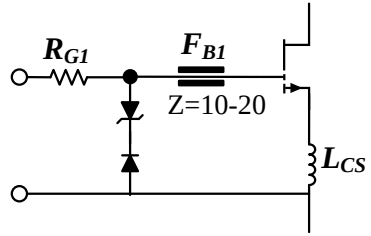
What causes the gate ringing/oscillation?

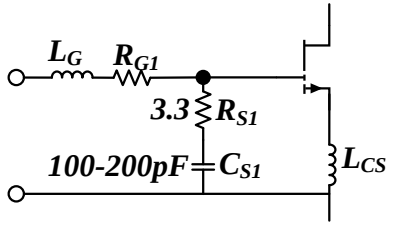
- Gate over/undershoot and ringing caused by high L_G
- Common Source Inductance L_{CS} Feedback path from power to gate loop (di/dt)
- Capacitive coupling via miller capacitor C_{GD} (dv/dt)



What to do if gate ringing/oscillation occurs?

- First improve the layout by reducing L_G, L_{CS} and external G-D coupling:
  - Locate driver as close to gate as possible
  - Low inductance wide PCB trace and polygon
  - Use kelvin source connection to minimize L_{CS}
- Select right R_G to tune turn-on slew rate
- Try negative gate bias (-3V) for turn-off
- At last resort try circuits below to damp the high frequency LC ringing & overshoot:
  - Use a ferrite bead with Z=10-20Ω@100MHz in series with gate. (ferrite bead may increase L_G but damp the high frequency gate current ringing)
  - RC snubber across G-S: example R=3.3/C=200-470pF

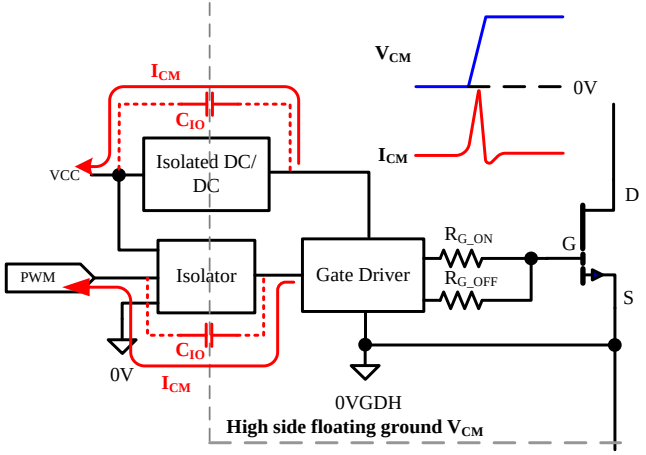




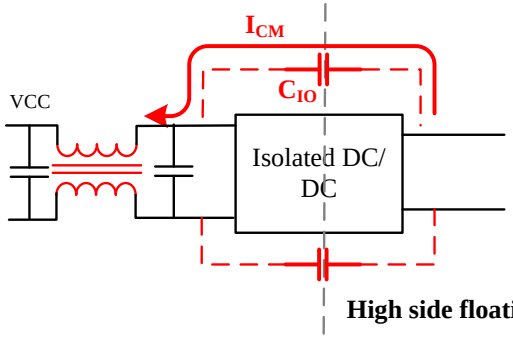
High side driver considerations

High side gate drive

- **GaN enables fast switching dv/dt >100kV/us:**
  - Minimize Coupling capacitance C_{IO}
  - CM current via C_{IO} limits CMTI
  - Use isolator/isolated gate driver with high CMTI
- **Full Isolated gate drive:**
  - Best performance
  - Isolation power supply – Minimize inter-winding Capacitance
- **Bootstrap:**
  - Common for lower voltage 100V half bridge design
  - Lower cost and simpler circuit
  - ***Choose the bootstrap diode with low C_j and fast recovery time. Watch for bootstrap diode power loss limit and recovery time for high-frequency operation.***
  - Post-regulation or voltage clamping may be required after bootstrap

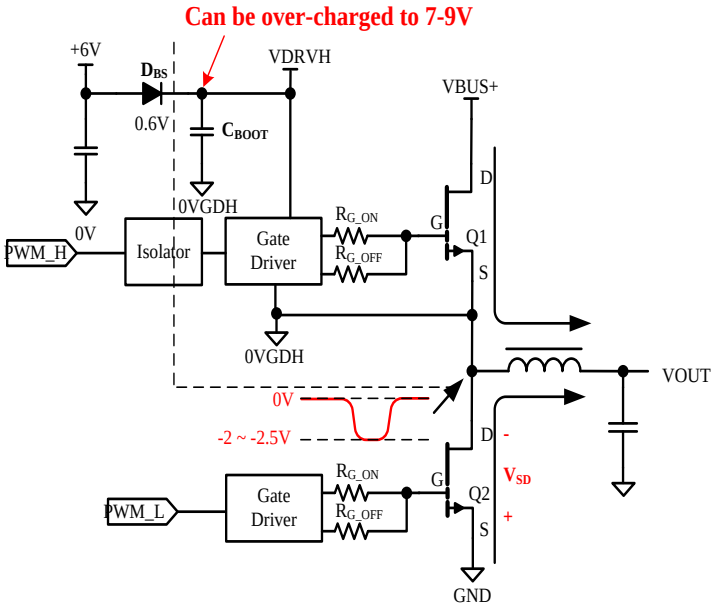


Optional common mode choke at input side to suppress CM noise



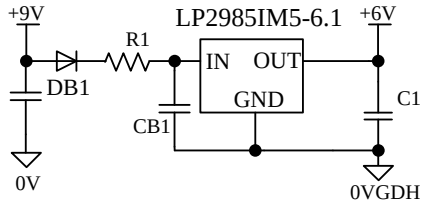
Bootstrap circuit

- Good for low cost 0-6V gate drive, need additional offset circuit for bipolar drive
- What is the problem with traditional bootstrap circuit?
  - GaN E-HEMT requires good regulation of gate bias (5-6V bias, max rating 7V)
  - LS free wheeling: Switch node negative voltage overcharges bootstrap capacitors (V_{GS}>7V)
  - HS free wheeling: Bootstrap diode voltage drops reduces V_{GS} below 6V
- Post-regulation or voltage clamping to ensure high side bias <7V

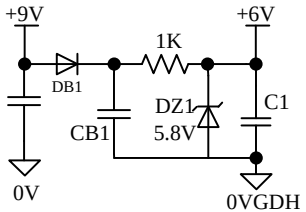


Bootstrap with post-regulation using +9V for regulated high side bias

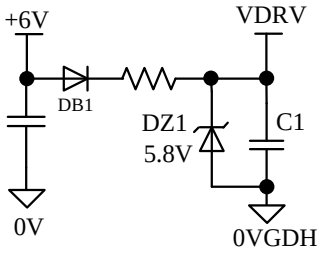
Use LDO to regulate to 6V



Use Zener diode



Bootstrap for Sync Buck (only need to clamp overcharge, example 100V sync buck)



Simple Zener diode to clamp to 6V

Criteria for selecting GaN E-HEMT gate drivers

- Choose gate driver with VDD and UVLO range that is compatible with 5-6V gate drive:
  - For 0-6V drive bias: use UVLO ≤ 4-5V (designed for 5V FET gate drive)
  - For -3/+6V bipolar drive: use driver designed for 9V gate drive (UVLO < 8V)
- Low pull-down resistance and high sink current to minimize miller effect:
  - Recommend ≥ 4A sink current (turn-on peak current requirement can be relaxed)
  - Low pull-down resistance,
  - Separate pull-up and down output pins preferred
- Isolated gate driver:
  - dv/dt CMTI rating: at minimum 50kV/us, preferred ≥100kV/us
  - Propagation delay matching: It affects the minimum dead time for half bridge. At minimum isolated driver with <100ns delay matching should be used, preferred <50ns
- Capable of high frequency operation: Fsw ≥ 1MHz
- 100V half bridge driver for GaN:
  - All above except isolation. Typically 100V driver is non-isolated with bootstrap. Voltage clamping or regulation is required after bootstrap
  - ≥ 1-2MHz operation with tightly matched propagation delay matching (≤20ns)

Gate driver recommendation

For 650V GaN half bridge (Totem pole PFC/LLC/Full bridge/Inverter):

- SiLab Si827x series (high CMTI >200kV/us, low UVLO for 6V), recommended P/N:
  - Single channel **Si8271** (single w/ split output)
  - Half bridge **Si8273/4/5** (HS&LS, PWM with DT Adj or dual)
  - Use 3V UVLO version (XX-GB) for unipolar 6V gate bias. For +6/-3V bipolar drive either 3V or 5V UVLO (XX-AB) version can be used
- Analog device half bridge driver **ADuM4223A/B** (footprint compatible with Si8273/4)

For non-isolated low side application (Flyback, Class E PA, Boost, SSSR), 100V or 650V

- Taxes Instruments **LM5114/UCC27511**/Maxim **MAX5048C** (footprint compatible)
- Can also be used with isolator for high side drive, or as secondary gate drive for adapting existing 12-15V gate driver
- Other verified low side drivers: **FAN3122**, **FAN3224/5** (dual), **LTC4441/MCP1407/IXDN609SI/TC4422**

100V half bridge (48V-12V Sync Buck, Inverter, Class D PA)

- TI **LM5113** (5V VCC)
- Linear Tech **LTC4444-5** (Synchronous MOSFET driver, 5-6V VCC)
- Linear Tech **LTC3895** (Sync. Step-down DC/DC controller)

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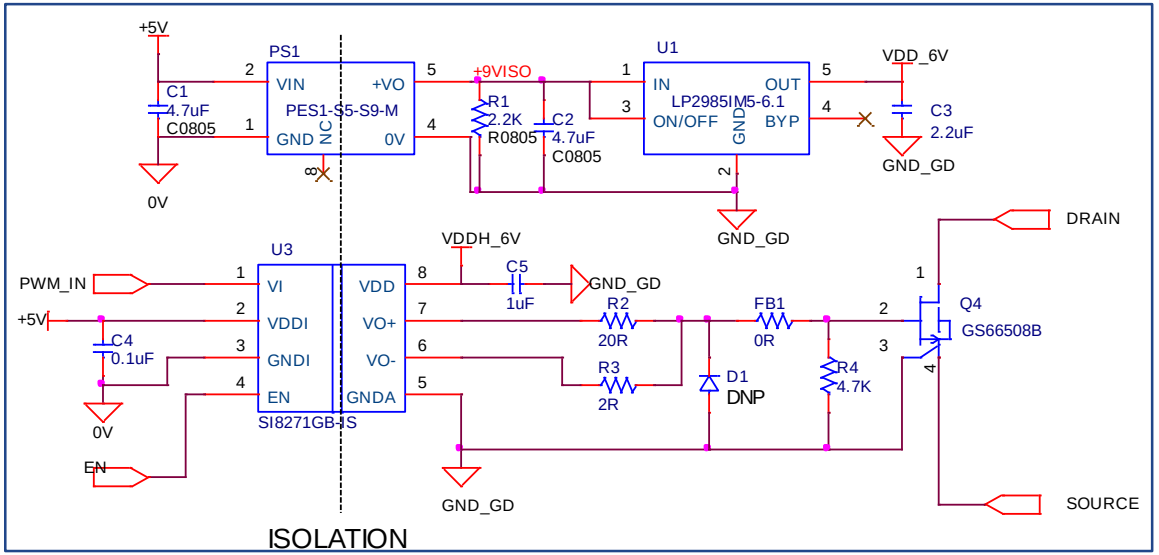
650V GaN Gate Drive Design – Unipolar gate drive

Fully isolated unipolar drive based on Si8271GB-IS

- **Pros:** Simple implementation, low dead time reverse conduction loss
- **Cons:** More sensitive to layout patristics compared to bipolar drive, gate drive layout and turn-on speed needs to be optimized for hard switching topology.
- Optional ferrite bead (use 10-20Ω@100mhz) and clamping diode for gate spikes/ringing

Applications:

- Good for high frequency ZVS application (no hard switching, lower dv/dt but dead time conduction loss is more critical)
- Application with tight optimum gate drive layout (lower power)



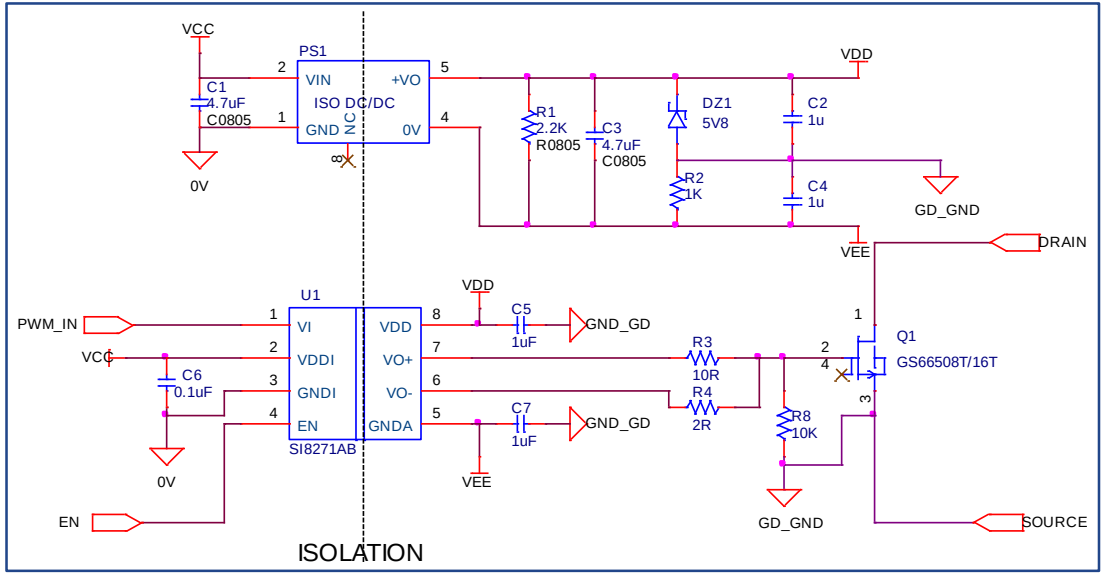
650V GaN Gate Drive Design – Bipolar gate drive

Fully isolated bipolar drive based on Si8271AB-IS

- **Pros:** Lower risk of cross conduction/gate oscillation, faster turn-on (lower switching loss), higher UVLO drivers can be used for GaN
- **Cons:** higher dead time reverse conduction loss (minimize dead time), it is a trade off between switching and dead time loss
- Use DZ1/R2 to split 9V to +6/-3V and create a biased gate return. No additional LDO is required as negative bias voltage regulation can be more relaxed

Applications:

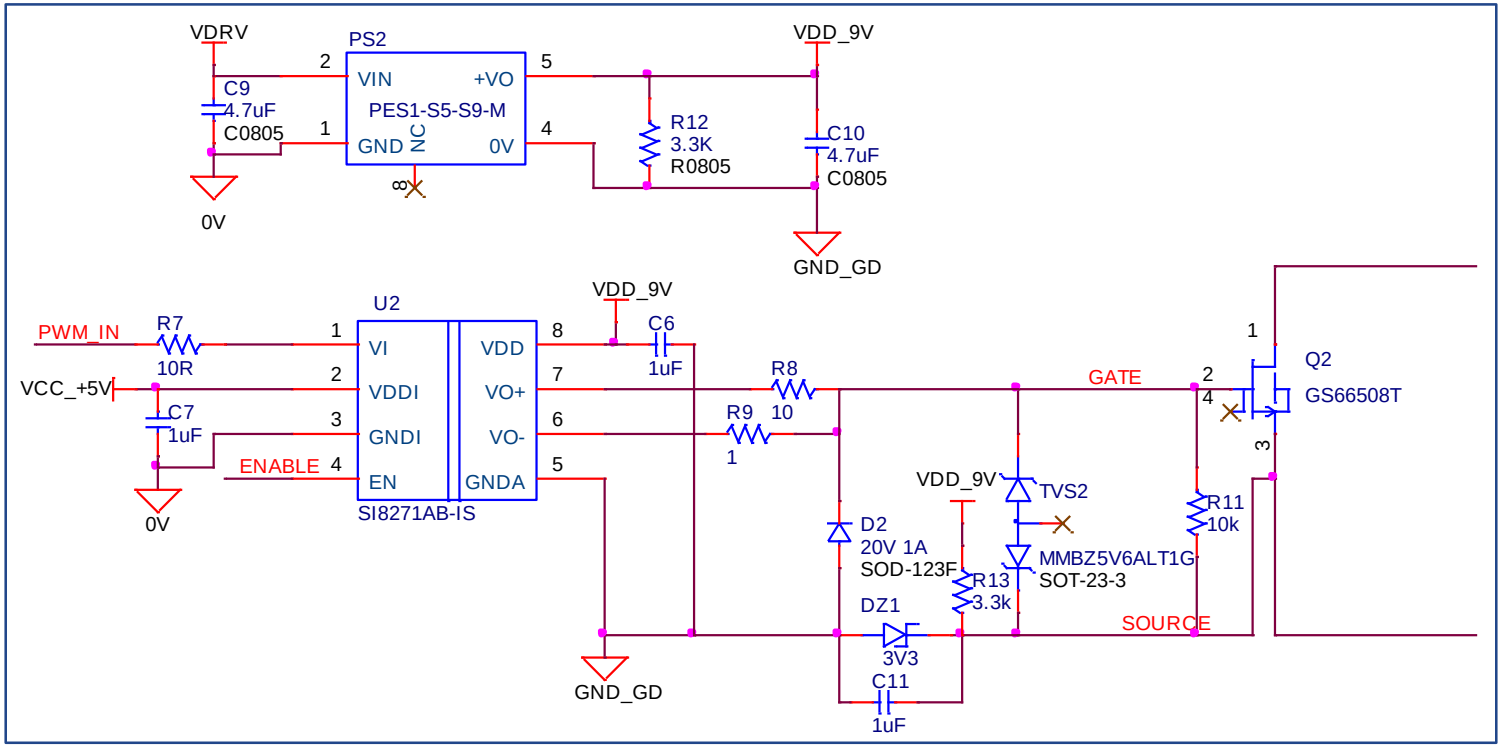
- Applications where tight gate layout is difficult due to PCB and thermal design
- Hard switching with relatively lower F_{SW} where switching loss dominates and dead time loss is less critical



650V GaN Gate Drive Design – Bias offset circuit

Offset circuit to generate +6/-3V from single 9V bias (isolated grounds)

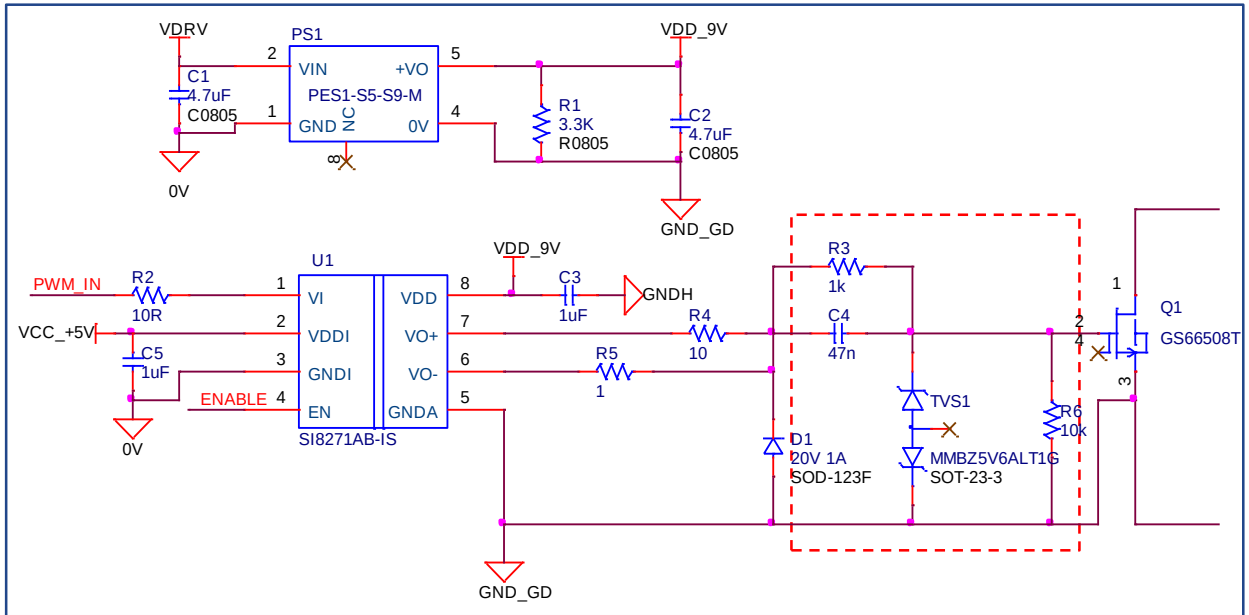
- With single end isolated 9V supply (return isolated from power ground), you can use this bias offset circuit to easily create -3V bias
- After startup, C11 will be charged by VDD and R13 until clamped by DZ1



650V GaN Gate Drive Design – Bias offset circuit

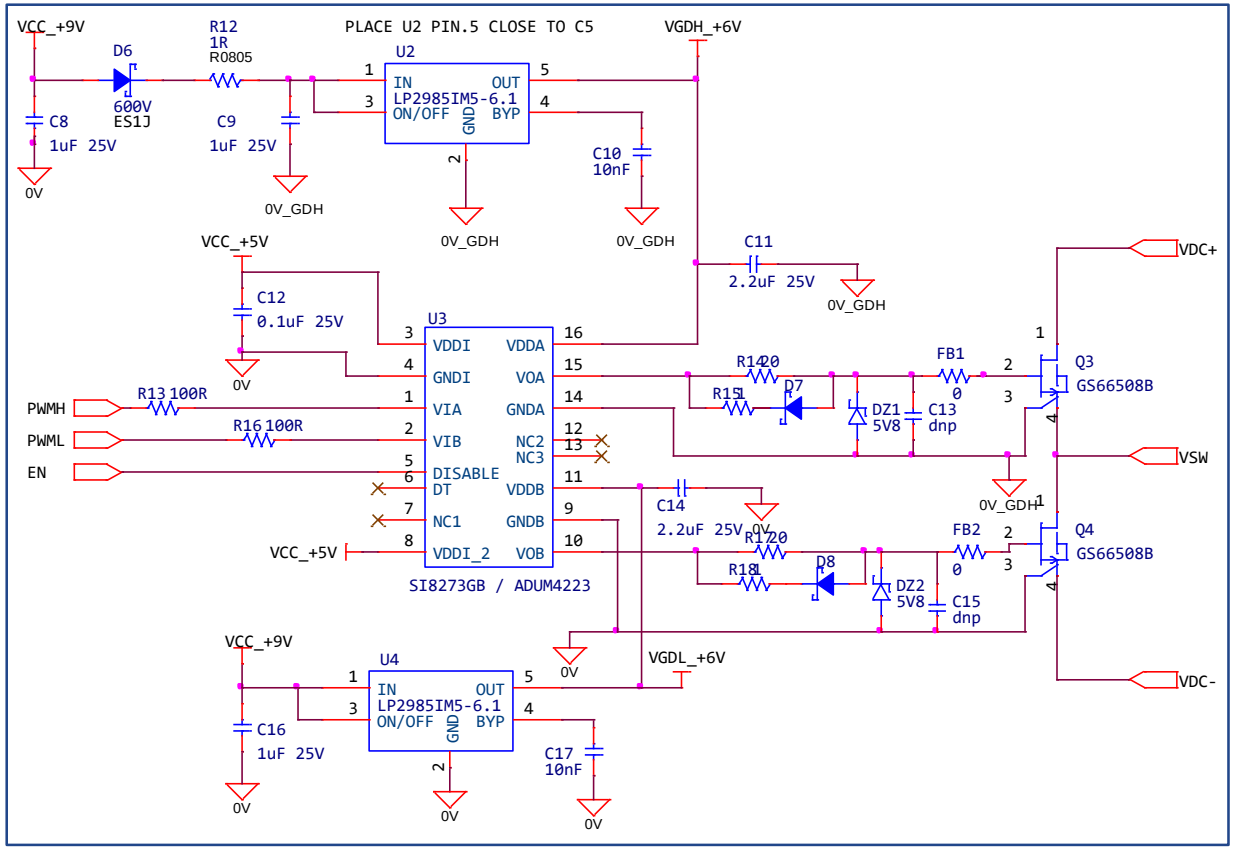
Bias offset circuit to generate +6/-3V from single 9V bias (bootstrap or common grounds)

- For bootstrap or low side with common ground between gate drive and power returns, the bias offset circuit needs to be at the gate side
- Back to back fast TVS diodes clamps gate signal to +/-6V
- C2 will be charged up to the remaining voltage (9-6=3V) after first turn-on pulse
- When turned off, C2 adds -3V bias to the G-S
- R2 supplies DC gate leakage current to maintain DC +6V on the gate



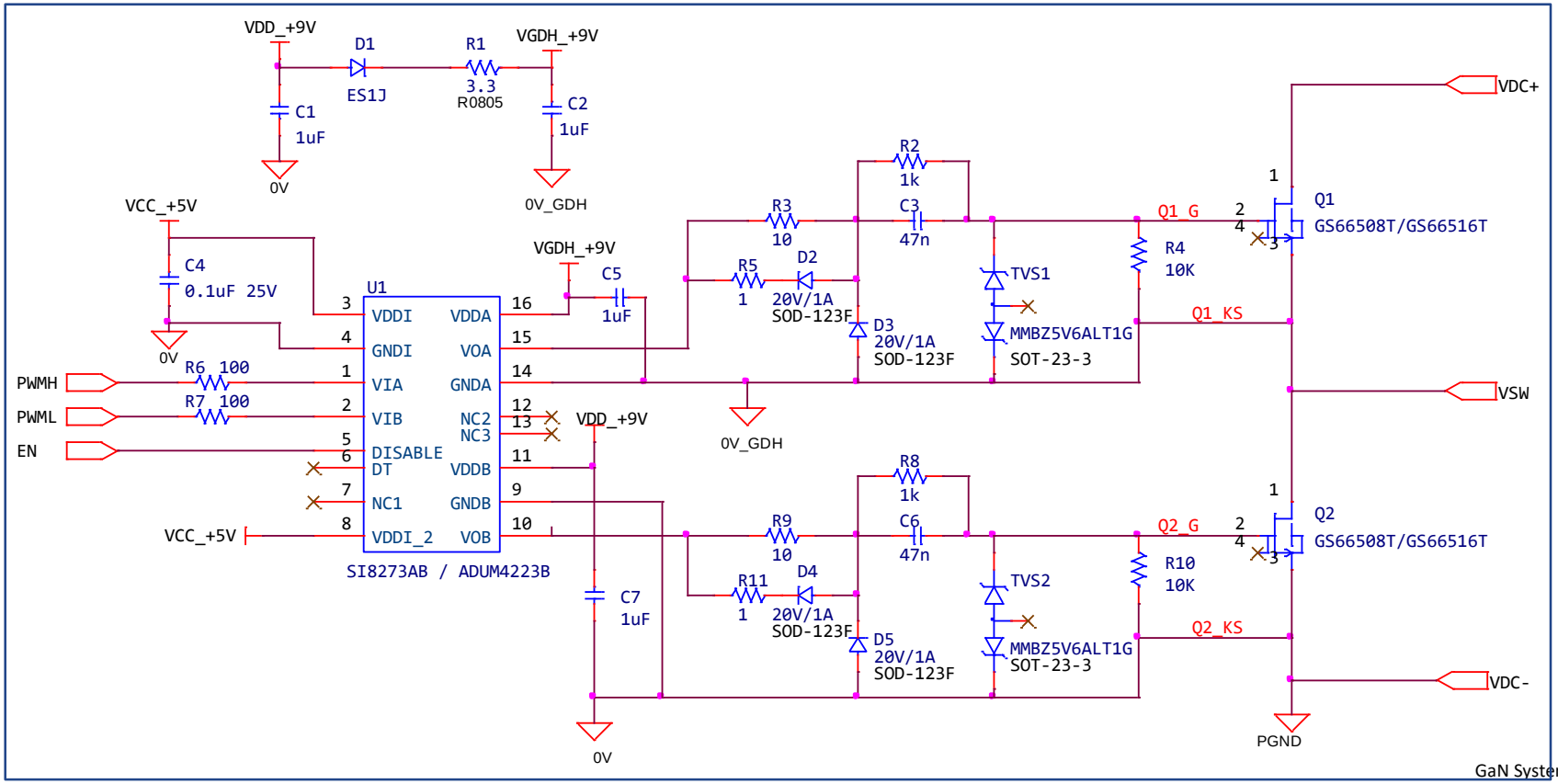
650V GaN Gate Drive Design – non-isolated bootstrap

- Non-isolated bootstrap circuit is preferred for cost sensitive design
- Based on half bridge driver Si8273 (or Adum4223)



650V GaN Gate Drive Design – non-isolated bootstrap

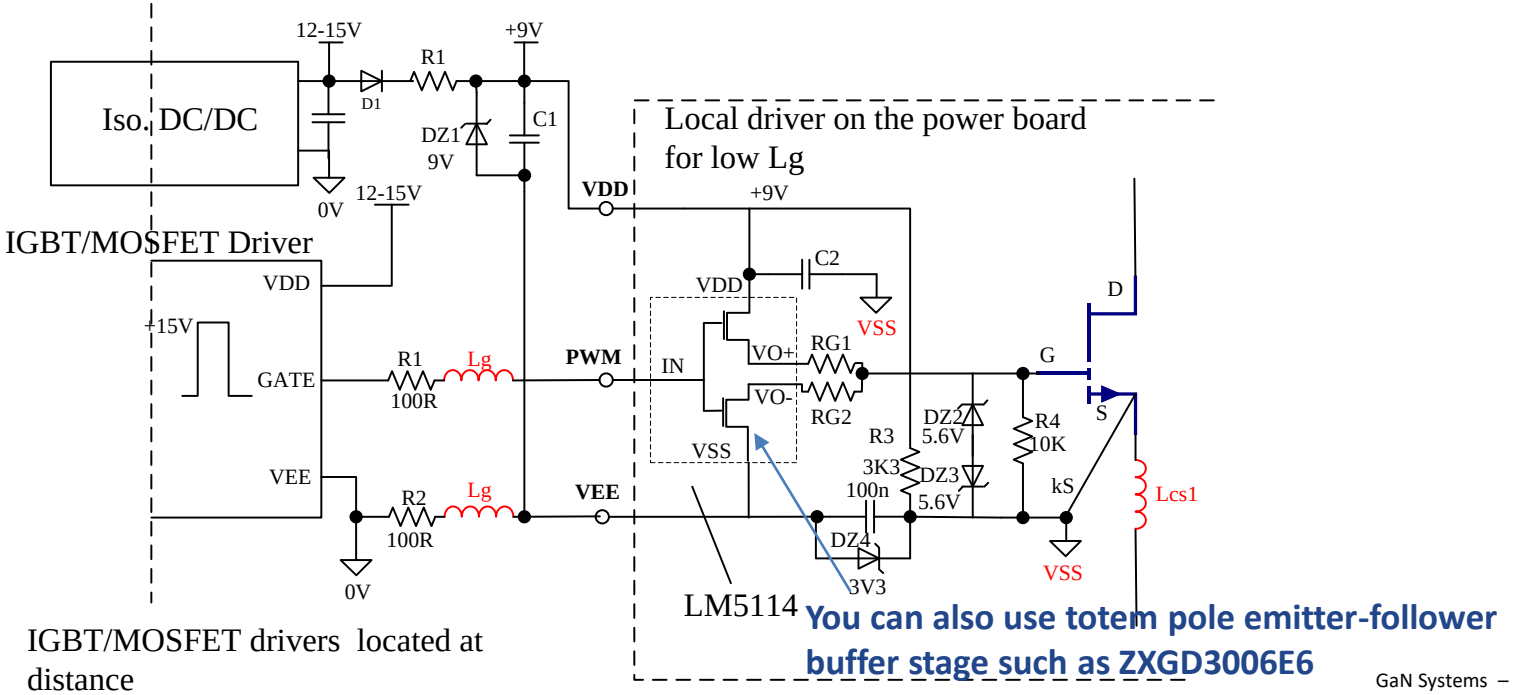
- Non-isolated bootstrap with half bridge gate driver
- 9V VDD with bias offset circuit for +6/-3V



650V GaN gate drive design ideas

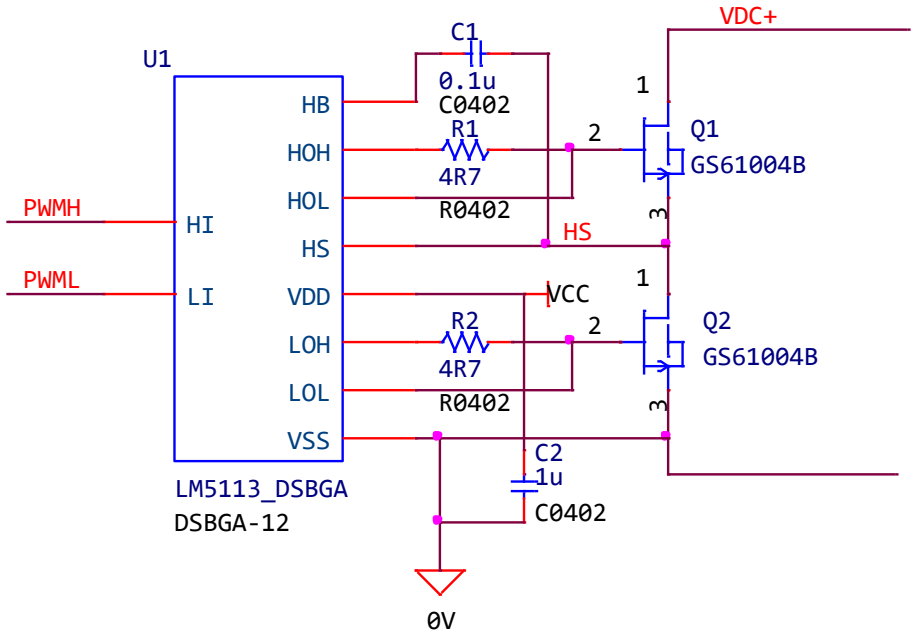
Use secondary local driver for adapting IGBT/MOSFET gate drive signals

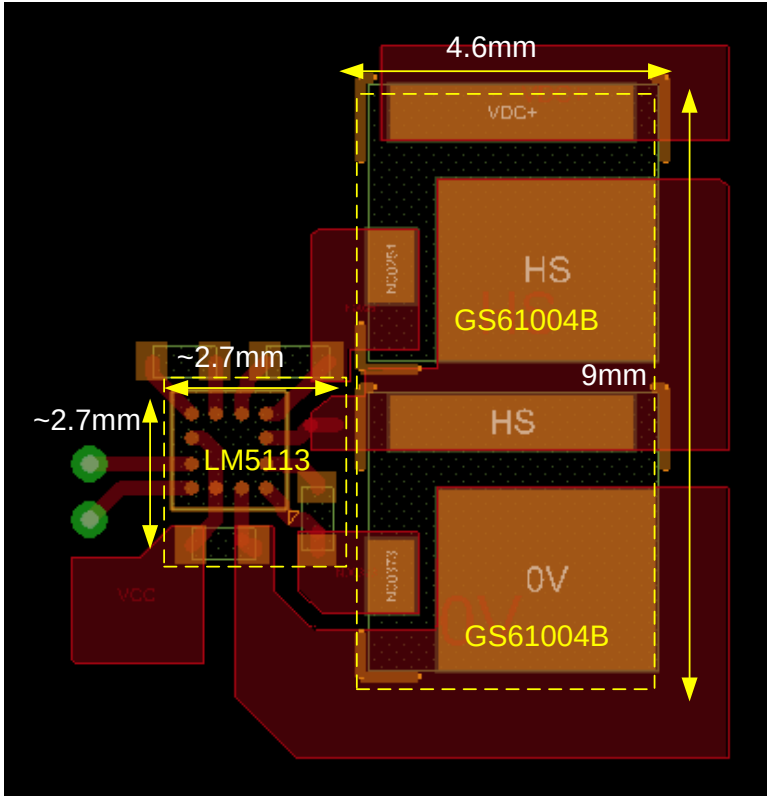
- Provide local optimum gate drive layout excluding high L_G and L_{CS}
- Allows longer distance between GaN and controller/driver for control/power board(module) design
- The isolated IGBT/MOSFET driver needs to be able to handle high CMTI dv/dt (>50kV/us, 100kV/us preferred)



100V half bridge design example

- GS61004B Half bridge using LM5113 for 48V DC/DC
- Discrete design compared to other integrated GaN module:
  - Comparable device performance
  - Similar PCB area (~49mm^2 including 2x GS61004B. LM5113 and R1/R2, excl. C1/C2)
  - Better thermal performance than integrated solution



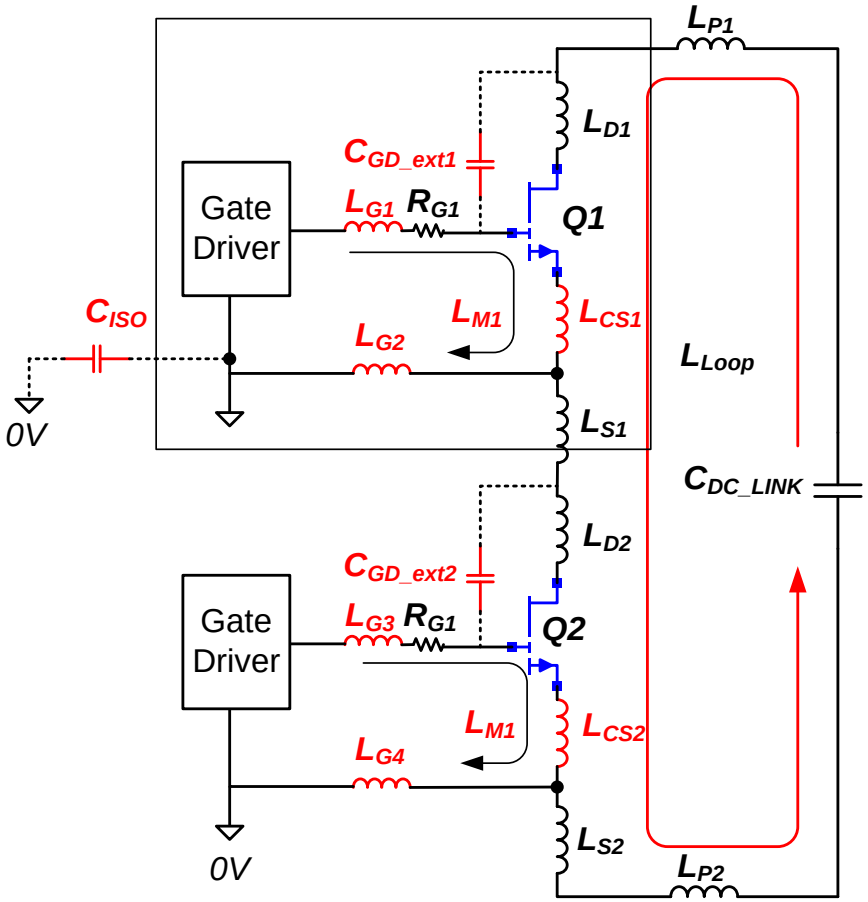


Agenda

- ❑ Basics
- ❑ Gate Drive Design considerations
- ❑ Design examples
- ❑ PCB Layout
- ❑ Switching Testing results

PCB Layout Checklist

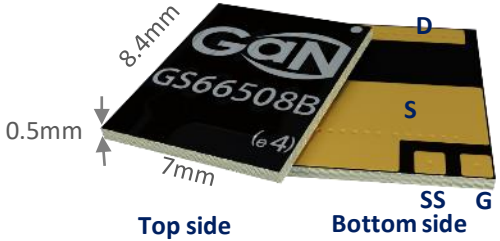
- Design for GaNPx embedded package
  - GaNPx bottom cooled B/P
  - GaNPx Top cooled
  - Thermal design
- Optimize and minimize layout parasitics in following orders :
  1. Common source / mutual inductance L_{CS}
  2. Gate loop inductance L_G
  3. Power Loop inductance L_{loop}
  4. Drain to gate loop capacitance C_{GD_ext}
  5. Isolation coupling capacitance C_{ISO}

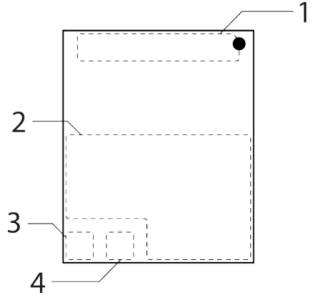


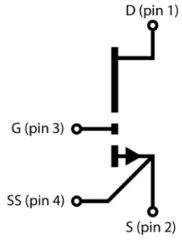
GaN*PX*™: Bottom cooled B type family

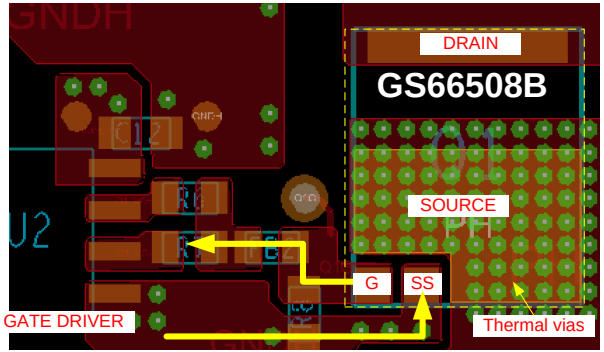
- Embedded package with extremely low inductance
- GS66508B includes dedicated kelvin source pin (SS)
- PCB cooling using thermal pad (S) and vias or metal core PCB for high power application

GS66508B (650V, 30A, 50mΩ)



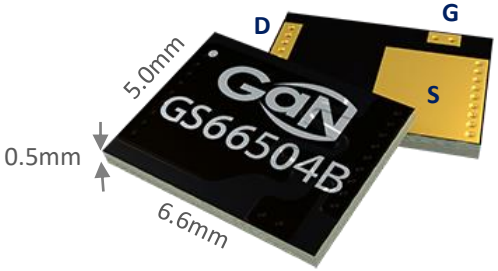




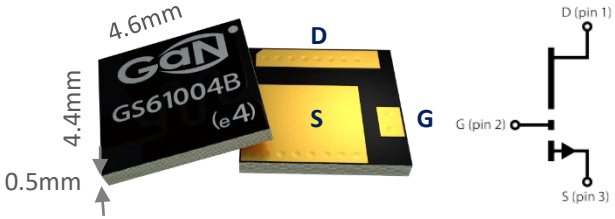


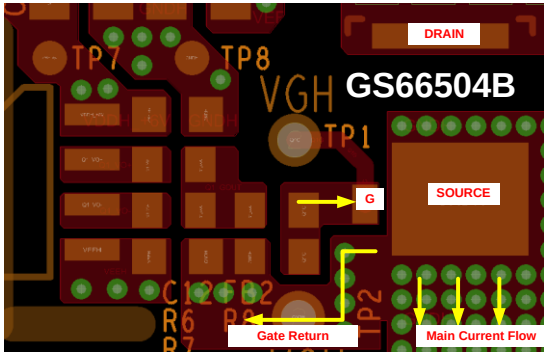
Use SS pin for gate return

GS66504B/GS66502B (650V, 15/7A, 100/200mΩ)



GS61004B (100V/45A, 15mΩ)



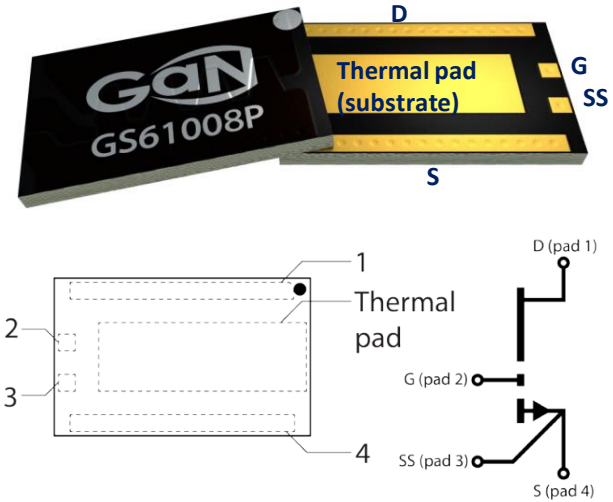


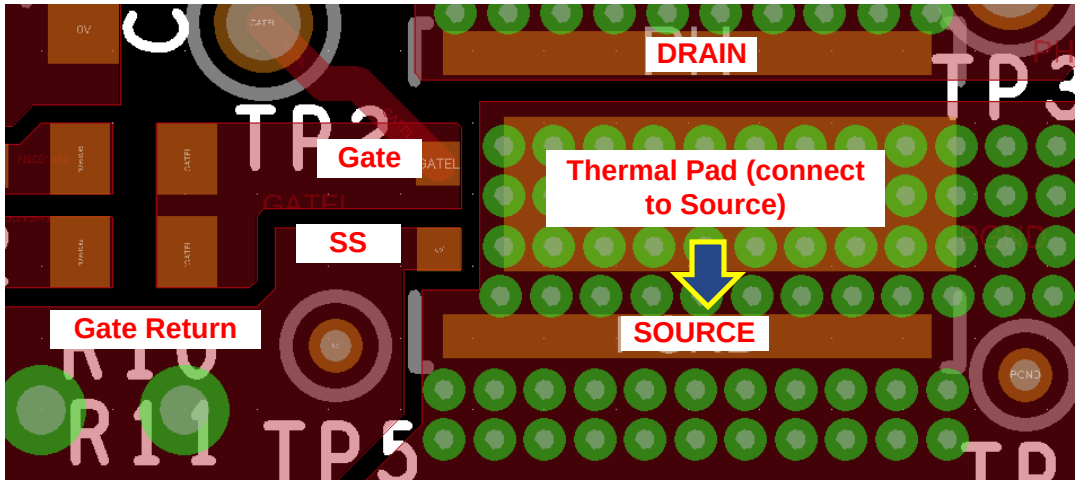
Create Kelvin source on PCB

GaN*PX*™: Bottom cooled P type

- Similar to B type except substrate (thermal pad) is floating on the package
- Use SS pin for kelvin source connection
- **The thermal pad must be always connected to its source pin on PCB**

GS61008P (100V/90A, 7.5mΩ)

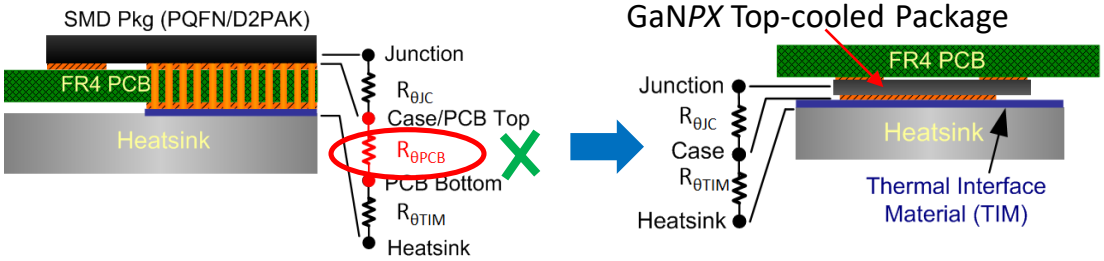




GaN*PX*™: Top cooled T Package

Eliminates the PCB from the thermal path:

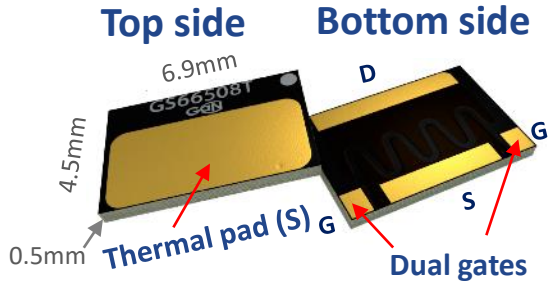
- Improved thermal performance
- Simplifies PCB layout
- Improved parasitics and higher power density



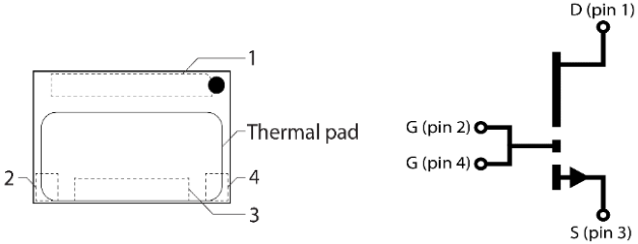
Design with T package

- Symmetrical dual gates for flexible layout, either one can be used for gate drive, easy for paralleling
- Create kelvin source on the PCB at the side
- Watch for creepage/safety isolation and mechanical overstress (pressure/bending force) on GaNpx

GS66508T (650V/30A, 50mΩ)



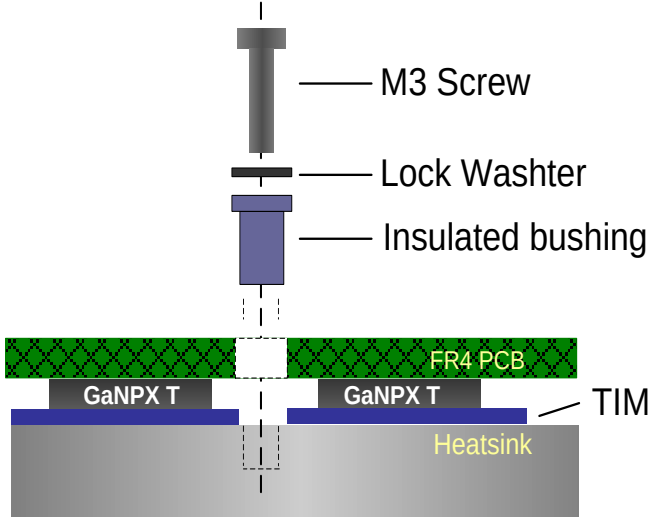
Thermal pad internally connected to Source. However it is not designed for carrying current



GaNPx T package - Mounting Techniques

Center mounting hole

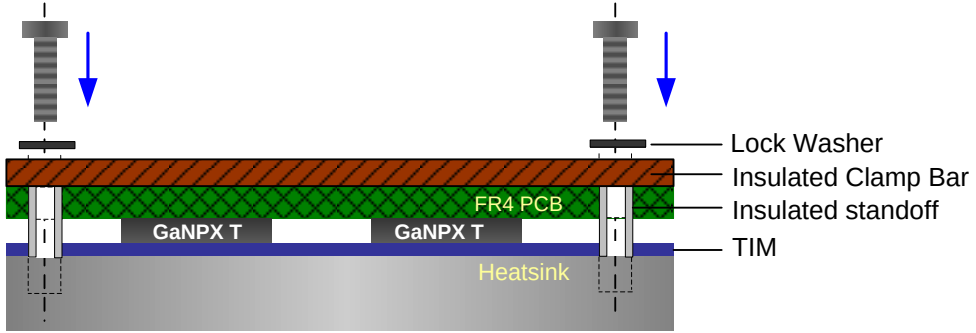
- Balanced pressure across 2 devices
- Typical recommended maximum pressure ~50psi: For M3 screw with 2 devices: ~2in-lb for GS66508T and 4in-lb for GS66516T
- Tested up to 100psi without failure
- Suitable for small heatsink attachment



2 or more mounting holes for large heatsink

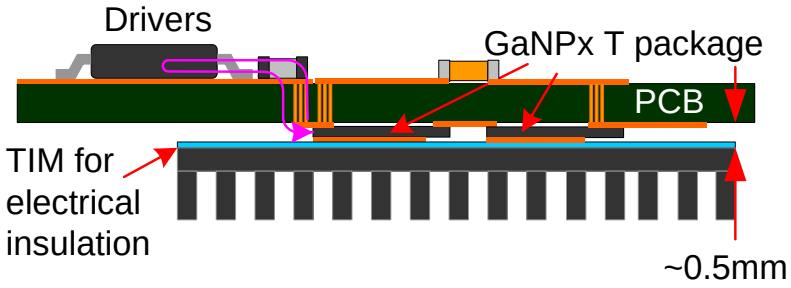
More susceptible to PCB bending stress:

- Excess PCB bending causes stress to GaN*PX* and other SMD parts which should be avoided
- Locate mounting Holes close to GaN*PX*
- Recommended to use a supporting clamp bar on top of PCB for additional mechanical support



Thermal design solutions with T package

GaNPx T package on the opposite side



- GaNPx located on bottom side for direct heatsink/Chassis attachment

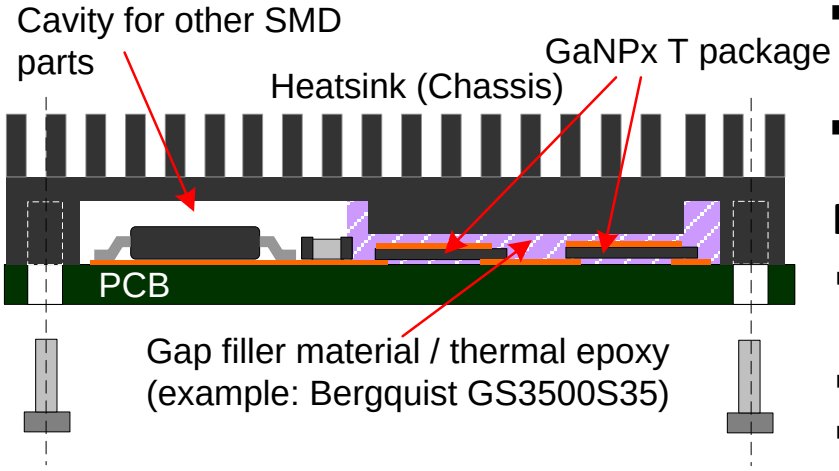
Pros

- Good thermal performance
- Simple heatsink design

Cons

- Mechanical stress
- Creepage distances
- Longer gate loop

GaNPx T package on the same side



- GaNPx at same side with other components
- Heatsink mounted to PCB with cavity to define the gap and accommodate other parts
- Fill the gap with gap filler or thermal epoxy

Pros

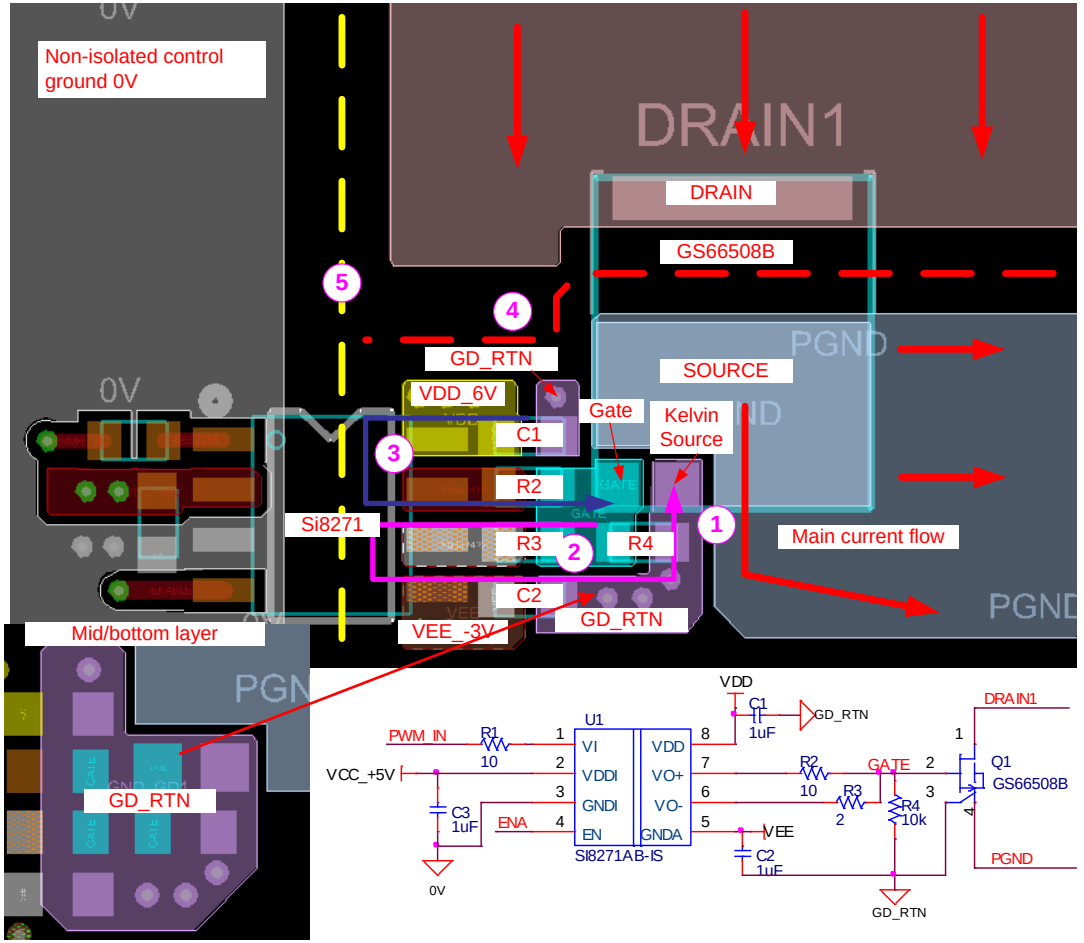
- No direct mechanical stress to GaNPx
- Single side placement
- Tight gate drive layout

Cons

- Higher thermal resistance
- Complicated Heatsink design

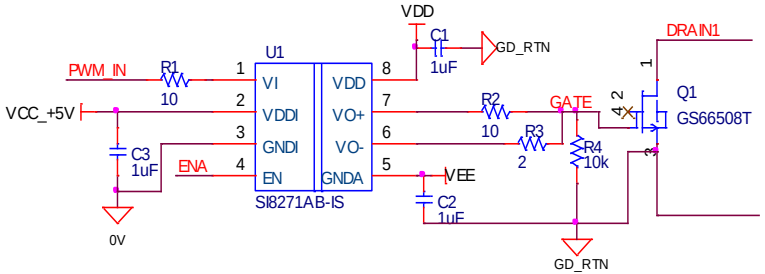
Layout best practice – Gate Drive

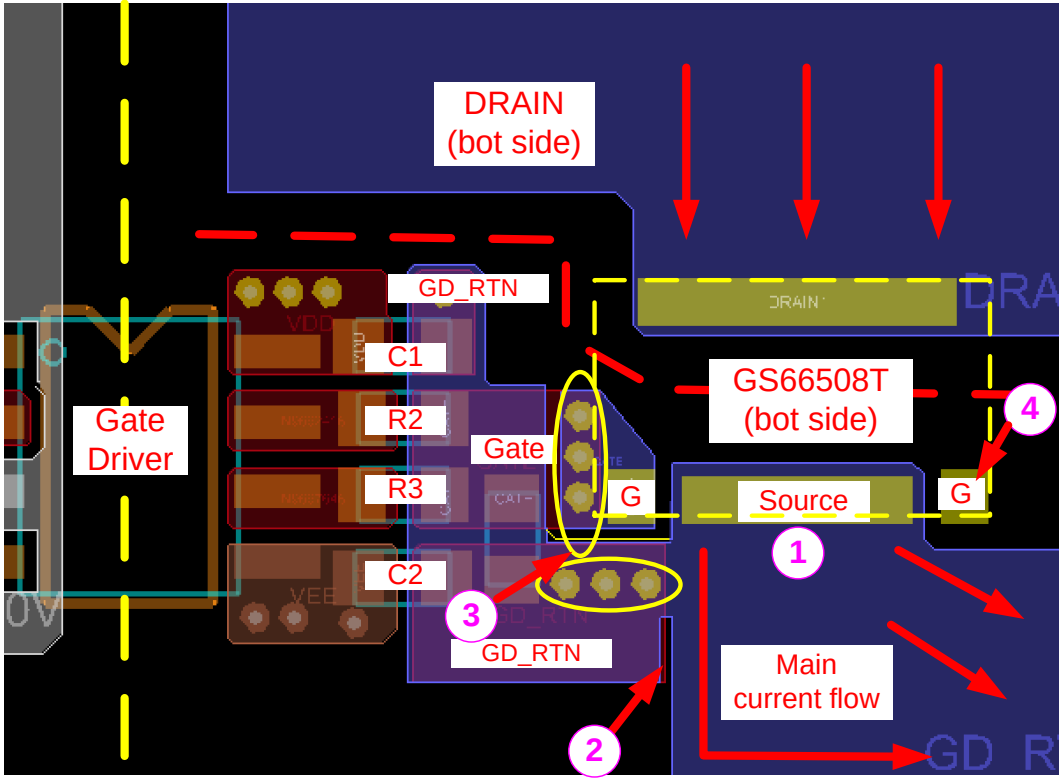
1. Use/create kelvin source to separate drive return and power ground (low L_{CS}). Physically separate high current loop and drive loop areas to minimize noise coupling
2. Minimize pull-down loop (Gate→R3 → U1 → C2 →GS_RTN, locate U1 and C2 close)
3. Minimize turn-on (pull-up) loop (locate C1 close)
4. Isolate and avoid overlap between gate drive and Drain copper pour
5. Isolate and avoid overlap from Drain/Source to the control grounds (CMTI, dv/dt)



Layout best practice – Gate drive with T package

1. GaNPx T package located at bottom side for heatsink attachment
2. Create kelvin connection to the source for Gate drive return (bottom side)
3. Use multiple vias for lower gate inductance from bottom to top side
4. Use one gate and keep the other floating



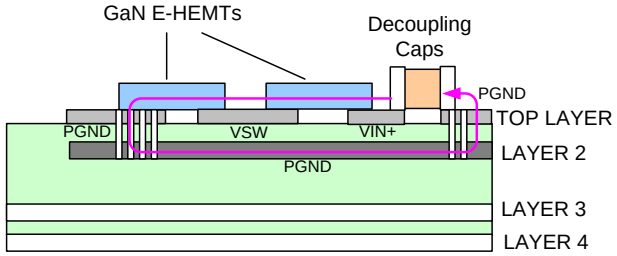


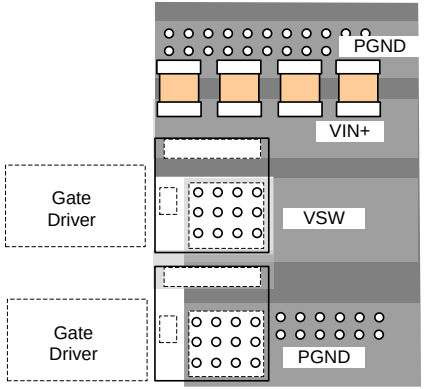
Layout best practice – Half bridge power stage

Design the half bridge power stage with tight loop and low inductance

Half bridge design 1

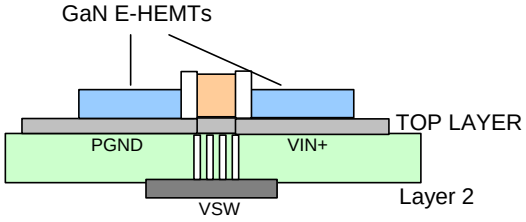
Use layer 2 as ground return (4-layer PCB)

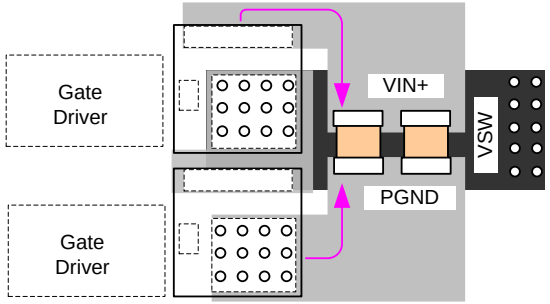




Half bridge design 2

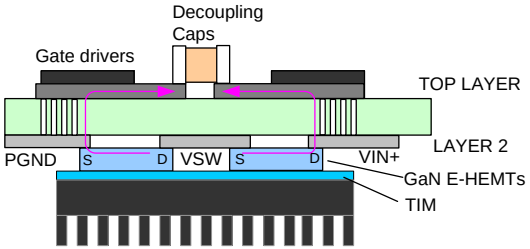
Only use top layer for power loop

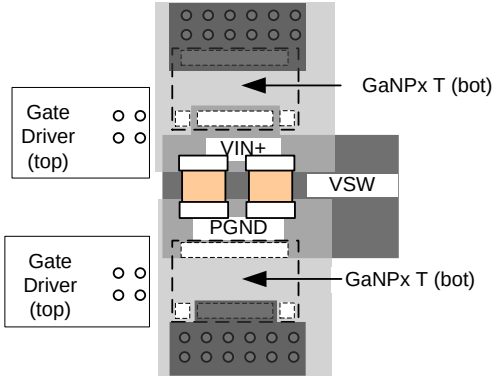




Half bridge design 3 (T Package)

For T package mounted on the bottom side of PCB:

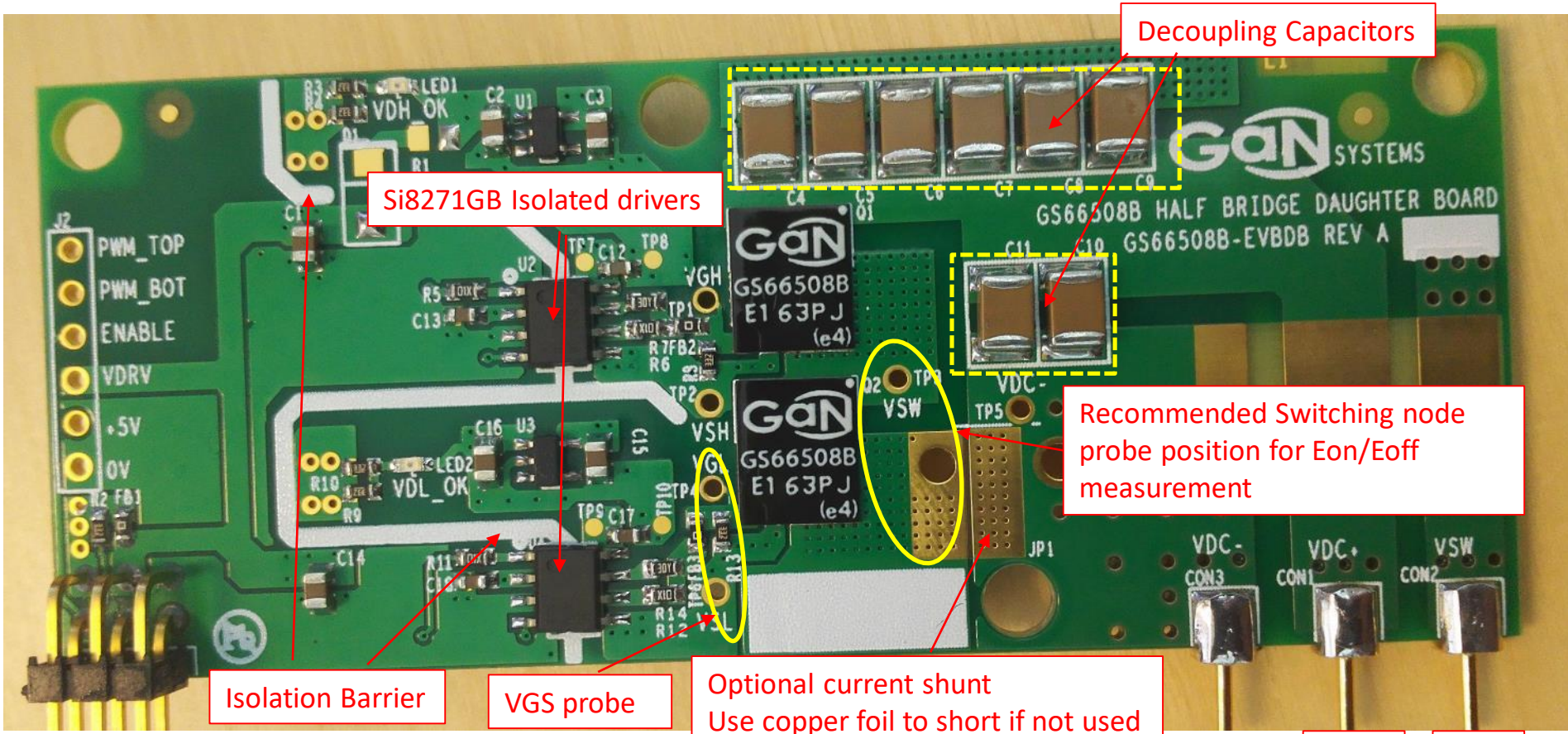




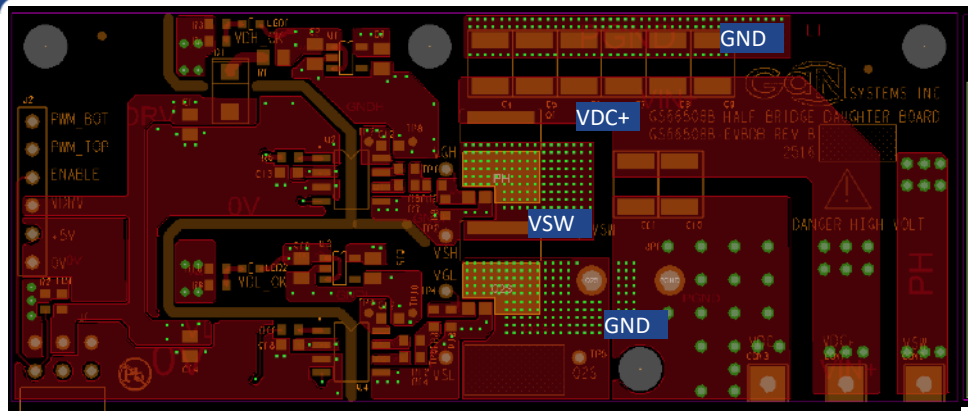
Agenda

- ❑ Basics
- ❑ Gate Drive Design considerations
- ❑ Design examples
- ❑ PCB Layout
- ❑ Switching Testing results

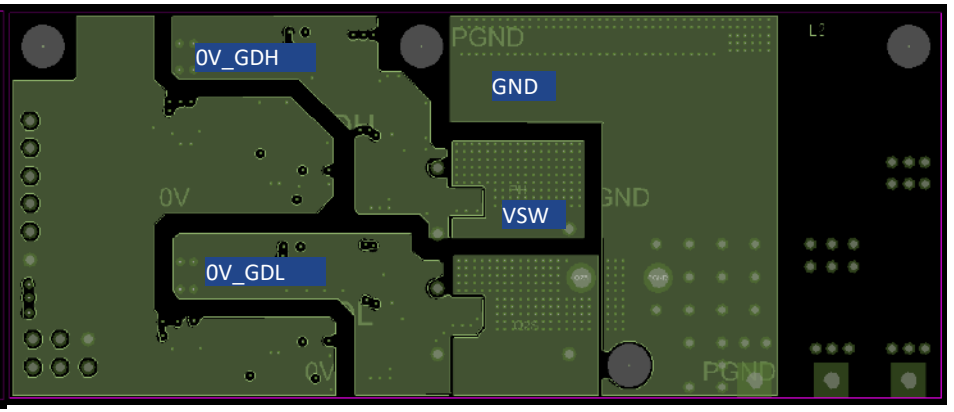
Switching Test – GS66508B Half bridge Eval board



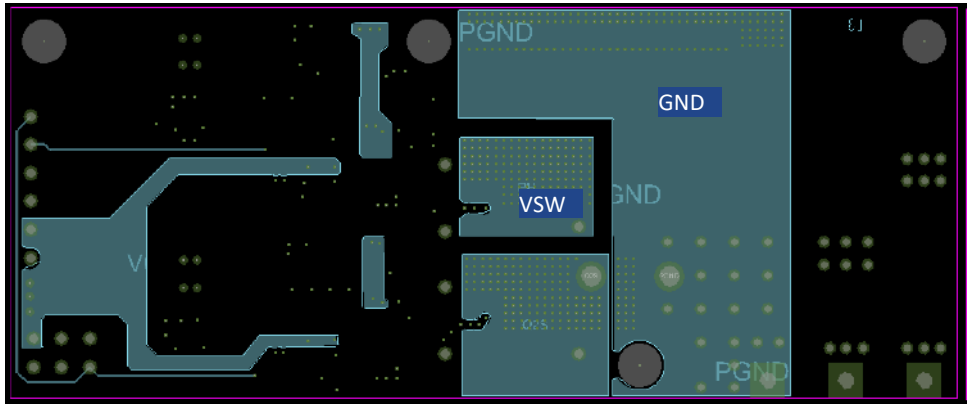
GS66508B-EVBDB PCB Layout



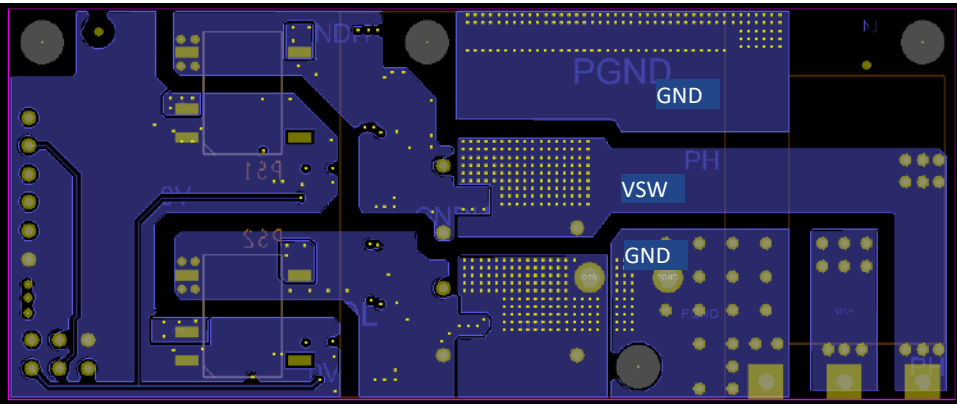
Top Layer



Mid layer 1



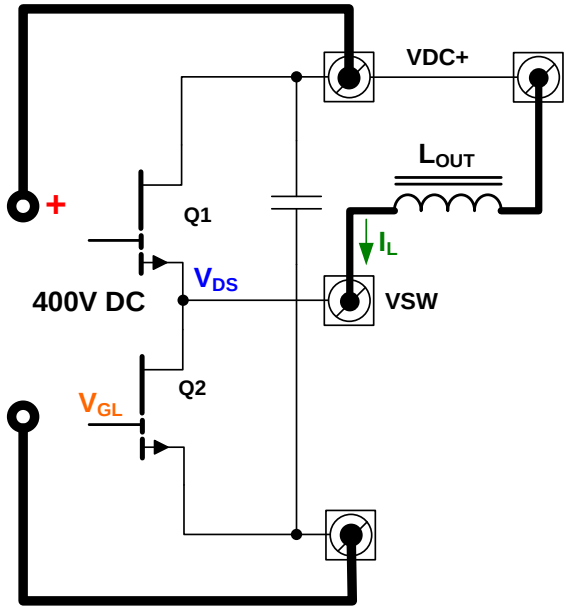
Mid layer 2

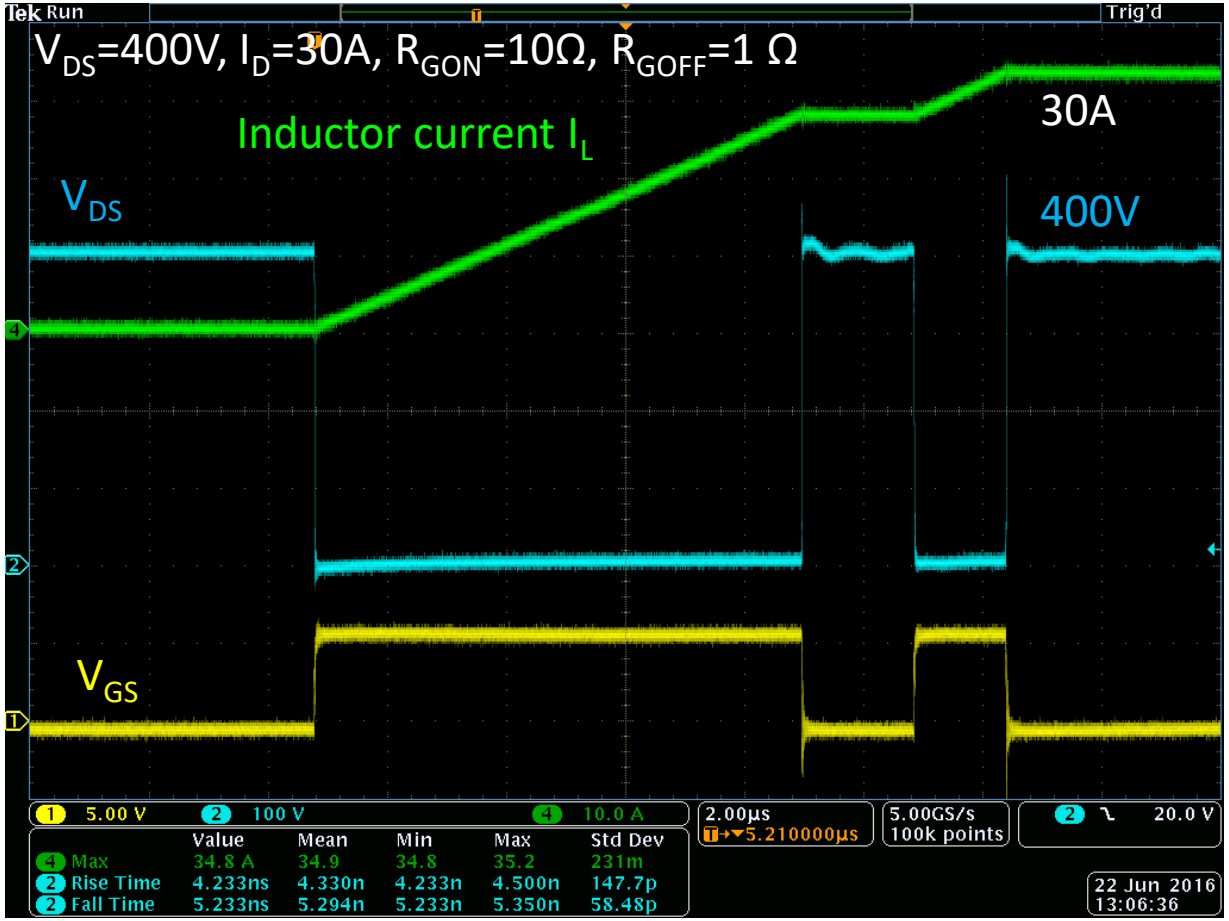


Bottom Layer

Double pulse switching test

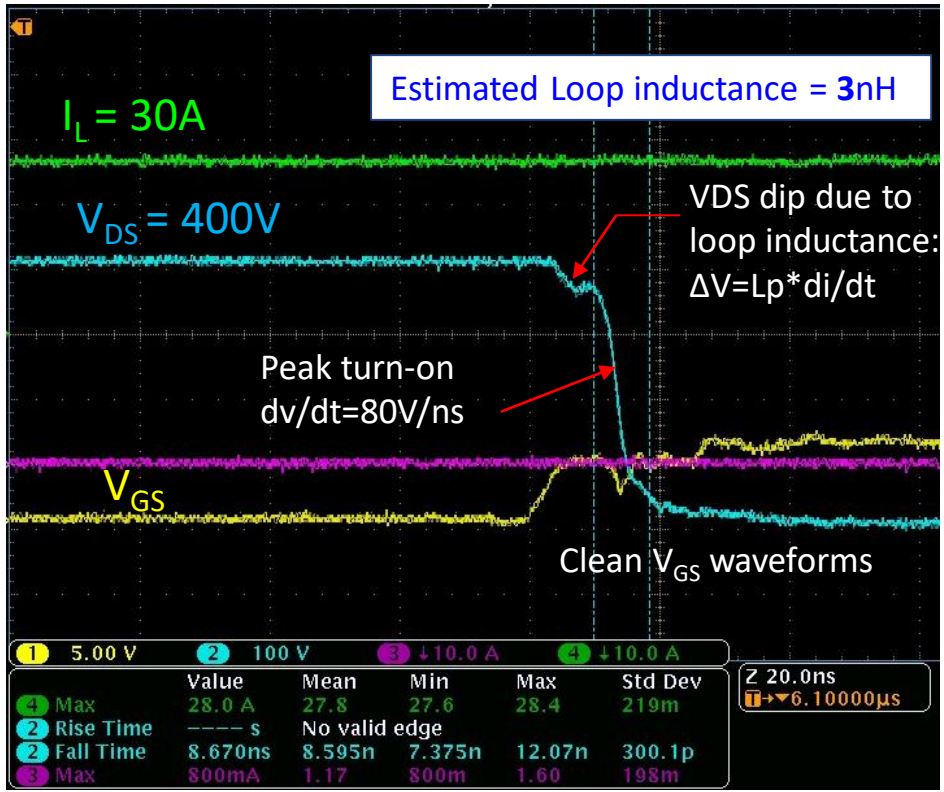
- GS66508B hard switched up to 400V/30A



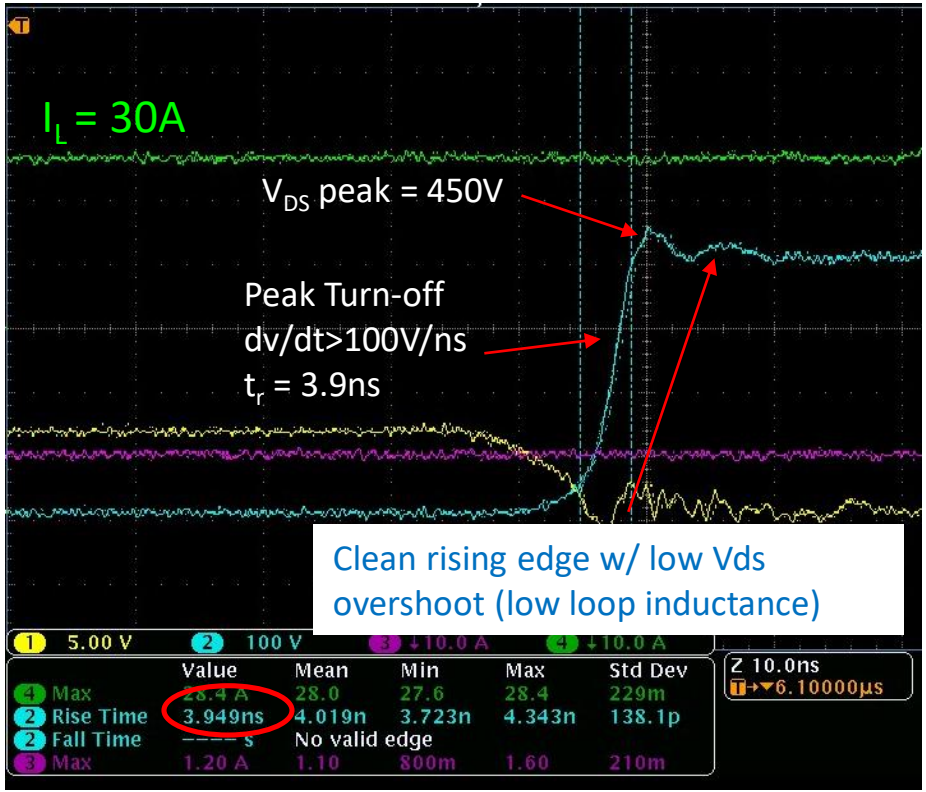


GS66508 Double pulse switching test

V_{DS}=400V, I_D=30A Hard Switching Turn-on



V_{DS}=400V, I_D=30A Hard Switching Turn-off



Summary

- This application guide summarized the key design considerations for GaN Systems GaN E-HEMTs. We started with the fundamental aspects of GaN E-HEMTs and then the gate drive design considerations were discussed. A list of recommended drivers and several gate drive reference designs were provided.
- The second part of this guide focused on the PCB layout and discussed the layout best practice by using GaN Systems Embedded package GaNPx.
- At last a real half bridge evaluation board design following the design recommendations in this document was built and its switching performance was tested.
- The switching test results showed fast and clean hard switching waveforms up to full rated current 400V/30A with minimum ringing/overshoot. This concluded that with optimum gate drive and board layout combined with low GaNPx inductance, GaN E-HEMTs exhibit optimum switching performance

Design resources

- **Datasheets, spice models:** http://www.gansystems.com/transistors.php
- **Evaluation boards:** http://www.gansystems.com/eval-boards.php
- **Application notes:** http://www.gansystems.com/whitepapers.php
- **PCB Footprint libraries:** http://gansystems.com/design_library_files.php
- **FAQ:** http://www.gansystems.com/faq-e-mode-hemts.php

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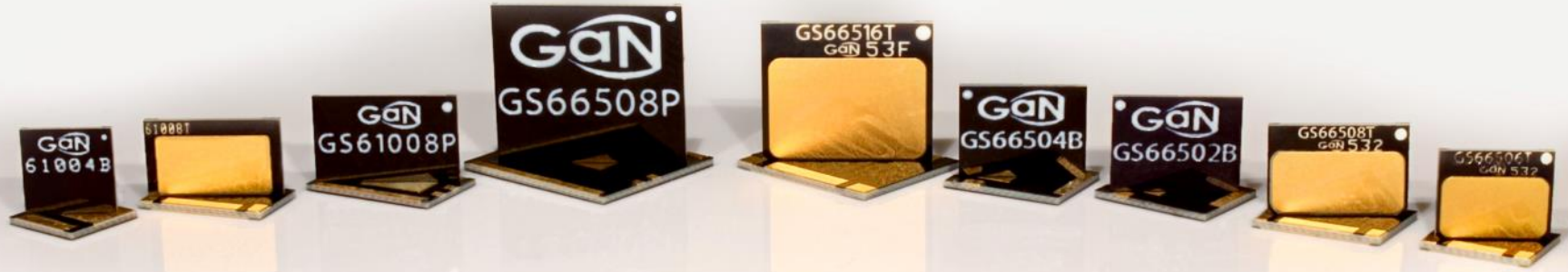

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