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Grinding of silicon wafers: A review from historical perspectives

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ABSTRACT

The majority of semiconductor devices are built on silicon wafers. Manufacturing of high-quality silicon wafers involves several machining processes including grinding. This review paper discusses historical perspectives on grinding of silicon wafers, impacts of wafer size progression on applications of grinding in silicon wafer manufacturing, and interrelationships between grinding and two other silicon machining processes (slicing and polishing). It is intended to help readers to gain a more comprehensive view on grinding of silicon wafers, and to be instrumental for research and development in grinding of wafers made from other materials (such as gallium arsenide, germanium, lithium niobate, sapphire, and silicon carbide).

Contents

1. Introduction

Semiconductor devices are the foundation of electronics industry—the largest industry in the world [1]. Silicon wafers are used as the substrates to build the vast majority of semiconductor devices [2]. In 2007, global semiconductor revenue was $270.9 billion [3]. The worldwide revenue generated by silicon wafers was $12.1 billion [4]. Part of the reason for the success of the industry has been the ability to reduce costs year upon year while meeting more stringent specifications.

Fig. 1 shows how wafer flatness and nanotopography specifications from the semiconductor industry have become more stringent over the years. Wafer flatness can be characterized in terms of a global or site parameter. The global parameter most commonly used is GBIR, or TTV (total thickness variation across the entire wafer). A frequently used parameter to measure site flatness is SFQR (site flatness, front reference surface, least-squares best-fit reference plane, range) [6]. It is the distance between the peak and valley of the wafer surface within a certain area with reference to a theoretical (least-squares best-fit) reference plane. While global flatness is still important, site flatness has become more critical. This development came about because, as the size of silicon wafers and the integration level of semiconductor devices increased, it became impossible for a lithography system to print the entire wafer in one step. Instead, a lithography system usually prints a small area (for example 26 mm × 8 mm) on a wafer at each step. This is repeated until the entire wafer has been covered. Each print (or, exposure) is

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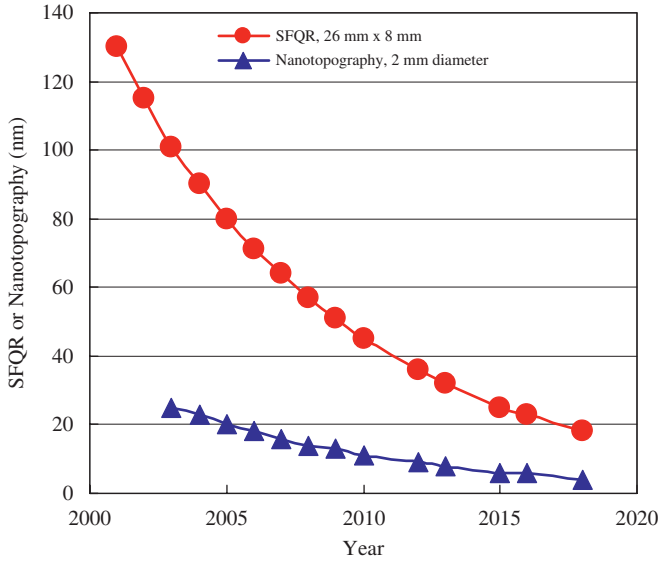

Fig. 1. Increasing flatness requirements by semiconductor industry (after [5]).

successful only if the receiving site is sufficiently flat meaning that every point on the wafer surface inside the site stays within the focus depth of the lithography system.

Nanotopography is defined as the deviation of the wafer front surface within a spatial wavelength range of approximately 0.2–20 mm [7]. It differs from flatness (SFQR) in that for nanotopography the wafer is measured in a free state, while for flatness the wafer is assumed to be held to a perfectly flat chuck by vacuum. A wafer is considered perfectly flat (SFQR = 0) as long as the front and back surfaces are parallel (even though the wafer may have surface irregularities on the front and backside of the wafer). However, the same wafer will exhibit nanotopography. Nanotopography has become very important in recent years as the integration level of semiconductor devices increased and more and more layers are lithographically etched or deposited onto the wafer surface. Such structures required chemomechanical planarization (CMP) as an intermediate step in device fabrication. If the starting wafer's nanotopography does not meet specifications, the uniformity of deposited layers is at risk during the CMP process [7,8].

To turn a single-crystal silicon ingot into wafers that meet specifications, a sequence of machining processes are needed, such as slicing (inner-diameter (ID) sawing or wire sawing), flattening (grinding or lapping), etching, and polishing [9–13]. The machining processes discussed in this paper are limited to those that machine the surfaces of silicon wafers. Other types of machining (such as profile grinding used to grind the edges of silicon wafers) are not addressed in this review.

There exist numerous articles on grinding of silicon wafers, including several review papers [14–19]. However, most research papers were focused on individual aspects of silicon wafer grinding; none of the review papers presented any historical views on grinding in manufacturing of silicon wafers; and there was little discussion in the literature on the interrelationships between grinding and other machining processes for silicon wafers.

This review paper discusses historical perspectives on grinding of silicon wafers, impacts of wafer size progression on applications of grinding in silicon wafer manufacturing, and interrelationships between grinding and two other silicon machining processes (slicing and polishing). It is organized into six sections. Following this introduction section, Section 2 describes extension of grinding from thinning of completed device wafers to flattening of sliced silicon (substrate) wafers. Section 3 discusses the impact of wafer size progression on applications of grinding in silicon wafer manufacturing. Sections 4–5 illustrate interrelationships between grinding and two other silicon machining processes (slicing and polishing), respectively. Section 6 contains concluding remarks.

2. From thinning of completed device wafers to flattening of sliced silicon wafers

This section describes a brief history of grinding from thinning of completed device wafers to flattening of sliced substrate wafers. It starts with an overview of semiconductor device manufacturing and needs for thinning (back grinding). Then it presents three types of single-side grinders (Blanchard type, creep-feed type, and in-feed type) developed for back grinding applications, and extension of in-feed grinders to flattening applications for substrate wafers. It also introduces simultaneous double-side grinding (SDSG) developed solely for flattening of substrate wafers.

Fig. 2 shows a typical process flow for making semiconductor devices (or, chips) [20–24]. For simplicity, some processes are omitted in the figure, for example, edge grinding, edge polishing, and laser marking. As shown in Fig. 2, through a series of processes (slicing, flattening, etching, polishing, and cleaning), a single-crystal ingot is converted into substrate wafers. On the front sides of these wafers, semiconductor devices are built (by a combination of deposition, lithography, etching, doping, and other processes [1,2]; detailed discussions on these processes are outside the scope of this paper).

Completed device wafers are routinely thinned before they are separated into individual dies (chips) [25–30] to allow the final assembled package thickness to be minimized. For some semiconductor devices required to operate at high power levels, wafer thinning improves the ability to dissipate heat by lowering the thermal resistance of the chip [31]. For applications such as smart cards and RFID labels, it is mandatory to thin silicon chips to a certain thickness [32]. Generally, back grinding is more cost-effective than alternative thinning processes such as wet etching [33,34] and plasma etching [35,36].

In back grinding, the removal amount is typically a few hundred microns (in wafer thickness). Usually, back grinding is carried out in two steps: coarse grinding and fine grinding. Coarse grinding employs a coarse grinding wheel with larger diamond abrasives to remove majority of the total removal amount required, as well as a faster feedrate to achieve higher throughput (the number of wafers processed within unit time). Usually, the damage induced by coarse grinding is too much and has to be removed by a fine grinding step. For fine grinding, a slower feedrate and a fine grinding wheel with smaller diamond abrasives are used to remove a small amount of silicon (for example, from 10 to 30 μm) [27,28].

Only single-side grinders that grind one side of the wafer can be used for back grinding. Initially used ones are of Blanchard type and creep-feed type (rotary-table vertical-spindle) [37–39]. Fig. 3 illustrates the Blanchard-type wafer grinder. A rotary table has several chucks aligned along a circle, and each chuck holds a silicon wafer. It is noted that wafers do not rotate around their own centers. A grinding wheel of a cup shape has a diameter larger than the wafer diameter. The rotation axis of the grinding wheel is located on the circle along which the centers of the wafers are aligned. During grinding, the rotary table feeds the wafers to the rotating wheel. The rotating wheel also moves toward the table surface at a certain feedrate. It usually takes the rotary table to rotate a large number of

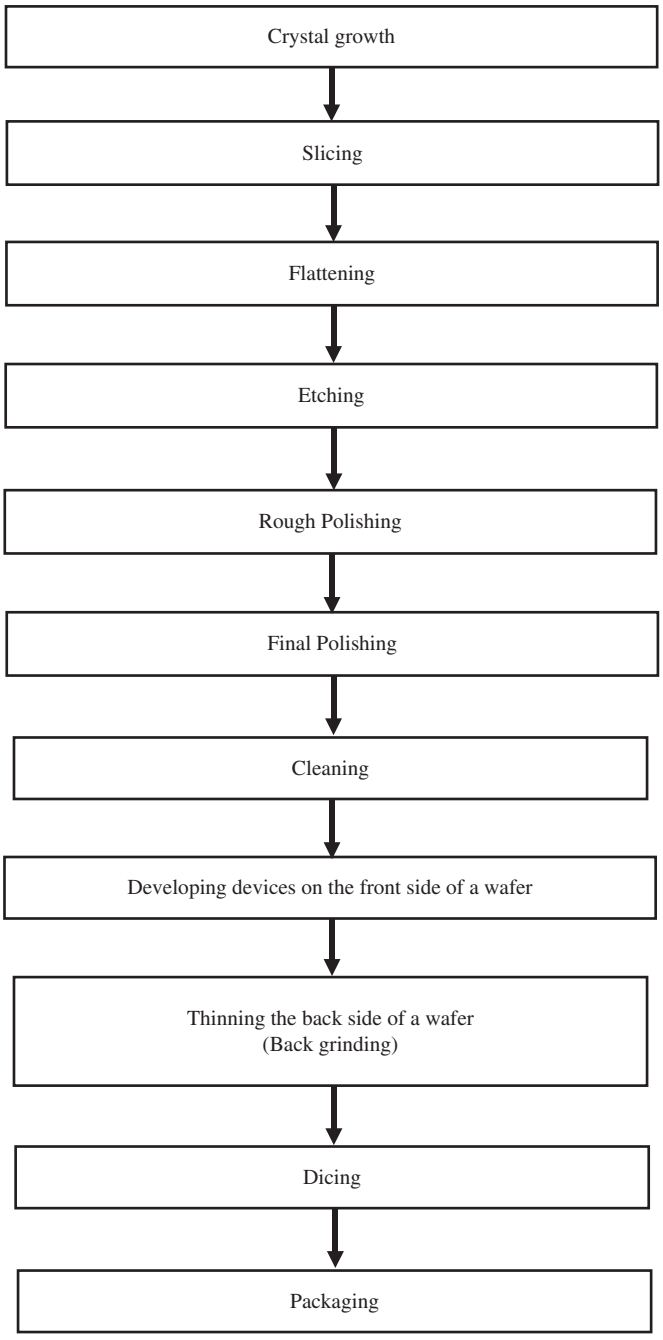

Fig. 2. Typical process flow for manufacturing of semiconductor devices (after [20–24]).

revolutions to remove a required thickness of silicon from the wafer surfaces.

Similar to Blanchard-type grinders, a creep-feed grinder has a rotary table that has one or multiple chucks with each holding a wafer (as shown in Fig. 3); wafers do not rotate about their own centers. A major difference is that, for creep-feed grinders, several (typically three) grinding wheels of a cup shape are used and each rotates around its own rotation axis. These wheels can have different diamond grain sizes ranging from coarse to fine. For example, three wheels can have grain sizes of mesh #320, #600, and #1700, respectively [39]. These wheels have a diameter larger than the wafer diameter. The rotation axes of the grinding wheels are located on the circle along which the centers of the wafers are aligned. During grinding, the rotary table feeds the wafer

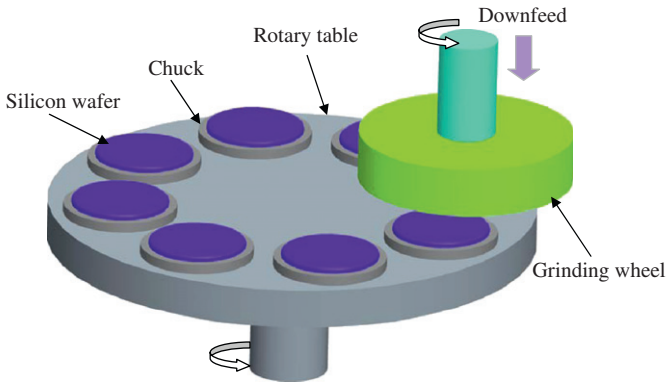

Fig. 3. Illustration of Blanchard-type wafer grinding (after [37–40]).

horizontally to the rotating grinding wheels. The grinding wheels are positioned above the rotating table in a way that the cutting surfaces of these grinding wheels will be at progressively lower positions relative to the table surface. For example, if a total of 100 μm needs to be removed from the wafer back surfaces, the three wheels can grind thicknesses of 70, 20, and 10 μm, respectively [39]. To achieve this when the rotary table has multiple wafers, at least one of the spaces between two adjacent wafers needs to be large enough to fit three grinding wheels. Through one rotation of the table, a desired total thickness of silicon is removed from each wafer surface.

For creep-feed grinding, since the wafers are finished through one rotation of the table, the grinding wheels rotate faster and the table rotates slower than in Blanchard-type grinding [39]. Comparing with Blanchard-type grinders, creep-feed grinders have better control over the target thickness of ground wafers and produce wafers with lower warp values [39]. Warp, a wafer shape parameter, measures the difference between the peak and valley "of the median surface of a free, unclamped wafer from a reference plane" [41]. The median surface of a wafer is "the locus of points in the wafer equidistant from the front and back surfaces" [41].

Both Blanchard-type and creep-feed wafer grinders have high throughput. However, they both produce poor flatness (TTV) on ground wafers. As illustrated in Fig. 4, the contact length (L) between the grinding wheel and the silicon wafer changes at every moment. Because the grinding force is nearly proportional to the contact length, it also varies at every moment, causing wafer thickness to vary from thin to thick to thin along the feed direction [40].

Later, another type of single-side grinding (SSG) machine (called an in-feed wafer grinder or wafer rotation grinder) was developed [38,40,42] with capability of producing better TTV on ground wafers. Fig. 5 illustrates this type of wafer grinder. During grinding, both the grinding wheel and the wafer rotate about their own axes simultaneously, and the wheel is fed towards the wafer along its axis. The rotation axis for the grinding wheel is offset by the length of the wheel radius relative to the rotation axis for the wafer. Because the contact length between the grinding wheel and silicon wafer is constant, the wafer flatness (TTV) ground by in-feed grinders can be significantly improved [40].

In-feed wafer grinders, capable of producing flat wafers, were introduced for flattening of silicon substrate wafers [20]. Extension of single-side wafer grinding from thinning (back grinding) of completed device wafers to flattening of substrate wafers is manifested by the history of wafer grinders at Disco Corporation, as shown in Table 1. Disco Corporation is a leading manufacturer of wafer grinders. Their first model (DFG-83H/6) of wafer grinder

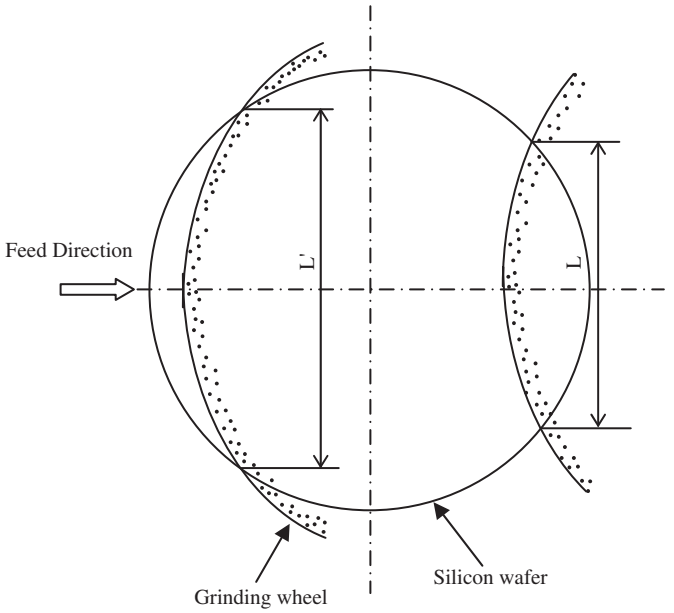

Fig. 4. Contact length between grinding wheel and silicon wafer in Blanchard-type and creep-feed wafer grinding (after [40]).

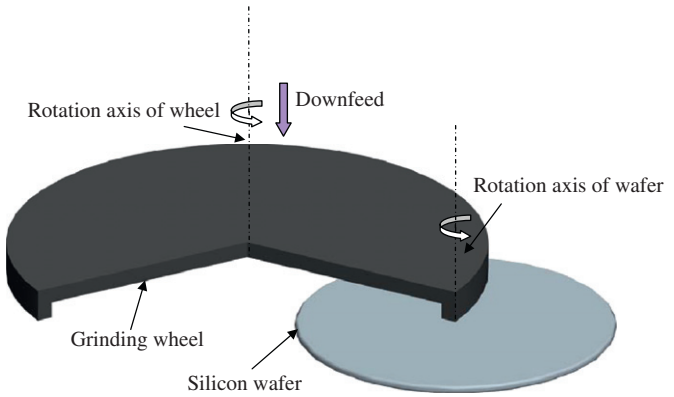

Fig. 5. Illustration of in-feed wafer grinding (after [43]).

Table 1
History of wafer grinders at Disco Corporation [44]

Year	Model	Application	Grinding type	Wafer size (mm)
1981	DFG-83H/6	Back grinding	Creep-feed	150
1988	DFG-82IF/8	Back grinding	In-feed	200
1994	DFG840	Back grinding	In-feed	200
1995	DFG830 (DFG840HS)	Flattening	In-feed	200
1997	DFG870	Flattening	In-feed	300
1998	DFG850	Back grinding	In-feed	200
1998	DFG860	Back grinding	In-feed	300
2001	DFG8540	Back grinding	In-feed	200
2002	DFG8560	Back grinding	In-feed	300
2004	DGP8760	Back grinding; polishing	In-feed	300
2005	DFG8360	Flattening	In-feed	300

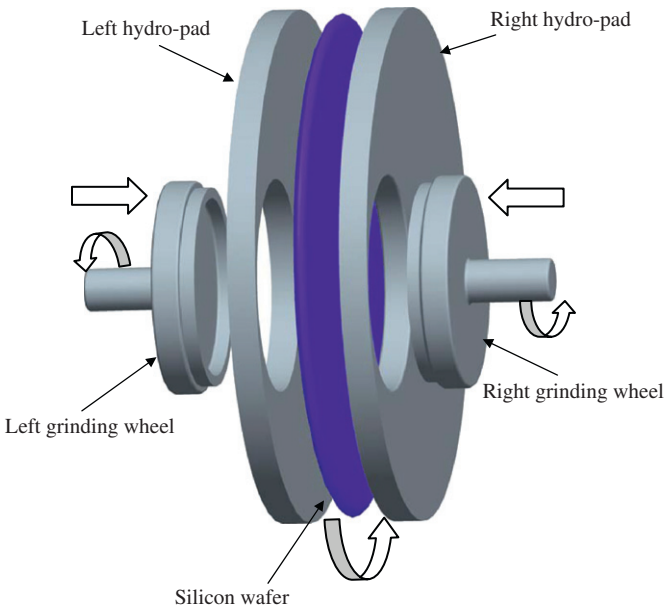

Fig. 6. Illustration of simultaneous double-side grinding (SDSG) (after [48]).

was of creep-feed type, built in 1981, for back grinding of 150 mm silicon wafers. A later model (DFG840) of in-feed type was built in 1994 for back grinding of 200 mm wafers and its modified version (DFG840HS) was introduced to flattening of sliced wafers.

Using an in-feed grinder (a SSG machine) for flattening of substrate wafers, it takes two operations to grind both sides of the wafer, one side per operation. It would be more economical if both sides of the wafer could be ground simultaneously. This motivated the development of SDSG for flattening of substrate wafers [45–47].

Fig. 6 illustrates SDSG. A silicon wafer is held by a pair of hydrostatic pads. These hydrostatic pads produce a water cushion between the respective pad and wafer surface to hold the wafer without physical contacts between the pads and the wafer during grinding. Two diamond cup wheels are located on the opposite sides of the wafer. Both sides of the rotating wafer are ground simultaneously between the two rotating wheels that are synchronously fed towards the wafer. It is noted that the wheel diameter is about half of the wafer diameter. More information on SDSG can be found in a review paper devoted to SDSG [17] and several recent patent applications [49–51]. Koyo Machine Industries Co., Ltd. is a major manufacturer of SDSG machines. Models DXSG300 and DXSG320 are for 300 mm wafers and model DXSG200 for 200 mm wafers [52].

3. Impacts of wafer size progression on applications of grinding in silicon wafer manufacturing

This section evaluates the impacts of wafer size progression on the role of grinding in flattening of sliced wafers. It first shows the progression history of wafer size in the past five decades. It then describes a typical lapping process and its advantages in flattening of small-size silicon wafers. Afterwards, it discusses why grinding instead of lapping was used for flattening of 200 mm wafers in some cases. Finally, it shows the advantages of SDSG in flattening of 300 mm wafers.

The size (diameter) of silicon wafers has grown from about 12.5 mm (0.5 in) nearly half a century ago to 300 mm (12 in) at present. Table 2 shows the size progression of silicon wafers. The driving force behind the increase in wafer size is manufacturing cost of semiconductor devices. The manufacturing cost drops dramatically when more identical semiconductor devices (chips) can be built on a single wafer [54–57].

Table 2
Progression of silicon wafer size (after [53])

Wafer size (mm)	Year
12.5	1960
25	1964
75	1973
100	1975
125	1979
150	1981
200	1985
300	1991

Table 3
Typical TTV specifications for silicon wafers of various sizes

Wafer size (mm)	TTV (μm)	Reference
75	25	[58]
100	10	[59]
125	10	[60]
150	10	[61]
200	10	[62]
300	3	[63]

As wafer size increased, flatness specifications also became more stringent. This becomes obvious when Fig. 1 and Table 2 are looked at together, and is also illustrated in Table 3. Table 3 lists typical TTV specifications for silicon wafers with various sizes. For example, TTV specification is 10 μm for 200 mm wafers (meaning that the total thickness variation over the entire 200 mm wafer <10 μm), and 3 μm for 300 mm wafers (meaning that the total thickness variation over the entire 300 mm wafer <3 μm). Since a 300 mm wafer has a much larger surface area than a 200 mm wafer, it is clear that the TTV specification for 300 mm wafers is much more stringent. Furthermore, it is common that tighter TTV specifications than those shown in Table 3 are required by certain semiconductor device manufacturers.

Size progression of silicon wafers has a number of impacts on the role of grinding as a flattening process in silicon wafer manufacturing. Such impacts are summarized in Table 4.

For flattening of silicon wafers with small diameters (less than 200 mm), lapping has been exclusively used [64]. For small wafer sizes, lapping offers higher throughput and lower overall cost than grinding (including both in-feed grinding and SDSG). Fig. 7 illustrates lapping process. A batch of wafers (for example, 25 wafers) are manually loaded into the openings of the carriers on a lapping machine. The loaded wafers are then lapped by the abrasive slurry (typically with alumina abrasives) injected between two lapping plates rotating in opposite directions [65–68]. It is noted that the abrasive slurry is not shown in Fig. 7.

As the industry moved to larger wafers, single-wafer tools became more cost effective and grinding (that grinds one wafer at a time) became more competitive than lapping (that laps a batch of wafers at a time). Grinding (as a flattening process for sliced wafers) has the following advantages over lapping:

(a) It uses fixed-abrasive grinding wheels instead of abrasive slurry and, hence, has a lower cost of consumables per wafer and can avoid the cost associated with treatment and disposal of lapping slurry;
(b) It has higher throughput for large wafers;
(c) It is usually fully automatic and, therefore, has a lower operating cost and fewer handling-related broken wafers; and
(d) It grinds one wafer at a time, making it easier to track individual wafers.

Table 4
Impacts of wafer size progression on the role of grinding in flattening of silicon wafers

Wafer size (mm)	Flattening process	Note
<200	Lapping	
200	Lapping → single-side grinding (→ lapping)	Changing from single-side grinding back to lapping was due to the replacement of ID sawing by wire sawing (see Section 4)
300	Simultaneous double-side grinding	

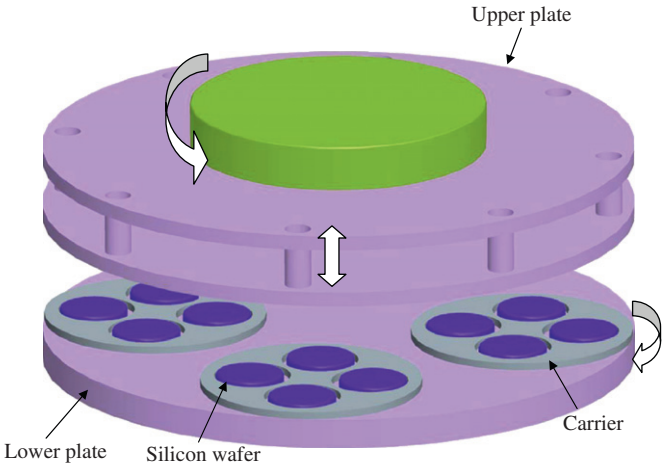

Fig. 7. Illustration of lapping (after [65]).

Due to the above advantages over lapping, SSG (in-feed type) started challenging the dominating role of lapping in flattening of 200 mm silicon wafers and made significant inroads into this territory. However, SSG as a replacement for lapping in flattening was never entirely accepted by the industry, partly due to a major change in slicing. The interrelationship between grinding and slicing will be discussed in Section 4.

For 300 mm silicon wafers, SDSG is the primary flattening process. As the wafer size increased to 300 mm, wafer breakage during manual loading and unloading in lapping became worse. As the same time, the cost effectiveness of single wafer tools became more prominent.

It is important to note that SDSG are no more advantageous over lapping for smaller wafer sizes. As shown in Fig. 6, the diameter of the grinding wheels in SDSG is about half of the wafer diameter. If wafers are small, grinding wheels will also be small, making it very difficult to realize cost-effective grinding operation. This is because, generally speaking, a grinding wheel needs to be operated at a sufficiently high speed (surface speed at the wheel segments) when grinding silicon wafers [43,69,70]. When a grinding wheel has a sufficiently large diameter, it is easy to achieve the high surface speed required. An alternative to achieve the high surface speed is to increase the rotational speed of a grinding wheel, and this often causes other problems (such as vibration). Furthermore, a grinding wheel with a smaller diameter usually has a shorter life than a wheel with a larger diameter, causing more frequent wheel changes.

Wafer size progression has significant impacts on, but is not the only factor of, transition of flattening from lapping, to SSG, and to SDSG. Other factors contributing to this transition include: (1) more stringent flatness specifications, (2) development of new

grinding technology (for example, SDSG) and improvement of existing grinding technology, (3) replacement of ID sawing by wire sawing as the dominating slicing process, and (4) industry-wide acceptance of simultaneous double-side polishing (DSP) for 300 mm wafers. Some of these factors will be discussed in details in the following sections.

4. Interrelationship between grinding and slicing

This section first gives an overview of two slicing methods (ID sawing and wire sawing) and discusses wire-sawing-induced waviness. It then compares lapping, SSG, and SDSG in their effectiveness of removing waviness. Finally, it contains a discussion about the effects of process change in slicing (from ID sawing to wire sawing) on process reversal in flattening (from grinding to lapping).

ID sawing had been exclusively used in slicing of silicon wafers for decades until the introduction of wire sawing [64]. ID sawing is illustrated in Fig. 8. The cutting tool is a circular steel blade with a hole in the middle. The blade is coated with diamond abrasives and rotates at high speed, slicing one wafer at a time. There is a mechanism to feed the ingot (or the blade) toward the blade (or the ingot). More information about ID sawing can be found in the literature [14,23,71–75].

Wire sawing technology made significant progress in the 1990s and has largely replaced ID sawing for slicing of silicon wafers with a diameter of 200 mm or larger. Fig. 9 depicts the principle of the wire sawing process. A single wire is fed from a supply spool to the wire guides that are grooved with a constant pitch (note that the supply spool and wire guides are not shown in the figure). A wire web is formed by winding the wire on the wire guides through 500–700 parallel grooves. The silicon ingot is pushed against the moving wire web and sliced into hundreds of wafers at the same time. Cutting is achieved by an abrasive slurry (not shown in the figure) that is supplied over the wire web and carried by the wire into the cutting zone. The slurry consists of a suspension of abrasive particles (the most commonly used abrasive is silicon carbide) [76]. More information about wire sawing can be found in the literature [76–79].

Compared to ID sawing, wire sawing has less kerf loss and can produce wafers with better quality (for example, smaller warp) [56,75]; and has higher throughput and thus a lower cost for wafers with a diameter of 200 mm or larger. Due to these advantages, wire sawing now dominates slicing operations for 200 and 300 mm silicon wafers.

When wire sawing replaced ID sawing, a new problem appeared: wire sawing-induced waviness. Waviness, as shown in Fig. 10, is also called long-cycle swelling or unevenness [81], or wavy stripes [82]. The generation mechanism of this waviness was not fully understood for a long time, making it very difficult to eliminate waviness at wire-sawing process. This waviness has to be removed by subsequent processes; otherwise, it will adversely affect wafer flatness, especially site flatness.

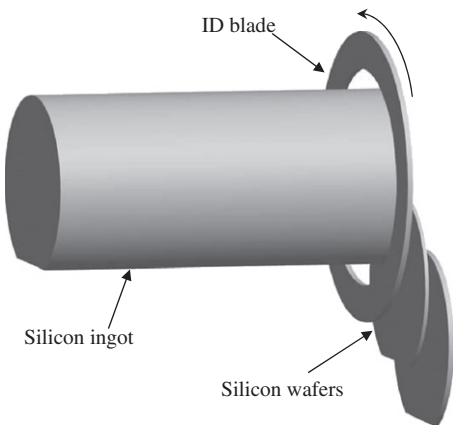

Fig. 8. Illustration of ID sawing (after [71,72]).

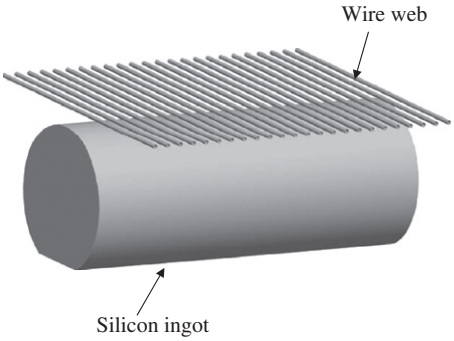

Fig. 9. Illustration of wire sawing (after [76]).

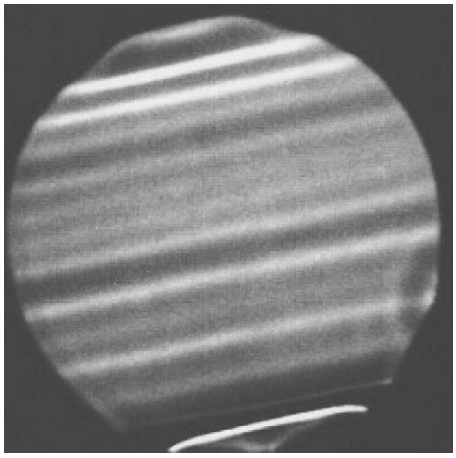

Fig. 10. Waviness induced by wire-sawing [80].

Lapping, SSG, and SDSG are different in their effectiveness of removing wire-sawing-induced waviness. In lapping, both sides of the wafers are machined simultaneously while the wafer is in a nearly free state. Therefore, waviness can be effectively removed [82].

SSG cannot effectively remove waviness [24,81–85]. Differences in waviness removal by SSG and lapping were investigated using finite element analysis (FEA) [84]. The results revealed that, under the same applied force, the relative peak displacement (the displacement of waviness peaks relative to the waviness valleys) at the deformed state in lapping was much smaller, only 1/55 to 1/36 of that in SSG. Smaller relative peak displacement is desirable for reducing or eliminating waviness. As illustrated in Fig. 11, if the median surface of a wavy wafer deforms elastically during machining (SSG or lapping), after the operation it will spring back to its original shape thus preserving the waviness. Many effects were exerted to improve the effectiveness of SSG in waviness removal, such as soft-pad grinding [83,86–88], wax mounting [89], and reduced vacuum [81]. However, none of these techniques were shown to be feasible in manufacturing.

In SDSG, both sides of the wafer are ground by a pair of wheels simultaneously, very similar to lapping where both sides of the wafer are machined simultaneously [42,54,56,90]. Therefore, SDSG is almost as effective as lapping in waviness removal [17,47–51,90].

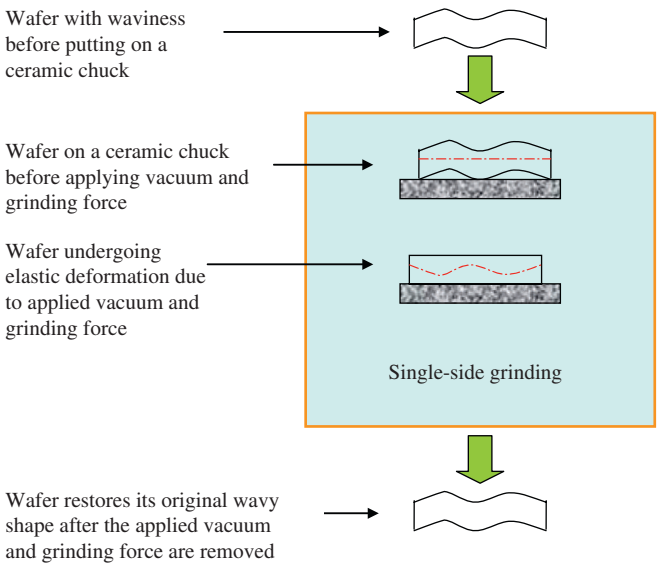

Fig. 11. Wafer deformation during single-side grinding (after [80]).

Table 5
Effects of slicing on the role of grinding in flattening of 200 mm silicon wafers

Slicing method	Flattening process	Note
ID sawing	Lapping	When 200 mm wafers were first manufactured, ID sawing was used to slice ingots into wafers and lapping was used to flatten sliced wafers
ID sawing	Grinding	Due to its significant improvement, in-feed wafer grinding became more cost effective than lapping for flattening and successfully replaced lapping in some cases
Wire sawing	Lapping	In-feed wafer grinding (single-side grinding) could not remove wire-sawing induced waviness, and hence was replaced by lapping to flatten wire-sawn wafers

The change of slicing from ID sawing to wire sawing has interesting effects on the role of grinding in flattening of silicon wafers, as shown in Table 5. When 200 mm silicon wafers were first manufactured, ID sawing was used for slicing of ingots into wafers and lapping was used for flattening. SSG (in-feed wafer grinding) gradually replaced lapping for flattening of ID sawn wafers [20], due to the benefits of grinding over lapping (as discussed in Section 3). At this stage, wafer grinding as a replacement for lapping was not entirely accepted by the industry. However, significant success was achieved where the ID sawing machines had a combined grinding and slicing operation. On these ID sawing machines [23,73], one side of a wafer is ground before the wafer is sliced off from the ingot, providing a flat reference plane for subsequent grinding processes.

However, when wire sawing replaced ID sawing for slicing, SSG became inferior to lapping, due to its inability to effectively remove the waviness induced by wire sawing. Therefore, lapping came back as the dominating flattening process for wire-sawn wafers.

5. Interrelationship between grinding and polishing

This section first describes two silicon wafer polishing methods: single-side polishing (SSP) and (simultaneous) DSP. It then presents etched-wafer fine grinding as well as its benefits and applications. Finally, it illustrates how which polishing method (SSP or DSP) is used will determine whether or not etched-wafer fine grinding should be considered in a manufacturing flow for silicon wafers.

SSP is illustrated in Fig. 12. A silicon wafer is mounted on a block that is attached to a polishing head. A polishing pad is attached on a rotary plate. Both plate (with pad) and wafer rotate around their own rotation axes. In addition, the polishing head oscillates across the pad surface. The polishing pad carries the slurry (consisting of chemicals and abrasives) to the interface between wafer and pad [92]. Material removal occurs as a consequence of a combination of (a) chemical reaction of slurry chemicals with silicon wafer surface, and (b) repeated mechanical interaction between pad and wafer with abrasives in between. A typical single-wafer polisher is Strasbaugh nFinity 6DZ [93]. It is also common to polish multiple wafers on one block, especially for small wafers. Typical multiple-wafer polishers include SpeedFam FAM50-SPAW and FAM59-SPAW [94].

When SSP is used to manufacture silicon wafers, only one side of the wafer is polished. The back side of the wafer remains as an etched surface. It is very difficult to achieve very good flatness on single-side polished wafers.

DSP is illustrated in Fig. 13. Wafers are put inside the openings of carriers, and both sides of the wafers are polished simultaneously by polishing pads mounted on the top and bottom plates (with slurry in between wafer and pad). Typical double-side polishers include Peter Wolters Microline AC 2000-P2, capable of processing 30 pieces of 200 mm wafers per batch and 15 pieces of 300 mm wafers per batch [96]; and SpeedFam DSM20B-5P-4D, capable of processing 15 pieces of 200 mm wafers per batch and 5 pieces of 300 mm wafers per batch [97].

DSP can achieve excellent flatness on polished wafers [22,46] and has become the standard for 300 mm wafers. However, DSP has not, so far, been widely used for wafers with a diameter of 200 mm or smaller. The primary reason is that DSP creates mirror finish surfaces on both front and back sides of the wafer. This causes problems in some older device manufacturing lines where some sensors on processing equipment cannot differentiate front side from back side of a wafer. Furthermore, wafers with both sides mirror polished tend to slip out during handling processes [22] that are not designed for handling double-side polished wafers.

Fig. 14(a) shows a typical process flow that uses SSP. Generally, a wet etching process can negatively affect flatness [55], and extended SSP can deteriorate flatness [20]. Although the wafer

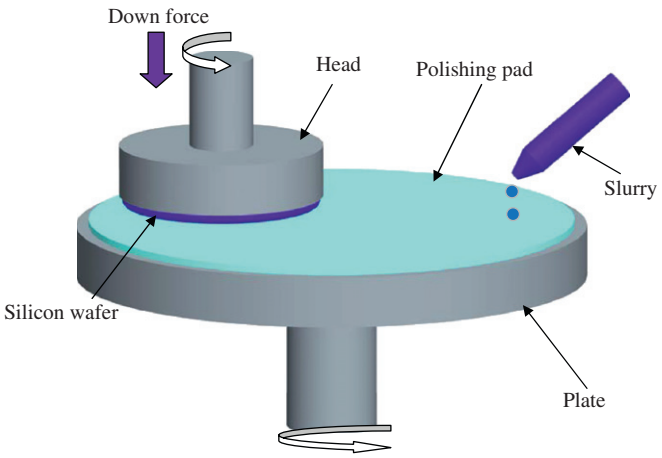

Fig. 12. Illustration of single-side polishing (after [91]).

flatness after flattening usually is very good, it can deteriorate somewhat during etching and polishing. Therefore, in some cases, wafers manufactured by this process flow cannot meet flatness requirements.

One technique to improve the flatness of single-side polished wafers is fine grinding of front sides of etched wafers prior to polishing [20,43,69,98]. The purpose of etched-wafer fine grinding is to improve the flatness of feedstock wafers to polishing and to reduce the material removed during polishing thereby achieving a higher throughput for polishing and better flatness for polished wafers. A process flow that includes etched-wafer fine grinding is shown in Fig. 14(b). This process flow can potentially reduce manufacturing costs because (a) it reduces polishing removal and cuts down the time of the expensive polishing operation, (b) it improves flatness and lowers the yield loss, and (c) etched-wafer fine grinding grinds wafers to a uniform thickness and eliminates the sorting operation for polishers that mount multiple wafers on one block. If multiple wafers with different thickness are mounted on one polishing block, these wafers will not have good flatness after polishing. Usually, thickness variation among etched wafers is quite large; hence, without etched-wafer fine grinding, a sorting operation is often needed before polishing, adding extra cost.

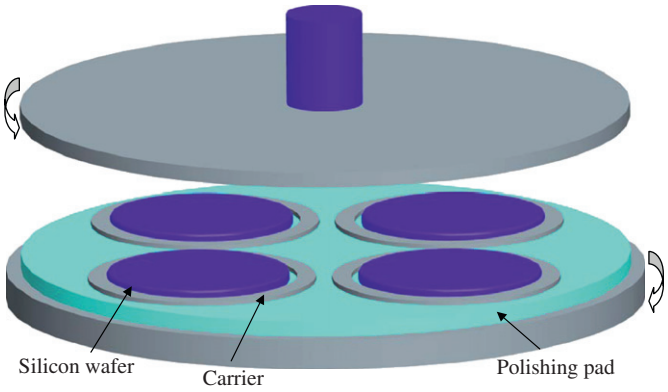

Fig. 13. Illustration of double-side polishing (after [95]).

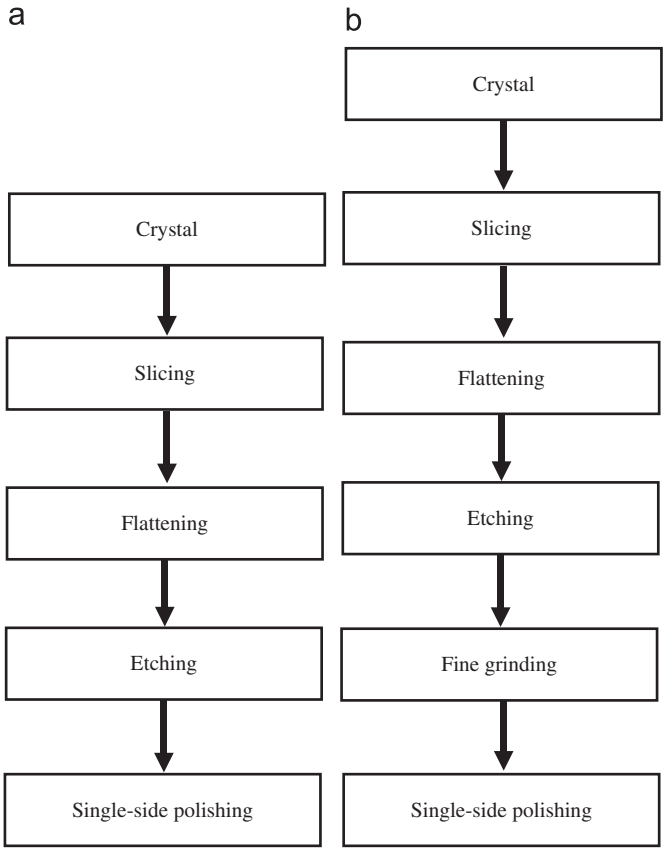

Fig. 14. Process flows for single-side polished wafers (a) without and (b) with fine grinding of etched wafers (after [98]).

However, the cost effectiveness of etched-wafer fine grinding is only apparent if the depth of grinding-induced damage is very shallow such that only a small removal is required in polishing. In order to reduce the damage depth on ground wafers, grinding wheels with very small diamond grains are desirable. As shown in Fig. 15, shallower damage depth can be obtained by using smaller diamond grains. However, when the diamond grains become very small (for example, 1 μm), it is very difficult for the wheel to maintain self-dressing ability [100]. Self-dressing ability refers to the wheel's ability to release worn grains and expose new grains without any external means.

Very few grinding wheels are commercially available for etched-wafer fine grinding. Disco Corporation probably is the only company that offers grinding wheels (model B-M01) for this application, using resin bond and 4/6 μm diamond grain size [101]. Published information of major wheel manufacturers [102–106] shows that the smallest diamond grain size used in resin- or vitrified-bond grinding wheels for silicon wafers is mesh #2000 or #4000 (grain size >2 μm). Metal-bond wheels with much finer diamond grains such as mesh #120,000 (average grain size is 0.13 μm) have been reported in electrolytic in-process dressing (ELID) grinding of silicon wafers [107]. But there has been no report on applications of ELID grinding in silicon wafer manufacturing. More information on ELID grinding of silicon wafers can be found in a review paper devoted to the topic [18].

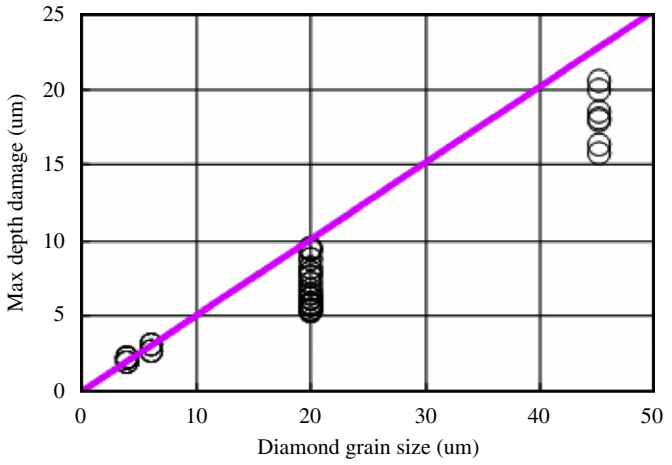

Fig. 15. Relation between diamond grain size and maximum depth of damage [99].

Table 6
Evolution of process flows for manufacturing of silicon wafers

Year	Process flow
< 1990	ID sawing→lapping→etching→polishing
1990	ID sawing/grinding→grinding (SSG)→etching→polishing
1995	Wire sawing→lapping→etching→polishing or Wire sawing→lapping→etching→fine grinding→polishing
2000	Wire sawing→SDSG→etching→polishing or Wire sawing→lapping→etching→polishing

Table 7
Comparison of major machining processes in silicon wafer manufacturing

Process	Machine	Machine cost ($k)	Typical abrasive	Throughput (wafer/hour)	Flatness	Roughness	Depth of damage (μm)
Slicing	Wire saw	600–800	Silicon carbide, free abrasive	High	Poor	Poor	5–15
Slicing	ID saw	200–400	Diamond, fixed abrasive	Low	Poor	Poor	5–15
Lapping	Lapper	700–900	Alumina, free abrasive	High	Good	Good	2–5
Grinding	Grinder	600–800	Diamond, fixed abrasive	High	Good	Good	2–5
Etching	Etcher	200–1200	None	Very high	Poor/good	Poor/good	None
Polishing	Polisher	1000–3000	Silica, free abrasive	Low/high	Very good	Very good	None

Use of etched-wafer fine grinding in a process flow requires capital investment (purchasing and installation of grinders) and additional costs (utilities, consumables, and labor). Furthermore, a cleaning step is usually required after etched-wafer fine grinding (before polishing). Inclusion of etched-wafer fine grinding into a process flow makes economic sense only if the cost reduction is greater than the added cost. For example, when flatness specifications are not very tight, a process flow with etched-wafer fine grinding will not make significant differences compared with a process flow without etched-wafer fine grinding. This is because both process flows can easily produce wafers that meet the flatness specifications. However, when flatness specifications are very tight, the percentage of out-of-specification wafers will be very high if a process flow without etched-wafer fine grinding is employed, resulting in much higher average wafer cost; and, therefore, the extra cost incurred by adding etched-wafer fine grinding can be justified.

Over time the flatness specifications became so tight (see Fig. 1) that they were difficult to meet on a single-side polished wafer. As a result, the industry moved to double-side polished wafers. Since flatness can be achieved more easily on double-side polished wafers, etched-wafer fine grinding does not provide additional benefits. Therefore, etched-wafer fine grinding is sometimes needed only in cases where wafers are polished on singe-side polishers and flatness specifications are so tight that additional cost of adding etched-wafer fine grinding can be justified.

6. Concluding remarks

Evolution of process flows for manufacturing of silicon wafers, as summarized in Table 6, is a result of many influencing factors: wafer size, flatness specification, development of new machines, and improvement of existing machines.

Machining processes used in manufacturing of silicon wafers can be classified into two groups. One group includes processes (such as polishing) which produce a wafer surface with excellent quality but are slow and expensive. The other group includes processes (such as lapping and grinding) which are faster and less costly but do not produce a surface that meets the requirements of semiconductor device makers. A comparison of these processes is provided in Table 7. To convert silicon ingots into wafers, multiple processes from these two groups are required to reach a series of compromises optimized to produce wafers that meet quality requirements at the lowest possible cost.

The criterion to determine whether and where grinding should be used in a process flow for manufacturing of silicon wafers is to achieve the lowest overall manufacturing cost while meeting the quality requirement of silicon wafers. For example, SSG (in-feed wafer grinding) was used for flattening of 200 mm ID-sawn wafers because of its lower overall cost of manufacturing. Another example is fine grinding of etched wafers that will be single-side polished.

It is important to consider the series of machining processes (slicing, flattening, and polishing) as a system. The system as a whole has to deliver wafers that meet all quality requirements. For example, wire-sawing-induced waviness can be removed by lapping, SDSG, or (simultaneous) DSP. At least one of these processes has to be in the system to guarantee that waviness be removed. For wire-sawn 200 mm silicon wafers, if only one side is polished, waviness has to be removed during flattening. Since SSG cannot effectively remove waviness, lapping has to be used for flattening.

Wafers made of other materials (such as gallium arsenide, germanium, lithium niobate, sapphire, and silicon carbide) currently being manufactured have much smaller sizes than silicon wafers. For many of them, the largest commercially available size is 125 mm in diameter. Understanding the effects of wafer size on the role of grinding in manufacturing of silicon wafers is instrumental when deciding if grinding should be employed for manufacturing of a certain size of wafers made of other materials. For example, if the wafer size is 150 mm or smaller, lapping would be a more cost-effective flattening process than SDSG. When choosing a flattening process between SSG and lapping, factors that need to be considered include the following. What is the slicing process (wire sawing or ID sawing)? If it is wire sawing, how severe is the waviness induced by wire sawing? Can the waviness be removed by SSG?

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