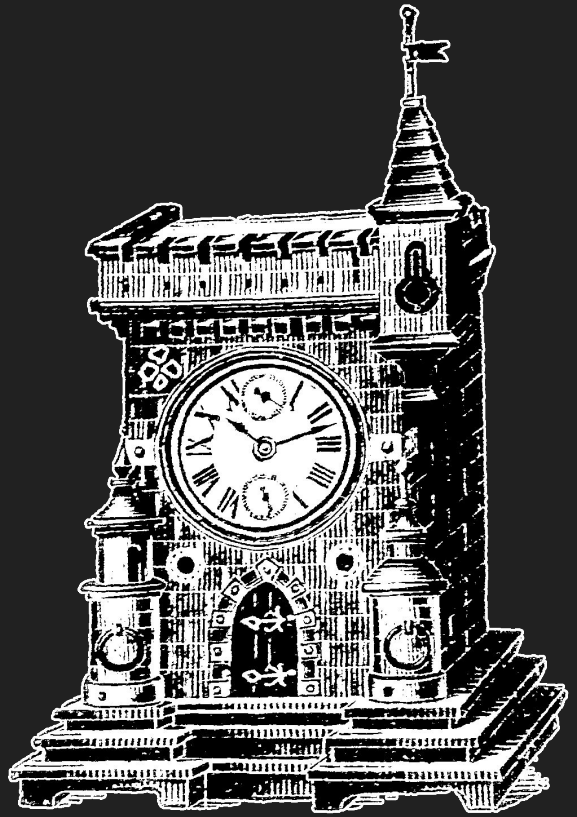
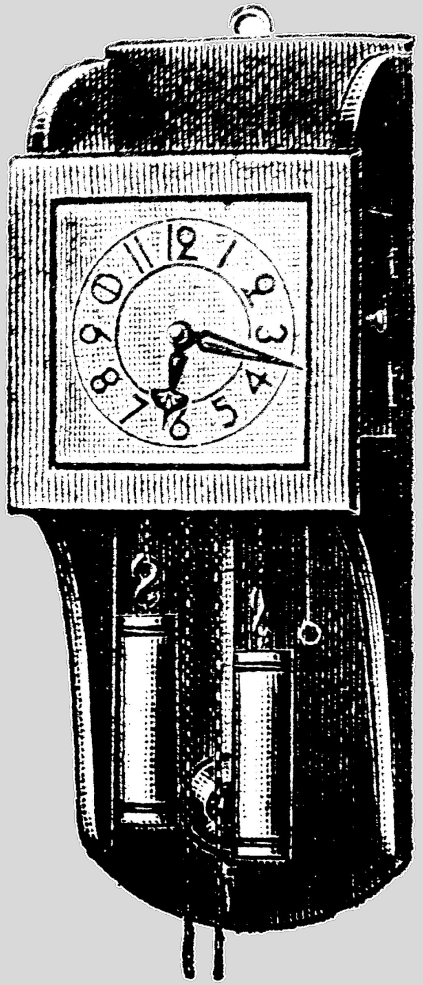


Grokking FPGA clock management

Philémon Gardet <phil@lse.epita.fr>
Jean-François Nguyen <jf@lse.epita.fr>

LSE Security System

Architecture



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Architecture Overview

- IO buffers
- PLLs / DLLs
- CLBs
- Interconnect
- Block RAM

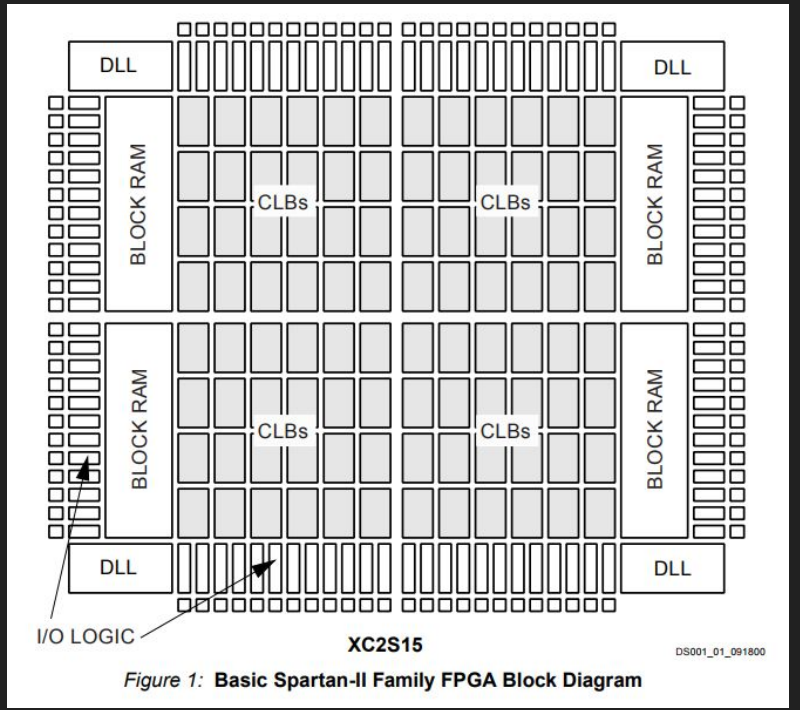


Figure 1: **Basic Spartan-II Family FPGA Block Diagram**

CLB - Configurable Logic Blocks

- Logic Cell:
  LUT, carry logic, storage
- Chained carry
- Fast adjacent interconnect
- `clk` signal

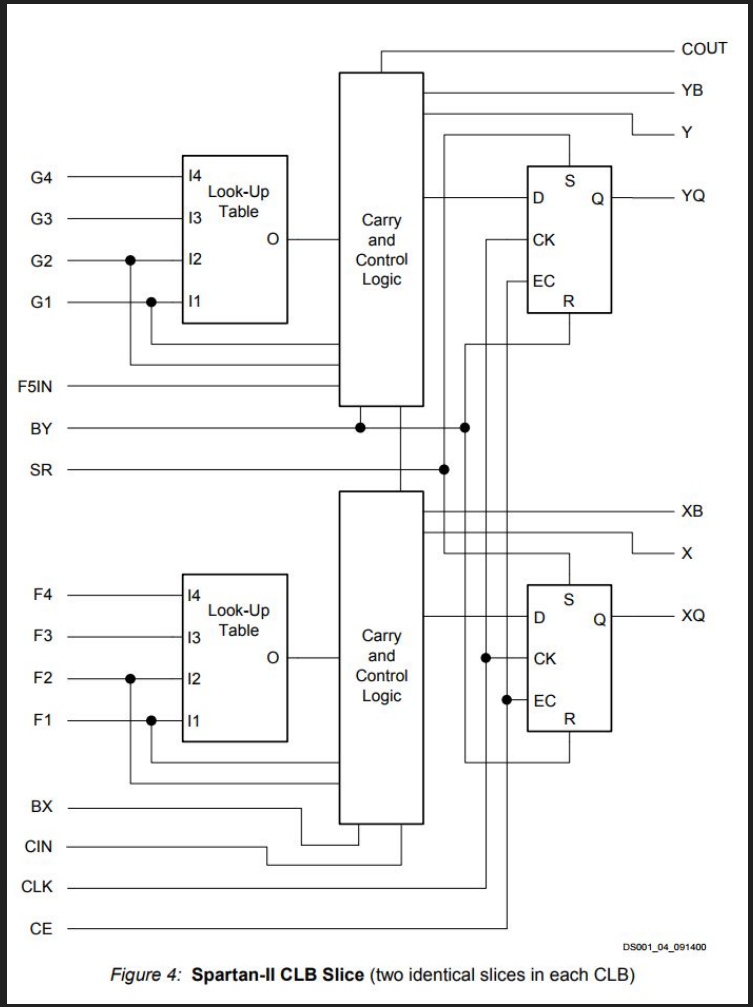
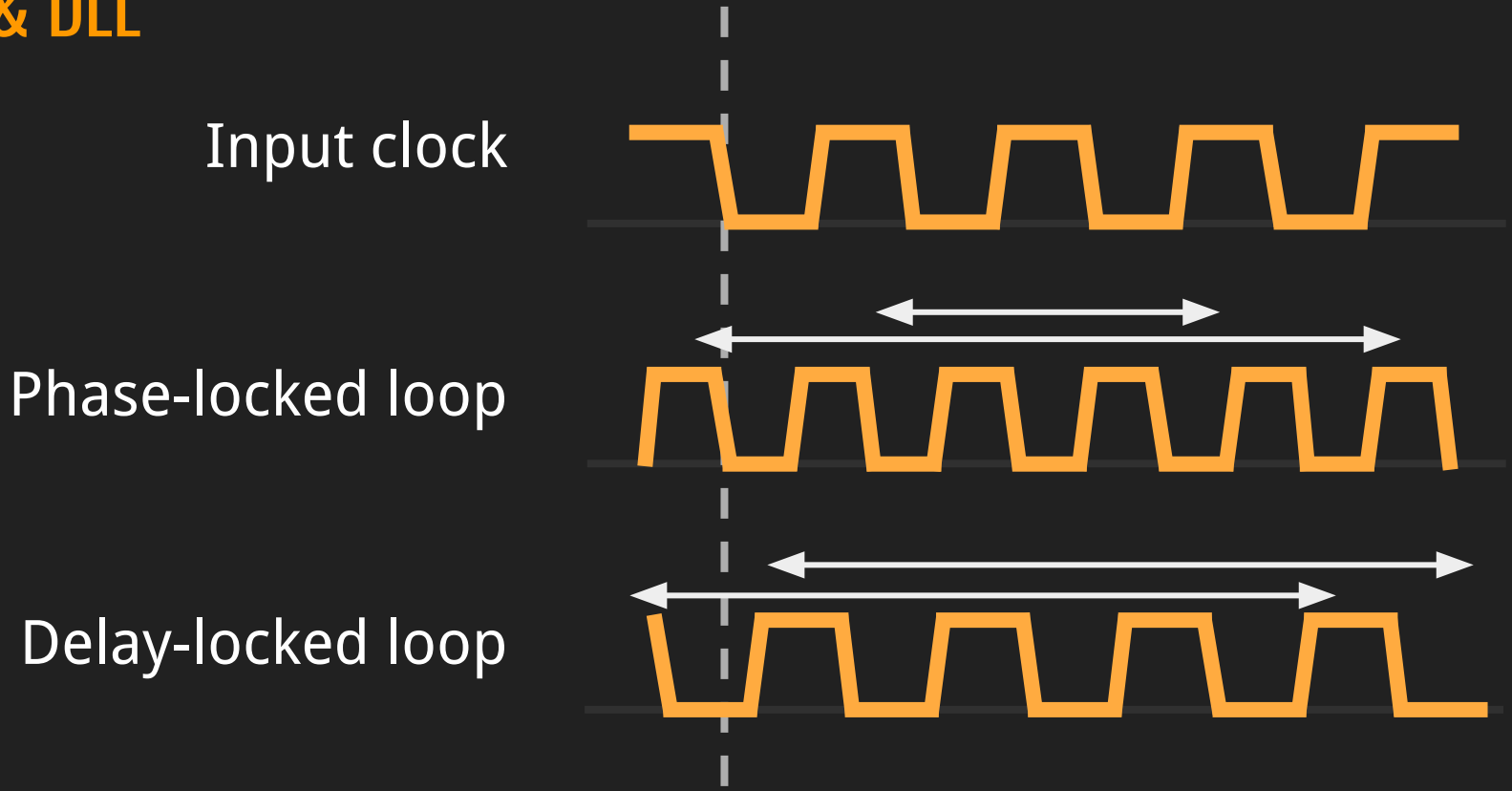


Figure 4: **Spartan-II CLB Slice** (two identical slices in each CLB)

PLL & DLL



Clock Networking

- Fan-out

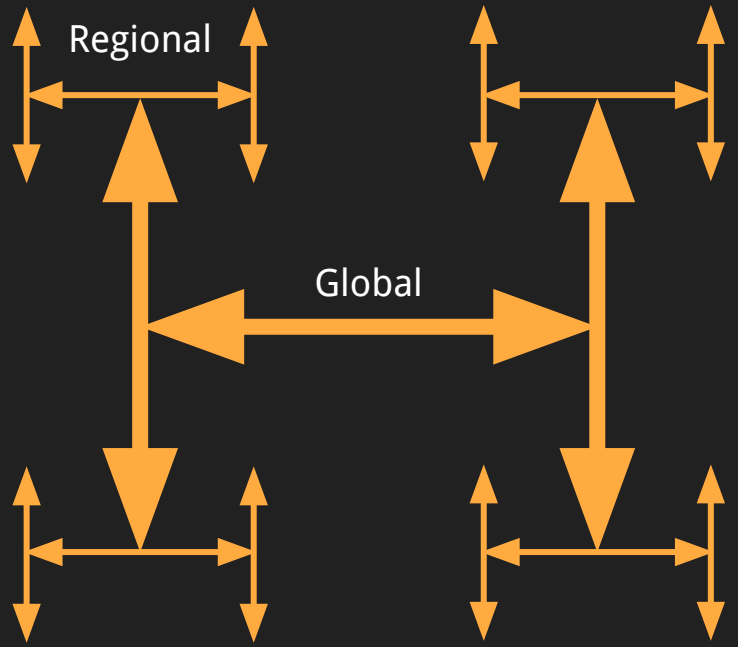
  Clock signal *intensity*

- Clock skew

  Different phases from the same source

Clock Networking - Clock Tree

- Global networks
  Low-skew / High fanout
- Regional networks
  Mid-skew / Mid fanout
- Edge networks
  Low-skew / high speed / IO



Clock Tree Strategy

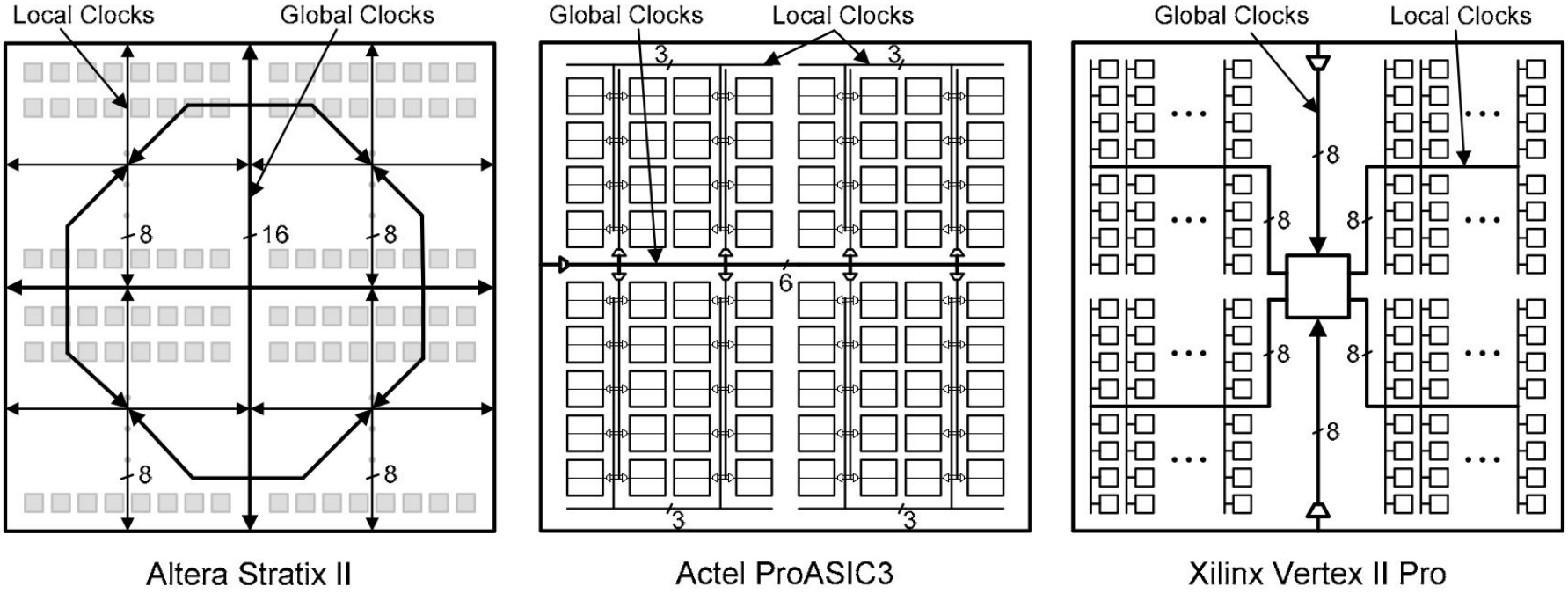
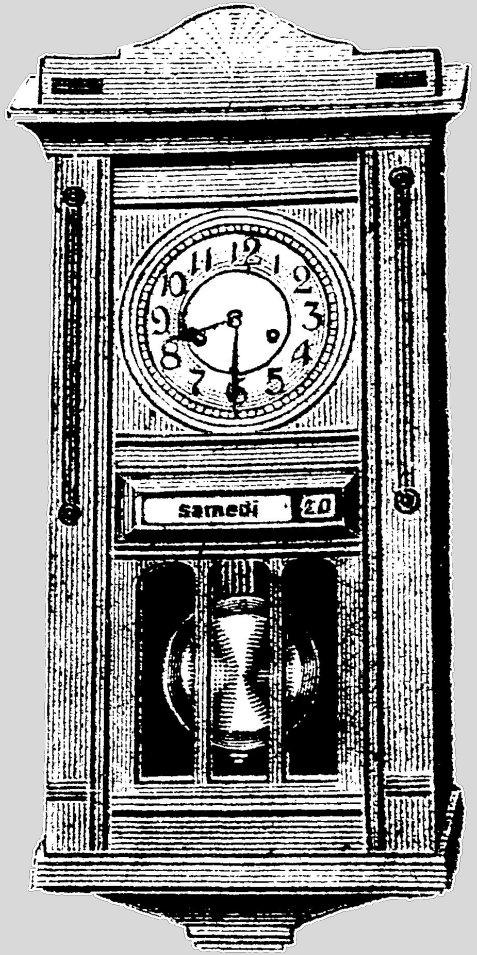


Figure 1: Commercial FPGA clock networks.

Timing considerations



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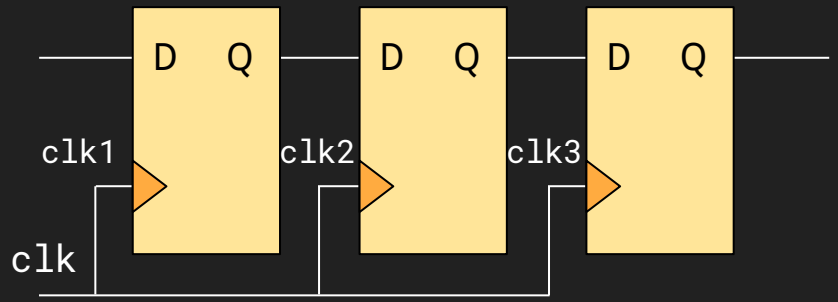
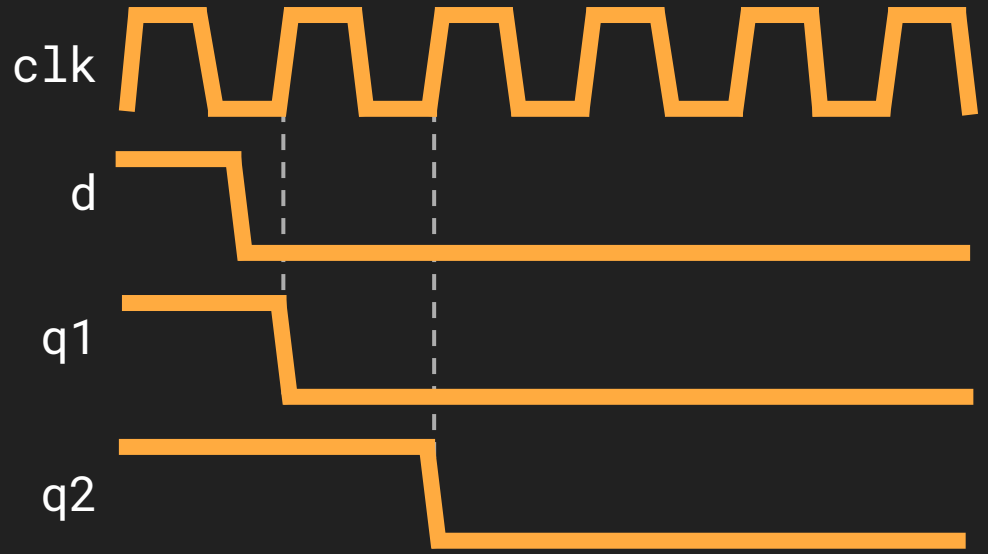
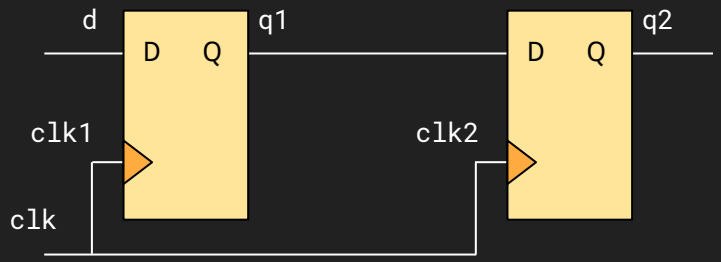
Clock Skew

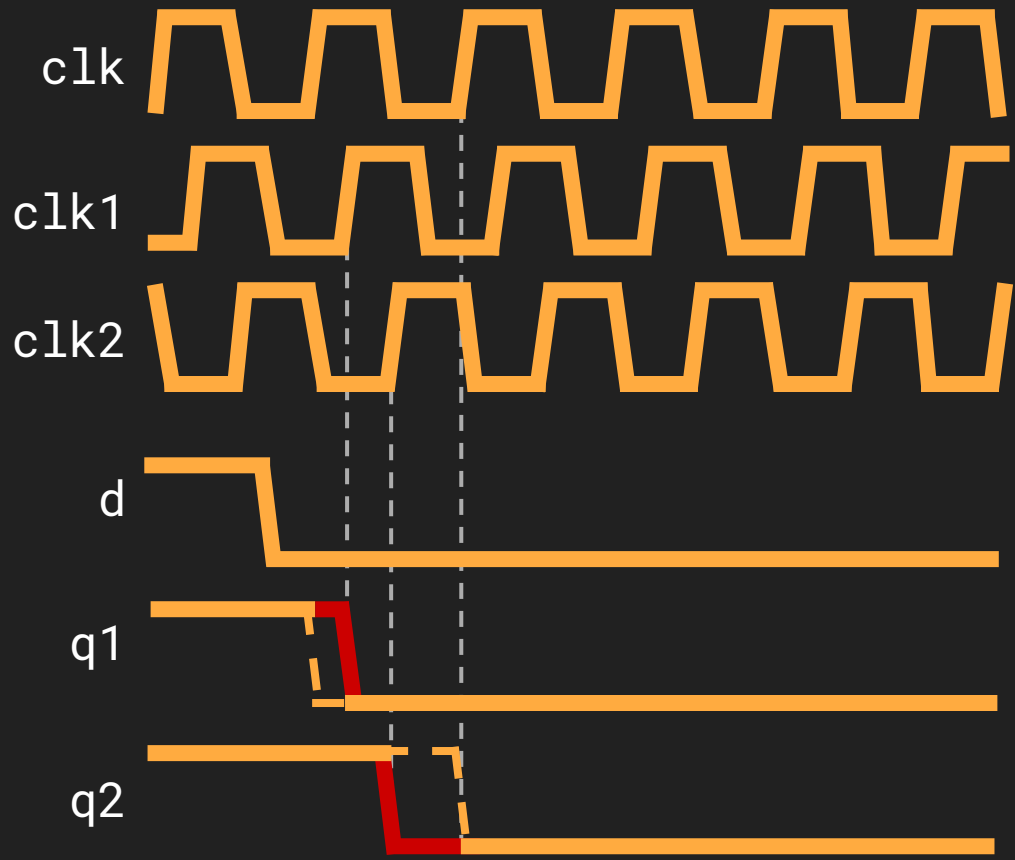


Short Path



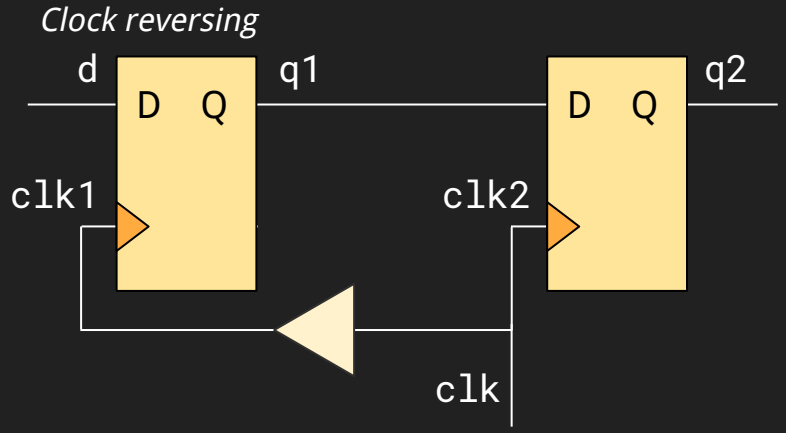
Short Path

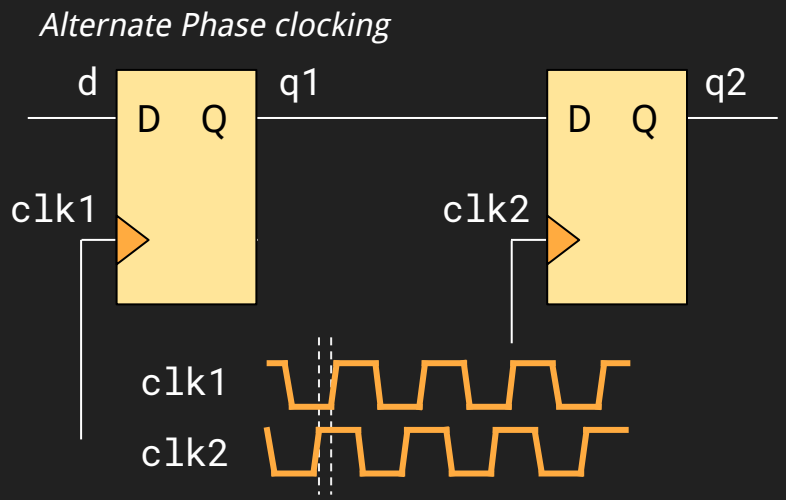




Short Path - Fixes

- Add delay in data path
- Clock Reversing
- Alternate Phase Clocking
  - DLL
  - Differents edge triggers
  - Clock buffering





Place and Route

- Routability
  - Avoid coupling capacitance or detours
- Timing constraints
  - Bound delay on each path
- Power consumption
- Yield

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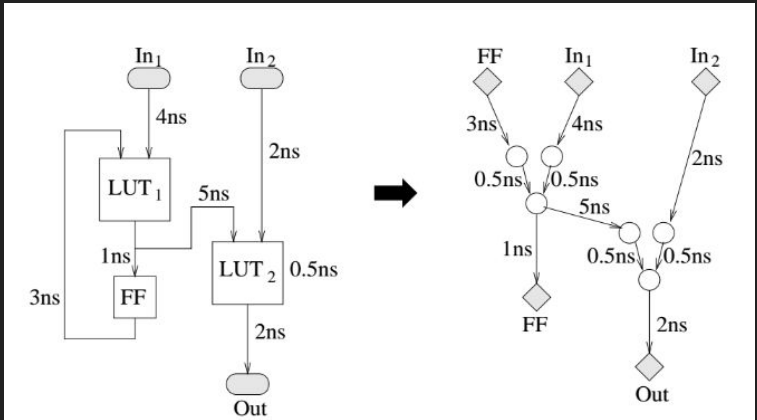
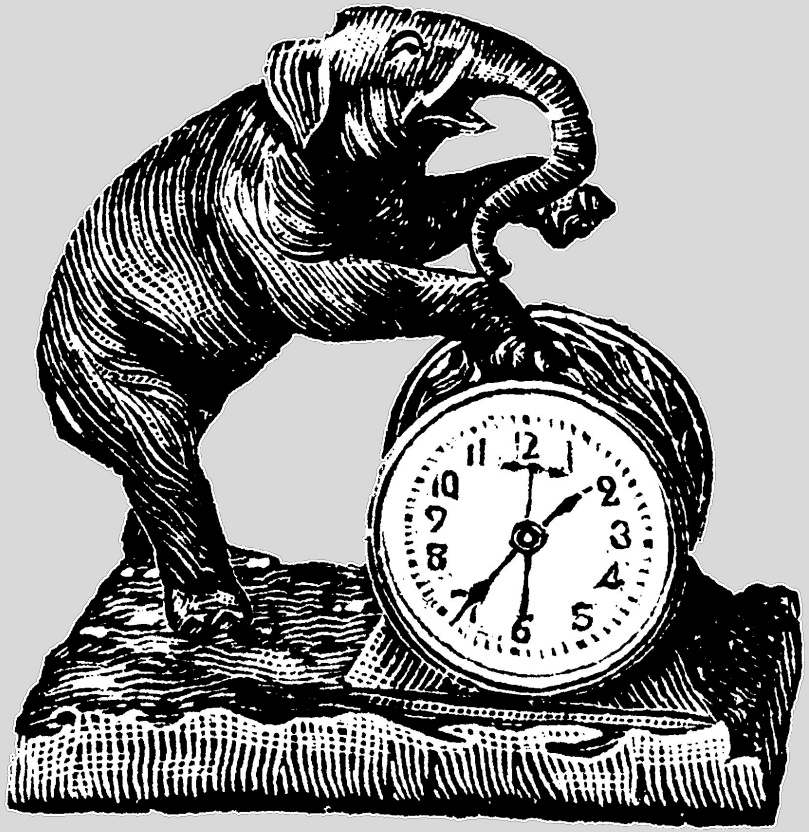
Timing Analysis

- *Minimum clock period* is dictated by the largest delay
- *Slack* is the tolerated delay before increasing the minimum clock period
- *Critical path* has a slack of 0



A timing graph for a simple circuit.

Asynchronous & others dumb things



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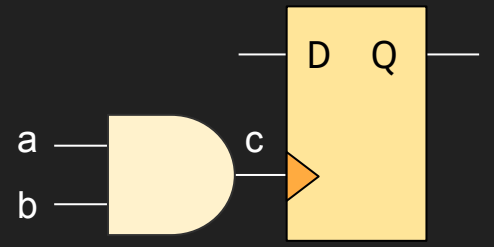
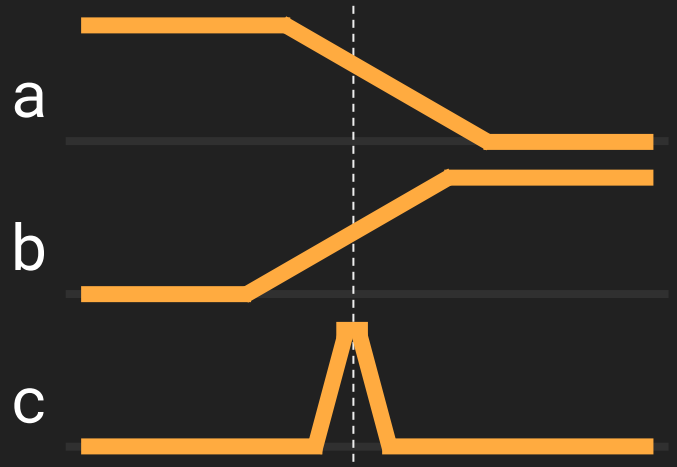
Metastability

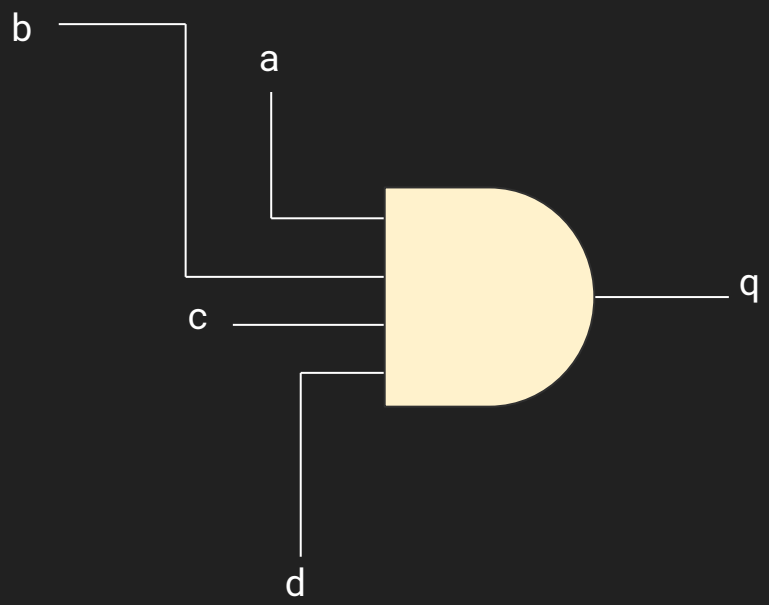
- Real world
  ⟶ transitive time
- Intermediate *logic* state
- Unknown behaviour if output feeds data to another stage





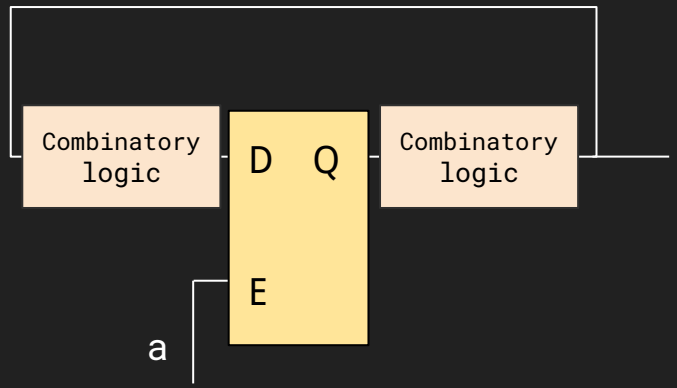
Combinatory Logic as Trigger - Short paths

- Without any synchronization no hypothesis about order
- Metastability possibility



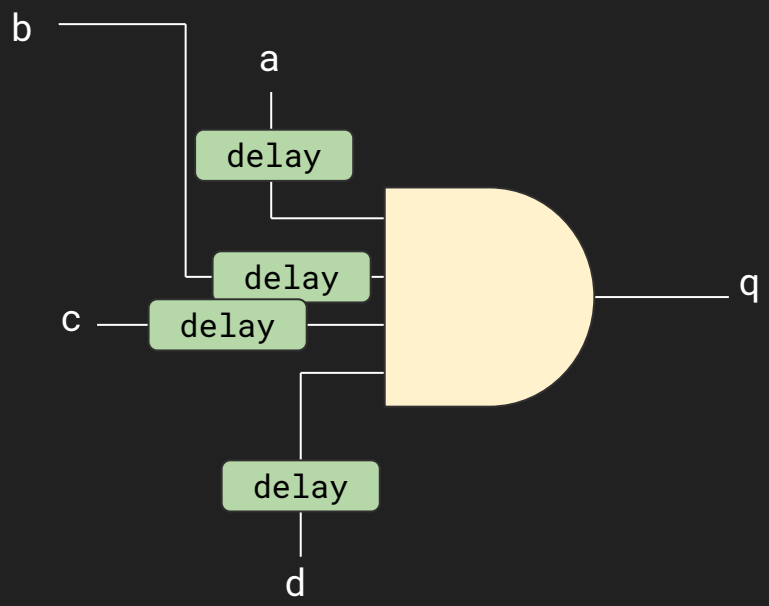
Latches - Race condition

- Asynchronous control
- Transitive state
- Loop ⟶ No idea about current state

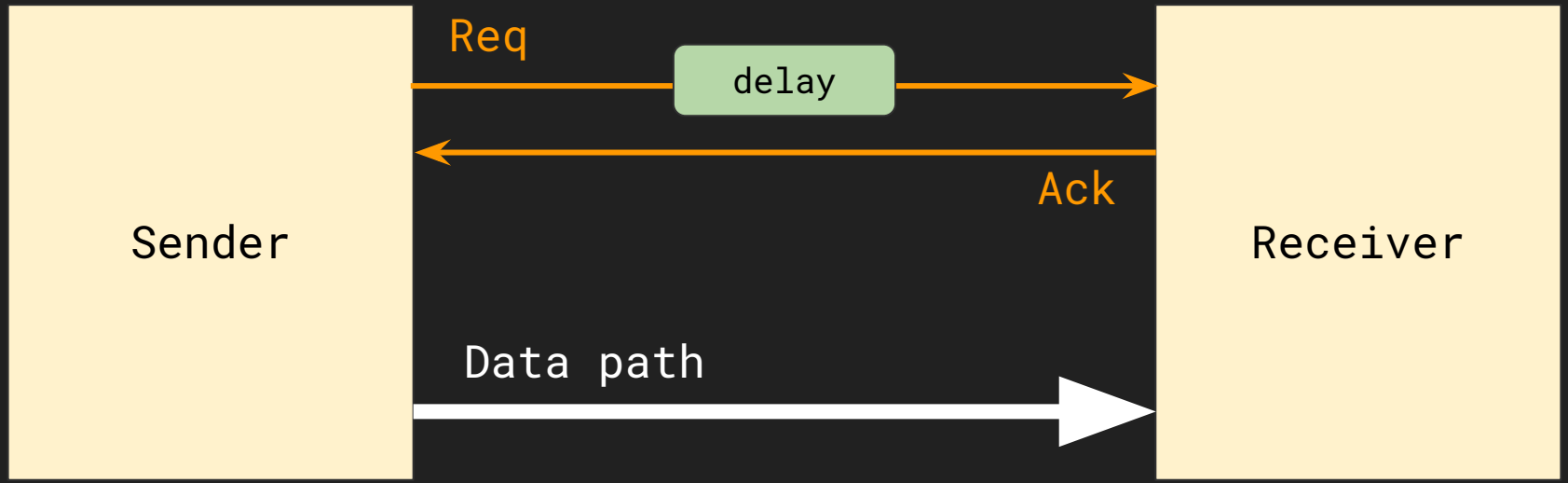


Combinatory Logic - Delay blocks

- Force delay on each input
- Control transitive state

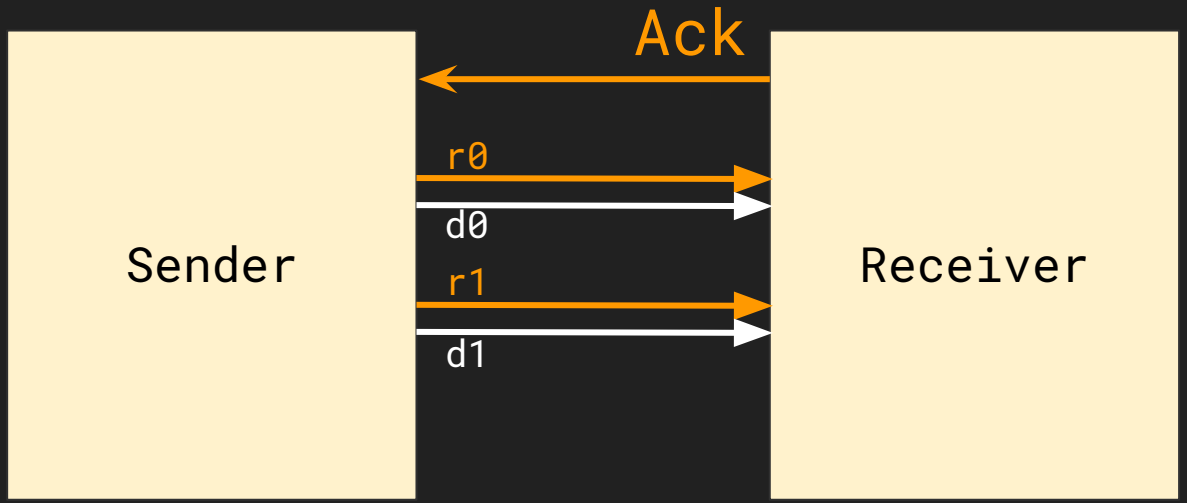


Handshaking pipeline



Delay to send req signal = worst data setting time

Asynchronous data encoding protocols - dual rail

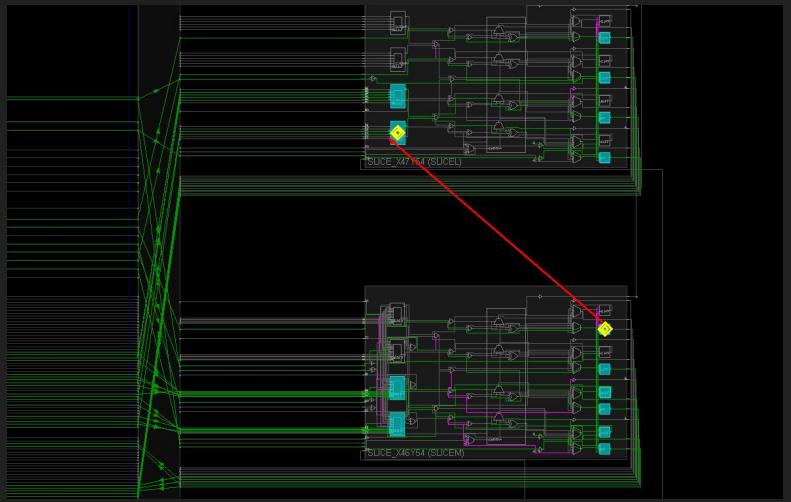


d	r	value
0	0	Null
1	0	1
0	1	0
1	1	*Invalid*

Double the data bus → Assure validity

Manual Place & Route

- No depend to place & route algorithms changes
- Control clock skew and delays
- Automatization optimized for asynchronous logic ?



Thank you!

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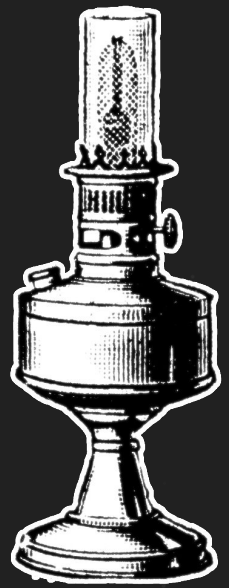

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