The EMI benefits of ground plane stitching in multi-layer power bus stacks

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Abstract: The effect on EMI of stitching multiple ground planes together along the periphery of multi-layer PCB stacks is studied. Power bus noise induced EMI and radiation from the board edges is the major concern herein. The EMI at 3 meters for different via stitch spacing and layer thickness is modeled with FDTD modeling. It is shown that the ground plane stitching effectively reduces the radiated EMI that results from fringing fields at the power bus edges. Two families of curves are generated to demonstrate the variation of the radiated EMI as a function of layer thickness and stitch spacing. Further studies show that the reduction of the EMI from ground plane stitching may be compromised by other radiation mechanisms.

I. Introduction

In printed circuit boards (PCB), the power plane and ground planes are typically of appreciable electrical extent, and may function as EMI antennas at high frequencies [1], [2], [3] and [4]. More specifically, for multi-layer structures with entire power and ground layers, the power and ground plane pair is essentially a radiating microstrip-patch antenna, where radiation occurs as a result of the fringing electric field at the board edges [5]. Alternatively, these fringing fields can couple to enclosure modes, or directly couple to slots and apertures and result in radiation. Therefore, for power bus geometries with multiple ground planes, stitching the ground planes together at the periphery of the board using closely spaced vias can effectively shield the board edges, and reduce the level of the radiation from the fringing fields. Although this concept is often applied in practice, little work has been done regarding the effectiveness of ground plane stitching and quantifying the via spacing. A recent study of ground-plane stitching focused on the cross-talk issue, while the radiated EMI was not considered [6]. Other reported via stitching works include controlling the cross talk between PCB traces by applying a double row of plated hole vias adjacent to the microstrip trace [7], or placing via fences on both sides of the stripline and studying their effects on the coupling between adjacent striplines [8].

The studies presented herein focuses on the impact of ground plane stitching on radiated EMI. A direct approach of performing an effective study on the EMI consequence of the ground plane stitching is to conduct a series of EMI measurements in a chamber. However, this requires sophisticated measurement facilities, and construction of numerous boards for a parametric study. In this work, FDTD modeling is used as the alternative tool, and radiated EMI for a GNC-VCC-VCC-GND four-layer structure with different layer thicknesses and ground plane stitch spacings is computed through the numerical modeling. A parametric study was conducted, and two families of design curves were extracted to provide quantitative direction of EMI mitigation for this particular radiation mechanism.

II. FDTD Modeling in Power Bus Stacks

A three-layer board was constructed, and $|S_{11}|$ measured to experimentally demonstrate the FDTD modeling on a multi-layer-PCB, especially for the case of a via penetrating a complete plane. The board was constructed by compressing a double-sided PCB and a single-sided PCB together, as shown in Figure 1. The PCB dimensions were *15 cm* × *20 cm*, with a *63-mil.* layer spacing FR4 dielectric. The signal was fed by a semi-rigid coaxial cable. The feeding point was *6 cm* away from the short edge, and *4 cm* away from the long edge of the ground plane. Two square apertures were cut in the middle plane by removing the copper cladding, so that signal and return pins penetrated the middle plane without contacting. The size of the aperture *was 1.5 mm* × *1.5 mm*. At each of the four board corners, two *47* Ω resistors were soldered to the planes, with one soldered to the middle and top plane, and the other soldered to the middle and bottom plane. The purpose of these resistors was to reduce the artificially high Q of the parallel planes, which requires excessive time steps in the FDTD modeling.

The $|S_{11}|$ of the test board was measured with an HP 8753D network analyzer and compared to the FDTD modeled results. In the FDTD modeling, the cell size was chosen as *1 mm* ×

1 mm × 0.04 mm, and the apertures in the middle plane were approximated with 4 cells. The dielectric loss had a prominent effect on the Q value of the mode resonances at higher frequencies and was necessary to be included in the numerical modeling. Although incorporating a frequency-dependent dielectric loss in the modeling is feasible, a simpler approach was taken by dividing the studied frequency range in half and using a uniform effective dielectric conductivity in each range [9]. For this particular problem, the effective conductivity of the dielectric material determined by matching experimental and FDTD results on a two-layer structure of similar material was *0.000035 S/cm* and *0.0002 S/cm* over the frequency range *100 MHz - 2 GHz*, and *2 GHz - 5 GHz*, respectively. The source in the FDTD modeling was a sinusoidally modulated Gaussian voltage source with a source impedance of *50 Ω*. The wire structures were modeled using the thin wire algorithm [10], and resistors were modeled as described in [11]. The comparison of the modeled results and the measured results is shown in Figure 2. The modeled results with higher dielectric loss agree well with the measured results at high frequencies, while the modeled results with lower dielectric loss agree well with the measured results at low frequencies.

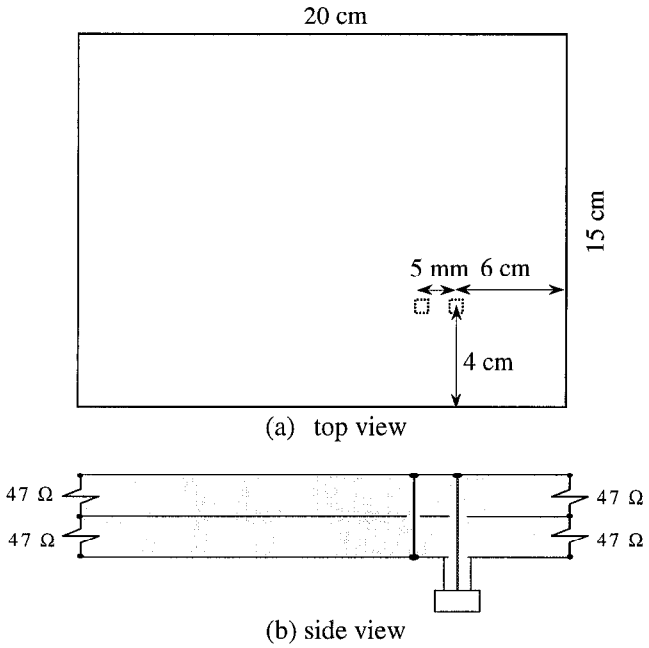


Figure 1. Geometry of the three-layer test board for the comparison of measured and FDTD results.

The modeled example contains basic geometries of interest in the power-bus problems. Therefore, the FDTD method is deemed suitable for modeling power-bus problems. A far-field calculation algorithm has also been incorporated in the FDTD modeling tool. The same modeling tool has been proven to correctly predict the |E| field at *3 m* for frequencies above 500 MHz [12], [13]. The FDTD method was then applied to model the radiated EMI at *3 m* from a GND-VCC-VCC-GND four-layer power-bus stack with different layer thicknesses and different ground plane stitch spacings. A parametric study was then conducted based on the FDTD modeled results.

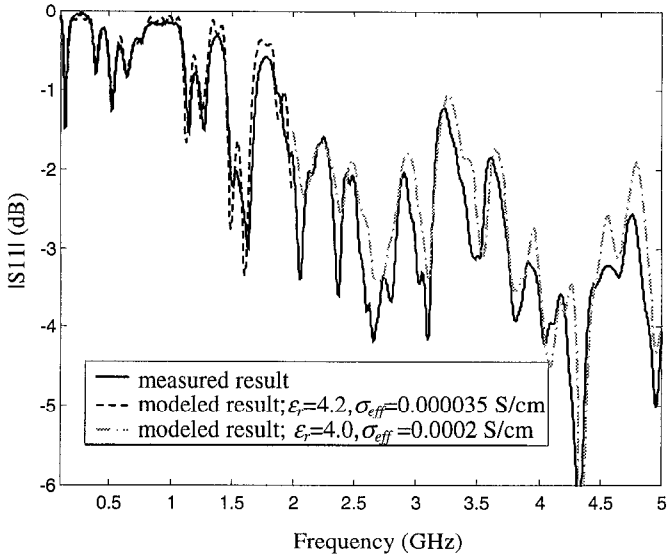


Figure 2. FDTD modeled and measured $|S_{11}|$ for the test board shown in Figure 1.

III. EMI Benefits of Ground Plane Stitching in Multi-Layer Power Bus Stacks

As stated in Section I, for designs that employ multiple power-ground layer sets, using via stitching to connect outer ground layers may mitigate EMI dominated by fringing edge electric fields of the power bus. An effective shielding enclosure is formed by the ground planes and the stitching vias that contains the fields within this structure. In this section, the EMI at 3 meters for different via stitch spacing and layer thickness is computed from FDTD modeling. Design curves are generated to demonstrate the variation of EMI as a function of the layer thickness and stitch spacing.

A four-layer PCB with a GND-VCC-VCC-GND power bus stack, as shown in Figure 3, was selected as the test bed for the FDTD modeling studies. The board was *15 cm × 20 cm*, and the layer thickness was *25 mils*. The relative dielectric constant was set as ε_r = 4.2, and the effective dielectric conductivity was *0.00035 S/cm* in the modeling to represent the dielectric loss of the board. The conductor on the VCC layers was recessed *8mm* at each of the four board edges. The feeding point was *6 cm* away from the *15-cm* edge, and *4 cm* away from the *20-cm* edge of the ground plane. The via holes on the two middle planes for wires to penetrate through and connect the top and bottom ground planes in the stack were modeled as *2 mm × 2 mm* apertures. The spacing between the two shorting wires was *3 mm*. The radius of all the wires in the stack was *24 mils*. This source configuration was used to

mimic connections and current injection by a source on the top of the board. A source placed on top of the board also radiates directly as shown later, and this additional mechanism was removed by placing the excitation interior to the planes, while maintaining the same current injection pathes.

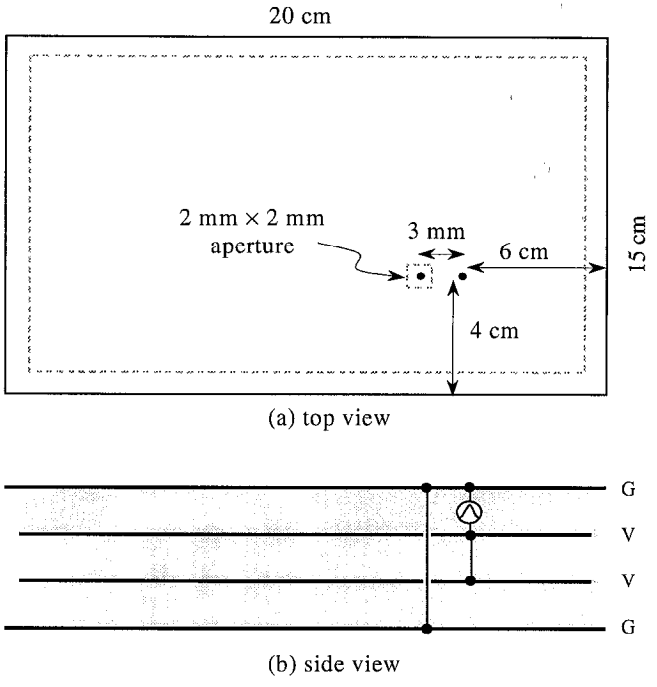


Figure 3. Schematic of the GND-VCC-VCC-GND power bus stack for the FDTD modeling.

The cell size in the FDTD modeling was *1 mm × 1 mm × 0.212 mm*. Each layer of the dielectrics was then modeled by 3 cells. The voltage source was a sinusoidally modulated Gaussian source with a *50 Ω* source impedance, and the wire structures were modeled using the thin wire algorithm. For the cases of stitching, the two GND planes were stitched together by a number of equally spaced wires around the periphery. All the stitching points were located *1 mm* (1 cell) away from the board edge. Four different stitch spacings, *2 mm, 3mm, 5mm,* and *10 mm*, were considered.

The radiated EMI at *3 m* was then computed from the FDTD modeling. The far-field observation point was selected broadside to the radiating power bus as illustrated in Figure 4. The modeled results for different stitching cases, together with the results of the case without stitching, are shown in Figure 5. The result for the case that only the top two layers are present is also shown in the same figure. All the modeled E-fields are the E_y polarization, and are normalized to a *1 mA* current source. The results indicate that stitching significantly reduces the EMI, and a denser stitching around the periphery of the board can improve the EMI performance for a radiation mechanism dominated by fringing fields from the board edge. The EMI reduction for denser stitch spacing is generally a constant over the studied frequency range of *500 MHz – 5 GHz*. The comparison of the two-layer stack and four-layer stack without stitching indicates that adding the two additional planes to the simple two-layer structure only slightly improves the EMI performance. This is due to the fact that the radiation predominantly results from the fringing field at the edges of the top two planes, and adding the additional planes has only marginal merits on mitigating the radiating source. Both the horizontal polarization (E_x) and the vertical polarization (E_y) were studied for all the cases. However, only the results for the E_y polarization are reported herein for brevity, since the conclusions drawn from the results of E_x polarization are the same.

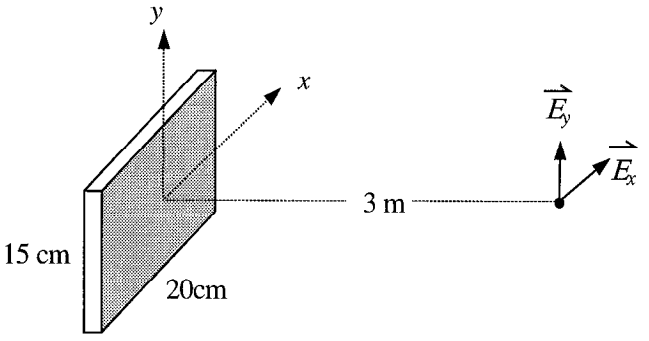


Figure 4. A schematic representation of the coordinate system and the E-field components of a far-field observation point broadside to the radiating power bus.

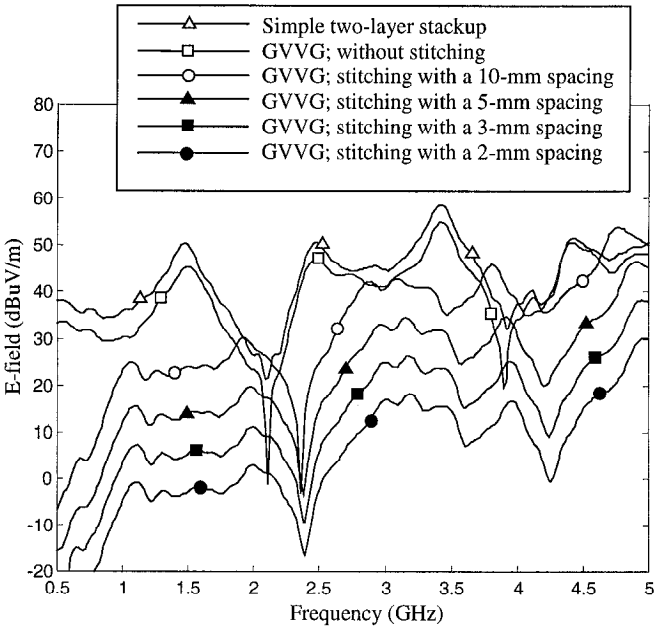


Figure 5. The FDTD modeled E-field at *3 m* (E_y polarization) for the multi-layer board with different stitching cases. The layer thickness was *25 mils* for all cases.

In the next step of the study, the uniform stitch spacing was fixed at *3 mm*, while the layer thickness varied as *15 mils, 25 mils, 40 mils, 60 mils,* and *100 mils*. The EMI at *3 m* was computed using FDTD modeling. The results are shown in Figure 6. Again, all the modeled fields are the E_y polarization, and are normalized to a *1 mA* current source. The results indicate that decreasing the layer thickness reduces the radiated EMI. This is because a thinner substrate increases the capacitance between the planes, which means smaller input impedance of the parallel planes. The power bus voltage was then decreased (since the source impedance was a constant of 50 Ω), which results in smaller radiation [5]. A similar conclusion based on experimental work has been previously reported in [14]. Also, this variation in radiation with substrate thickness is consistent with that reported in the microstrip patch antenna literature [15]. The EMI reduction for smaller layer thickness is generally a constant over the studied frequency range.

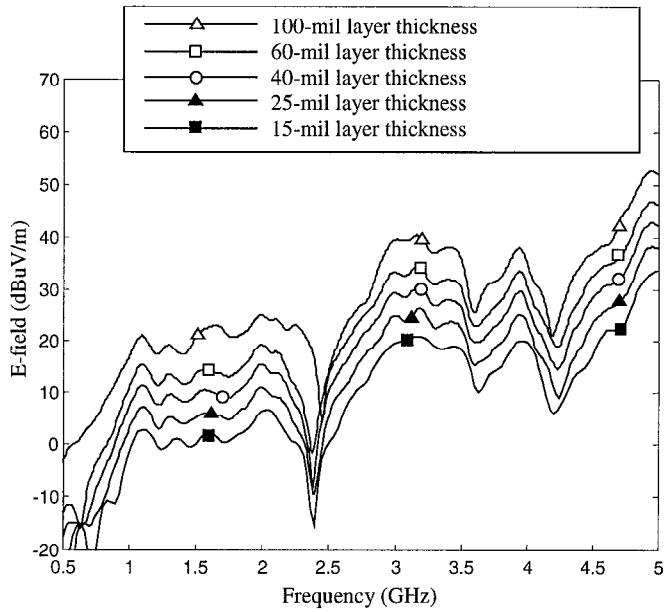


Figure 6. The FDTD modeled E-field at *3 m* (E_y polarization) for the multi-layer board with different layer thicknesses. The stitch spacing was *3 mm* for all cases.

The FDTD modeling was then applied to other cases with different stitch spacing and different layer thicknesses, and altogether 20 cases were studied for the stitch spacings of *2 mm, 3 mm, 5 mm, 10 mm* and the layer thicknesses *of 15 mils, 25 mils, 40 mils, 60 mils, 100 mils*. The objective was to develop design curves that reflect the EMI variation as a function of layer thickness and stitch spacing. Two families of curves were generated from the results of these 20 simulations. Figure 7 shows a family of curves that reflect the variation of the EMI as a function of layer thickness. Each curve is the relationship between the E-field at *3 m* and the layer thickness. Different curves have different values of stitch spacing. The modeled E-field of the *15-mil* board with *2 mm* stitch spacing is used as the reference (set to *0 dB*). The results for a *5-mil.* layer-thickness are extrapolated from the nearly linear variation of the curves with board thickness. Another family of curves was generated from the same results to have a clearer view of the functional relationship between the EMI at *3 m* and the stitch spacing. This family of curves is shown in Figure 8. The results indicate that the radiated field has an approximately exponential relationship to the stitch spacing (so is linear in the log-log-scale plot in Figure 8) for the cases considered with the stitch spacing ranging from *2 mm* to *10 mm*.

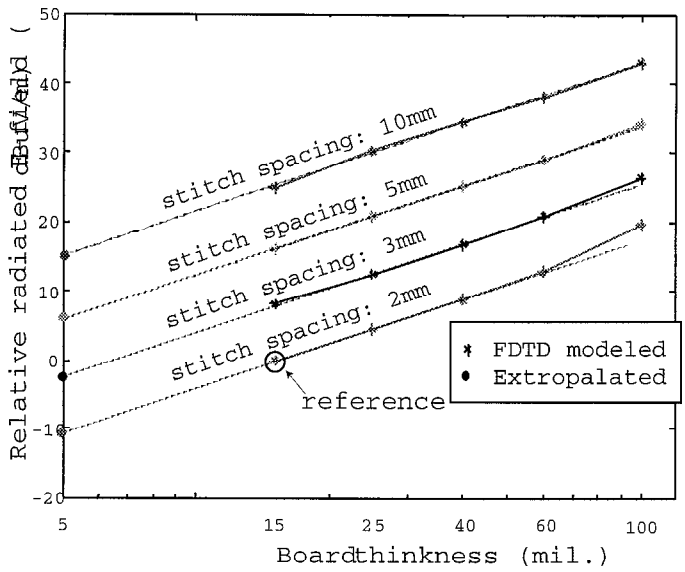


Figure 7. The EMI at *3 m* varies as a function of layer thickness for different uniform stitch spacings.

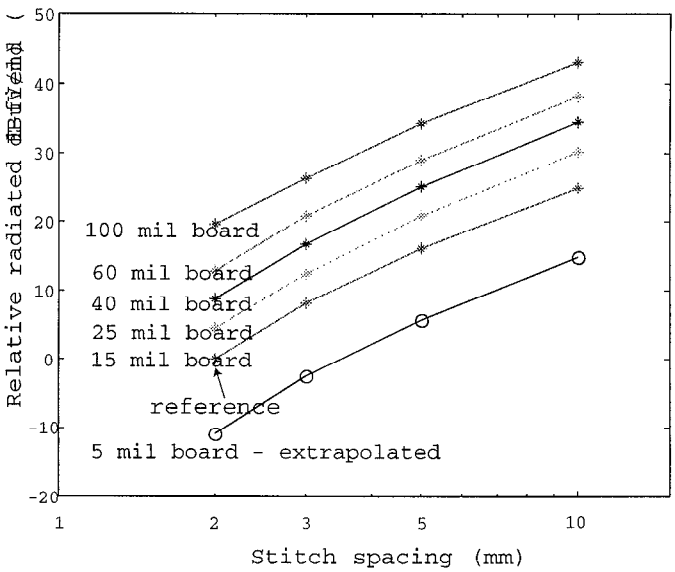


Figure 8. The EMI at *3 m* as a function of stitch spacing for different layer thicknesses.

In the study presented above, the power planes were driven by a source in between the top two layers of the circuit in order to eliminate other possible radiation mechanisms, and focus on the effects of ground plane stitching on radiation dominated by fringing fields at board edges. To take the study a step further, the case with the planes being driven by a source on top of the board was also considered. The schematic is shown in Figure 9. The geometry is the same as that shown in Figure 3, except that the source is placed on top of the board and there is a *3-mm* long wire routing above the top plane. The spacing between the wire and the top plane is one cell (*8.33 mils*).

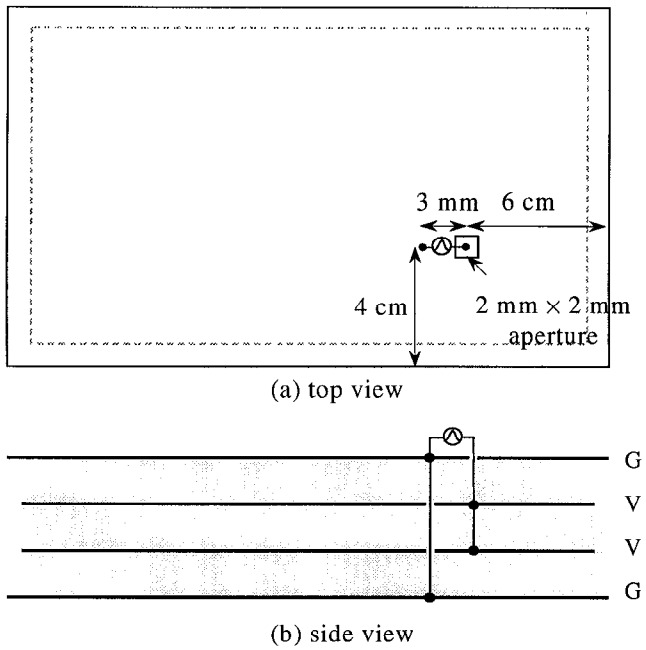
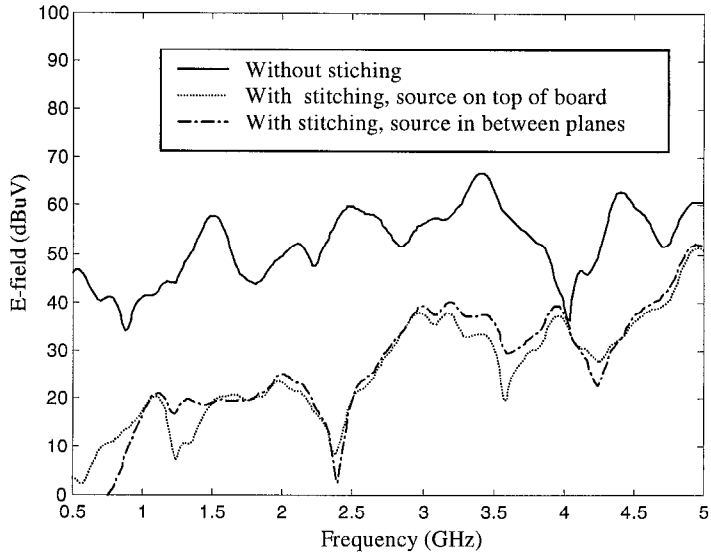
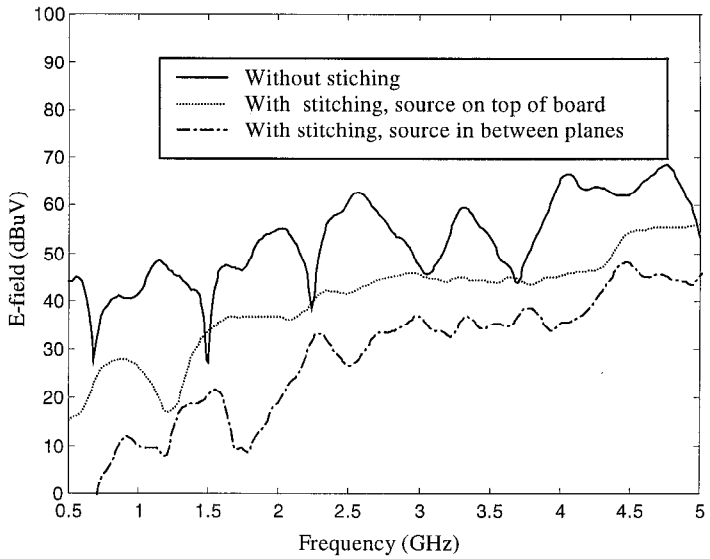


Figure 9. Schematic of the GND-VCC-VCC-GND stack with source placed on top of the board.

For the case without stitching, the FDTD modeled E-field is almost the same for both cases of source placements, interior and exterior to the planes (the comparison is not shown herein for brevity). This is because the radiation is dominated by the the fringing field at the edges of top two planes, which is almost at the same level for both configurations with different source placements. For the case of a uniform stitching with a spacing of *3 mm*, the difference of the EMI between the two types of source placement is shown in Figure 10. The source placement has little effect on the *3-m* E-field of vertical polarization. However, the *3-m* E-field for the horizontal polarization with source located above the plane spacing was on average approximately *10 dB* higher than that with the source placed in between planes. This polarization-dependent behavior is due to the horizontal routing of the *3-mm* wire on top of the board, which is a dominant radiation mechanism when there is dense ground plane stitching around the board edges. The results indicate that the EMI reduction using ground plane stitching can be limited by other radiation mechanisms.



(a) vertical (E_y) polarization



(b) horizontal (E_x) polarization

Figure 10. The FDTD modeled *3-m* E-field for different source placements.

IV. Summary and Conclusions

The EMI benefits of the ground plane stitching in multi-layer power bus stack were studied herein. Experimental work was conducted to corroborate the validity of the FDTD method in power bus modeling. The good agreement between the measurements and FDTD modeling provides confidence in the FDTD method for developing the power bus design approach.

The EMI benefits of the ground plane stitching were demonstrated through the FDTD modeled E-field of a GND-VCC-VCC-GND four-layer power bus stack. Different layer thickness and different stitching spacing were considered. A number of simulations were conducted, and designed curves were generated to demonstrate the variation of radiated EMI as a function of the layer thickness and the stitch spacing.

Generally, for PCBs with multiple power and ground layers, arranging the layer stackup such that ground layers are the first complete layers (or portions thereof) from the top and bottom board sides, and stitching the ground planes together all around the edges can achieve in excess of *10-20 dB* EMI reduction for EMI dominated by the fringing edge fields on the power bus. A minimum of *2 mm* stitch spacing was investigated, for which approximately *20 dB* EMI reduction was achieved.

The EMI mechanism of concern in this study was radiation dominated by the fringing electric field at the edges of the power area. Other potential EMI coupling paths and radiation mechanisms that are related to noise on the DC power bus include power bus noise conducted through the power pins of a connector and coupled to a radiating structure on a different board, coupling to an I/O line that transitions through the DC power bus, and direct radiation from the active components themselves. For the PCBs whose dominant EMI coupling mechanism comes from the fringing field of the power bus, the EMI improvement of the functioning system from the ground plane stitching can be compromised due to other second-level coupling mechanisms, which may show up and become a dominant one when the original dominant coupling mechanism is mitigated.

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