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Hardening-By-Design Techniques for Analog and Mixed-Signal ASICs

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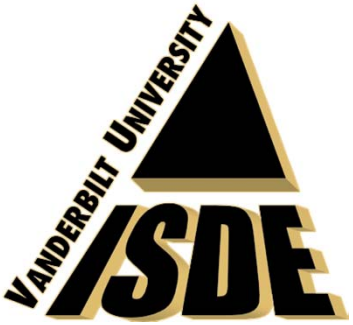

SE Mitigation in Analog and Mixed-Signal ASICs

- Motivation for radiation-hardened-by-design analog and mixed signal integrated circuits
- Background: Cross-domain response mechanisms and complex error signatures
- Overview: Mitigation of radiation effects
  - *device-level (technology and/or layout modifications)*
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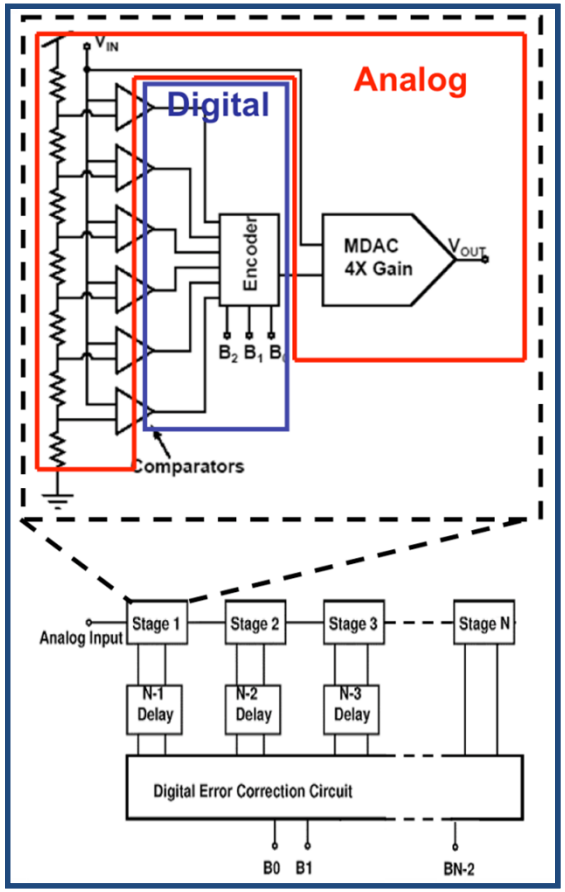
Motivation for RHBD Analog & Mixed-Signal

- The ability to put entire systems on a chip has increased the demand for mixed analog/digital (mixed-signal) circuits
  - *if analog functionality can be done with digital technology, it will be!*
  - *but, most ICs still require some analog – processes usually have a separate and higher VDD specifically for analog*



Block Diagram of a Pipelined Analog-to-Digital Converter

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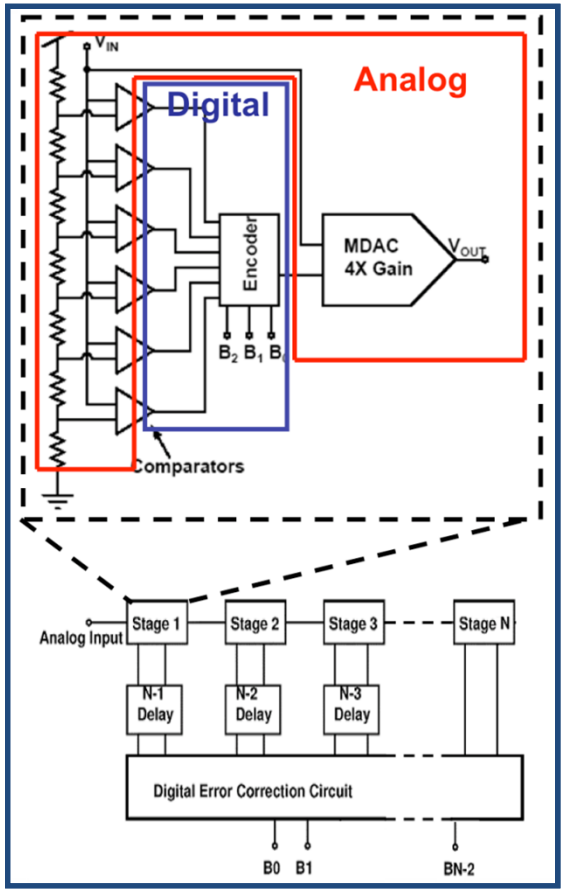
  - *but, most ICs still require some analog – processes usually have a separate and higher VDD specifically for analog*
- Single-event effects (SEE) present challenges for analog & mixed-signal (A/MS) systems
  - ***single-event transients (SET) are subject to cross-domain response mechanisms***
  - ***SE mechanisms may not be tractable using conventional analysis techniques***
  - ***new SE error metrics may be required due to the complexity of sub-circuits and functionality***



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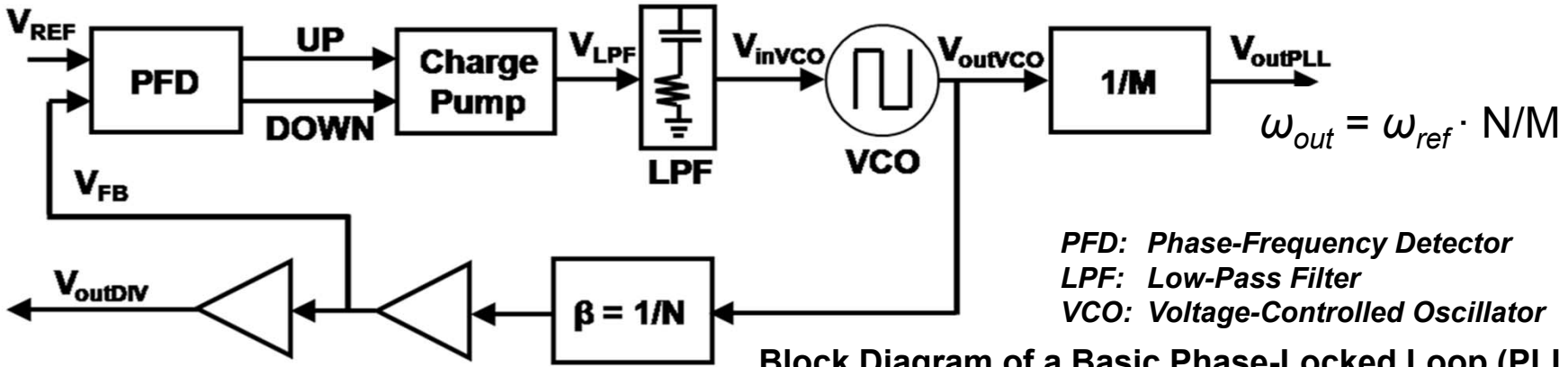
Cross-Domain Response Mechanisms

- Mixed-signal circuits are required to bridge analog and digital domains - as a consequence, designs are often subject to a variety of response mechanisms
  - *steady-state and transient*
  - *low-frequency and RF*
  - *digital noise and sensitive analog components*
- Single-events are subject to all interactions



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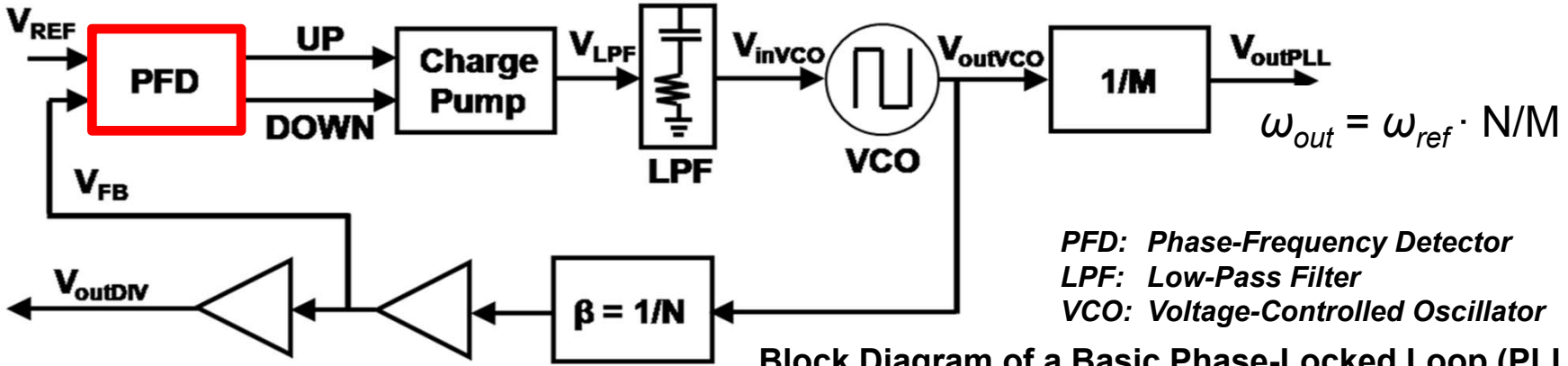

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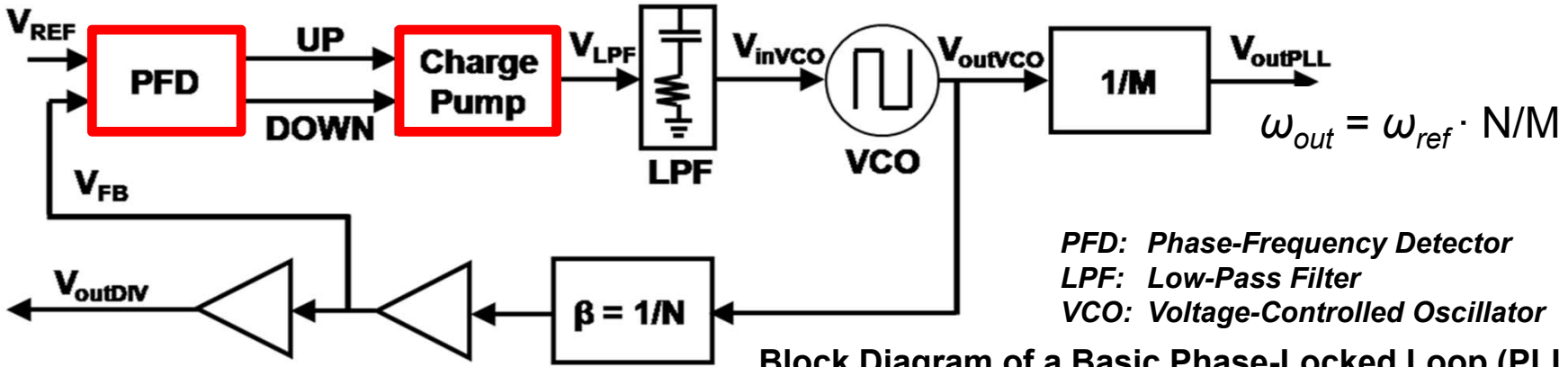

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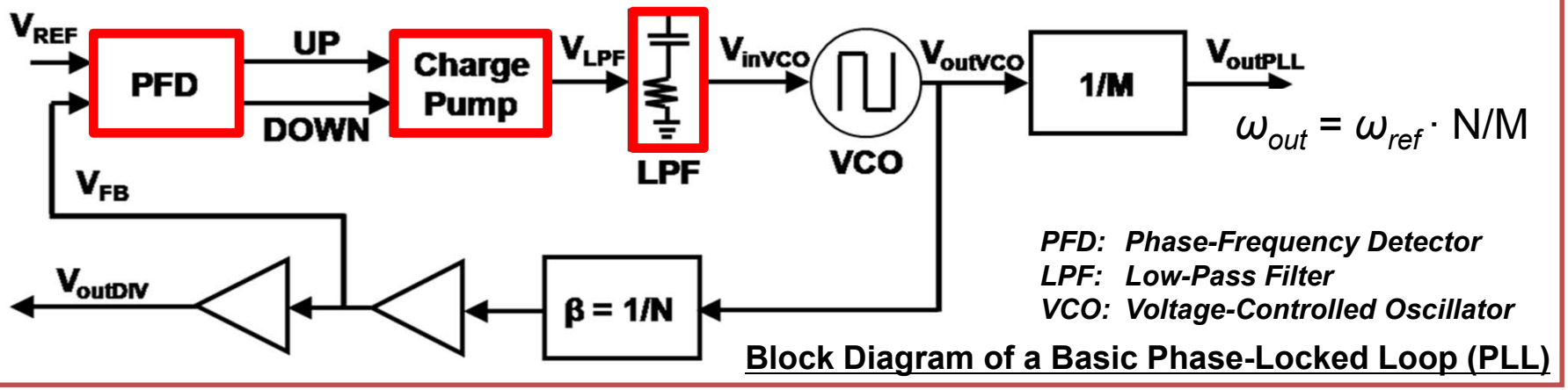

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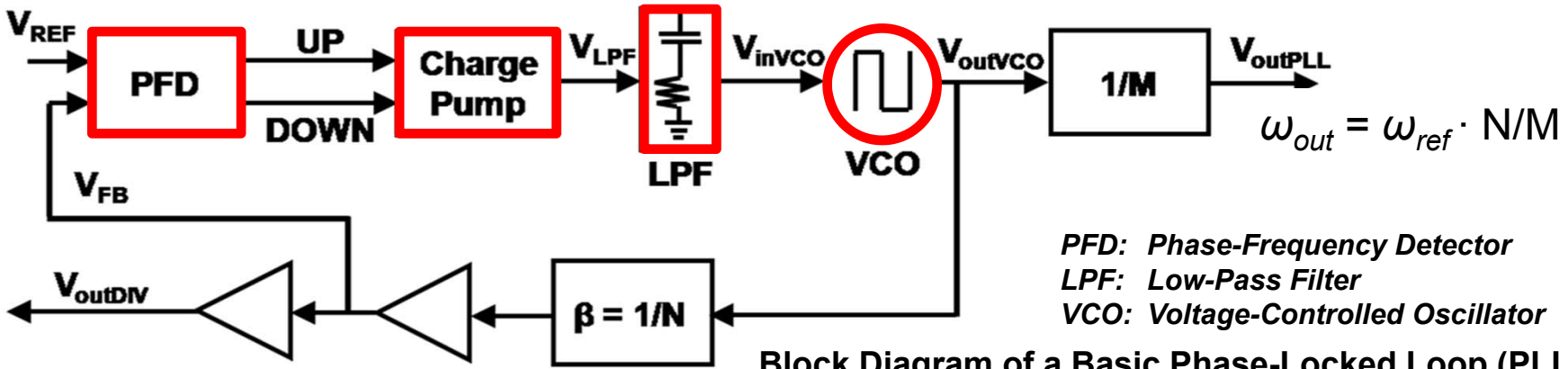
Phase → Digital (V) → Analog (I) → Analog (V) → Frequency



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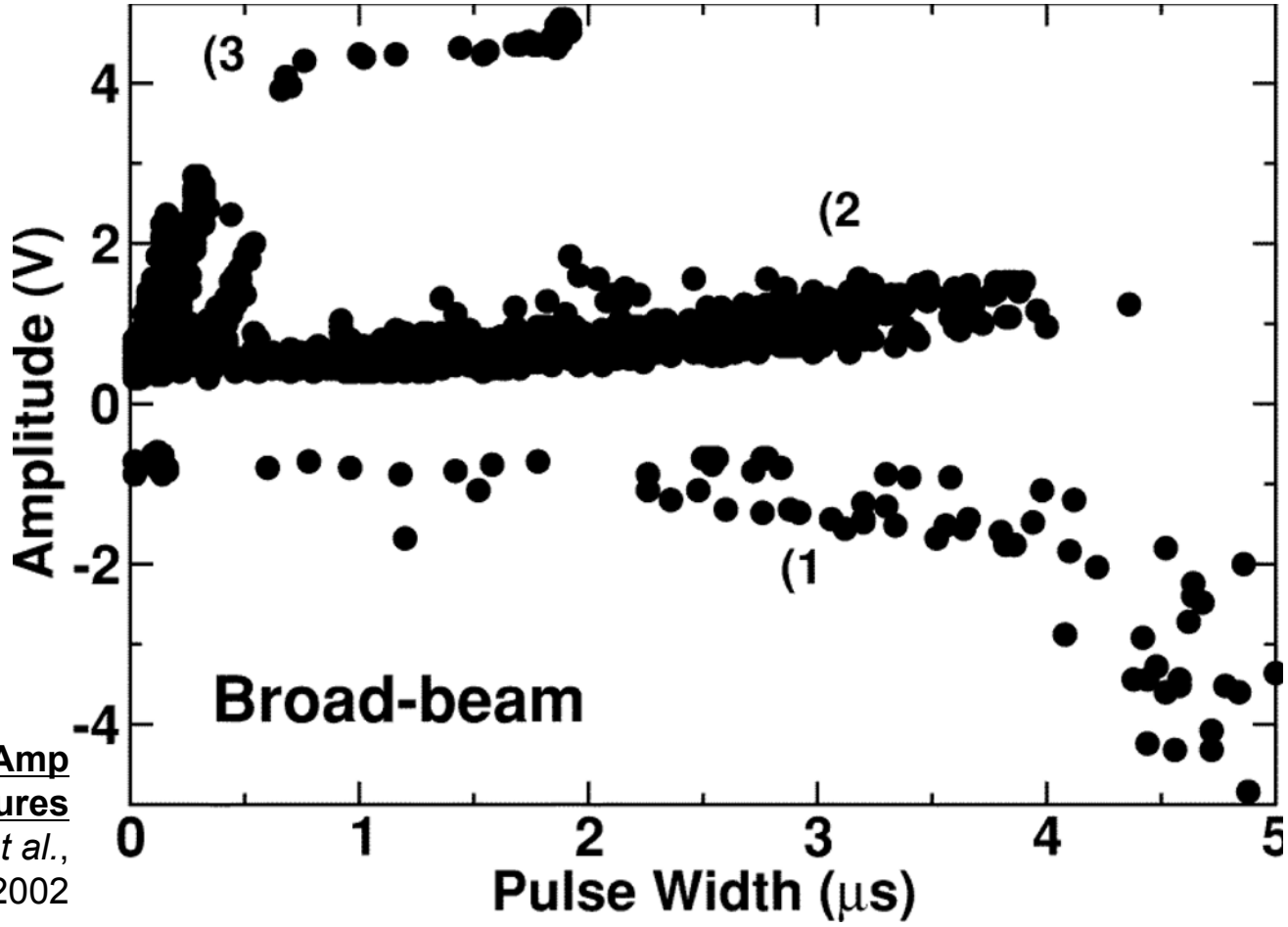
Complex Response Signatures

- No standard metric for SE in analog and mixed-signal (AMS) systems, as the effect of an SE is dependent on the **topology**, **function**, and the **operating mode**



LM124 Op Amp SEE Signatures
Boulghassoul, *et al.*, 2002

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Mitigation of Radiation Effects

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What about SE Performance?

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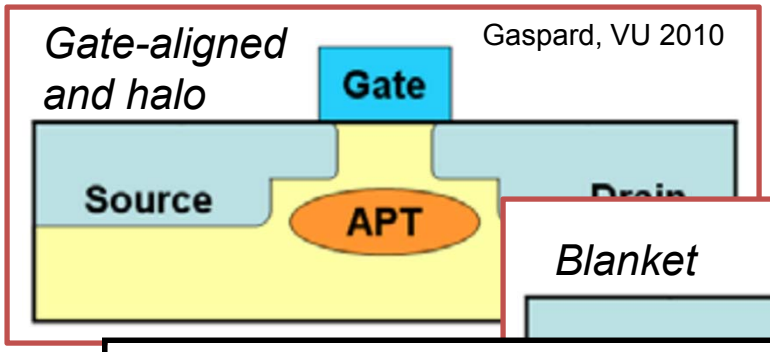

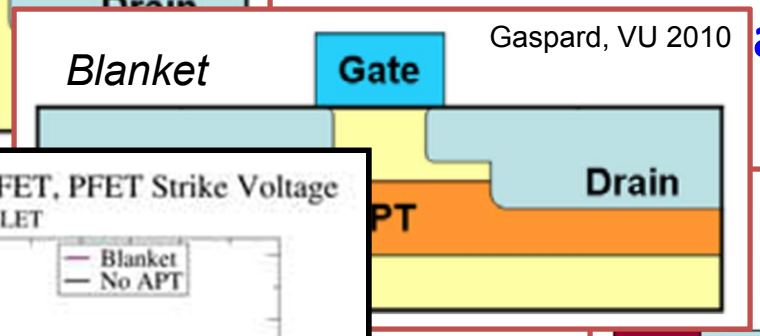

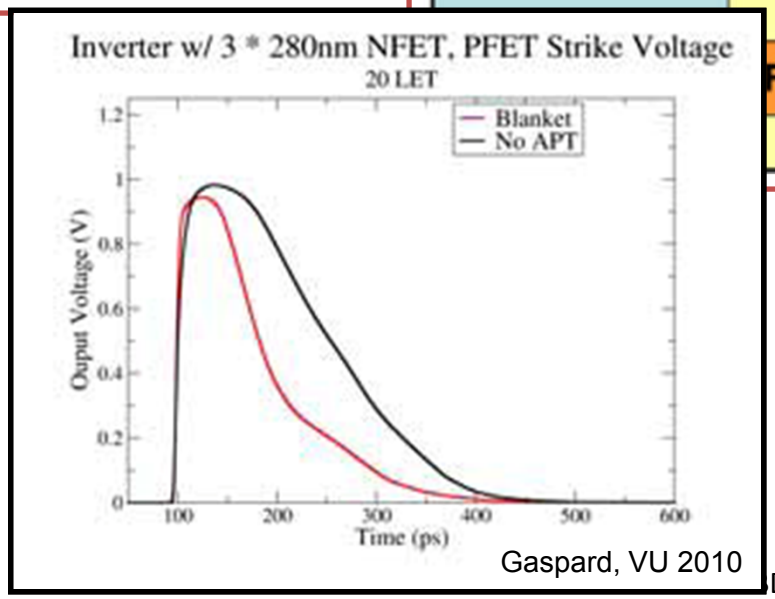

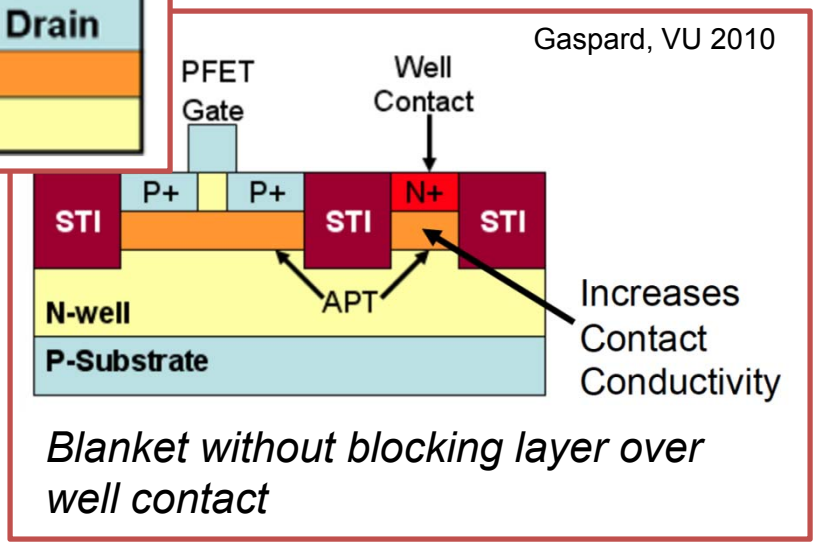

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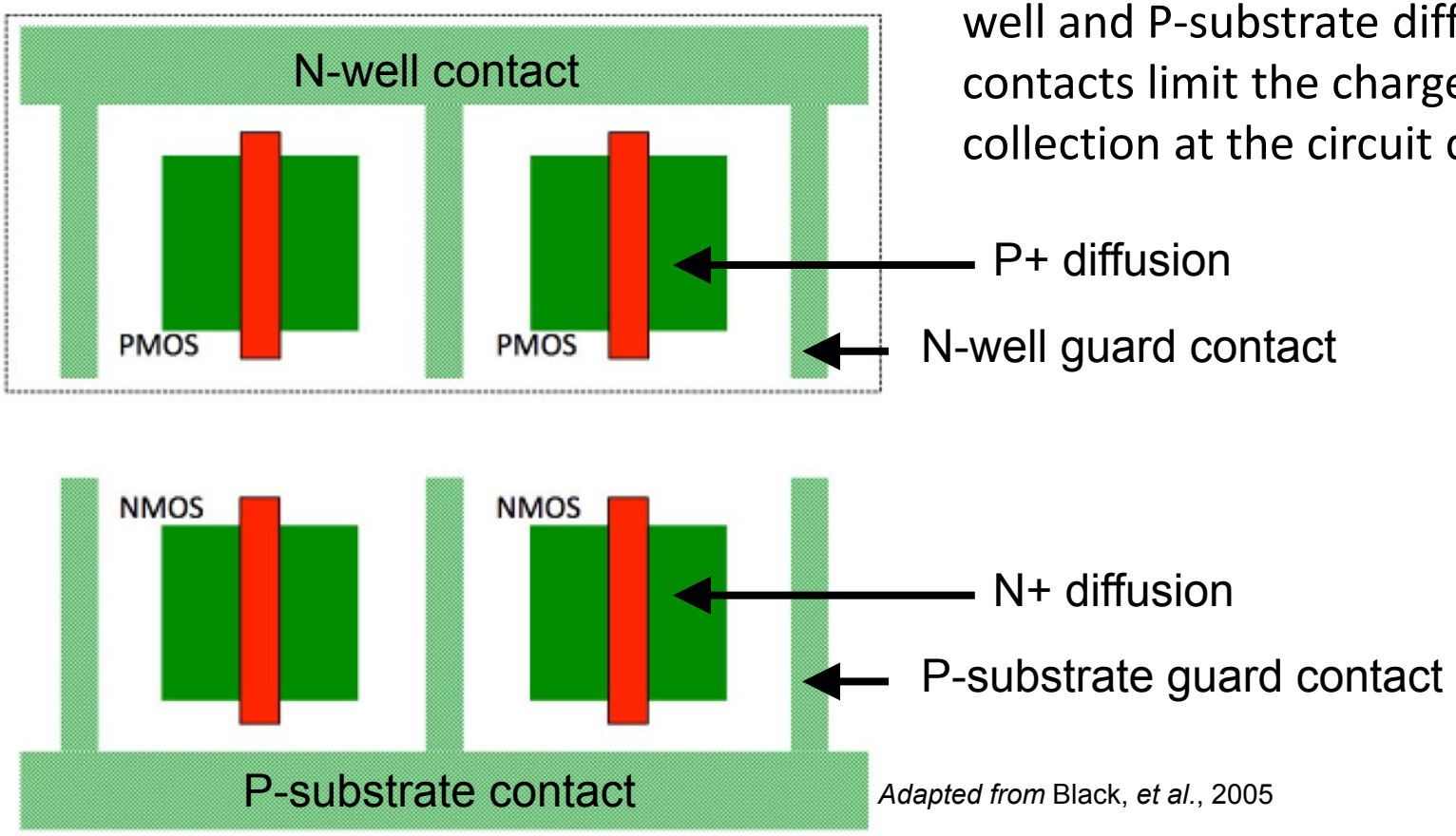
For example: Guard contacts, formed from N-well and P-substrate diffusion contacts limit the charge collection at the circuit diffusions



Adapted from Black, *et al.*, 2005

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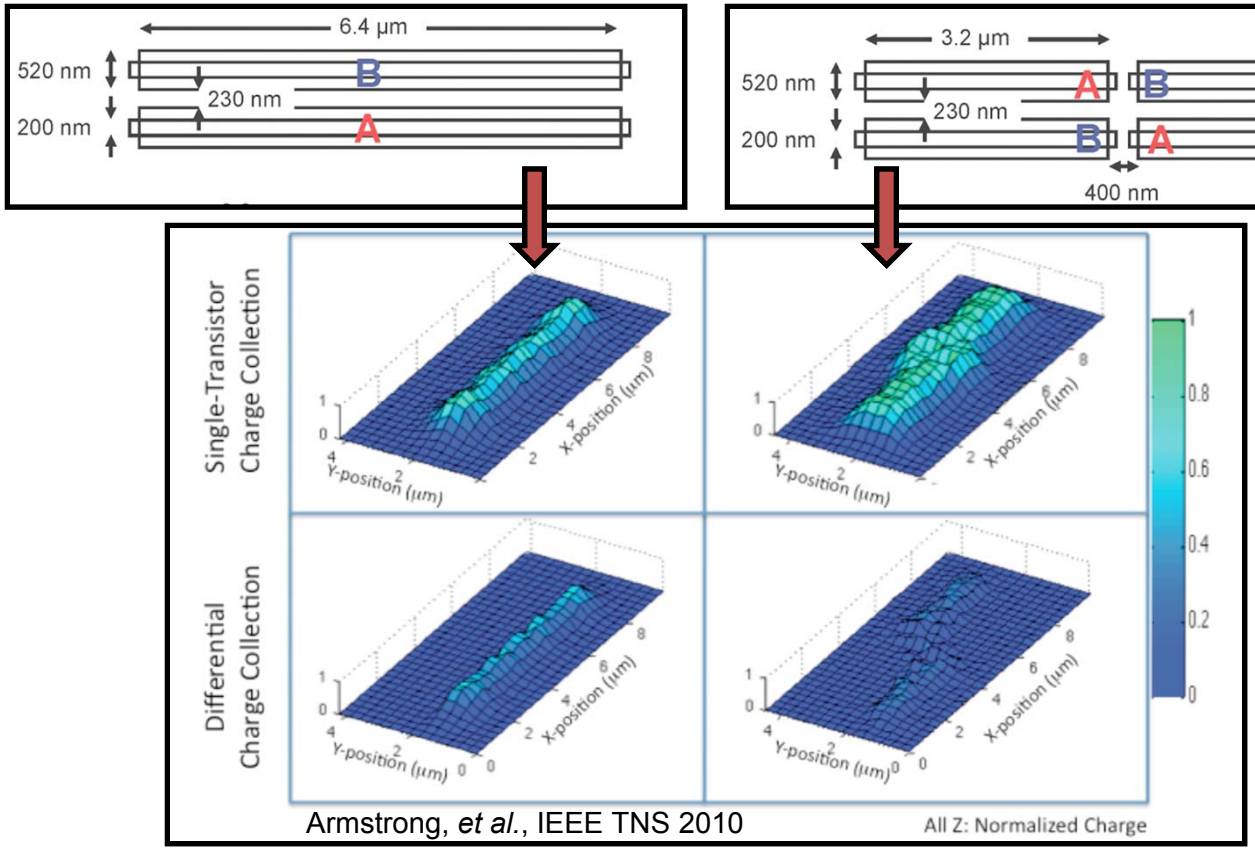

Armstrong, *et al.*, IEEE TNS 2010

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Can we utilize charge sharing to reduce SETs?

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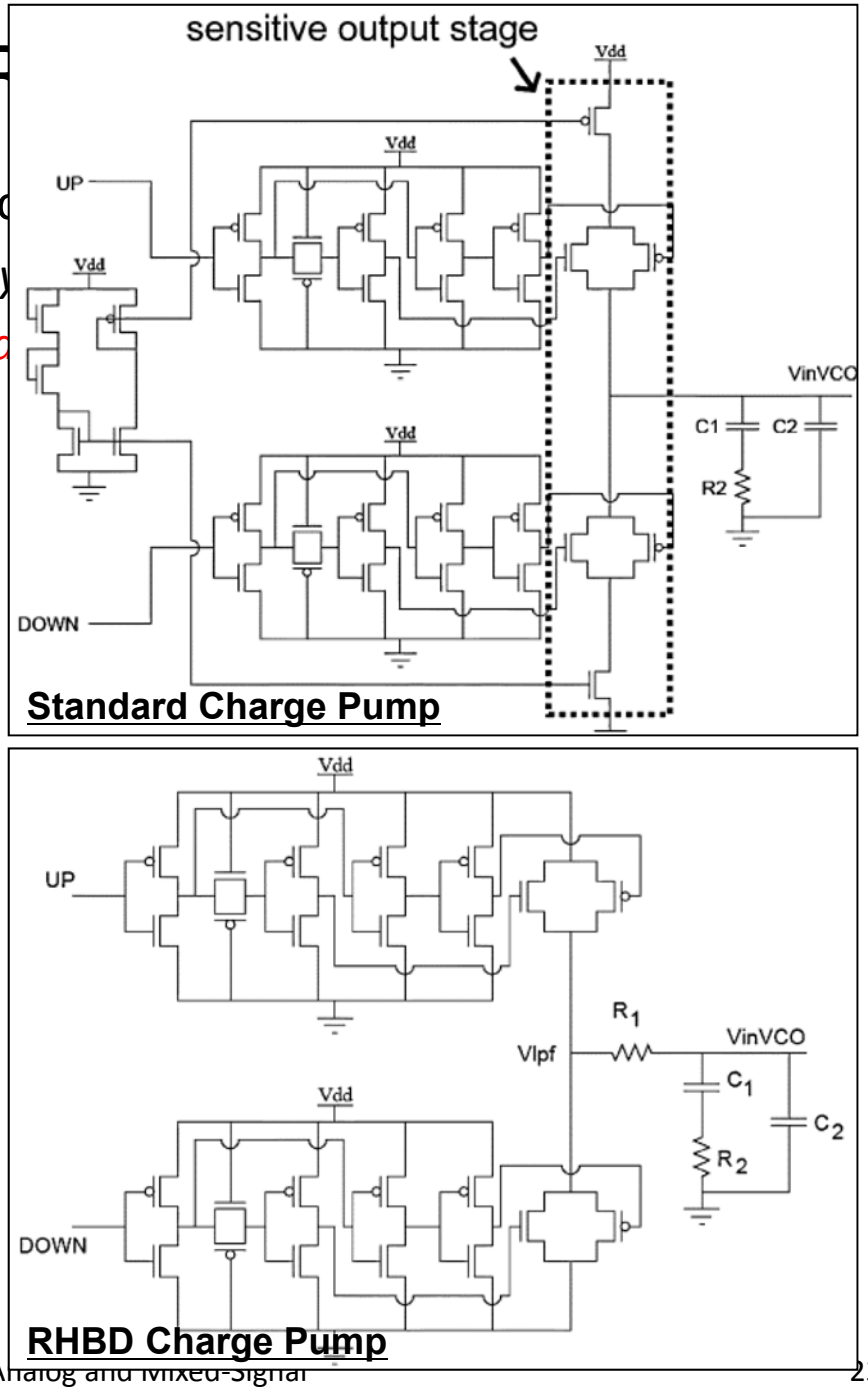

Loveless, *et al.*, IEEE TNS 2007

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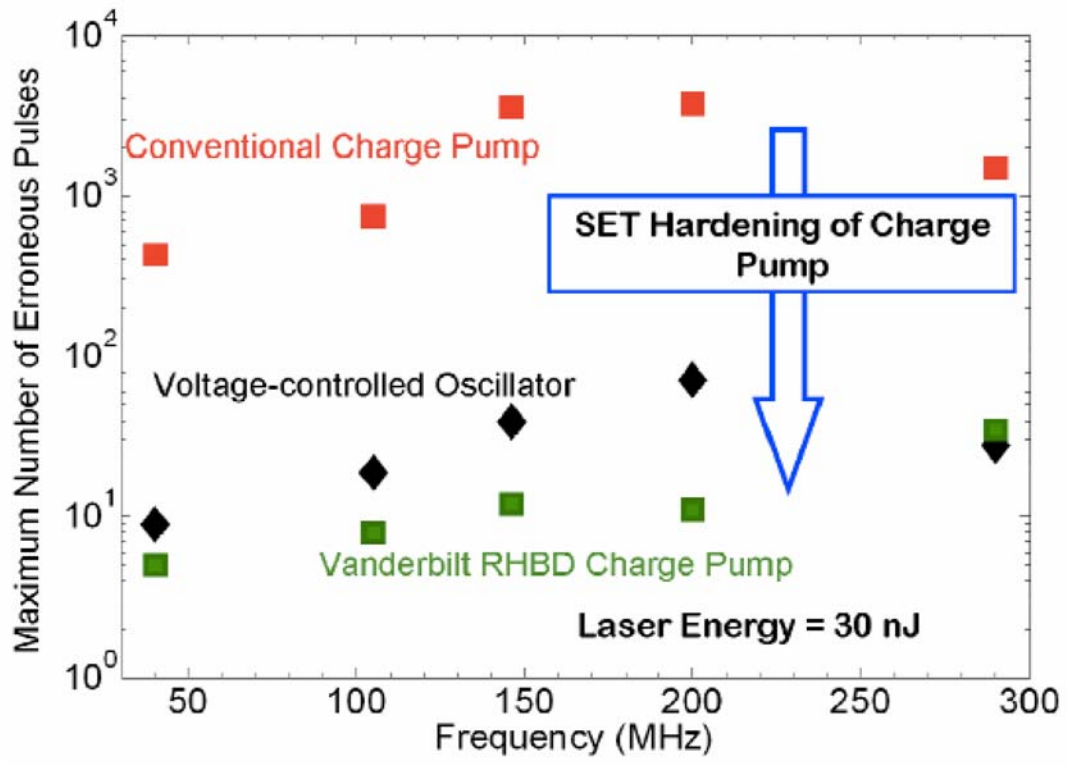

Loveless, *et al.*, IEEE TNS 2007

Can this technique be applied to other circuits?

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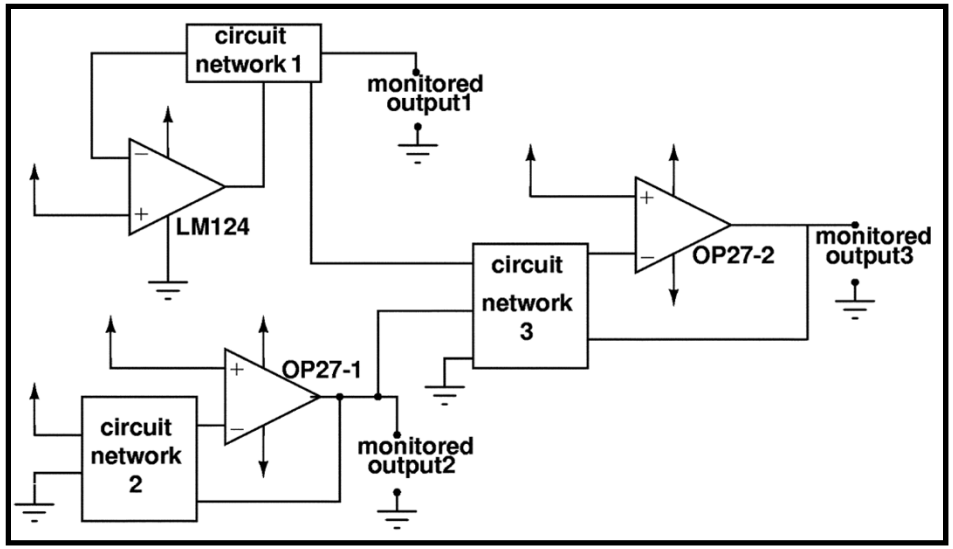
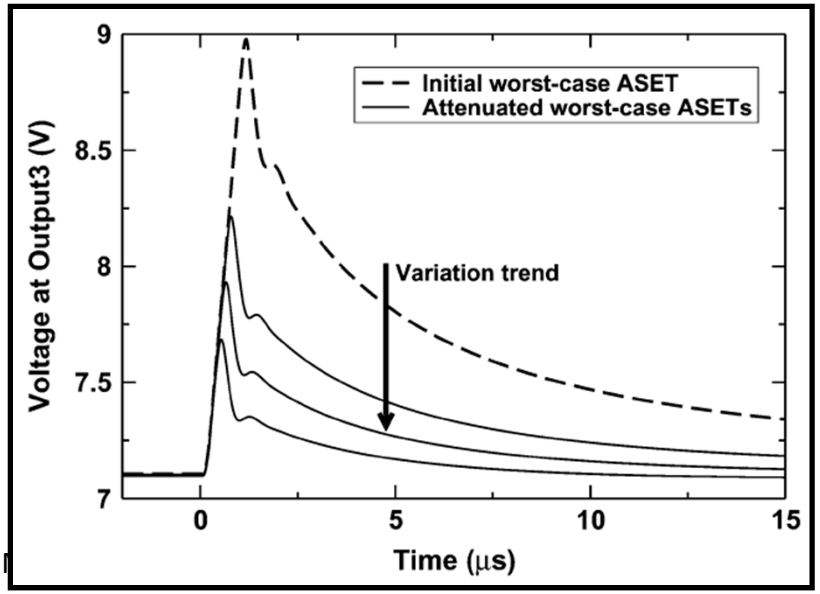


Block Diagram of Satellite Power Distribution Controller/Monitor

Boulghassoul, et al., IEEE TNS 2004



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Classification of Mitigation Techniques

- Generally, ASET mitigation involves one or both of the following, irrespective of the technology:
  - ***reducing*** *the amount of* ***collected charge (Q_{col})*** *at a metallurgical junction through:*
    - layout alternatives such as guard rings, drains, or diodes around MOS devices; n-rings, substrate-tap rings, and nested minority-carrier guard rings in BJT devices
    - substrate engineering (e.g., use of charge blocking layers in the substrate)
    - use of very thin epitaxial silicon layer (e.g., silicon-on-insulator (SOI))
    - addition of dummy collector for charge collection in HBT devices
    - increased substrate and well contacts (reduced substrate and well impedances)

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  - ***increasing*** *the* ***critical charge (Q_{crit})*** *required to generate an ASET*

    conventional, perhaps "brute force" methodology include:
    - increasing the transistor sizes (buffering)
    - increasing the drive currents
    - increasing the supply voltage
    - increasing capacitor sizes

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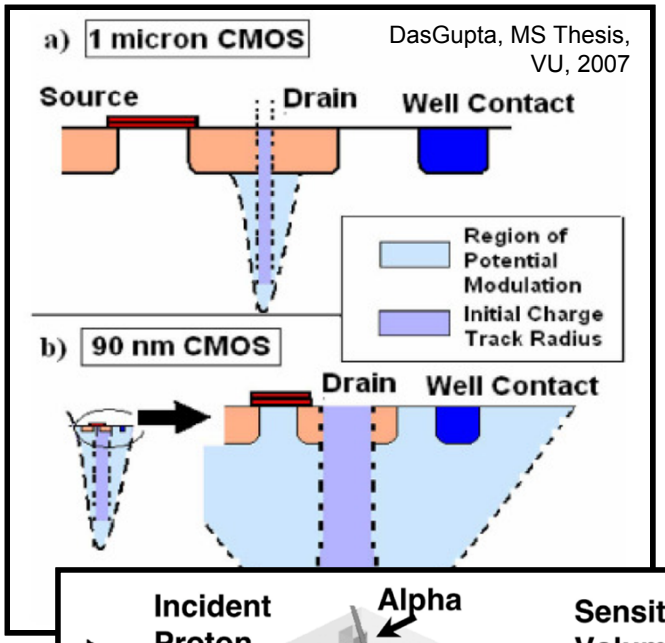
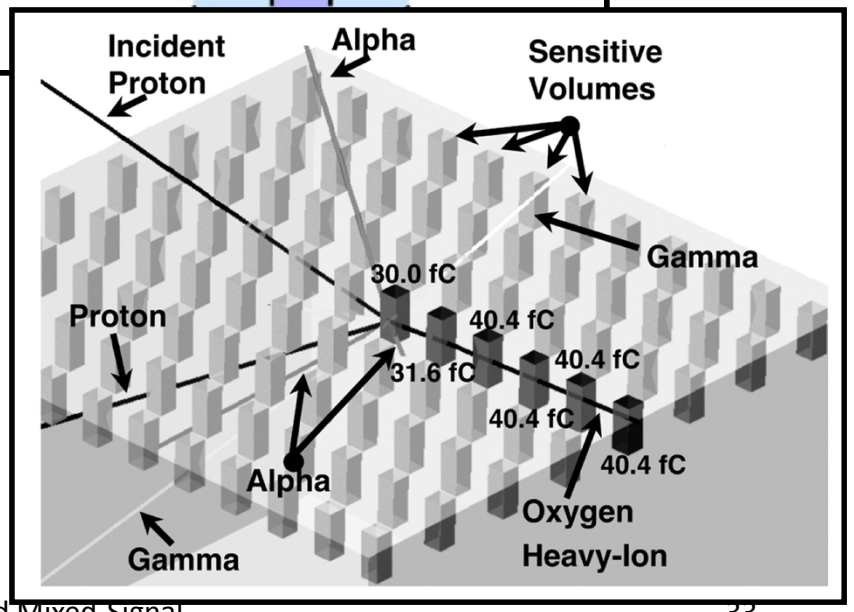
  Device, layout, circuit, and/or system modifications

Layout-Level Mitigation

- Layout-level mitigation: transistor- or circuit-level modification of layout cell arrangements for reducing the amount of collected charge at critical device junctions
- In recent years, "charge sharing" between transistors has become commonplace:
  - *decreased spacing of devices with technology scaling can increase the charge collection at nodes other than the primary struck node*
  - *layout-level mitigation is becoming increasingly important for ensuring radiation hardness*

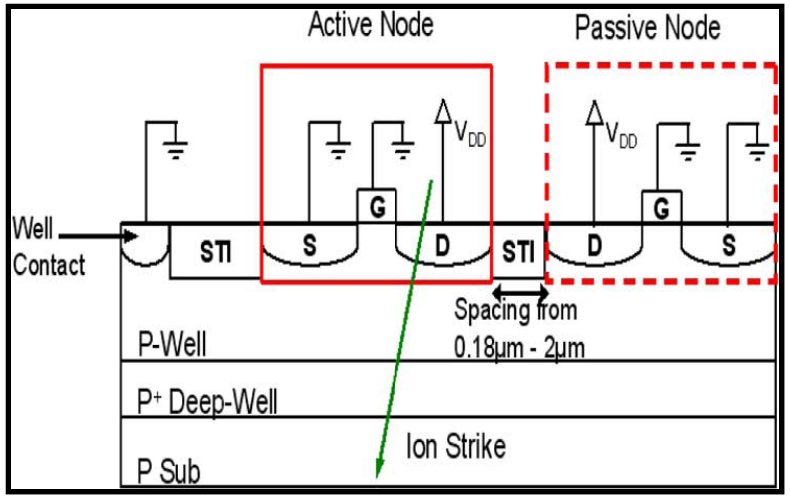




Tipton, et al., IEEE TNS, 2006

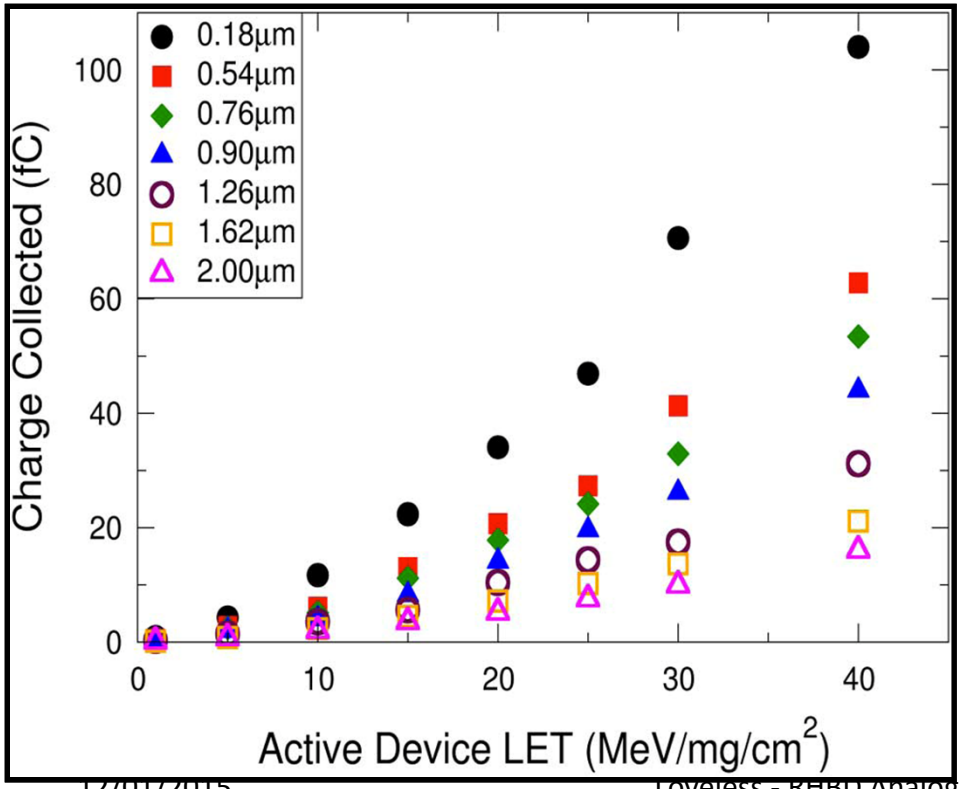
Layout-Level Mitigation: Nodal Separation

- Nodal separation:
  - *increasing the distance between devices can reduce the amount of charge collected on "passive" devices*



NMOS Cross Section Showing Active (Device Struck by Ionizing Particle) and Passive (Device that Indirectly Collects Charge) Device

Amusan, et al., IEEE TNS, 2006



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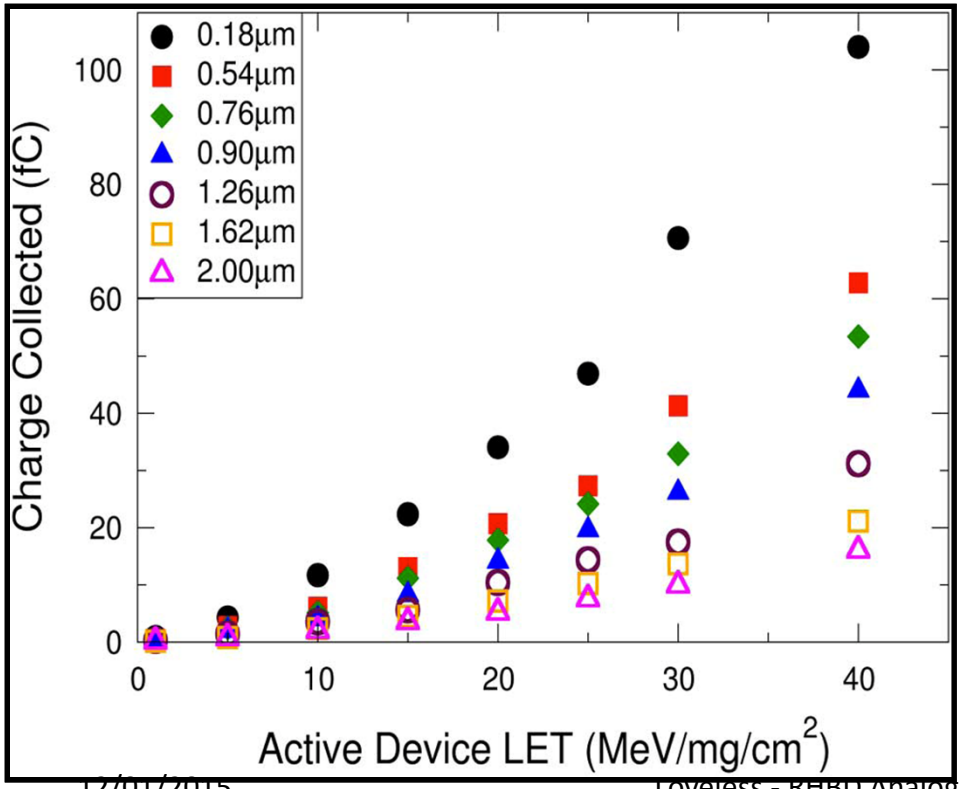

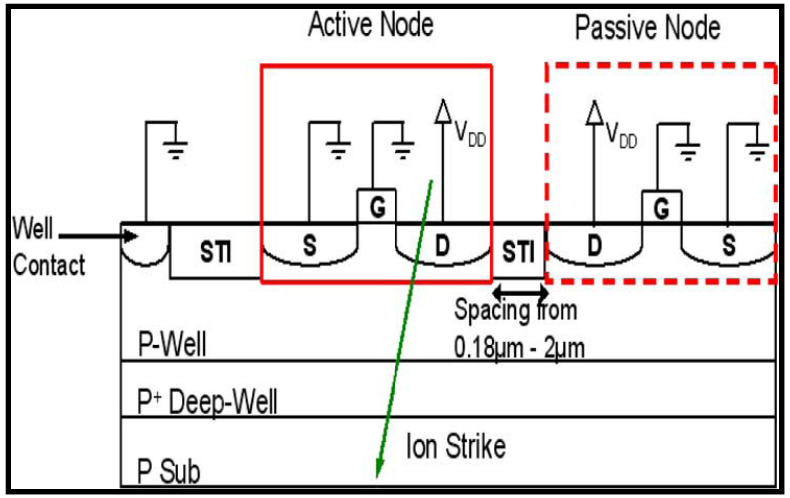

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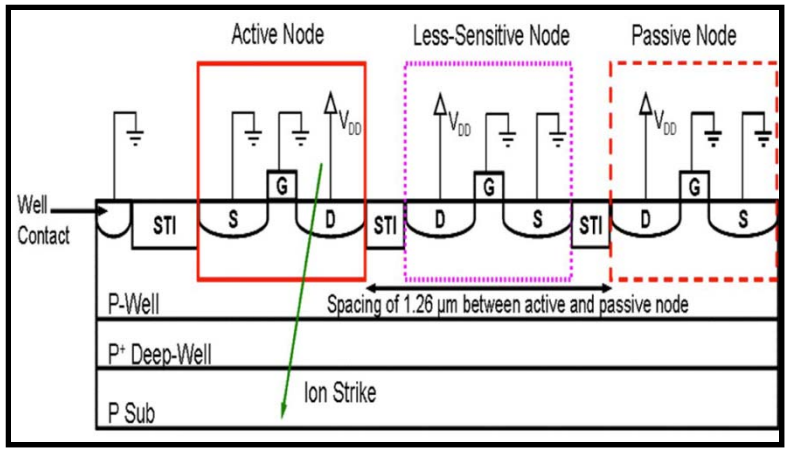
Large (Inefficient) Spacing Required To Mitigate Entirely

Nodal Separation of Two PMOS Devices (130 nm CMOS): Charge Collected on Passive Device

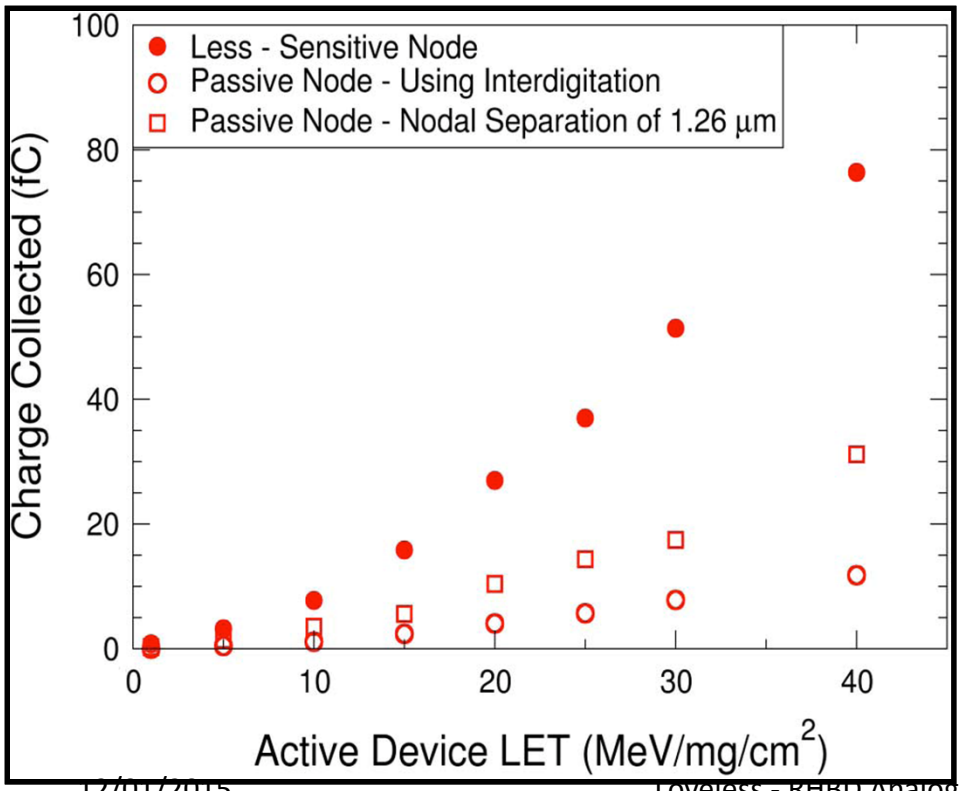
Layout-Level Mitigation: Interleaving

- Interdigitation (Interleaving):
  - *"less sensitive" devices placed between critical nodes*
  - *gain benefits of nodal seperation whithout adversely affecting total area*

Amusan, et al., IEEE TNS, 2006



NMOS Cross Section Showing Active and Passive Devices: Less-Sensitive Node is Placed Between Active and Passive Devices



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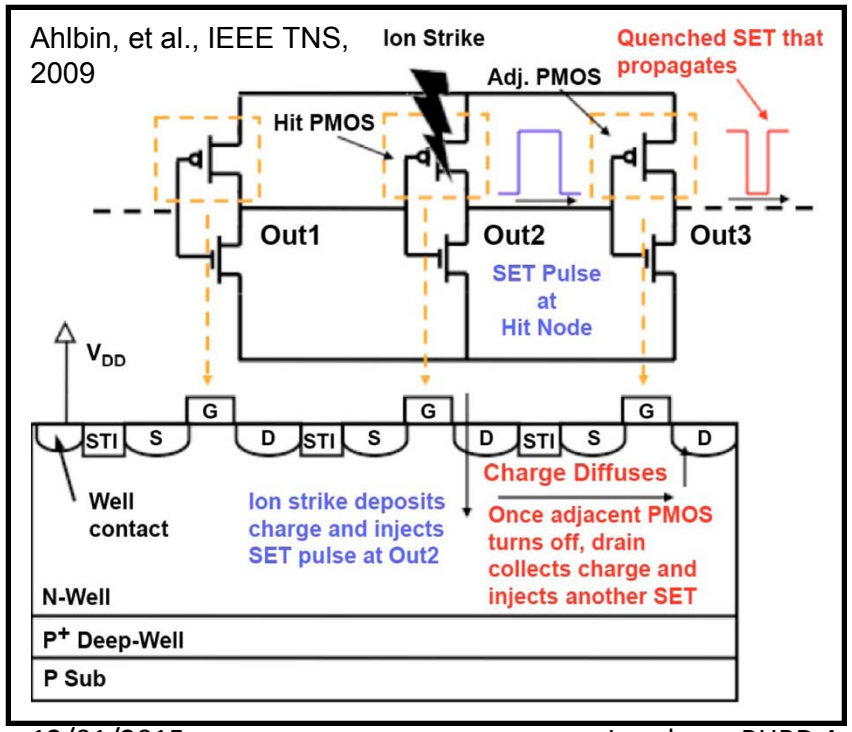

Illustration of Pulse Quenching: Quenching is a Consequence of the Interaction of Charge Diffusion (Sharing) between Devices and Electrical Signal Propagation

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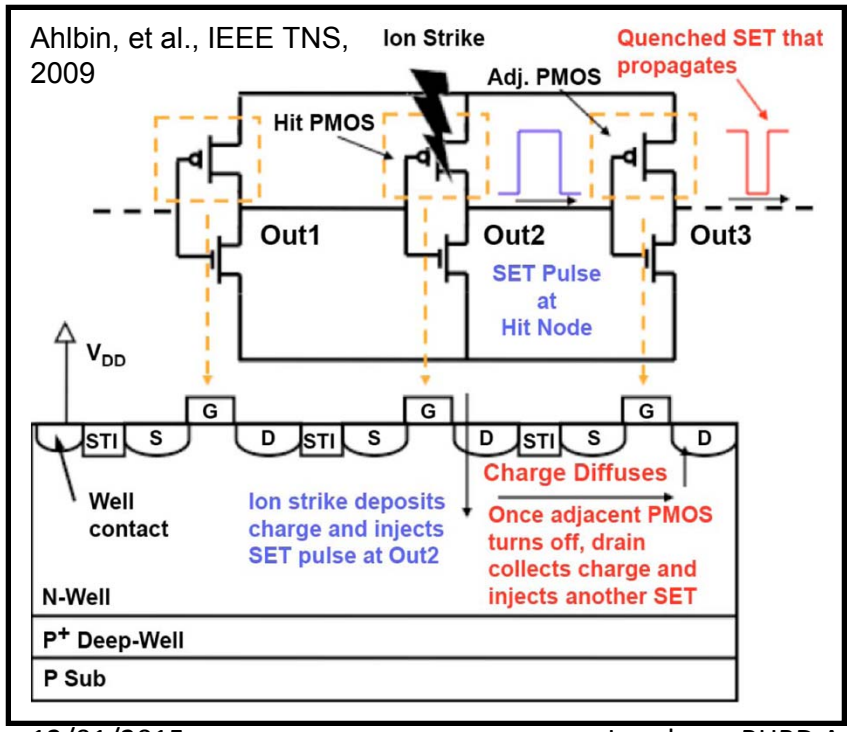
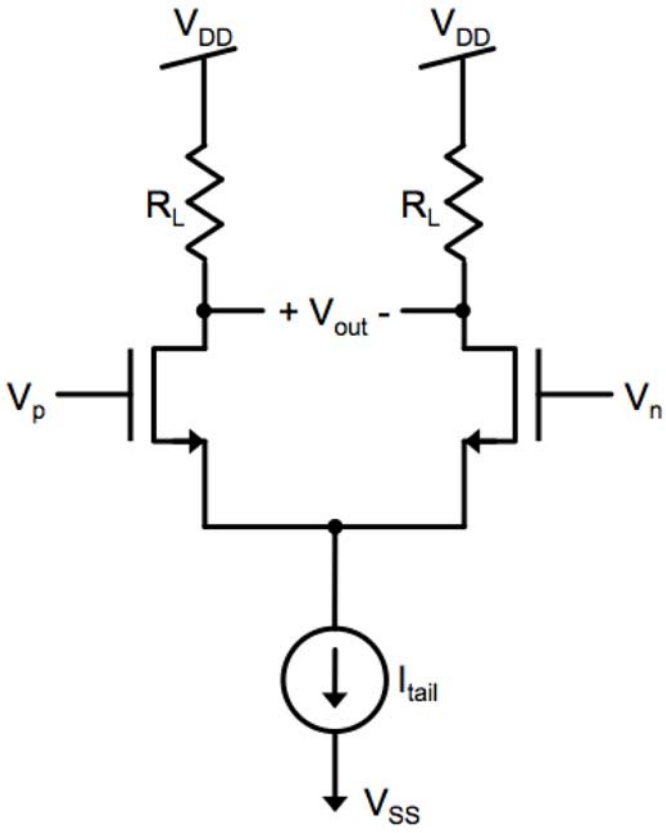


A Similar Mechanism can be Exploited for AMS ASICs

Illustration of Pulse Quenching: Quenching is a Consequence of the Interaction of Charge Diffusion (Sharing) between Devices and Electrical Signal Propagation

Hardening Via Charge Sharing: Differential Design

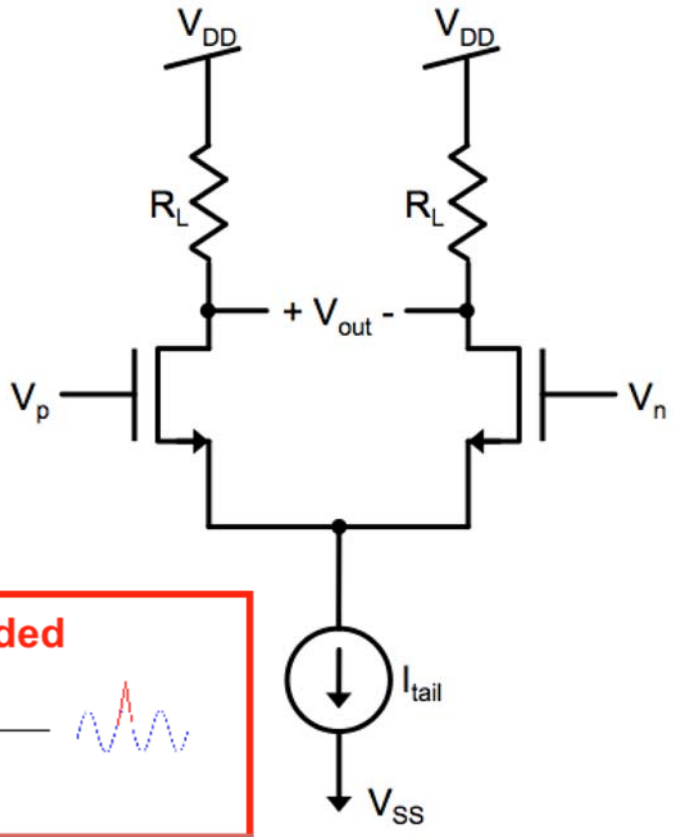
- Differential topologies are standard in most high-performance analog designs, including amplifiers, data converters, and switched-capacitor circuits
  - *improved dynamic output range and noise rejection over their single-ended counterparts*
  - *highly sensitive to Single-Event Effects!*



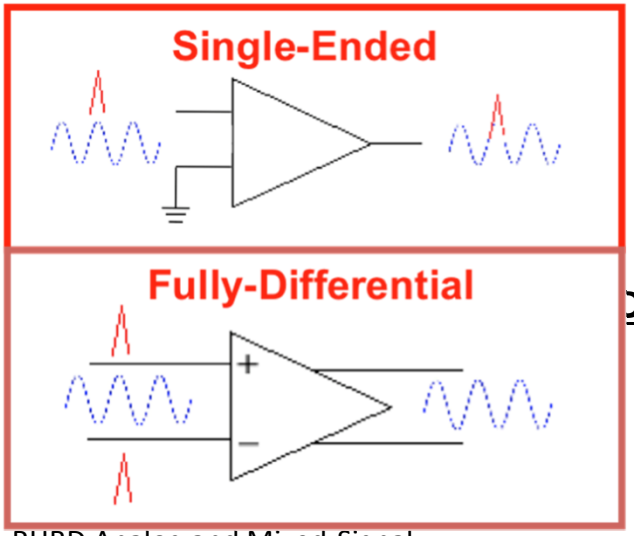
Basic Differential Pair

Hardening Via Charge Sharing: Differential Design

- Differential topologies are standard in most high-performance analog designs, including amplifiers, data converters, and switched-capacitor circuits
  - *improved dynamic output range and noise rejection over their single-ended counterparts*
  - *highly sensitive to Single-Event Effects!*
- Fully differential topologies reject common-mode noise
  - *by maximizing charge sharing such that a single-event transient (SET) is common to both datapaths, the SET can be rejected!*

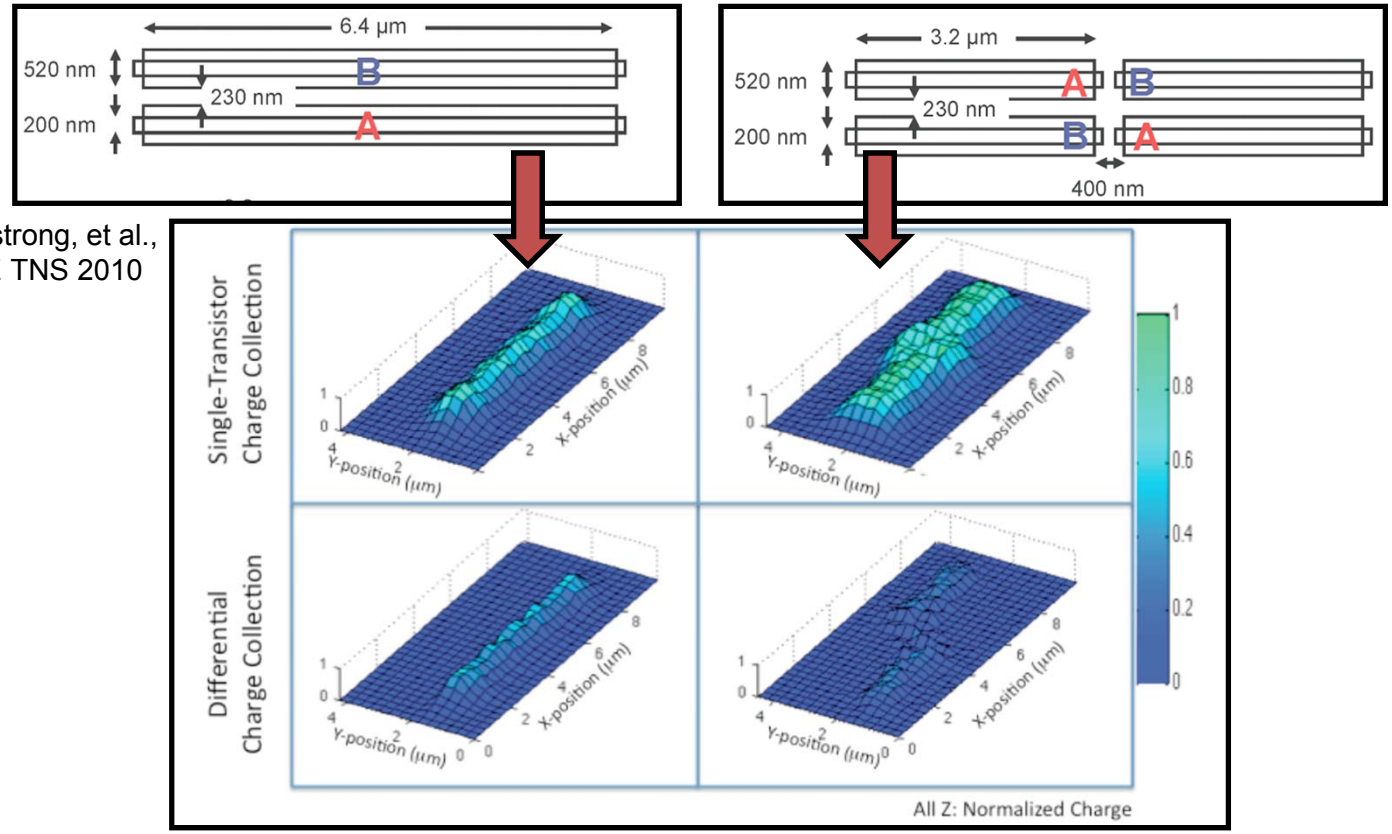


Differential Pair



Hardening Via Charge Sharing: Differential Design (Layout Level)

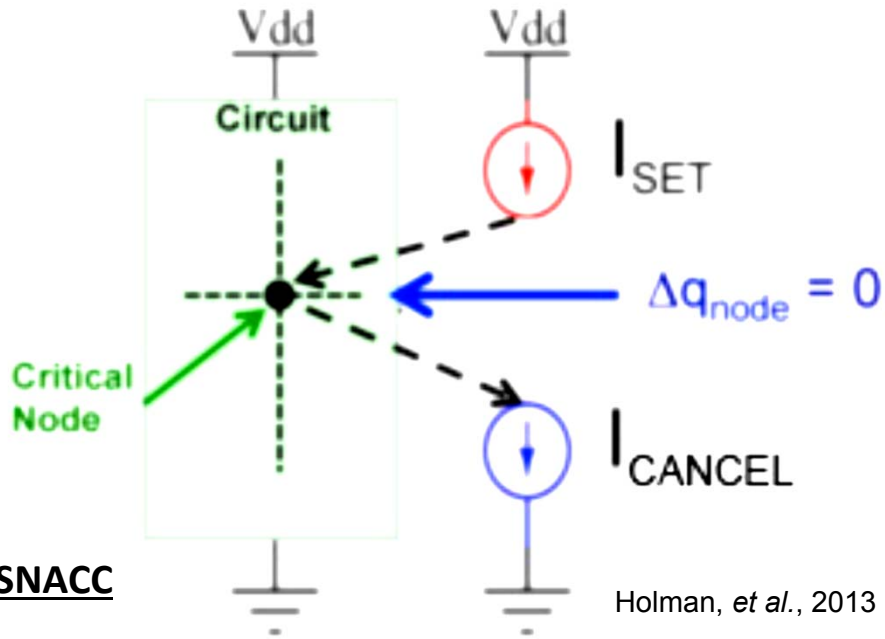
- Differential charge cancellation (DCC) layout - similar to common centroid - can be utilized to maximize charge sharing and reduce the differential charge collected on a node



Measured Collected Charge (Normalized) During Laser Two-Photon Absorption Irradiation

Hardening Via Charge Sharing: Combined Layout and Circuit Level

- The DCC hardened layout technique takes advantage of charge sharing between adjacent transistors by using common-mode cancellation in differential signal path
- Hardening Via Charge Sharing (HCS) can be extended beyond layouts alone and exploited at the circuit level
  - *For example: Sensitive Node Active Charge Cancellation (SNACC) can be used for balancing collected charge with equal but opposite charge at a critical node*

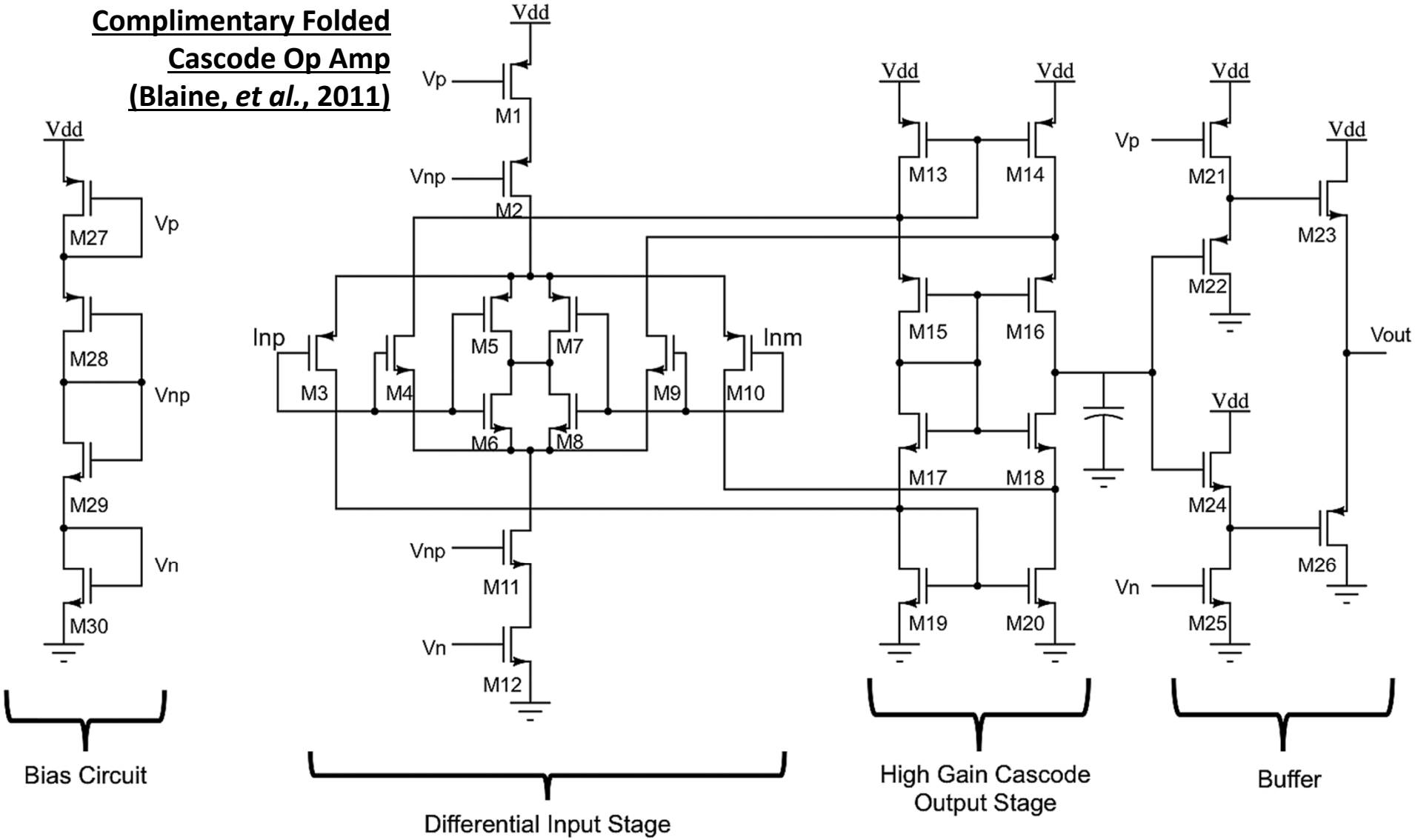


Concept Drawing of SNACC

Holman, *et al.*, 2013

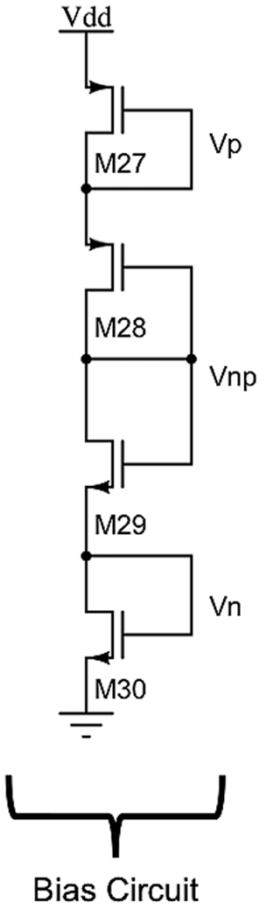
Hardening Via Charge Sharing: SNACC Design and DCC Layout

Complimentary Folded Cascode Op Amp (Blaine, *et al.*, 2011)

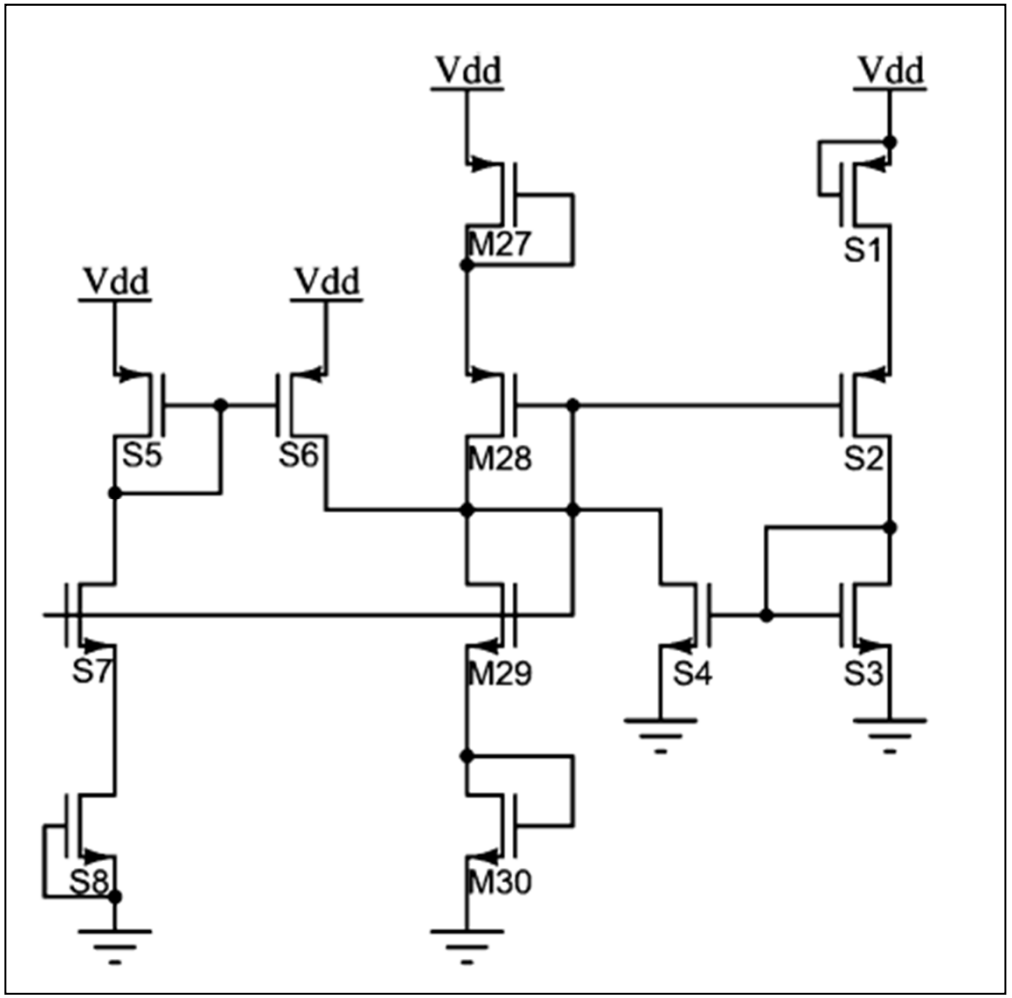


Hardening Via Charge Sharing: SNACC Design and DCC Layout

Complimentary Folded Cascode Op Amp (Blaine, *et al.*, 2011)



Bias Circuit with M-SNACC (Multiple-Node SNACC) Applied (Blaine, *et al.*, 2011)



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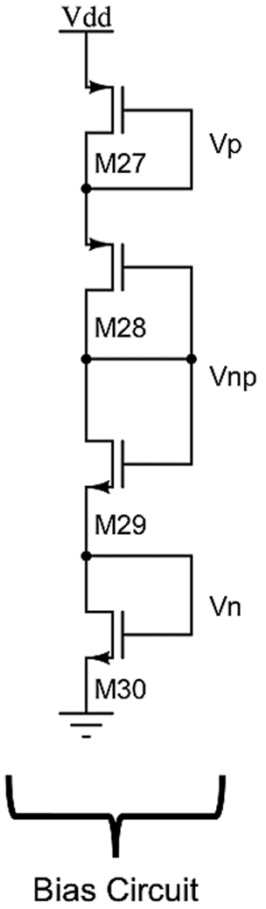

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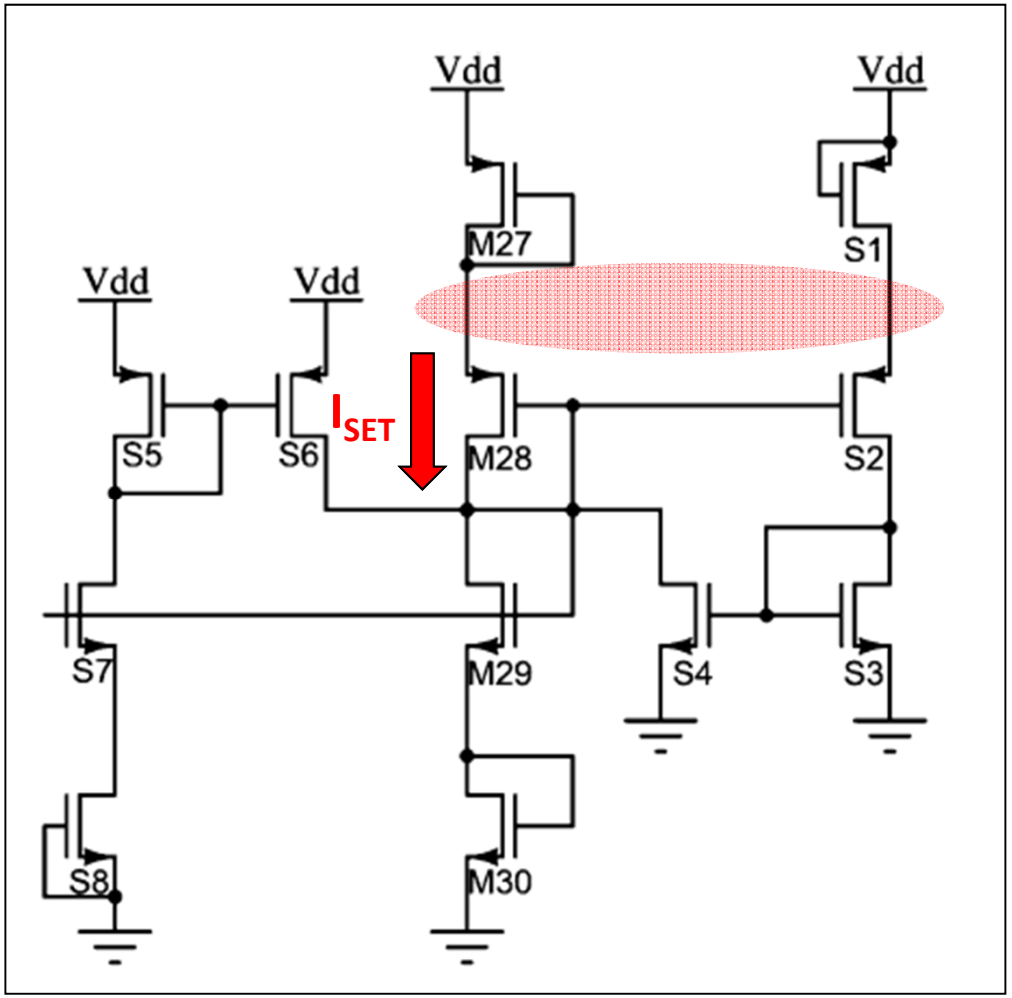

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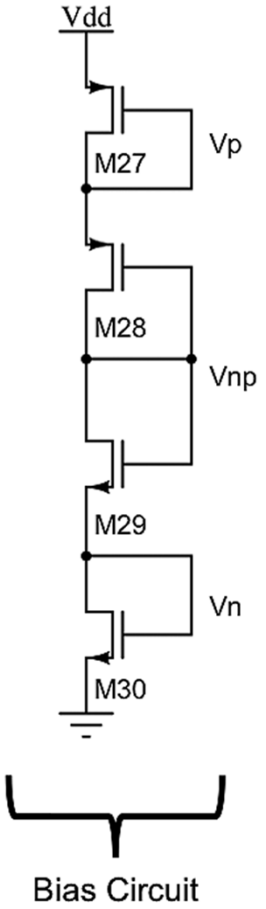

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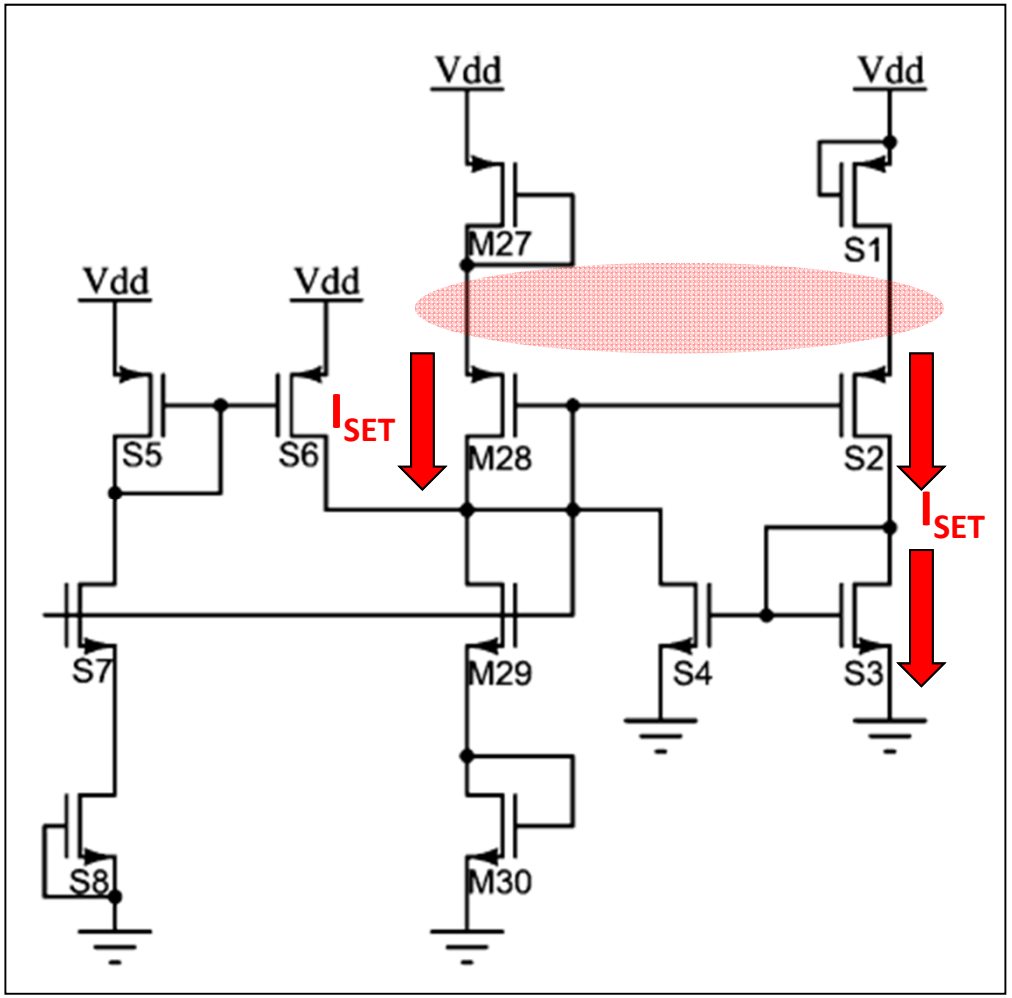

Hardening Via Charge Sharing: SNACC Design and DCC Layout

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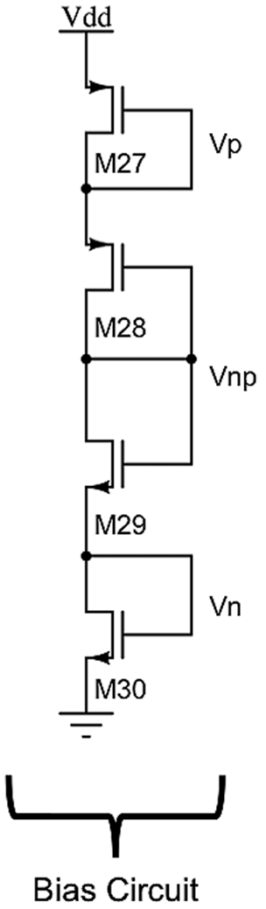

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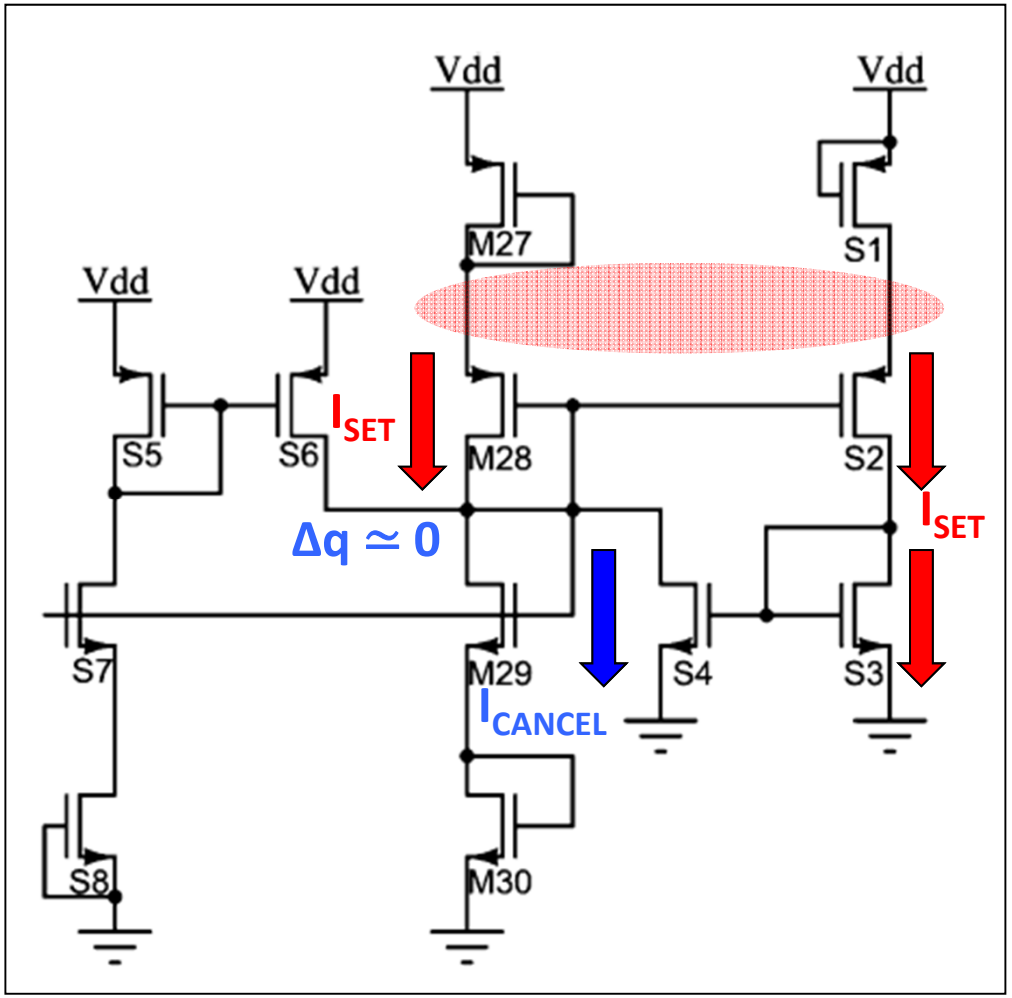
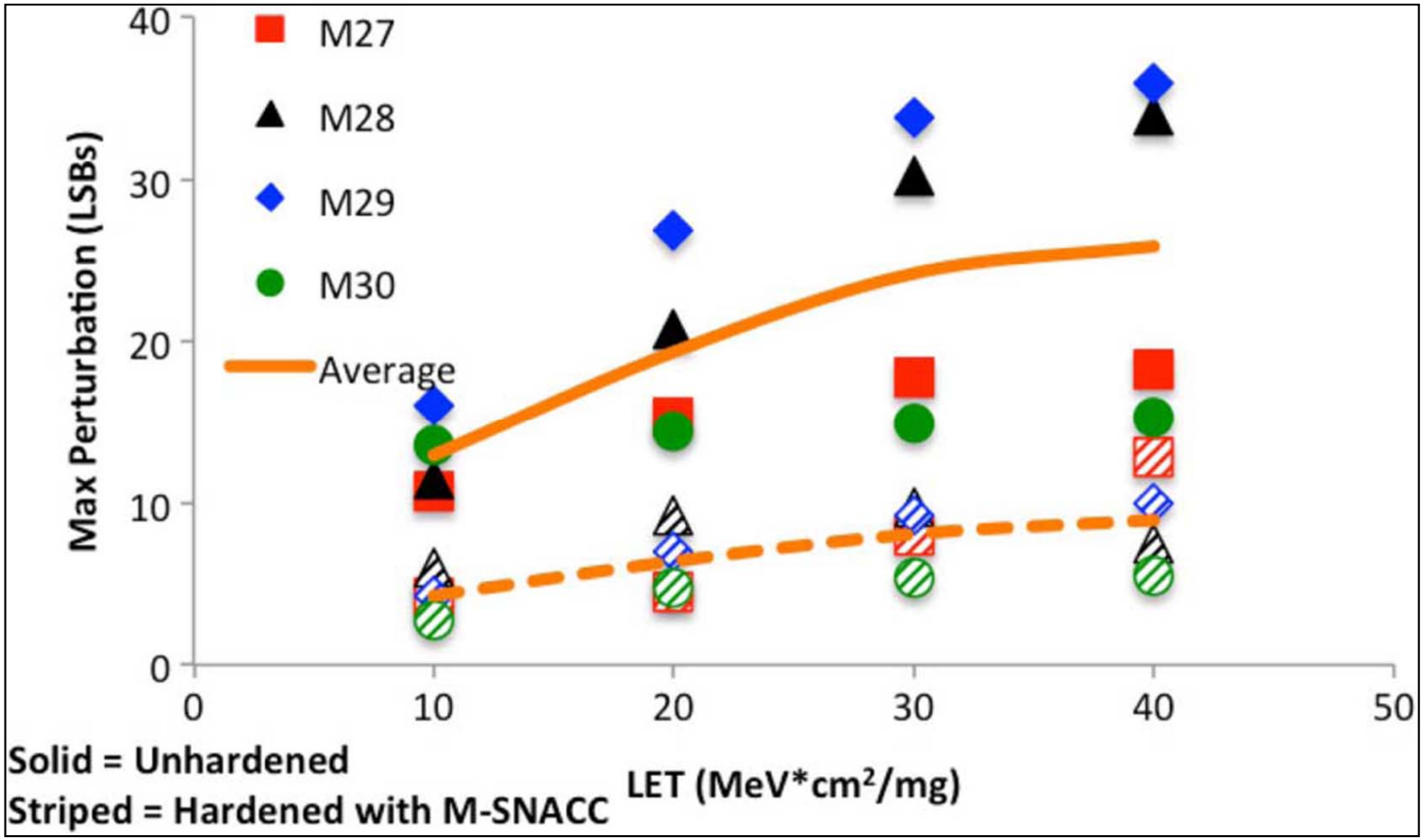
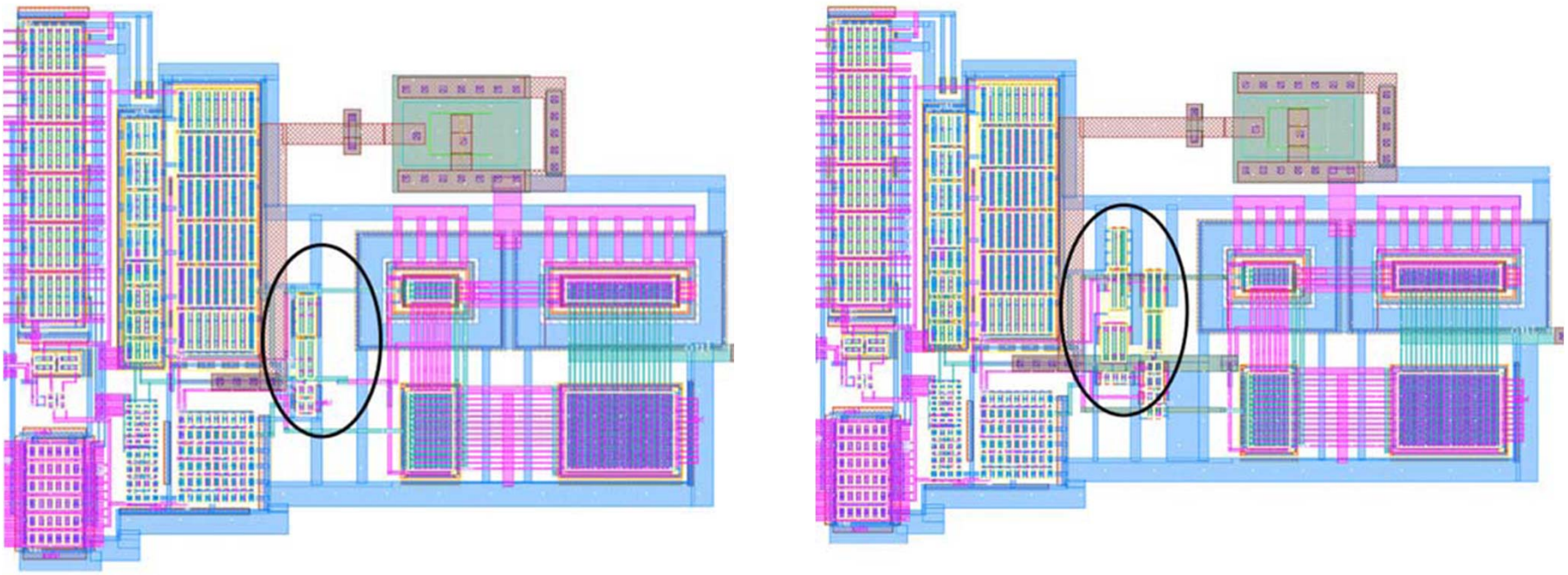


Hardening Via Charge Sharing: SNACC Design and DCC Layout



Simulated Max Perturbation (in LSBs assuming an 8-bit DAC at 1.2 V) versus LET for Strikes to Bias Circuit in 90 nm Op Amp

Hardening Via Charge Sharing: SNACC Design and DCC Layout



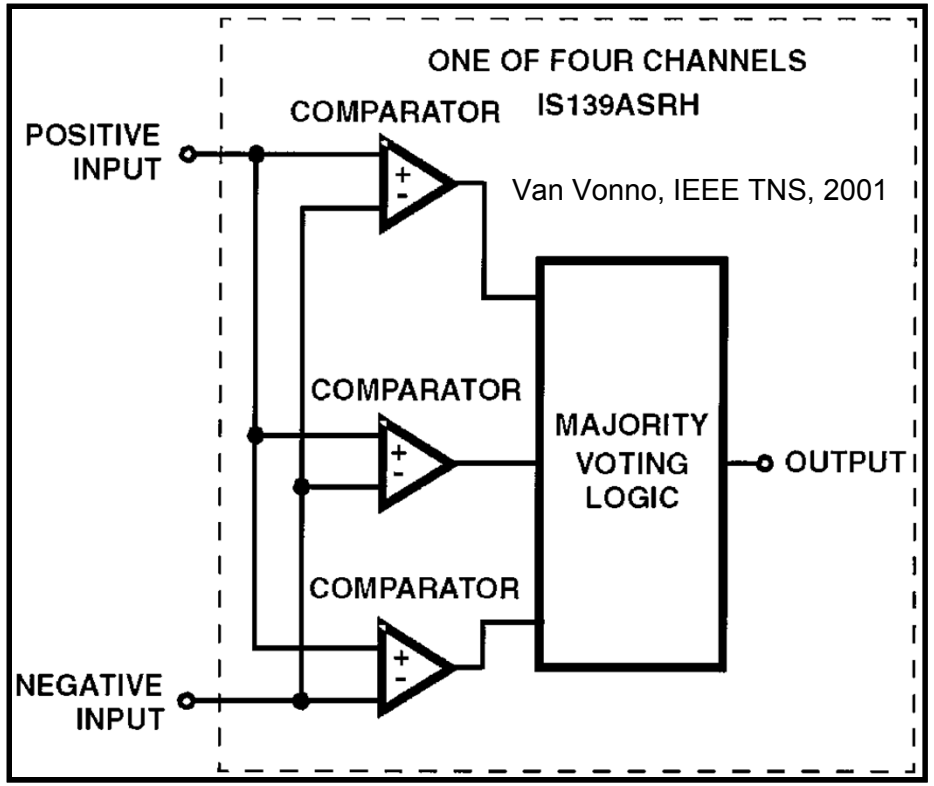
Layout Views of Un-Hardened and RHBD Op Amps in 90 nm Technology with Bias Circuits Circled – RHBD Design Implemented with 7% Area Penalty

Circuit- and System-Level Mitigation

- In cases where technology-, device-, and layout-level mitigation do not yield the desired performance specifications, ASET mitigation may be achieved through modification of the circuits and or systems
- A/MS designers are accustomed to “design-around-constraint”
- Single-event transient performance is an additional design constraint that can often be counteracted if:
  - *cross-domain response mechanisms are understood*
  - *analysis techniques adequately capture the single-event effects*
  - *appropriate error metrics are defined*
  - ***tradeoffs are balanced!***

Circuit- and System-Level Mitigation: Triple Modular Redundancy

- Triple Modular Redundancy (TMR):
  - *three identical copies of a circuit; majority voting at the output*
  - *while more common in digital electronics, TMR has been successfully implemented in **mixed-signal circuits** with digital output signatures, such as the voltage comparator*
  - *not straight forward for analog circuits*

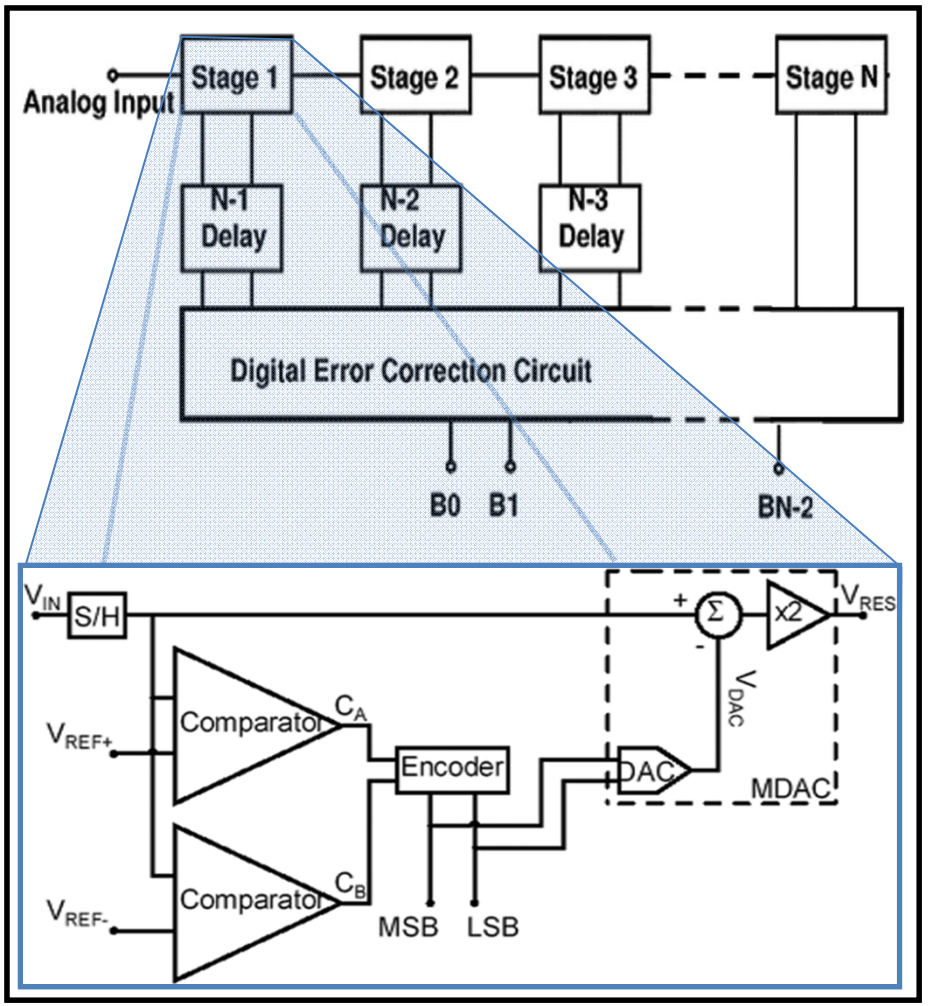


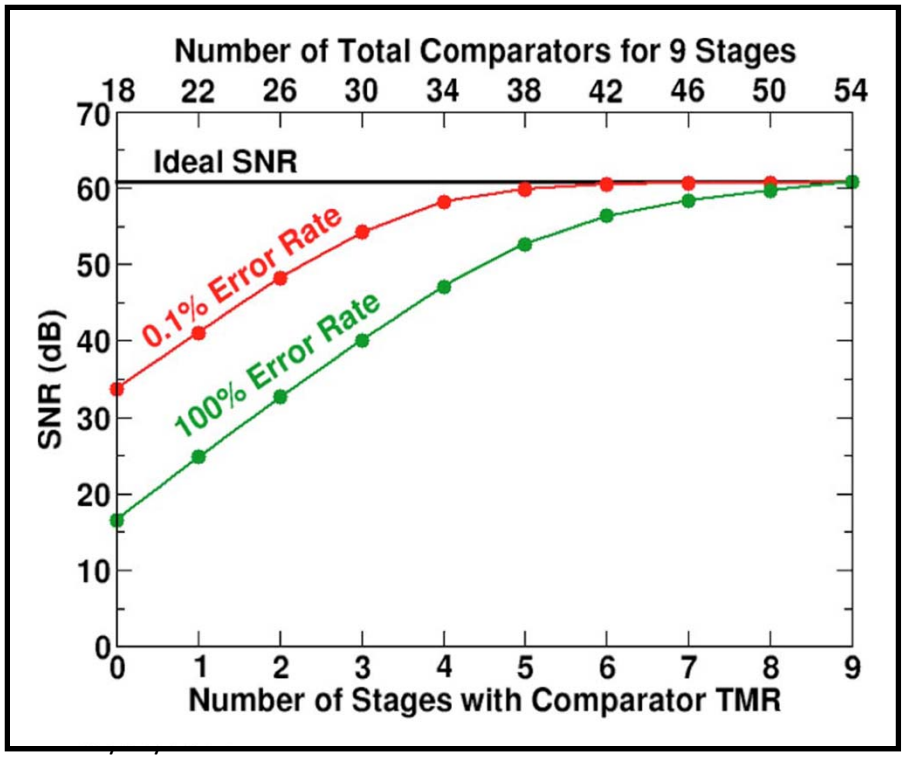
3x Power and Area Penalty

Circuit- and System-Level Mitigation: Triple Modular Redundancy

- Triple Modular Redundancy (TMR):
  - *when used in a pipelined analog-to-digital converter (ADC) TMR need only be applied to the first 50% of the stages*

Olson, et al., IEEE TNS, 2008

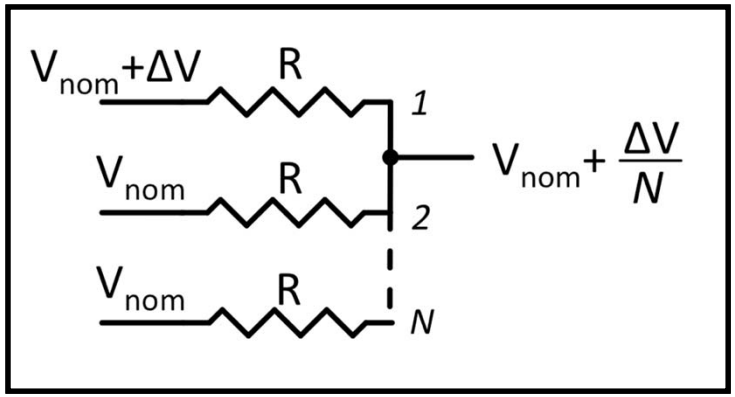




Signal-to-Noise Ratio at ADC Output for Randomly Injected Errors

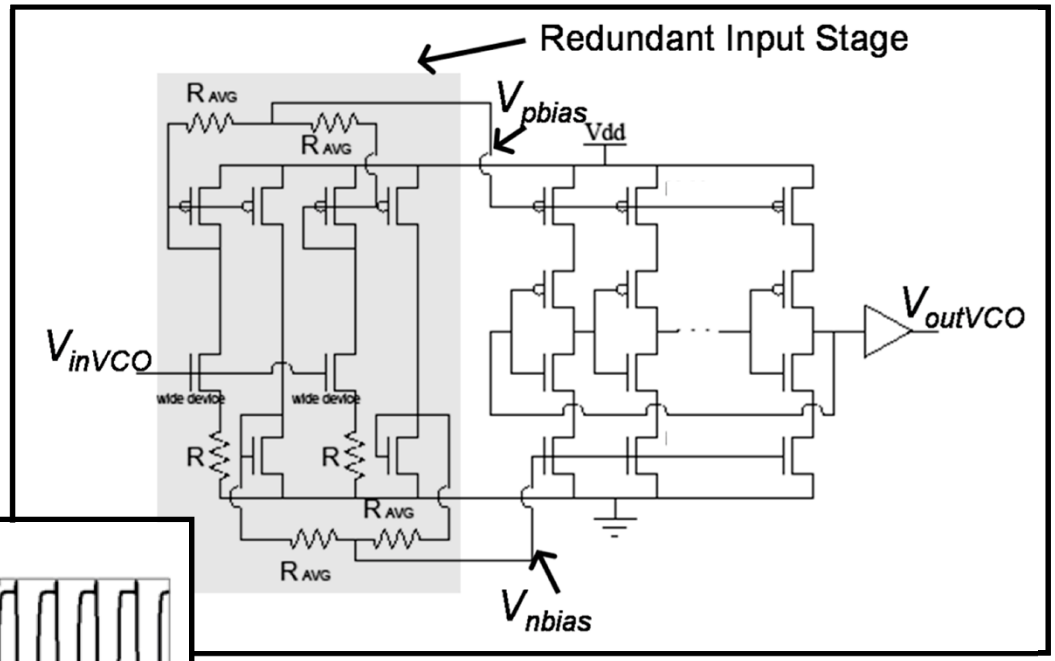
Circuit- and System-Level Mitigation: Averaging

- Analog Averaging:
  - *form of hardware redundancy for the reduction of spurious transients*
  - *accomplished by replicating and parallelizing a circuit N times, and connecting the replicated nodes together through parallel resistors to a common node*

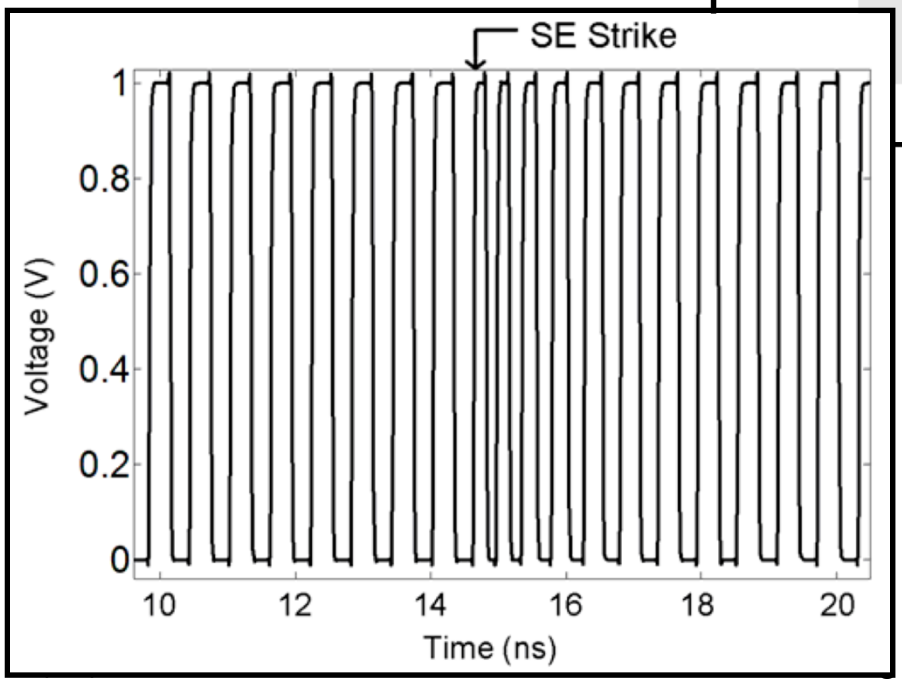


Circuit- and System-Level Mitigation: Averaging

- Analog Averaging:
  - *implemented in a voltage-controlled oscillator (VCO), averaging two stages is shown to decrease output phase displacement by 35%*



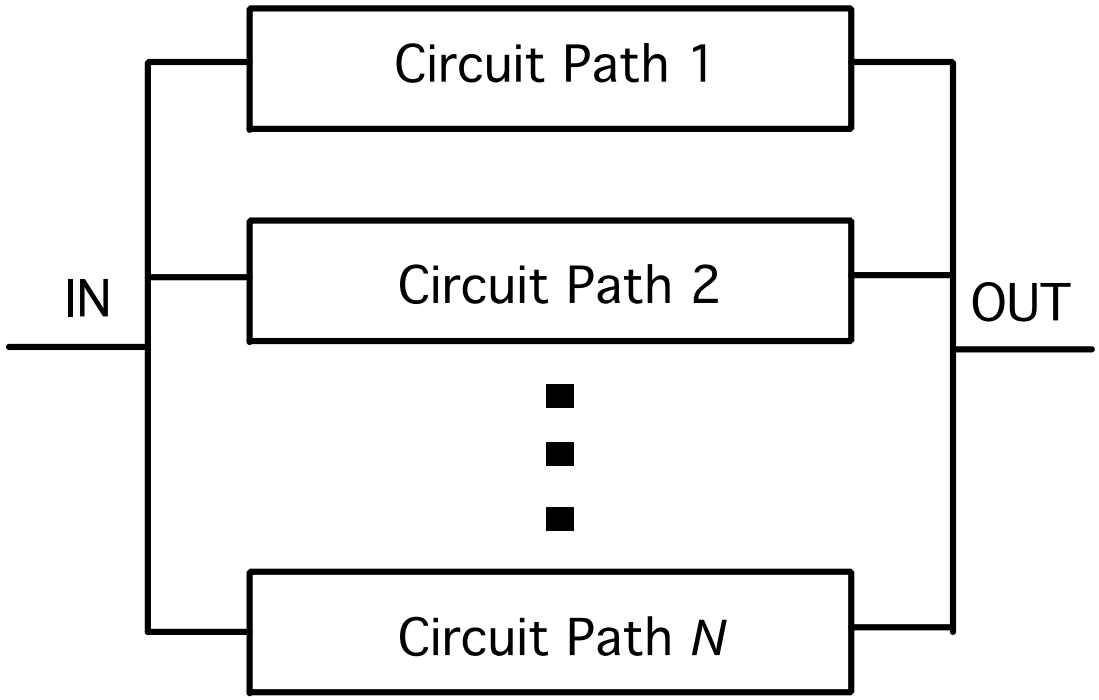
Loveless, et al., IEEE TNS, 2007



Typical Response Following a Strike in the Bias Circuit: Output Frequency is Temporarily Increased from 1.6 GHz to 3.0 GHz

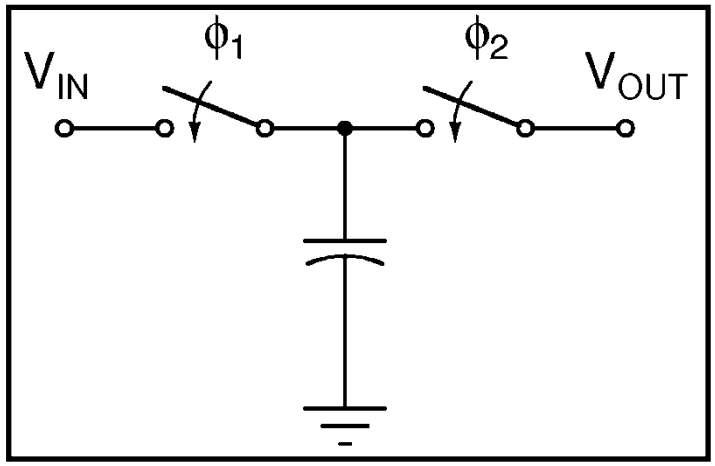
Hardening Via Node Splitting

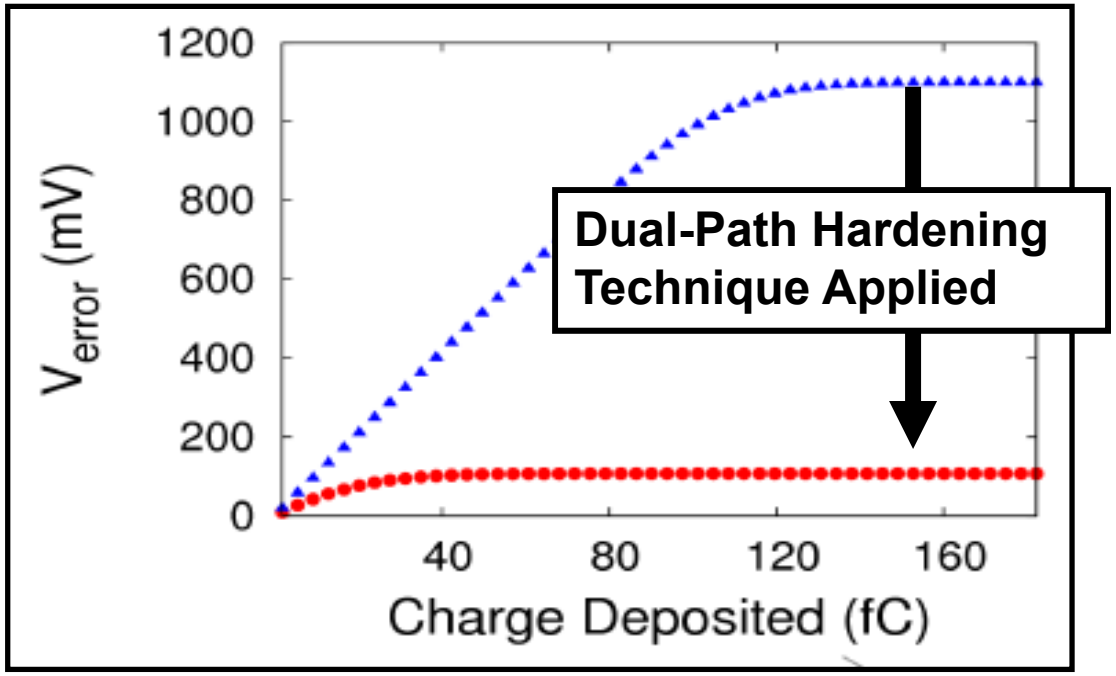
- One versatile methodology for hardening AMS circuits is that of *node splitting*
- Discrete- or continuous-time
- Negligible impact on performance, area, power dissipation
- Form of redundancy – however, circuit is *divided* into 2 or more paths (ideally, struck path is disabled during ion strike)



Hardening Via Node Splitting: Dual-Path Hardening

- Differential Design and Dual-Path Hardening
  - *conventional wisdom: avoid floating nodes in designs for radiation environments*
  - *dual-path hardening technique has been developed that dramatically decreases floating nodes vulnerability in switched-capacitor mixed-signal circuits*

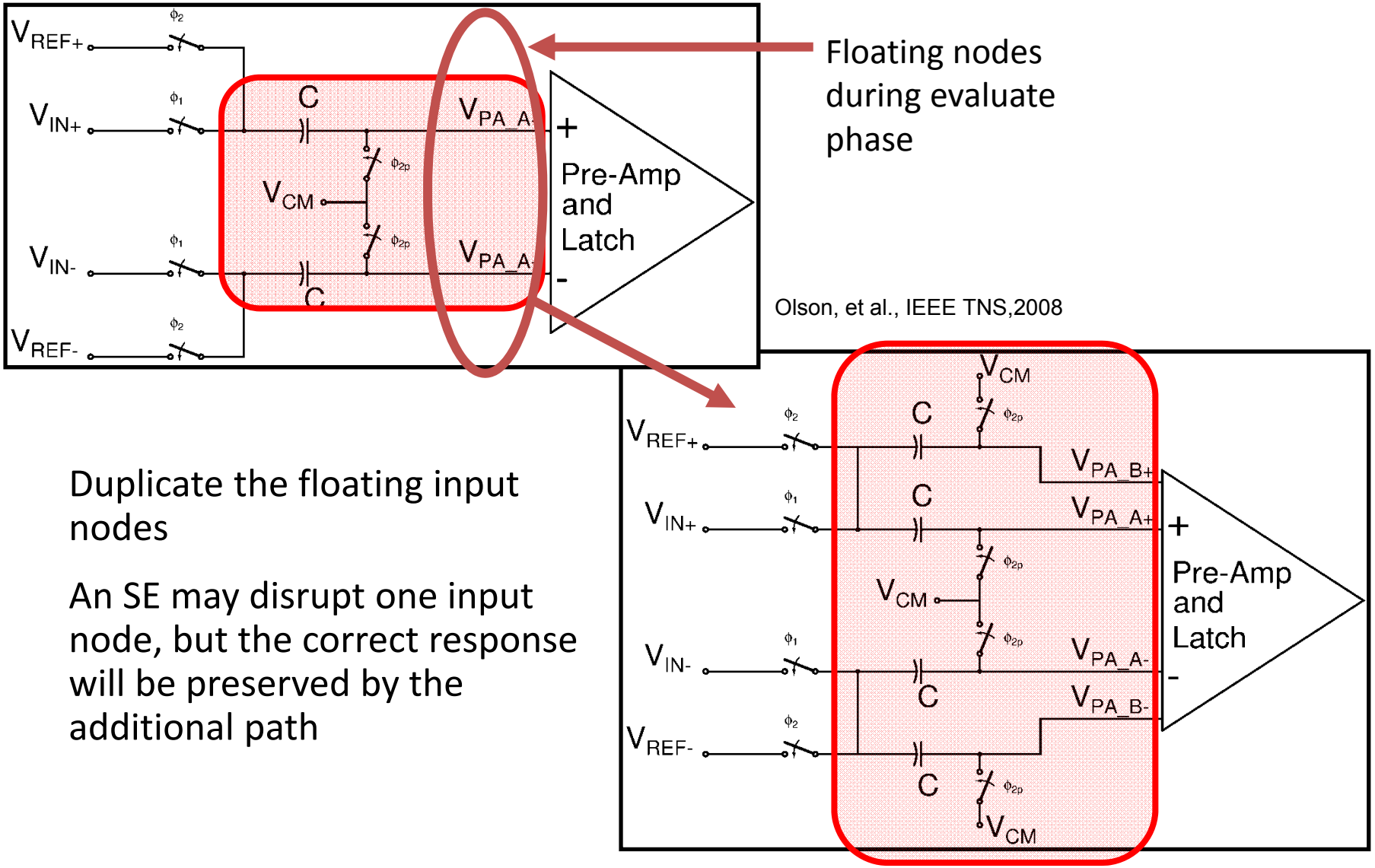




Fleming, et al., IEEE TCAS II,2008

Dual-Path Hardening:

Switched-Capacitor Network

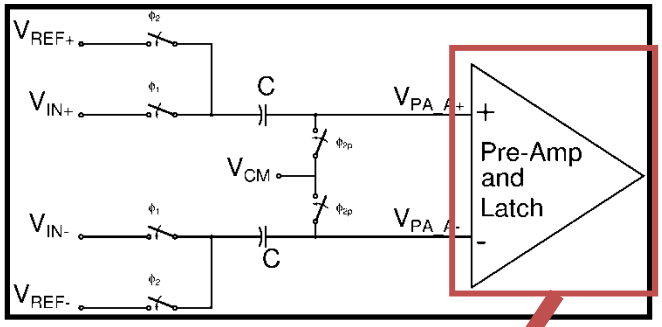


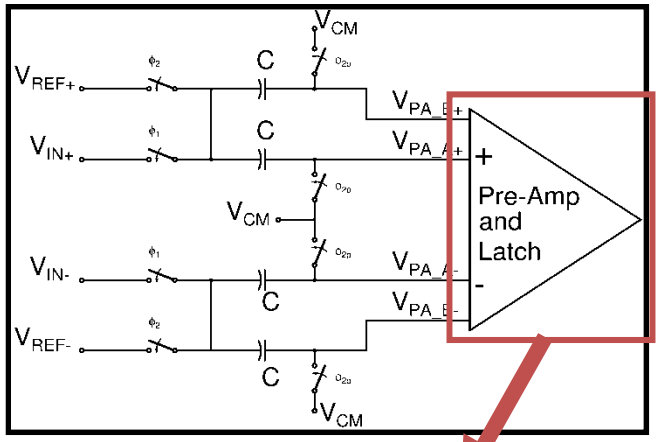
Duplicate the floating input nodes

An SE may disrupt one input node, but the correct response will be preserved by the additional path

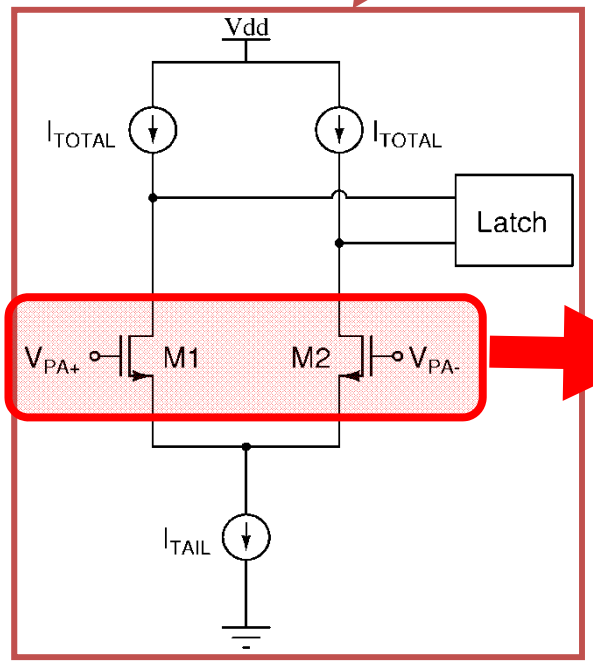
Dual-Path Hardening:

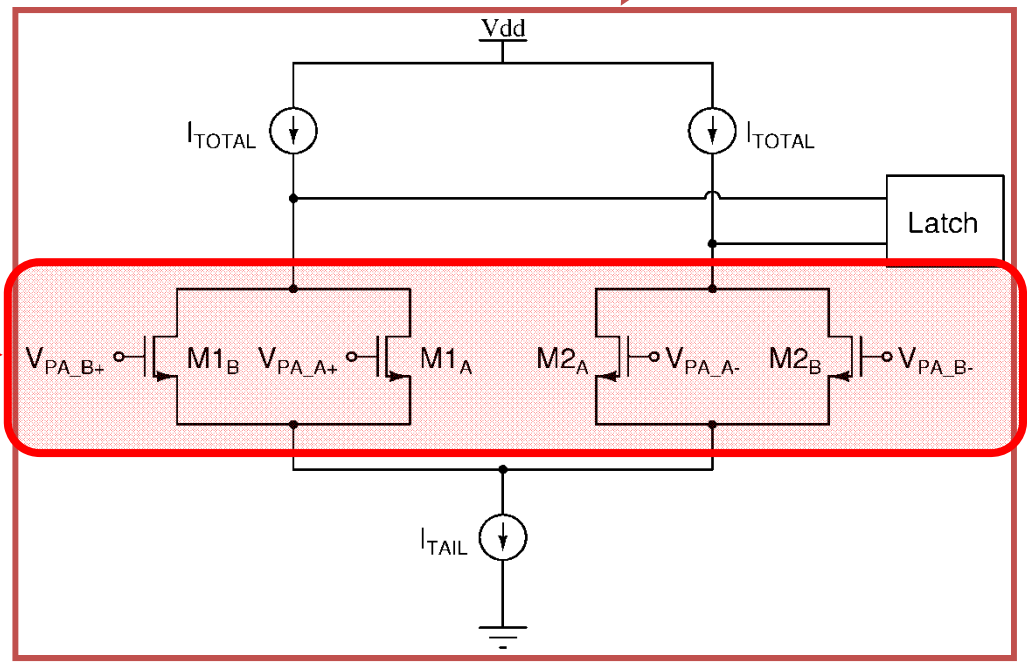
Pre-Amplifier and Latch



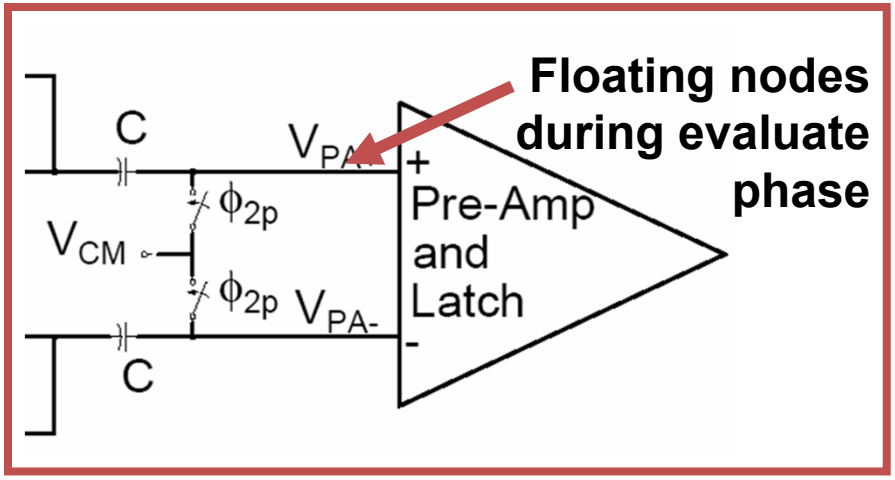


Olson, et al., IEEE TNS,2008

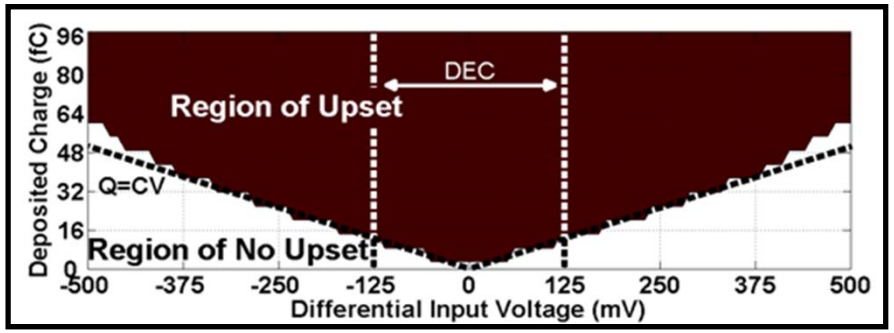




Hardening Via Node Splitting: Dual-Path Hardening

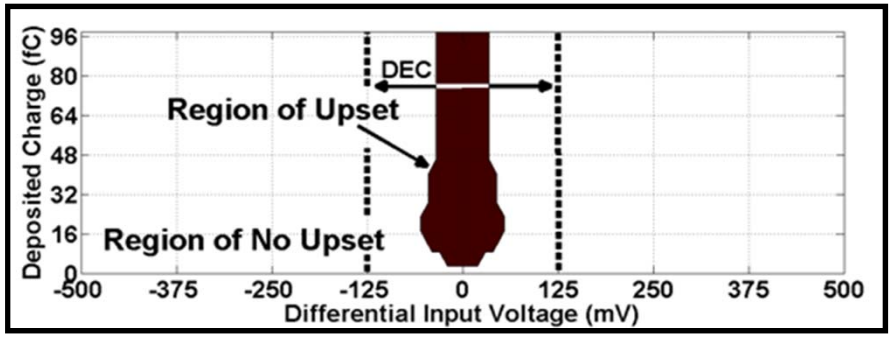


90 nm CMOS Simulations of Baseline



Olson, et al., IEEE TNS,2008

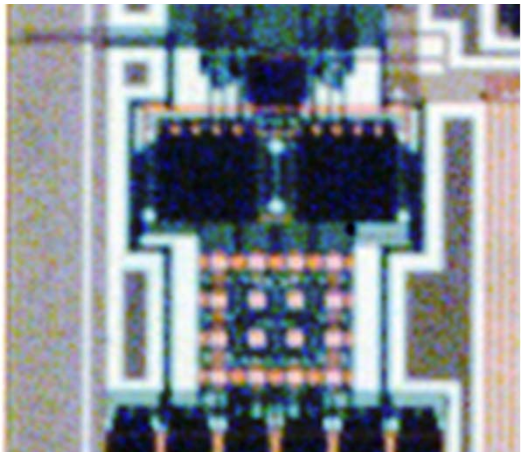
Dual-Path Hardening



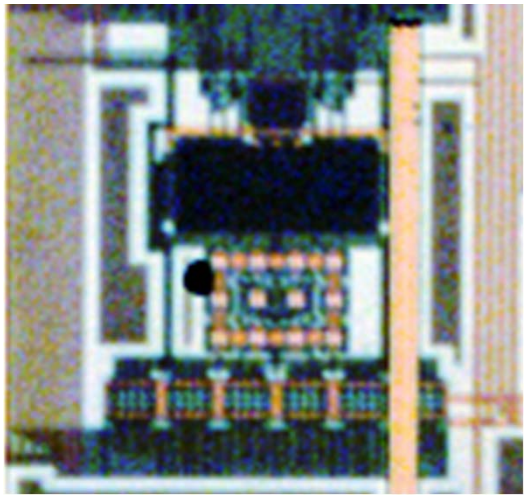
- Maximum differential input voltage vulnerable to SEU increases roughly linearly with collected charge at the rate of Q=CV
- Dual-path hardening decouples the comparator response from increasing collected charge

Hardening Via Node Splitting: Dual-Path Hardening

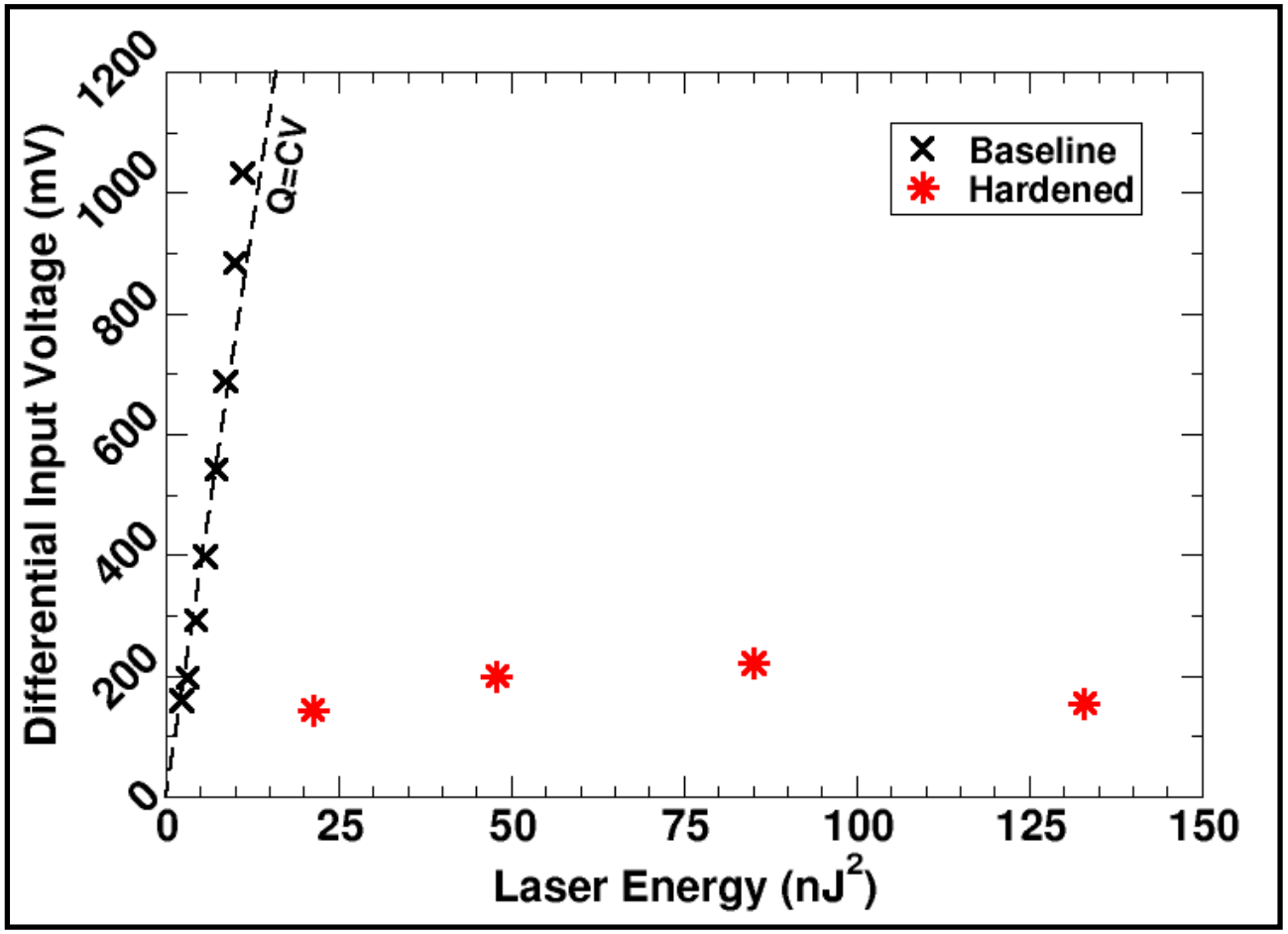
RHBD Comparator



Baseline Comparator



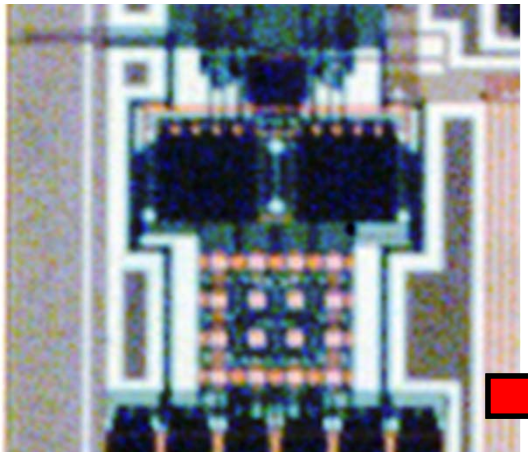
Olson, PhD Dissertation, VU, 2010



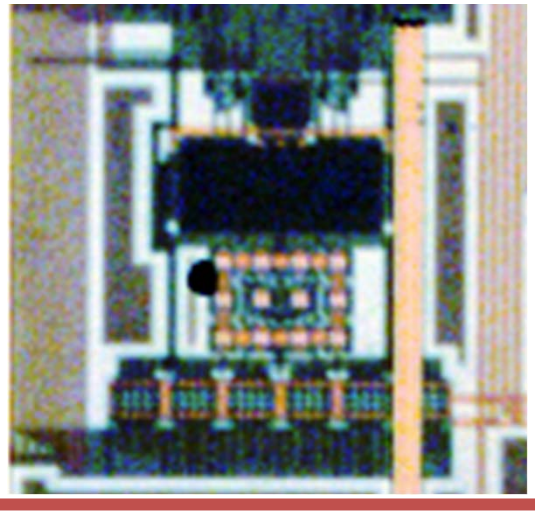
Differential Input Voltage Excursion Following Laser Two-Photon Absorption Irradiation

Hardening Via Node Splitting: Dual-Path Hardening

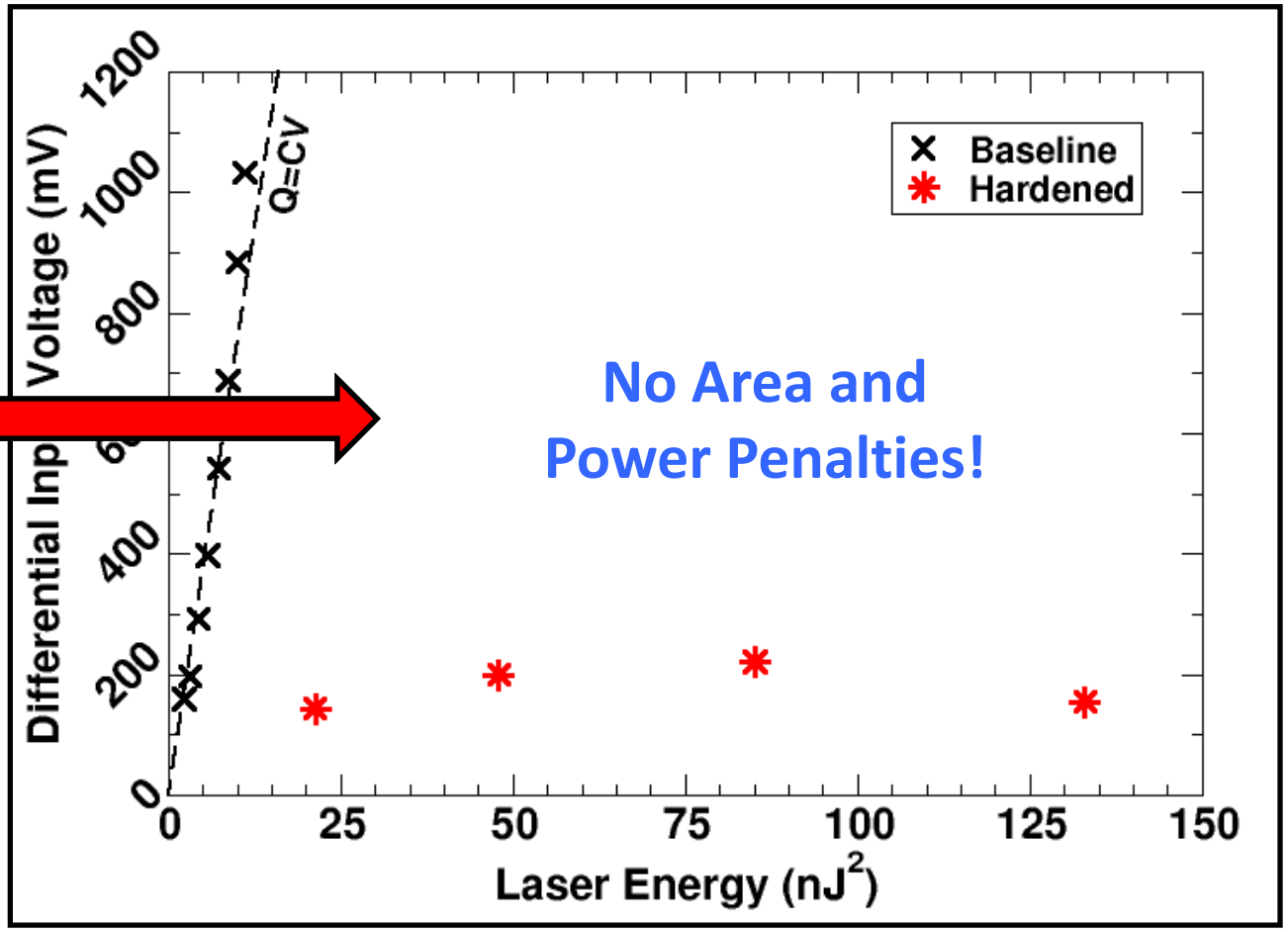
RHBD Comparator



Baseline Comparator



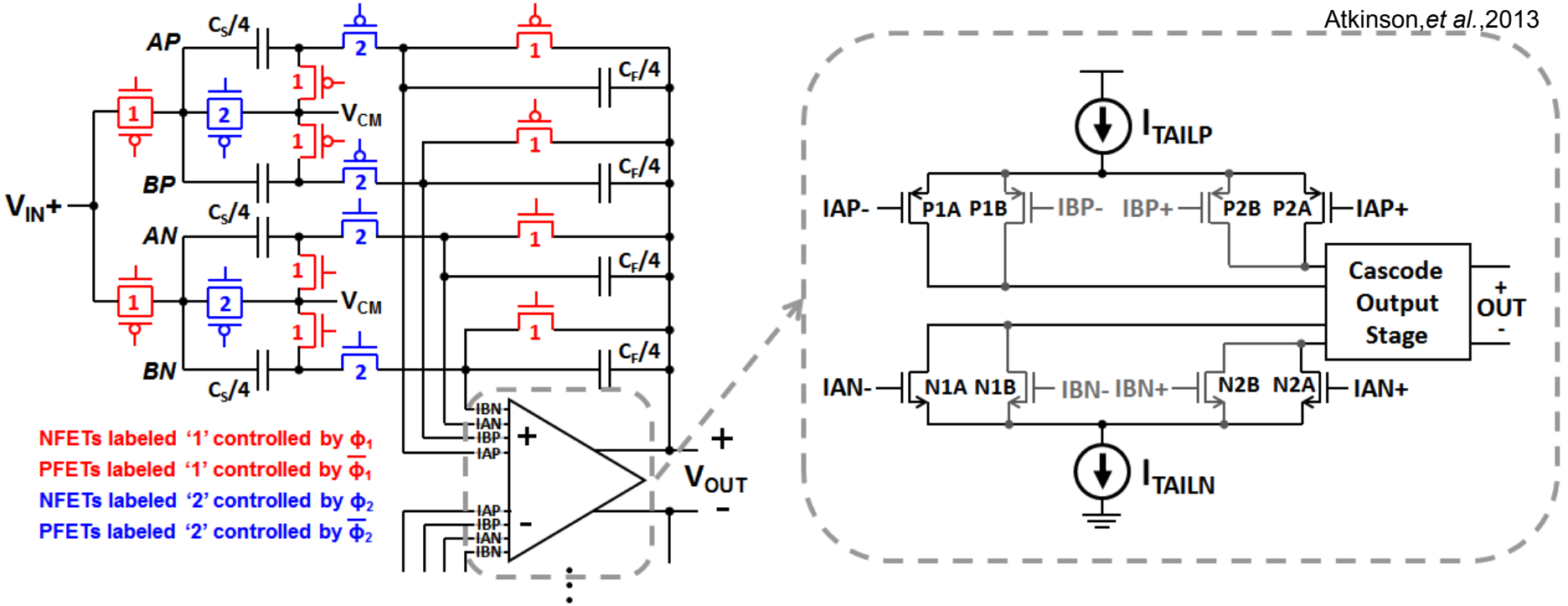
Olson, PhD Dissertation, VU, 2010



Differential Input Voltage Excursion Following Laser Two-Photon Absorption Irradiation

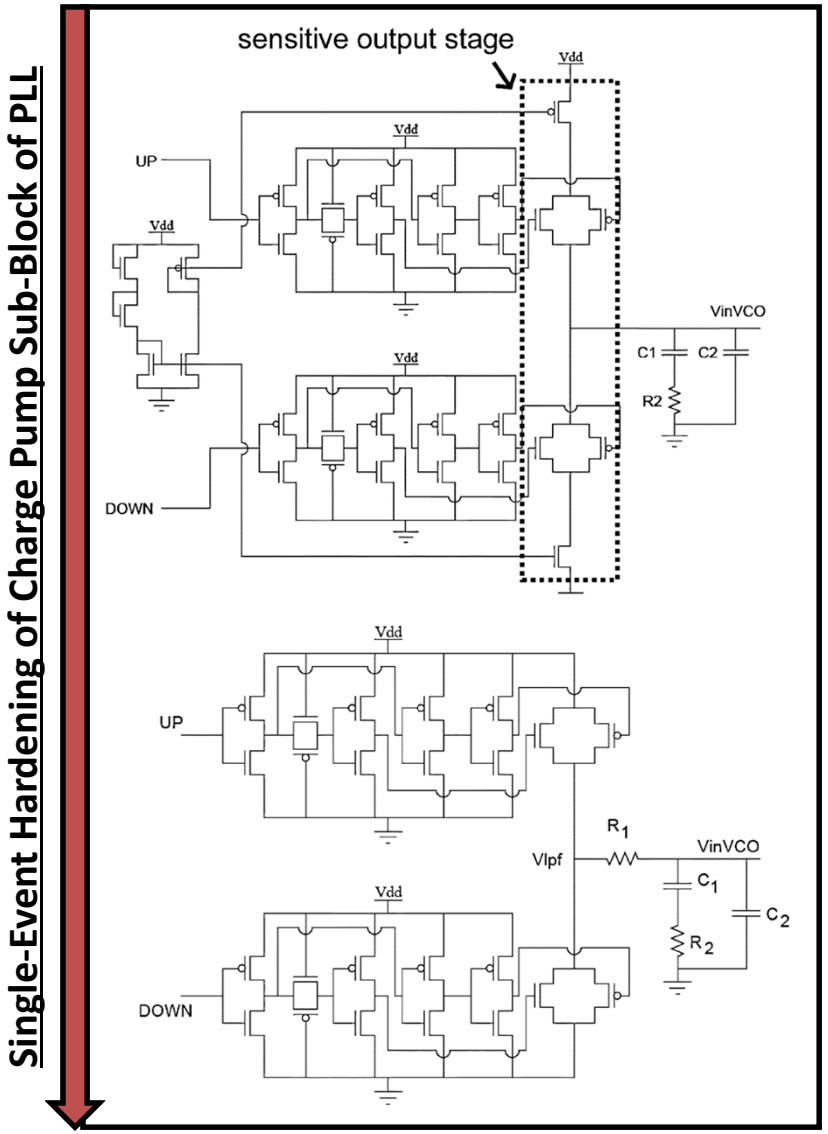
Hardening Via Node Splitting: Quad-Path Hardening

- The main drawback of dual-path hardening is that the transistor switches must be the same type as the input transistors (ensures that the struck path will be disabled, but also ***limits dynamic input range***)
- Quad-path hardened designs address this limitation at the added cost of increased layout complexity (though at no area or power penalties!)



Circuit- and System-Level Mitigation

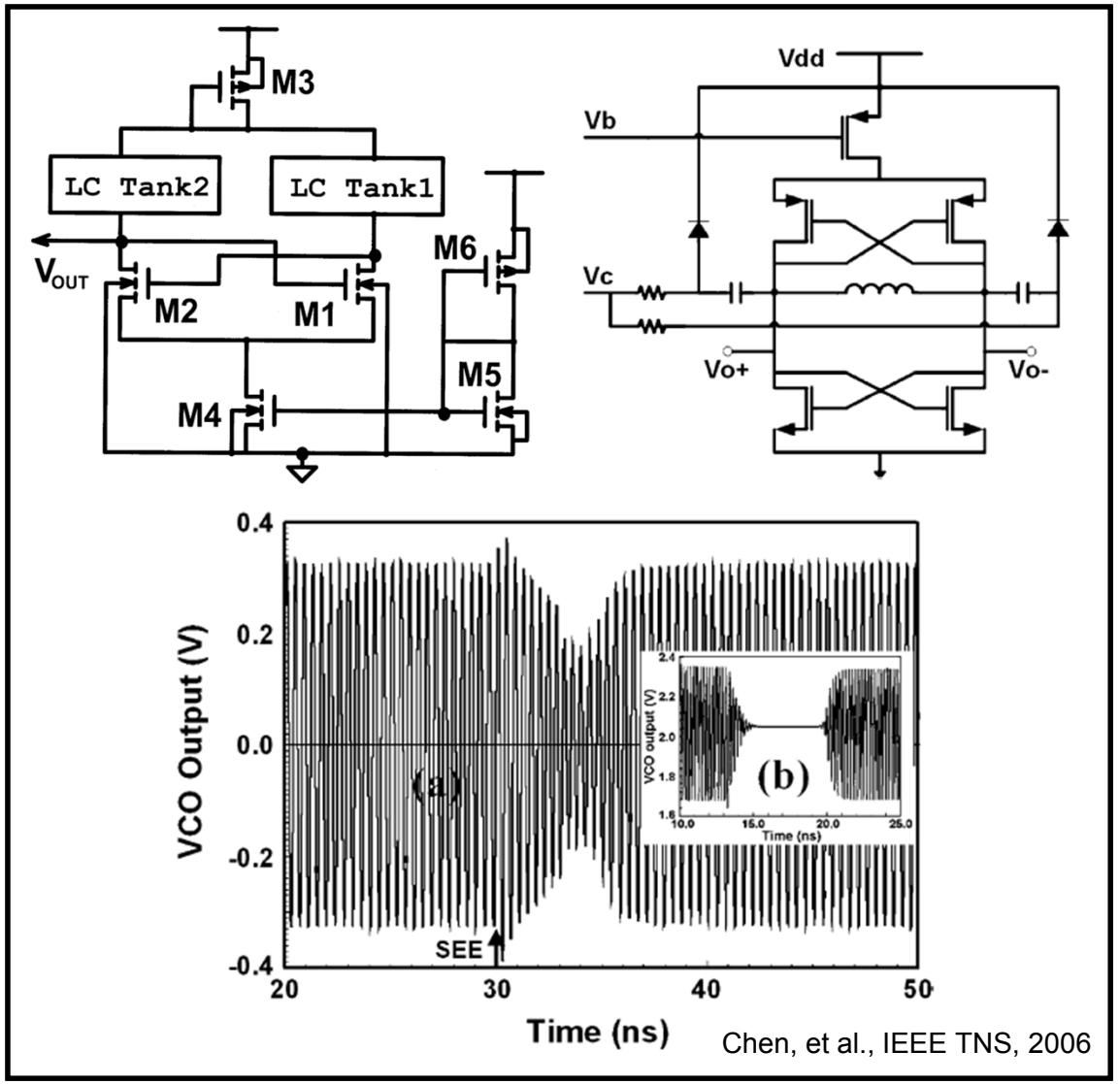
- Resistive Decoupling
  - *effectively increases the time constant seen by the two storage nodes and limit the maximum change in voltage during a single-event, thus increasing Q_{crit}*
- Filtering
  - *high-frequency transients may be filtered by decoupling nodes sensitive to ASETs and introducing a time constant through a series resistor or low-pass filter*
- Increased Capacitance
  - *increases the amount of charge, Q_{crit}, required to generate an ASET*



Loveless, et al., IEEE TNS, 2006

Circuit- and System-Level Mitigation

- Reduction of High Impedance Nodes
  - *high impedence nodes have consistenly been identified as the culprits!*
  - *can be reduced or eliminated at the circuit- or transistor-levels*

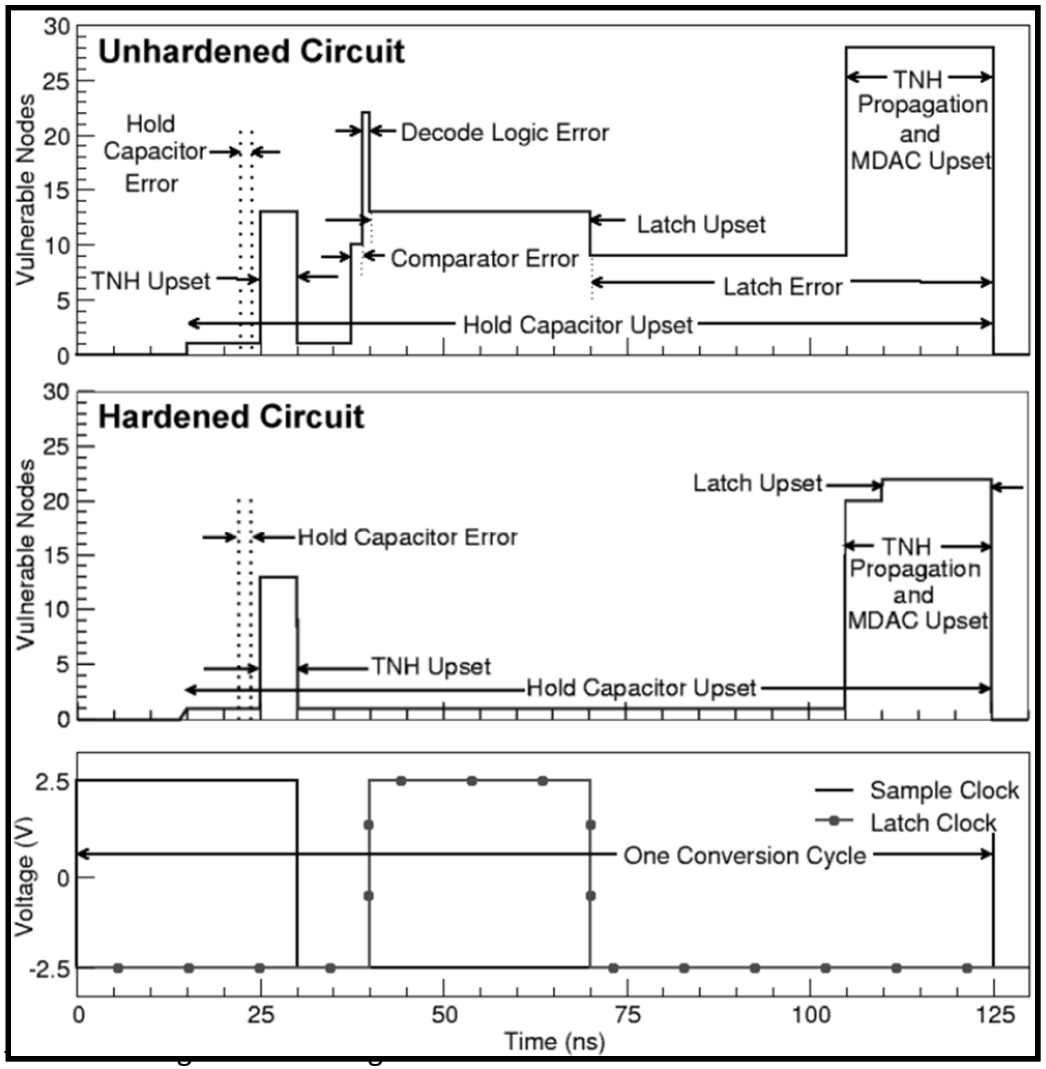


Single Event Mitigation By Elimination of High-Impedance Nodes in an LC Tank Oscillator

Circuit- and System-Level Mitigation

- Reduction of Window of Vulnerability (WOV)
  - *more common for ditigal systems - shows system dependence on clock*
  - *WOV analysis may indicate vulnerable regions within circuit and help predict upset probabilities*

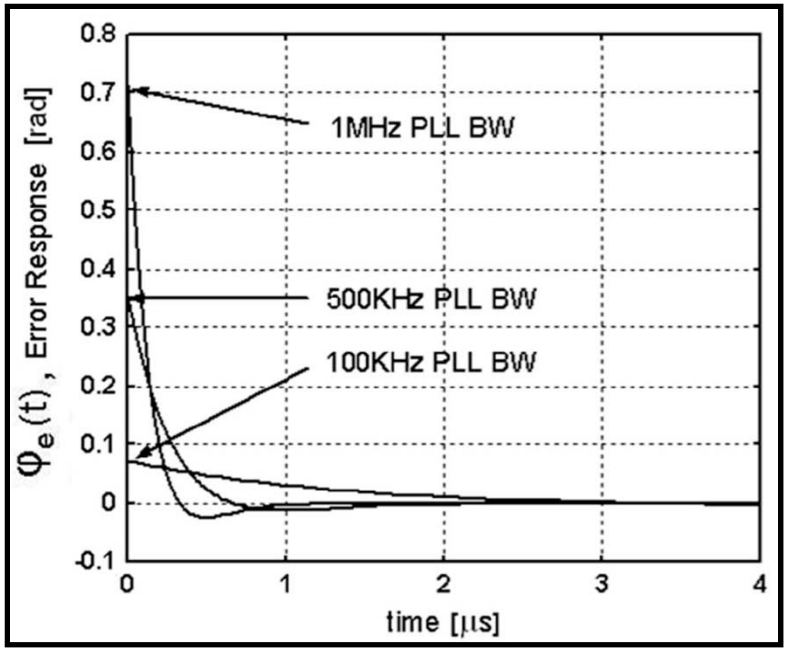
Kauppila, et al., IEEE TNS, 2004



Simulated WOV of a Pipelined Analog-to-Digital Converter

Circuit- and System-Level Mitigation

- Modifications in Bandwidth and Gain
  - *in general, many works on amplifiers, phase-locked loops, voltage-controlled oscillators, … have shown that **reduction in bandwidth** results in **reduction in SE vulnerability***



Error Response versus Time During a Single Event in the PLL at Various Bandwidths

Chung, et al., IEEE TNS, 2006

Circuit- and System-Level Mitigation

Boulghassoul, et al., IEEE TNS, 2004

- Modifications in Bandwidth and Gain
  - *in general, many works on amplifiers, phase-locked loops, voltage-controlled oscillators, … have shown that **reduction in bandwidth** results in **reduction in SE vulnerability***
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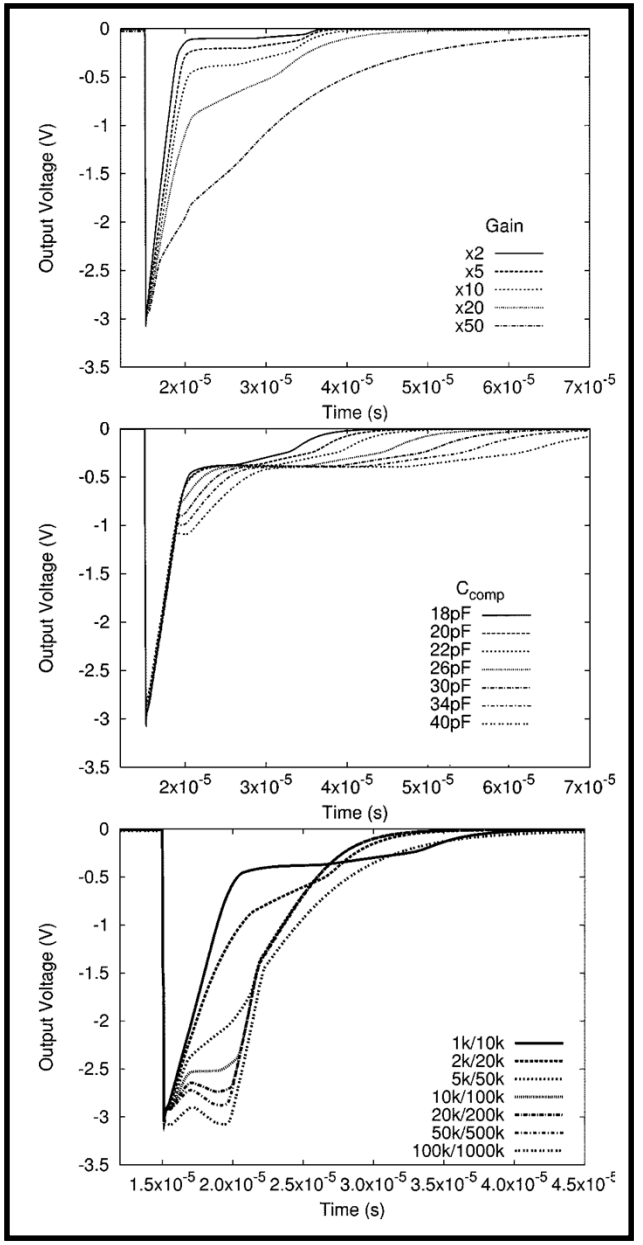

SET Dependence on Gain, Capacitance, and Resistance Values in Various Stages in an LM124 Op-Amp

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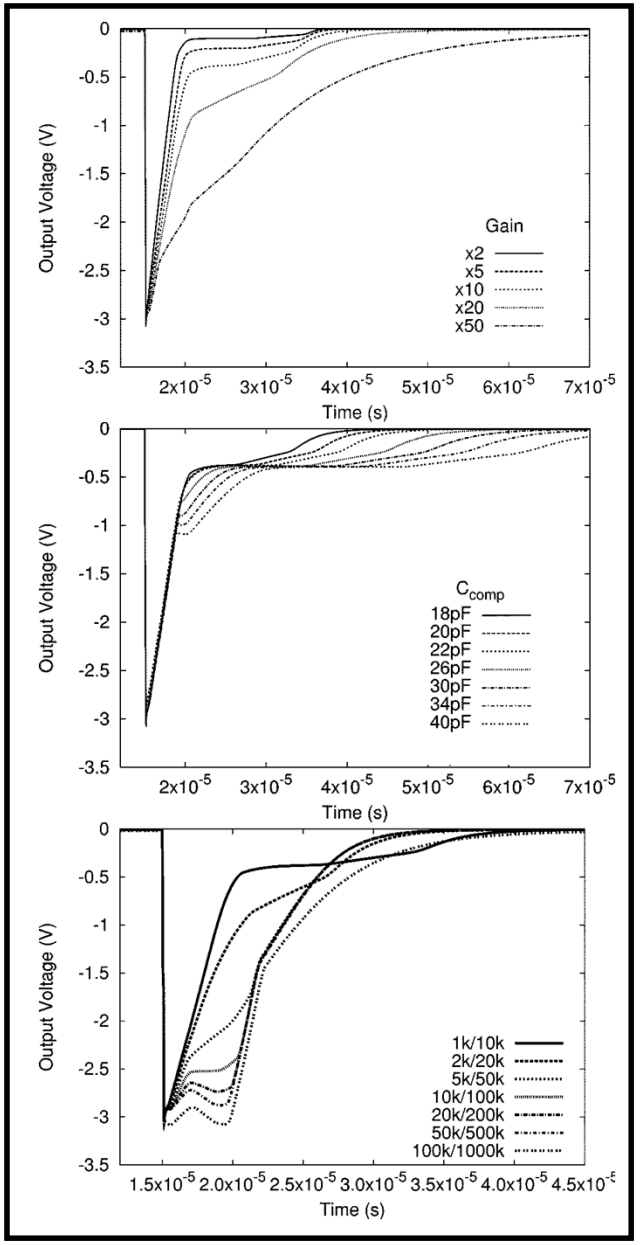
Ex. "Faster operational amplifier with a smaller gain will have a better SET response than a slower operational amplifier run at a high gain. It also seems to be best to use the smallest practical values to set the closed-loop gain of the amplifier", *Sternberg, et al.*



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- Modifications in Operating Speed and Current Drive
  - *analog circuits have been shown to exhibit reduced ASET vulnerability for increased operating frequency*

Contrary to that seen in digital circuits

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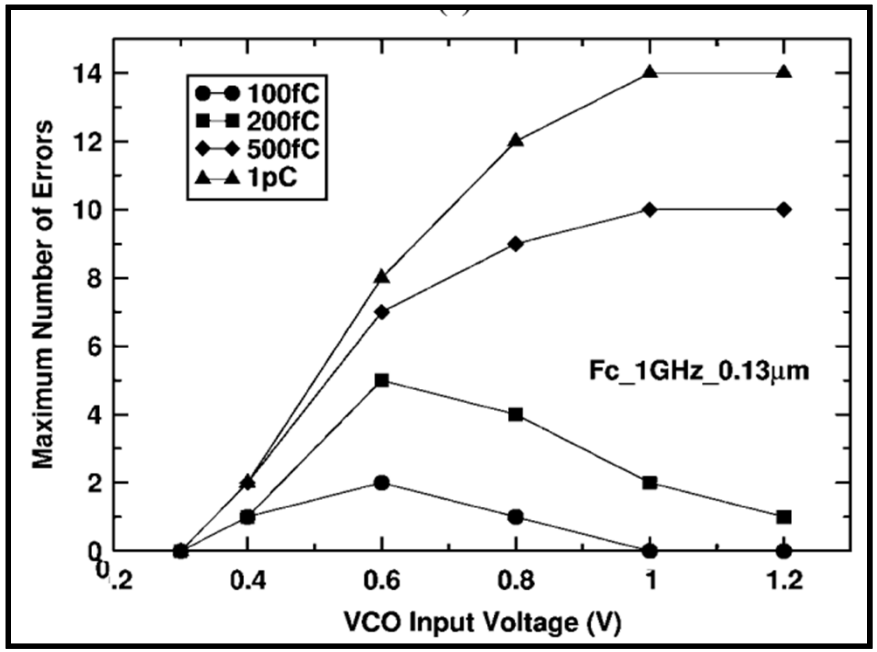
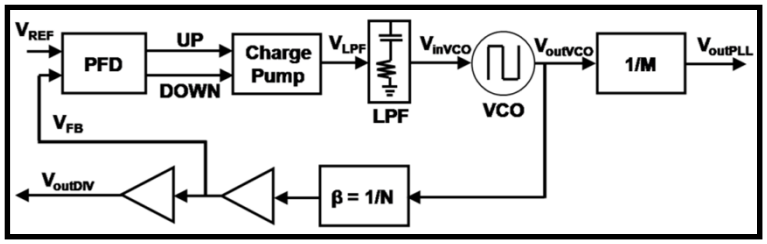
  - *important to attribute the improvement to either speed or drive strength (increased bias current is a well-known technique and is often used in AMS circuits for improved SET performance)*



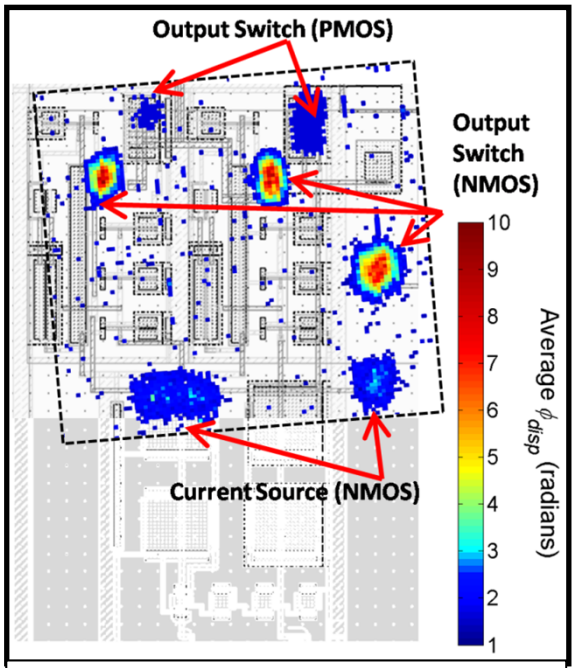
Number of Errors in VCO Output Bits Versus Input Voltage (Proportional to Drive Strength and Frequency)

Circuit- and System-Level Mitigation

- PLL used as an example to illustrate complex inter-dependencies
- Laser SET mapping performed on charge pump sub-circuit (most sensitive block)
  - *output signals following 10 strikes per x-y location were recorded*
  - *frequency/phase transients extracted from transient output*



Two-Photon Absorption Laser-Induced SET Map of PLL Sub-Circuit (Charge Pump)



200 MHz; 3.5 nJ/pulse

Loveless, et al., IEEE TNS, 2010

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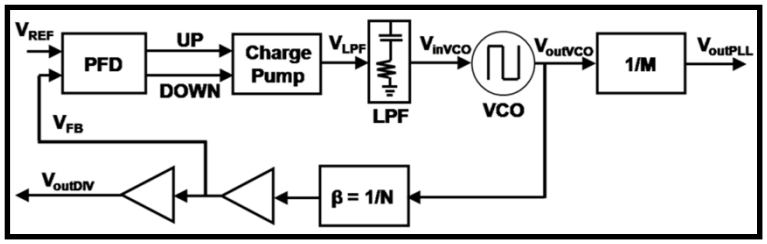

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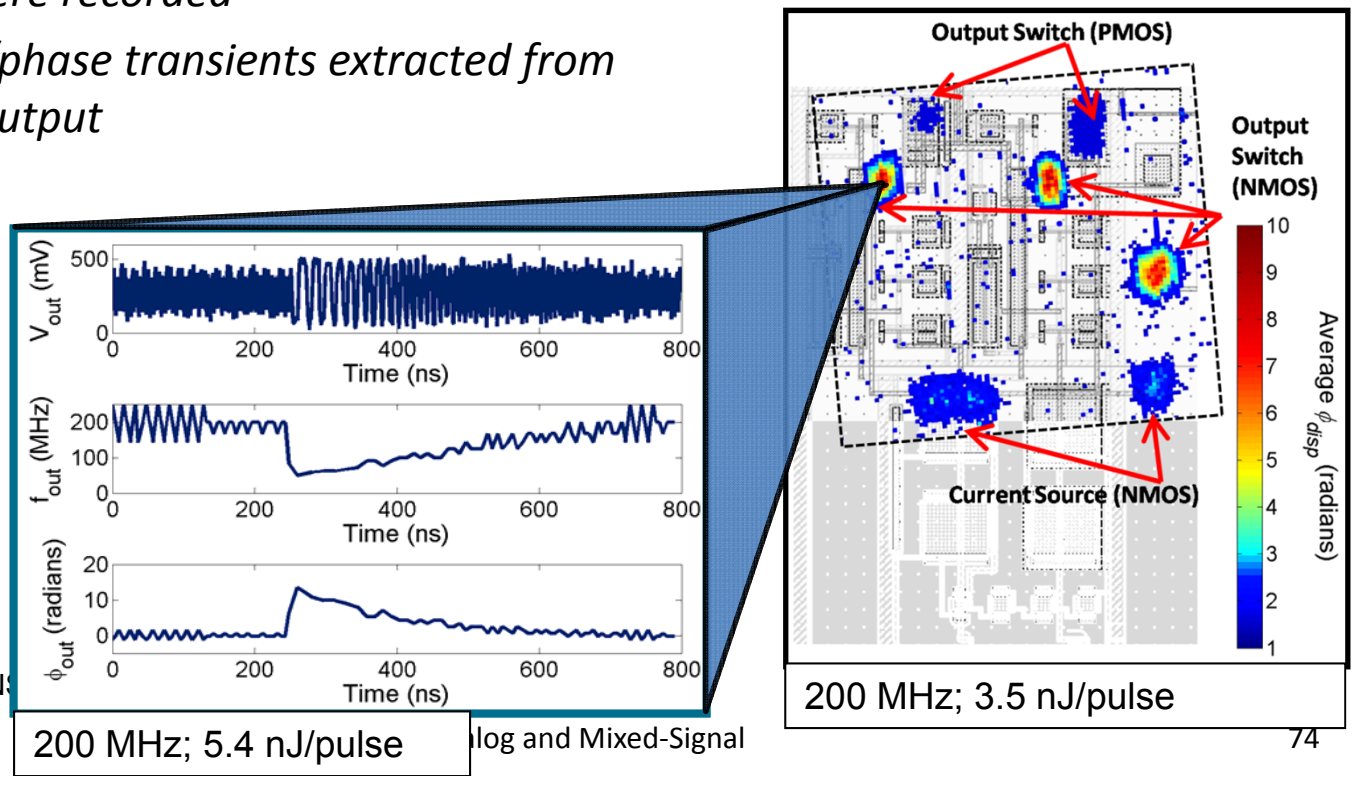
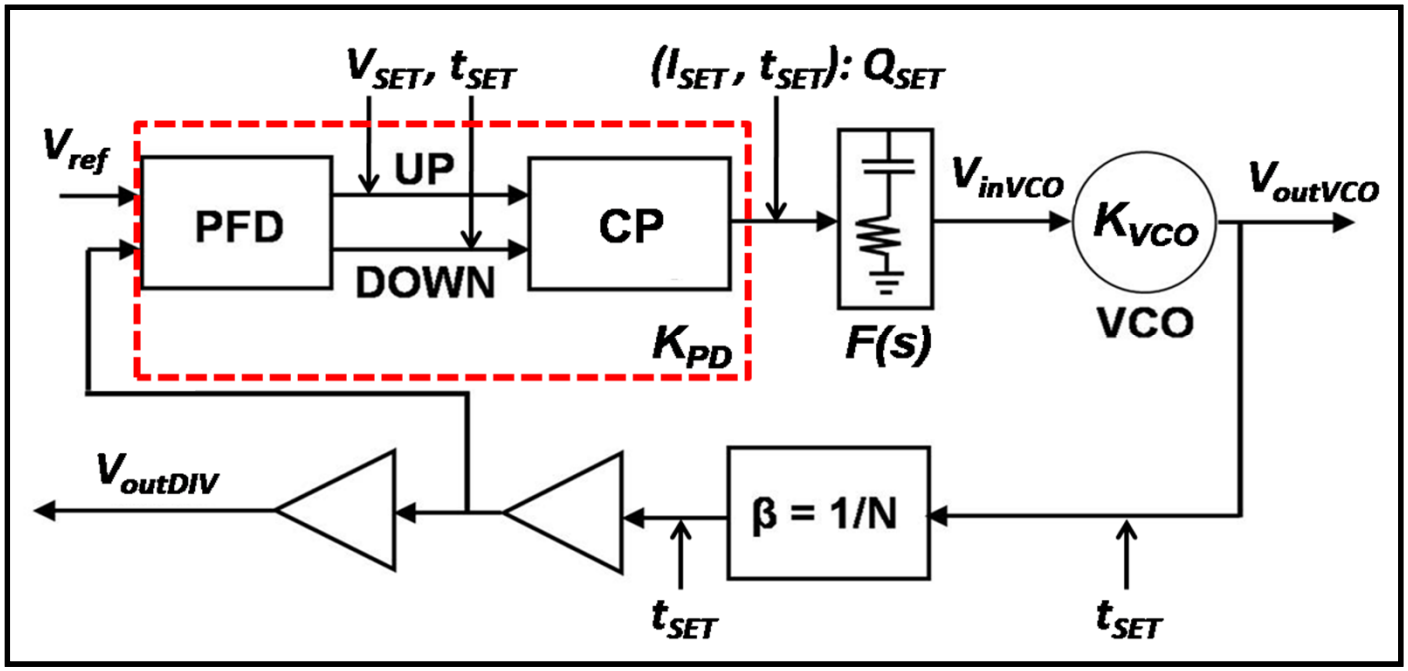


Transient Propagation Model



- Transient propagation model developed by assuming initial perturbation(s) are due to single *impulses* rather than continuous non-deterministic sources

- Resulting equations describe loop recovery time, frequency perturbation, V_{inVCO} perturbation, and output phase displacement!

Transient Propagation Model

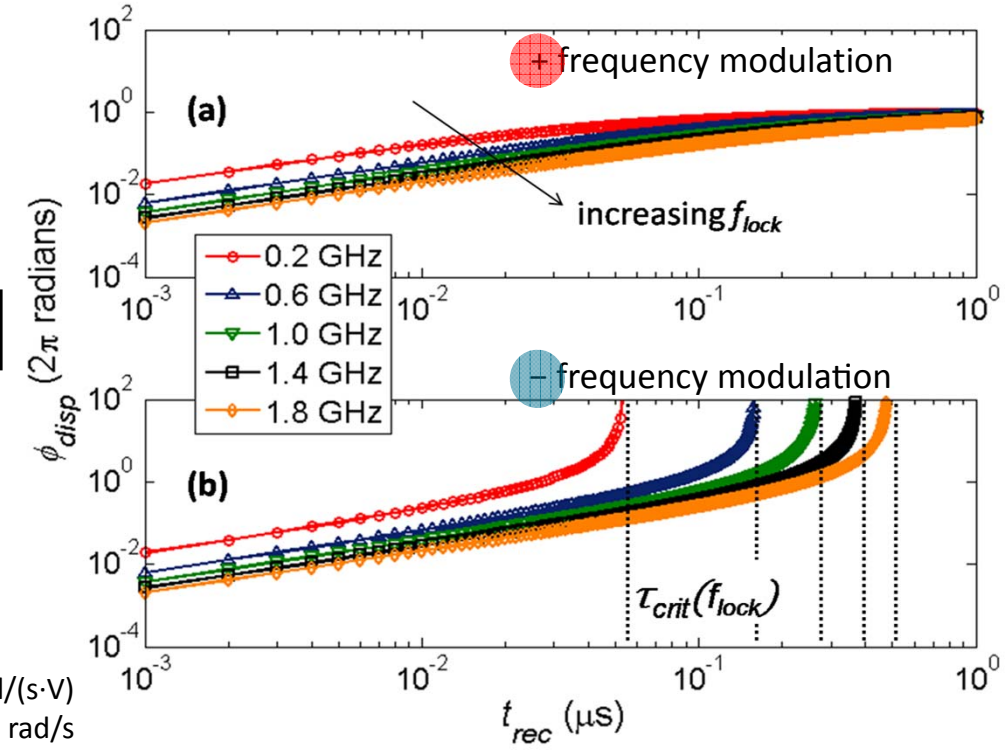
Ideal Recovery Times For Transient Perturbations Generated Within Each PLL Sub-Circuit

Sub-Circuit	t_{rec}
PFD	t_{SET}
CP	$Q_{SET}/I_{CP} + t_{SET}$
VCO	$\lvert T_c \rvert$
β	$\lvert T_{c,DIV} \rvert$

Output Phase Displacement

$$\varphi_{disp} = \frac{2\pi\omega_n^2 t_{rec}}{\beta f_{lock} \pm \omega_n^2 t_{rec}}$$

Output Phase Displacement vs. t_{rec} for Various Lock Frequencies



PLL Critical Time Constant

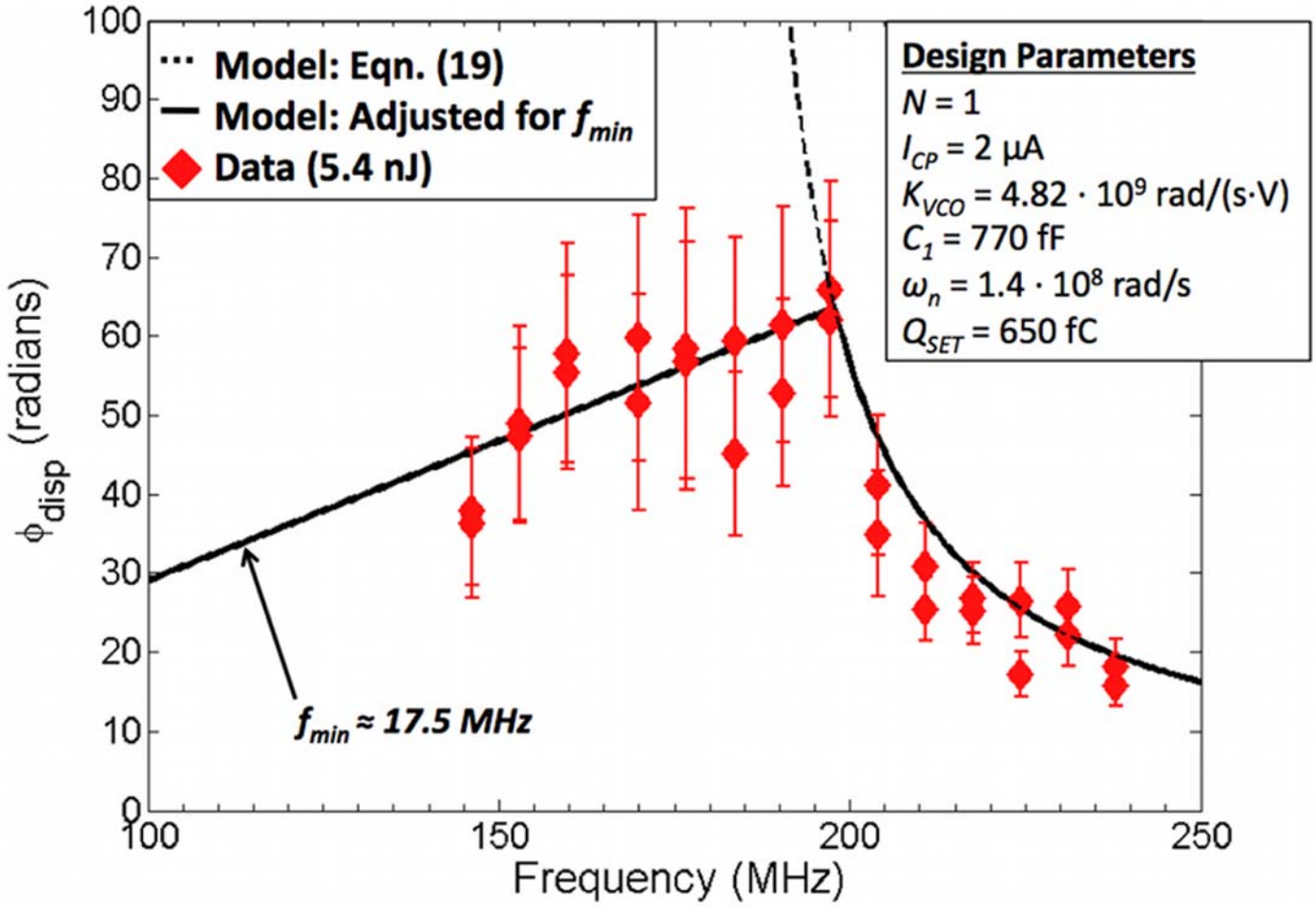
$$\tau_{crit} = \frac{\beta f_{lock}}{\omega_n^2}$$

PLL Design Parameters (90 nm 9SF)

I_{CP}	2 μA	K_{VCO}	$2.5 \cdot 10^{10}$ rad/(s·V)
C_1	2.14 pF	ω_n (β=1)	$6.1 \cdot 10^7$ rad/s

Loveless, et al., IEEE TNS, 2010

Transient Propagation Model



- Model was used to predict worst-case response of PLL, which was not observed during any prior experimentation!
- Further experiments validate competing effects within the PLL and importance of high-quality models for AMS circuits

Summary

- The ability to put entire systems on a single chip has increased the demand for mixed analog/digital (mixed-signal) circuits
- Single-event (SE) phenomena present challenges for analog & mixed-signal (A/MS) systems
  - *single-event transients (SET) are subject to cross-domain response mechanisms*
  - *SE mechanisms may not be tractable using conventional analysis techniques*
  - *new SE error metrics may be required due to the complexity of sub-circuits and functionality*
- However, there is a common thread:
  - *single-event performance of analog electronics tends to be dominated by:*
    - gain-bandwidth
    - speed
    - drive strength
    - high-impedance nodes

Mitigation Techniques Should Specifically Address Parameters in the Design Phase
Design-Around-Constraint

THE UNIVERSITY OF TENNESSEE CHATTANOOGA

Hardening-By-Design Techniques for Analog and Mixed-Signal ASICs

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