High-*k* Gate Dielectrics

by Durga Misra, Hiroshi Iwai, and Hei Wong

Microelectronics has been the most important driving force for almost all kinds of technology evolutions in the past four decades.[1,2] The size of the metal-oxide-semiconductor (MOS) transistor, which underpins Si microelectronics, has been reduced to a factor of 1,000 (Fig. 1). Silicon MOS technology has now been developed into two extremes: as fine as *nanometer size* in the device structures and as large as *gigascale* in terms of number of transistors in a chip. The downsizing rate of the MOS component is really impressive; now, we have sub-100 nm gate length transistors in production and R&D for 5 nm gate length devices is also on the way.[2] The technology is expected to continue its historical advancing rate with Moore's law for a couple of decades although there are many constraints ahead (Fig.2).[3] [Editorial Note: This topic has been addressed recently in these magazine pages, see *Interface*, Spring 2005.] With this trend, the silicon gate oxide will be scaled down to its physical limit[4] to keep the proper functioning of the transistors in the sub-10 nm technology node.

Physical and Technological Limits of Silicon Oxide

The gate oxide is the first device dimension reaching the atomic scale (~10 Å). The atomic scale gate dielectric has become the most critical constraint for further downscaling of the MOS transistors. Thirty years ago, the gate oxide thickness was 120 nm and now it is 1.2 nm in production, which is much thinner than the direct tunneling limit for SiO_2 (about 3 nm). Power consumption is a primary concern for high-performance logic integrated circuits with the tunneling gate oxide. For 1.2 nm thick silicon oxide, the gate leakage current density reaches 100 A/cm^2 at 1 V (see Fig. 3). Such large currents would not be acceptable in most applications. In the 70 nm technology node, the required gate oxide thickness is about 0.7 nm, which is only two atomic layers of silicon oxide and is the ultimate limit of bulk silicon oxide.[4] However the actual technologically feasible thickness is well above this physical limit because of the large leakage current as well as the nonscalable features of the film properties and fabrication technology. In the nanometer thick dielectric film, the interface layer is so thick (compared to the total oxide width) that any nonuniformity in chemical composition and even the surface roughness can cause pronounced fluctuations of the device characteristics. If we allow the oxide thickness to fluctuate with a half-monolayer, which means 5% of the oxide thickness, then the smallest oxide film thickness to meet this tolerance is 1.6 nm (Fig. 3), which is very close to the oxide thickness used in our current complementary (C)MOS technology. If one could relax the fluctuation to 8%, then the minimum thickness would be 1 nm and could be used in the 80 nm technology node in these years. Introducing physically thicker high-*k* materials, while maintaining the same value of the capacitance required for controlling the current flow in the channel, can resolve all the aforementioned problems.

High-*k*: The Hope of Next Generation Gate Dielectrics

Introducing higher dielectric constant ($k > 10$) insulators [mainly transition metal (TM) oxides] is therefore indispensable for the 70 nm technology node and beyond, despite the fact that most of the high-*k* materials have much poorer properties than the conventional silicon oxide which has been used as gate dielectric material for over 40 years. There are many problems associated with the ionic high-*k* materials. High *k* TM oxides have poor thermal stability and poor interface quality with the silicon substrate. In addition, the interface and oxide trap densities are one to three orders of magnitude larger than those in silicon oxide. Recently, TM silicates such as $HfSiO_x$ have been preferred because they have better thermal stability compared to their oxides. The dielectric constant of TM silicates is less than TM oxides but higher than silicon oxide.

The underlying physics for these undesirable properties is governed primarily by the ionic nature of the TM-oxygen bonds. TM oxides are formed by transferring the d-state and s-state valence electrons of the metal into the oxygen 3s or 3p empty orbitals. The metal-oxygen bonds are more or less ionic. Because metal oxidation can take place easily, the oxide film would have a large amount of oxygen vacancies and would be easier to be partly crystallized. These mechanisms give rise to the high trap density in metal oxides. Because the TM elements can also react with the substrate Si atoms at low energy, they produce silicate and silicide bonds.[5] The interfacial metallic silicide bonds, working as interface traps,[5] can also lower the conduction band offset energy. The ionic or polarized metal-oxygen bonds are also the reason for high-*k* values and the existence of soft optical phonons, which

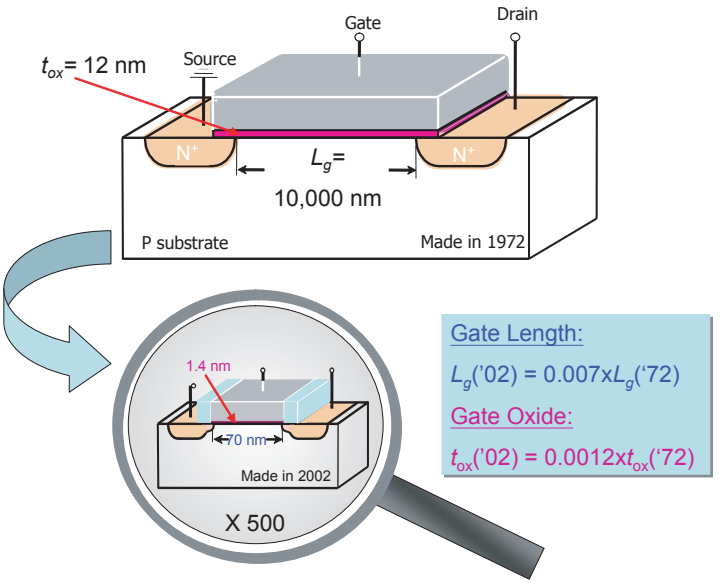

FIG. 1. The feature sizes of MOS transistors have been scaled down to a factor of 1,000 since 1972.

further induce a large leakage current and channel mobility degradation. These fundamental limitations must be overcome. The remaining part of this article has the full story. The technology for fabricating high quality high-*k* materials, the properties of the high-*k*/Si interfaces, the origins of the defects, and the reliability issues of the future gate dielectric materials are discussed below.

Deposition Techniques

TM-based high-*k* dielectric materials are typically deposited on crystalline silicon rather than thermally grown. To achieve desired electrical characteristics the deposited dielectric must have excellent interfacial and bulk properties in addition to good uniformity. Appropriate processing reactors with matching chemical precursors are therefore required such that many properties of the deposited dielectric film can be optimized. Various technologies such as (*i*) chemical vapor deposition (CVD), (*ii*) plasma enhanced chemical vapor deposition (PECVD), (*iii*) metallorganic CVD (MOCVD), (*iv*) atomic layer deposition (ALD), (*v*) plasma enhanced atomic layer deposition (PEALD), (*vi*) physical vapor deposition, (*vii*) molecular beam epitaxy, (*viii*) ion beam assisted deposition, (*ix*) reactive sputtering, (*x*) thermal evaporation, and (*xi*) sol-gel deposition are being used to deposit high-*k* dielectrics on silicon. Although these techniques have their advantages and disadvantages, manufacturability and production of excellent quality films ultimately dictate which of the candidates enjoy wide acceptance. In addition, predeposition surface preparation also plays an important role in obtaining excellent electrical characteristics whereas postdeposition treatments such as sintering or annealing often improve the film characteristics. MOCVD and ALD are the two most widely studied deposition techniques for depositing dielectrics such as Al_2O_3, ZrO_2, HfO_2, $ZrSiO_x$, and $HfSiO_x$.

High-*k* Films Deposited by MOCVD

Dielectrics such as HfO_2 and $HfSiO_x$ are typically deposited by MOCVD at temperatures in the range of 450-550°C on a thin interfacial layer (IL) of rapid thermal oxide or chemical oxide. The precursors that provide excellent decomposition characteristics can be tetrakis(diethylamido)hafnium (TDEAH) and tetrakis(dimethylamido)silicon (TDMAS)[7] along with O_2. As shown in Fig. 4, in addition to a HfO_2 layer

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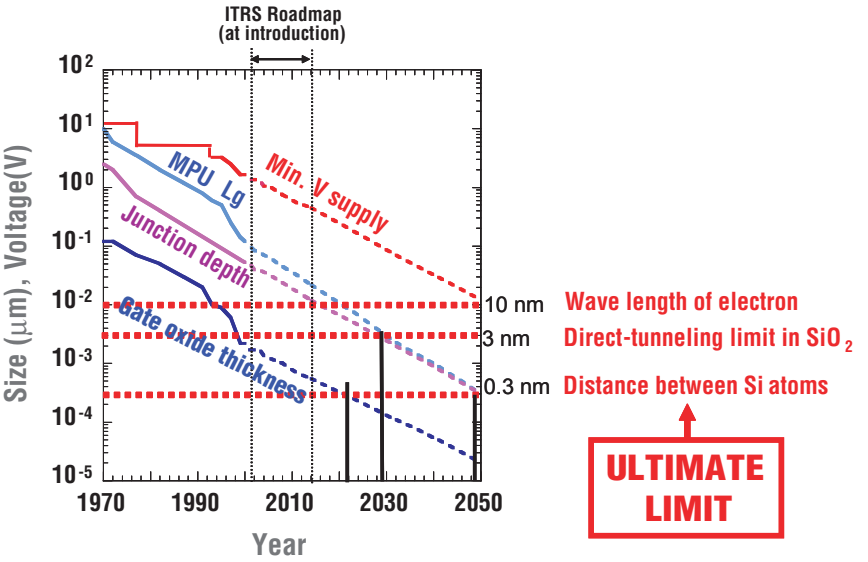

FIG. 2. Trend in MOS device parameter scaling and the prediction made in the 2003 International Technology Roadmap for Semiconductor (ITRS 2003).[3]

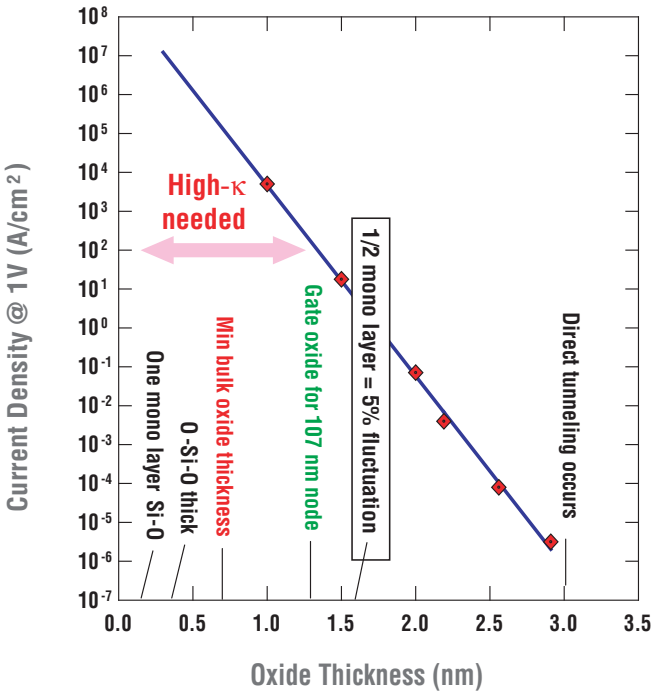

FIG. 3. The direct tunneling current increases exponentially as the tunneling gate oxide becomes thinner. Markers depict the data from quantum mechanical calculation by Lo et al.[6] *Oxide thinner than 1.2 nm would result in too large a gate leakage current and difficulties in process control; high-*k *material must be used.*

deposition, Hf-silicate formation takes place at the interface because of interdiffusion of Hf and Si atoms where Hf diffuses into the SiO_2 layer and/or the Si diffuses into the HfO_2 layer.[8] This is beneficial because more Hf-rich ILs with a higher *k* value is important when downscaling effective oxide thickness (EOT) values. During deposition of these films, N_2O/ O_2 can be used for *in situ* nitridation of the dielectric layers. Additionally, by optimizing the deposition temperature and time during MOCVD deposition, the quality of the HfO_2 layer can be improved significantly.

ALD of High-*k* Films

The ALD process refers to a binary chemical reaction sequence where each chemical precursor is self-limiting that leads to monolayer saturation. Fig. 5 contains a schematic of the ALD process with alternating HfCl and H_2O exposures[9] for depositing HfO_2 on silicon. ALD provides excellent step coverage and reduces the breakdown voltage of dielectric films such as HfO_2. However, like MOCVD, the dielectric film also nucleates on an oxide-coated silicon, which leads to a reduction in the effective dielectric constant. In ALD, HfO_2 films grown using $HfCl_4$ and water, the deposition temperature controls growth rate, roughness, density, microstructure, and the impurity content. The films deposited at higher temperatures show improved electrical characteristics. Film roughness also increases with increasing deposition temperature. Therefore temperature optimization is crucial. Postdeposition annealing also plays an important role in optimizing electrical characteristics in ALD dielectrics.[10]

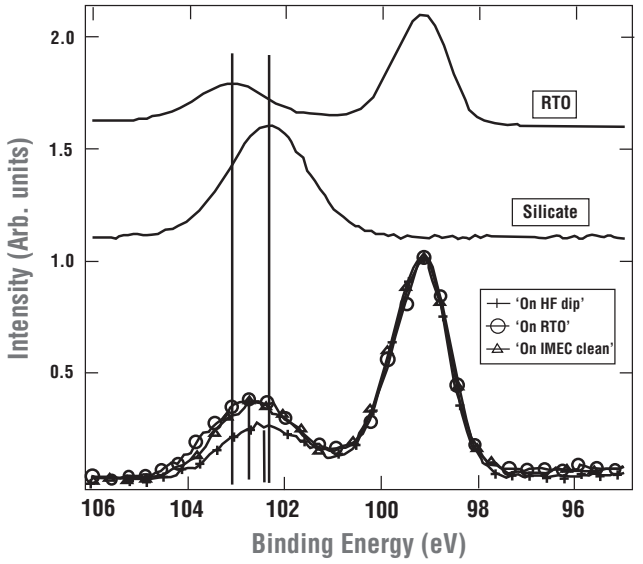

FIG. 4. X-ray photoelectron spectra recorded for MOCVD HfO_2 layers deposited at 485°C (60 s deposition time) on different starting surfaces. As a reference, a 1 nm rapid thermal oxide (RTO) and a Hf-silicate film are added. After deposition, a Hf-silicate like interfacial is formed for all starting surfaces.[8]

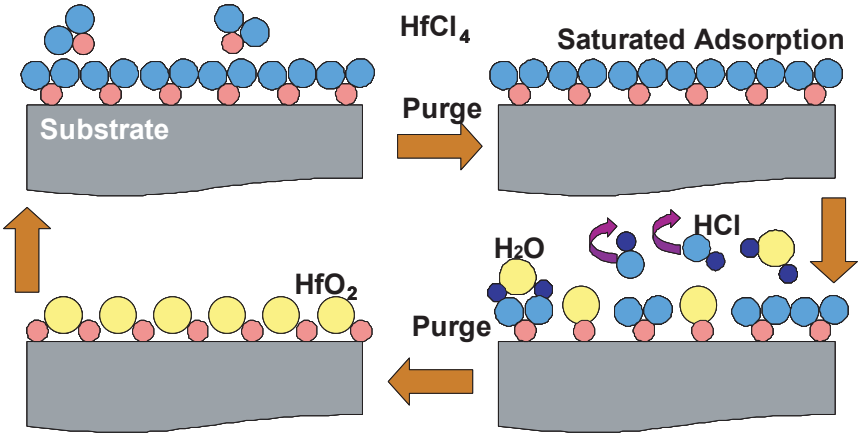

FIG. 5. Schematic of ALD process with alternating HfCl and H_2O exposure[9] to deposit HfO_2 on silicon.

Electrical Properties and Reliability Issues

The major problem in high-*k* materials is that they are yet to meet the electrical characteristics that SiO_2 or most recently SiON, can offer. Figure 6 shows the transistor characteristics of different n-channel devices with similar EOTs. As can be seen, the electrical characteristics of devices with HfO_2 and hafnium silicates, still must be significantly improved. The fundamental electrical property that determines the application of these metal oxides in CMOS devices is their charge trapping characteristics. Charge trapping can alter the threshold voltage of transistors over time and subsequently affect the defect nature of the dielectrics. In addition to charge trapping in the bulk high-*k* layer, the contribution from the interface traps present in between the high-*k* layer and the interfacial layer and in between the substrate and the interfacial layer, is significant. As far as the deposition method is concerned, charge trapping in high-*k* dielectrics is almost identical in both ALD and MOCVD deposited HfO_2 due to the large number of preexisting traps. As described earlier, the origin of the preexisting traps is tied to the way these dielectrics are formed. The energy levels of the traps in the high-*k* dielectric bandgap are deep and help in trap assisted tunneling. These deep traps can be annealed but an increase in shallow traps may appear due to crystallization of the high-*k* film.

Defects or leakage current have always been at the forefront with the evolution of new technologies or introduction of new materials in CMOS technology. To match the properties of high-*k* dielectrics with those of conventional silicon oxide, the existence of various defects and how they affect the reliability through trapping of charge at the defect sites must be looked at. In bulk high-*k* devices, shallow electron traps at the conduction bandedge have been found to be inherent in the most recent studies. These traps are closely related to charge transport and charge redistribution during stress. The shallow traps, considered to be the root cause of trapping, especially for low voltage

stress, also control charge detrapping and redistribution during relaxation after removal of stress. There are reports that permanent trap creation may not be possible for low stress levels in high-*k* materials and charge trapping is reversible by applying stress of opposite polarity. But Houssa *et al.*[11] report neutral trap and positive charge generation in the bulk high-*k* material and at the interfacial layer, respectively, under high negative stress voltage. Fig. 7 shows the effect of stress as a function of temperature on the leakage current through a TiN/$HfSi_xO_y/SiO_2$ gate stack. Electron trapping and neutral trap generation in the bulk of high-*k* rather than at the interfaces seem to be dependent on the stress voltage and temperature.[12]

Several misconceptions are possible in reliability studies of high-*k* gate materials. For example, when the devices are subjected to an electrical stress, poststress leakage current is typically slightly higher than the prestress leakage at low positive and negative gate biases, *i.e.*, within the range of trap-assisted tunneling regime. But at comparatively high positive/negative gate bias, poststress leakage current can be lower than the prestress value. This is a typical example of stress-induced leakage current, which is attributed to neutral trap generation. But, one must be careful with high-*k* dielectrics as shallow traps with energy levels lying within 0.3-0.8 eV below the conduction bandedge give rise to extensive electron trapping during stress, which distorts the internal electric field. Significant relaxation induced detrapping takes place after the stress. Detrapping from shallow traps may also occur during poststress current-voltage measurement, which increases poststress leakage even in the trap-assisted tunneling regime. Therefore, adequate time for relaxation must be provided before a poststress current-voltage measurement is made. Besides, dominance of negative charge trapping near the injection side that causes electric field distortion can help the injected electrons see a triangular barrier, the effect being, poststress leakage is lower than the prestress value and the shift is parallel.

Systematic studies of charge trapping and trap generation characteristics of various high-*k* gate stacks, especially for high stress levels and at elevated temperatures, and interpretation in terms of spatial and energy level distribution of these traps are currently being carried out by many groups. The use of high-*k* dielectrics will become routine when many of these reliability problems are solved.

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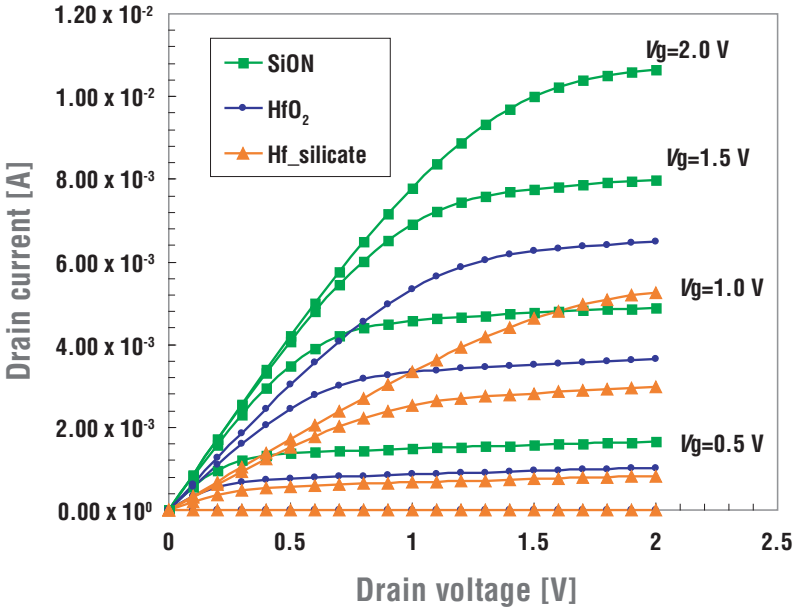

*FIG. 6. Transistor characteristics of different n-channel devices with high-*k *dielectrics as gate materials and with similar EOT.*

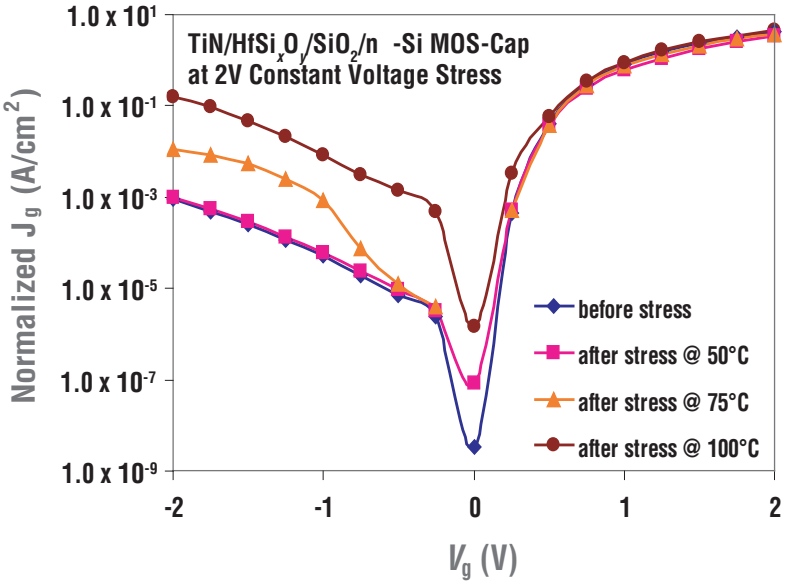

FIG. 7. Normalized current density J_g of TiN/$HfSi_xO_y/SiO_2$ gate stack stressed at different temperatures with a constant voltage stress of 2 V.

Conclusion

In this article, we have presented the requirements, current status of fabrication/processing, electrical properties, and reliability issues of high-*k* dielectrics. We have considered two important processing steps out of many for their popularity. The electrical properties and reliability must be investigated further before high-*k* materials become an integral part of nanoscale CMOS devices. ■

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