High-Performance 5LPE Implementation Next-Generation Arm “Hercules” CPU

Kevin K. Yee (Samsung), Fakhruddin Ali Bohra (Arm), Edson Gomersall (Cadence)

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High-Performance 5LPE Implementation Next-Generation Arm “Hercules” CPU

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Marketing Director, IP & Ecosystem
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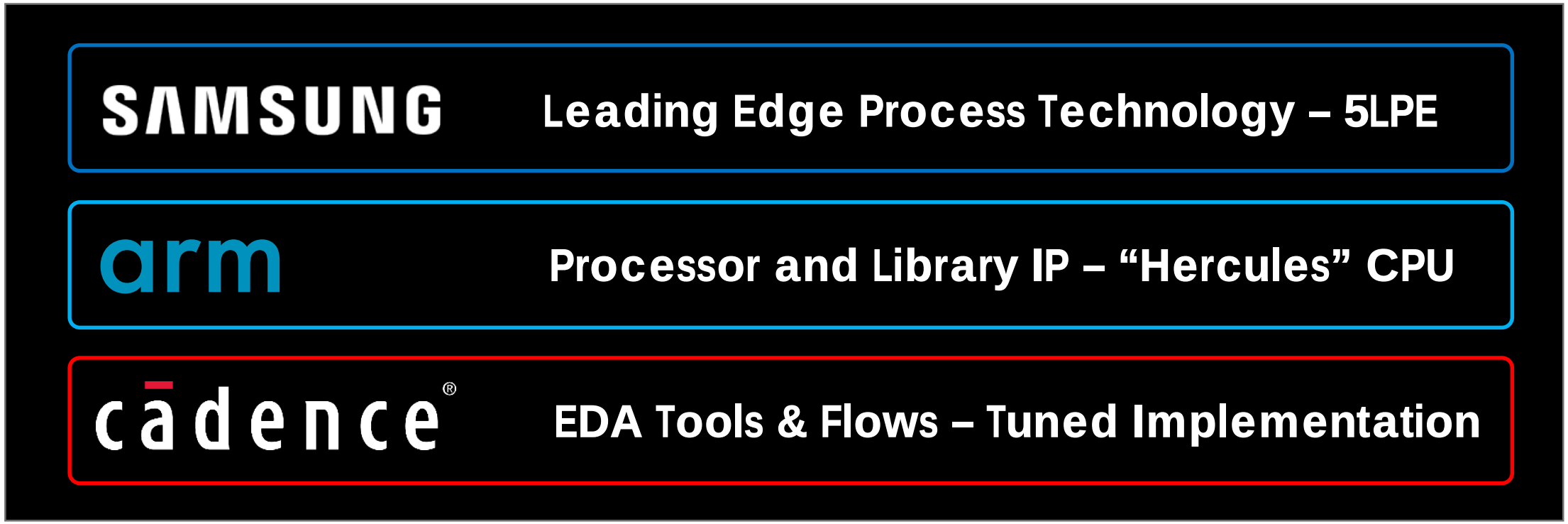
Cadence, Arm, Samsung Foundry Partnership

Cadence, Arm, Samsung Foundry Collaboration

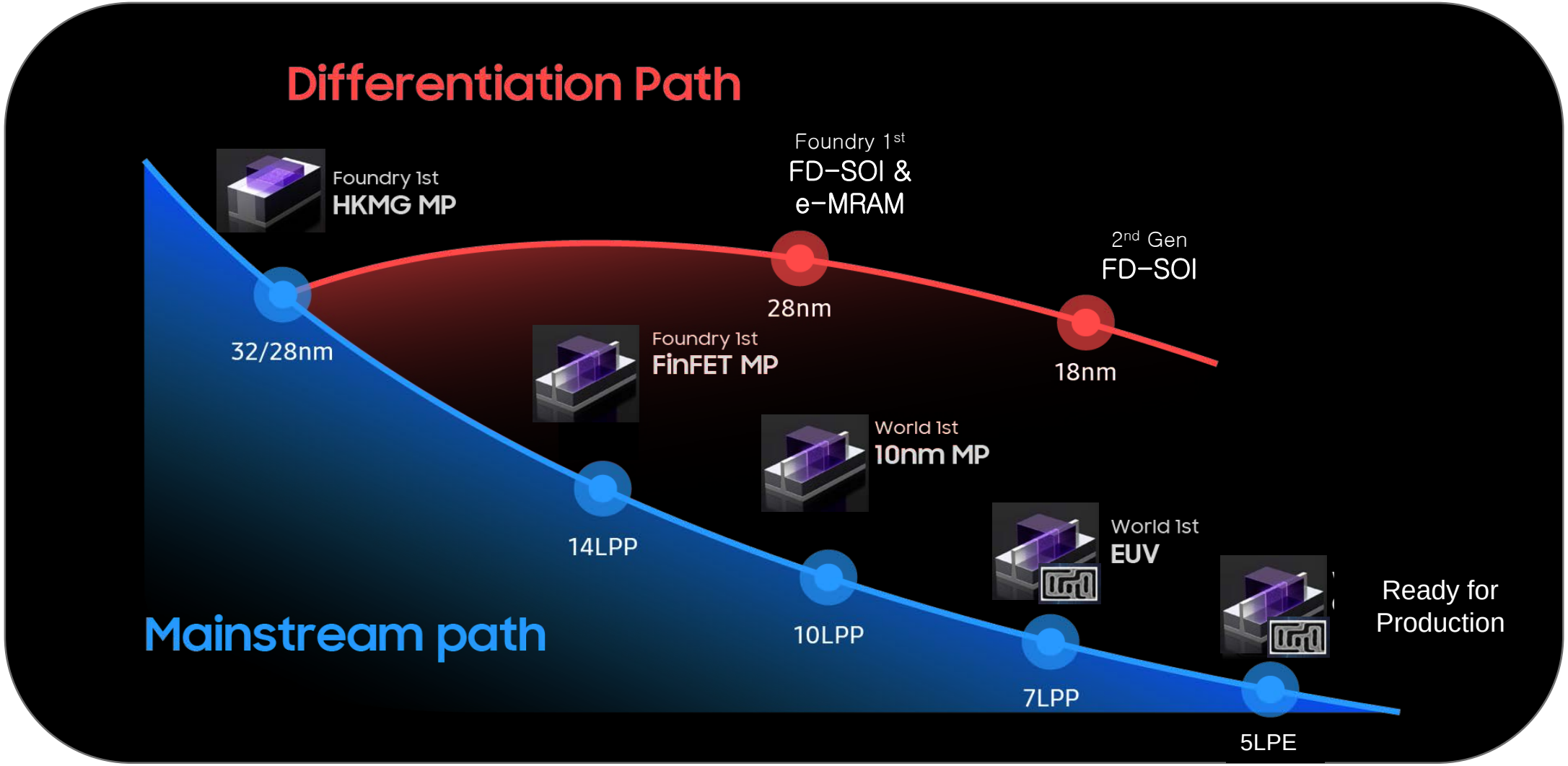
Enabling the Next Level of Innovation



Delivering the Most Optimized High-Performance Solution!

Samsung Foundry Technology Leadership

Leading the industry with many 1st



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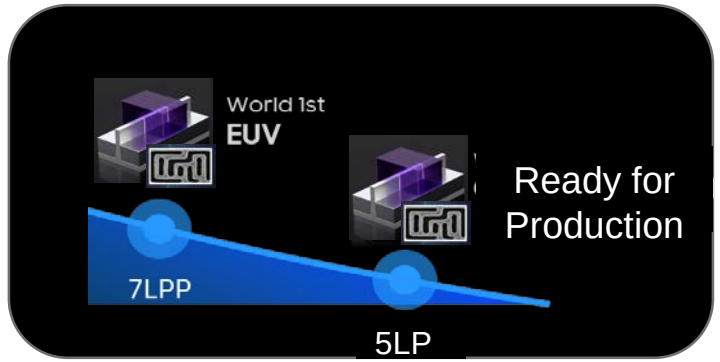
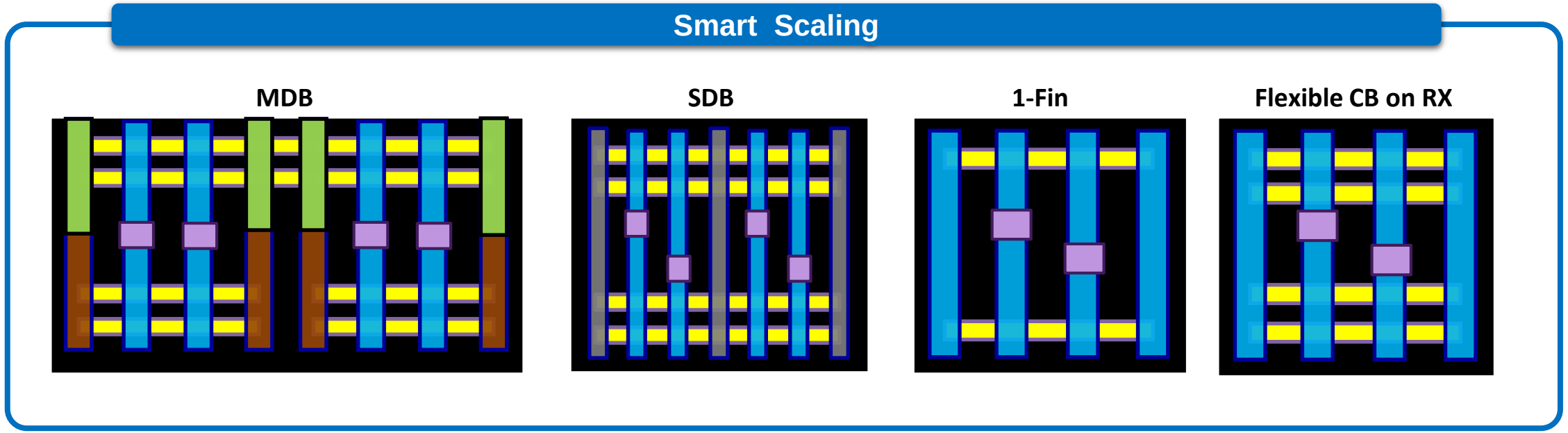
Why 5LPE?

Full EUV technology – ready for production



- **2nd gen. EUV technology**
- **7LPP compatibility: IP re-use, yield leverage, easy migration**
- **Enhanced features to 7LPP: MDB, SDB, single fin cell, CB on RX edge**



5LPE Process Overview

Easy migration from 7LPP

IP re-usability with boosted transistor performance

- GR compatibility, same SRAM, same TR structure
- 1.11x perf boosted by Low-k spacer, DC enhancement, etc.

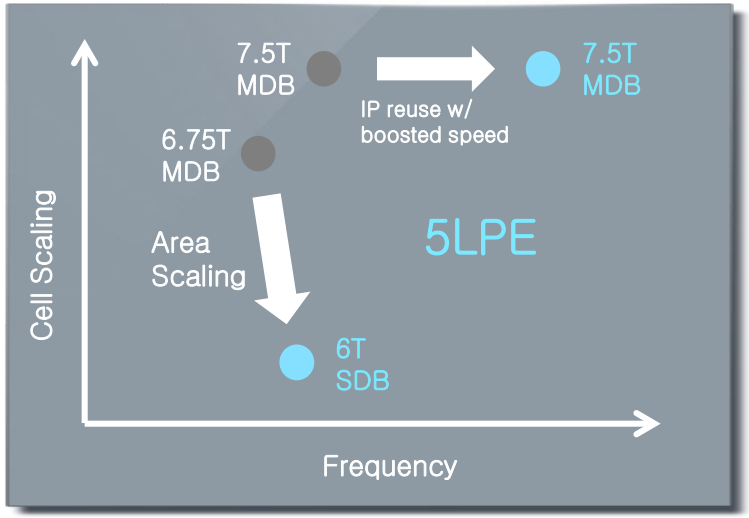
Smart scaling with 6T SC offering

- 0.70x block-level area due to 6T with SDB and CB on RX edge

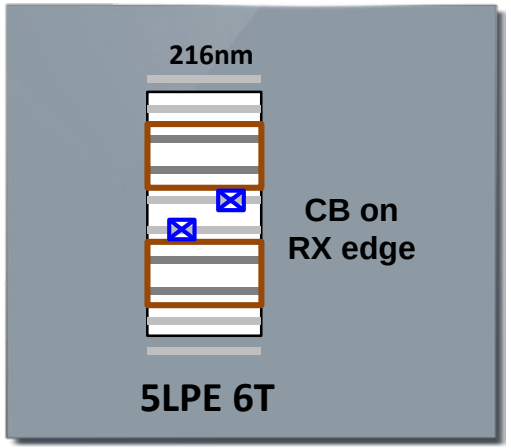
Superior power efficiency by 6T SDB with 1-Fin

- 0.80x block-level power

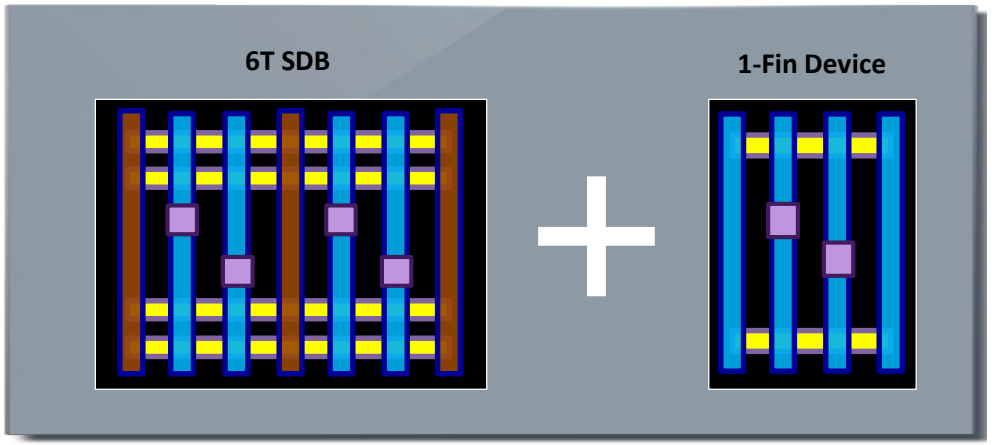
Migration Enhancement



Lower track standard



Superior power efficiency



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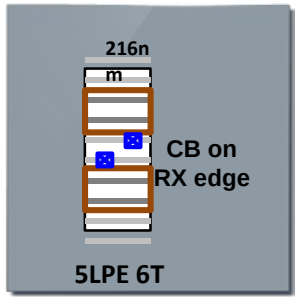
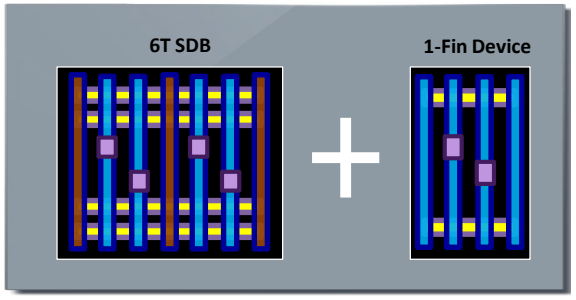
5LPE Technology Enhancements

Enabling 36M2, SDB, 1FIN, CB on RX-edge & 6T



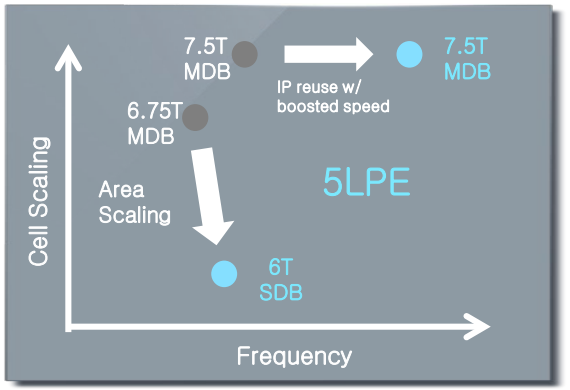


- **IP re-usability with boosted performance**

	7LPP	5LPE	Note
FP	27FP		**Compatible**
CPP	54CPP/60CPP		**Compatible**
SRAM bitcell	P026/P032		**Compatible**
Vop, Vth, Lgate	0.75V, RVT/LVT/SLVT, 8nm/10nm		**Compatible**
M1/M3/M4	40nm/36nm/44nm		**Compatible**
M2	48nm	**+ 36nm**	**Enhance**
Diffusion Break	MDB	**+ SDB**	**Enhance**
Min NFIN	2FIN	**+ 1FIN**	**Enhance**
CB	CB on STI	**+ CB on RX-edge**	**Enhance**
Standard Cell	7.5T	**+ 6T**	**Enhance**

5LPE Key Feature Comparison

7.5T for performance, 6T for area & power



- **7.5T: Performance driven with 60CPP and MDB**
- **6T: Area & power driven with CB of RX edge, SDB and 36M2**

Track		7.5T [HD]	6T [UHD]
Cell Height [nm]		270	216
Tech Definition	FP [nm]	27	27
	CPP [nm]	**60**	54
	M1 [nm]	40Bi	**40Uni**
	M2 [nm]	60	**36**
	DB	**MDB**	**SDB**
	CB	CB on STI	**CB on RX edge**
Design Feature	FIN #	3:3	2:2
	Signal Track	6	5

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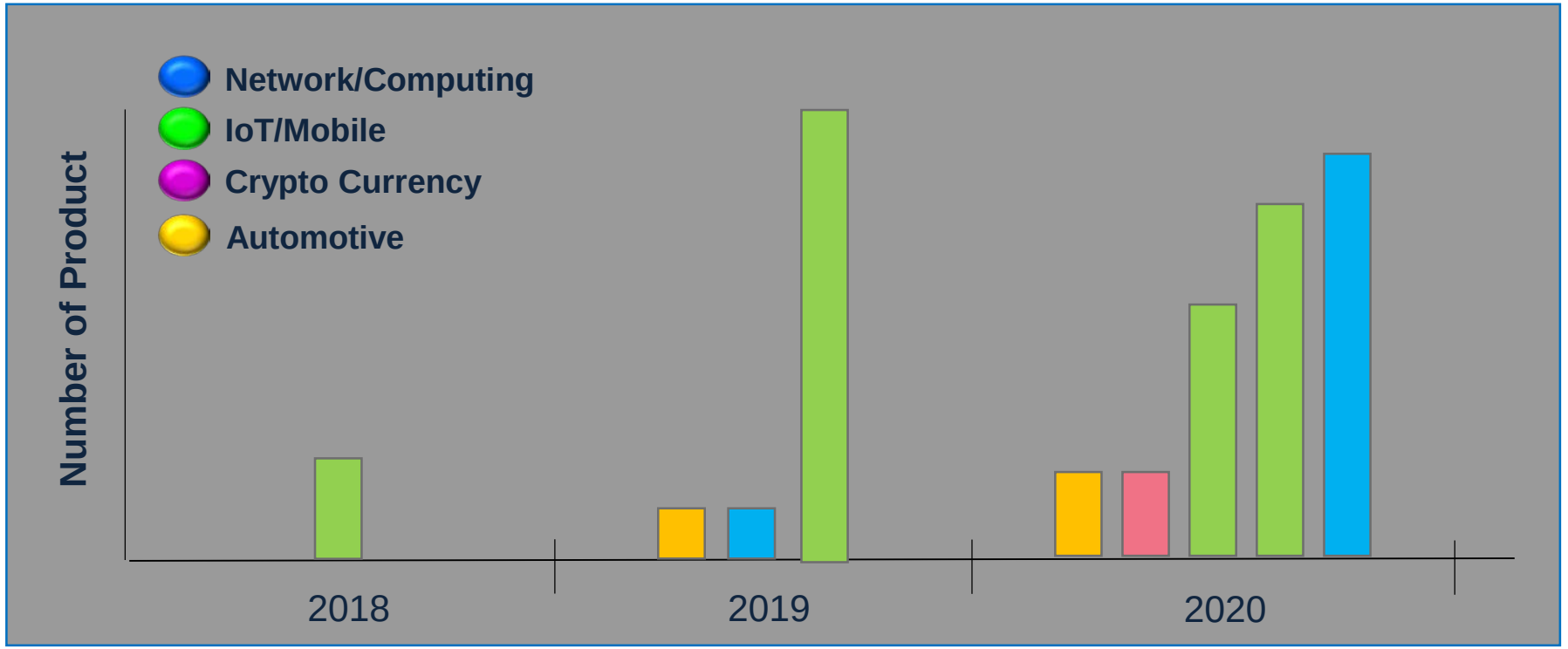
5LPE Broad Market Adoption

7.5T for performance, 6T for area & power

- **2018: 7nm production tapeout**
- **2019: 5nm production tapeout**
- **2020: Main node will be 5nm**



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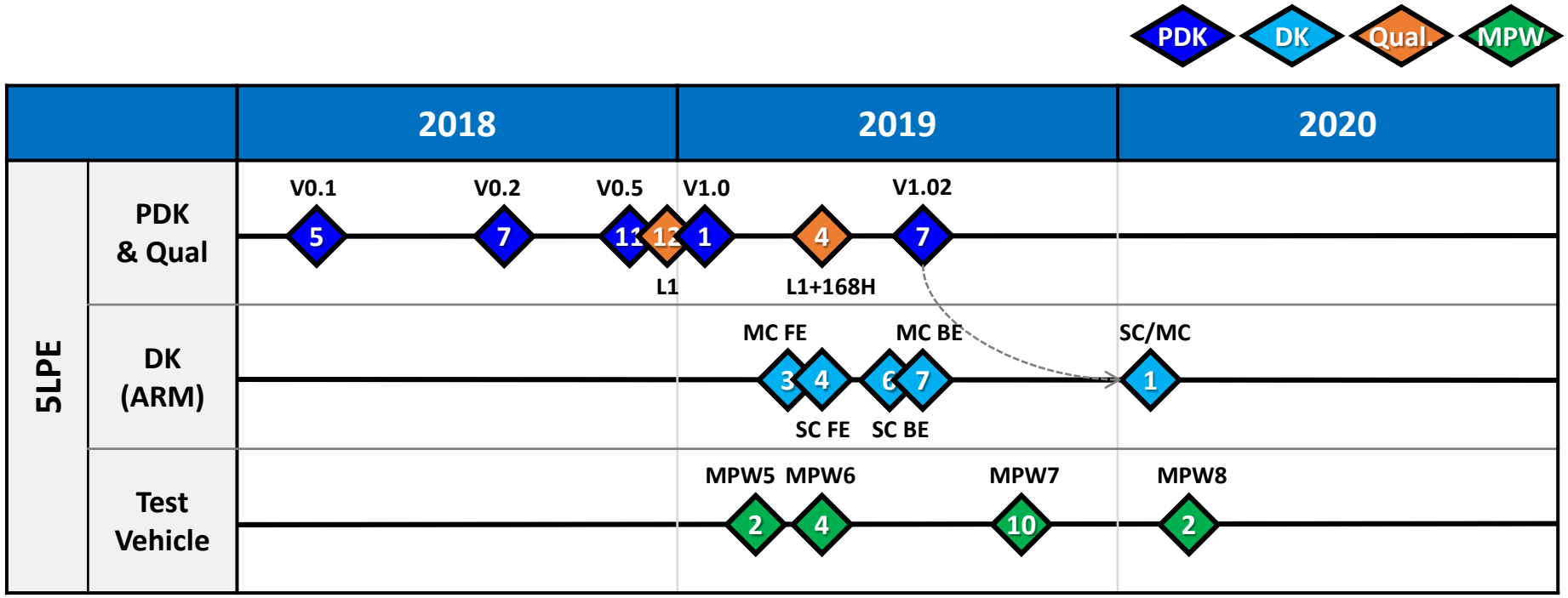
5LPE Availability

Key milestones

- **PDK v1.0: Released Jan'19**
- **L1+168H: Completed Apr. '19**
- **MPW MTO: Feb'19**



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Samsung Advanced Foundry Ecosystem

Join us!

9am – 7pm
October 17, 2019
SAMSUNG@FIRST CAMPUS

REGISTER NOW!:
https://events.samsungatfirst.com/foundry-safe-forum-2019/

High-Performance 5LPE Implementation Next-Generation Arm “Hercules” CPU

Fakhruddin Ali Bohra
Senior Principal Design Engineer
Arm

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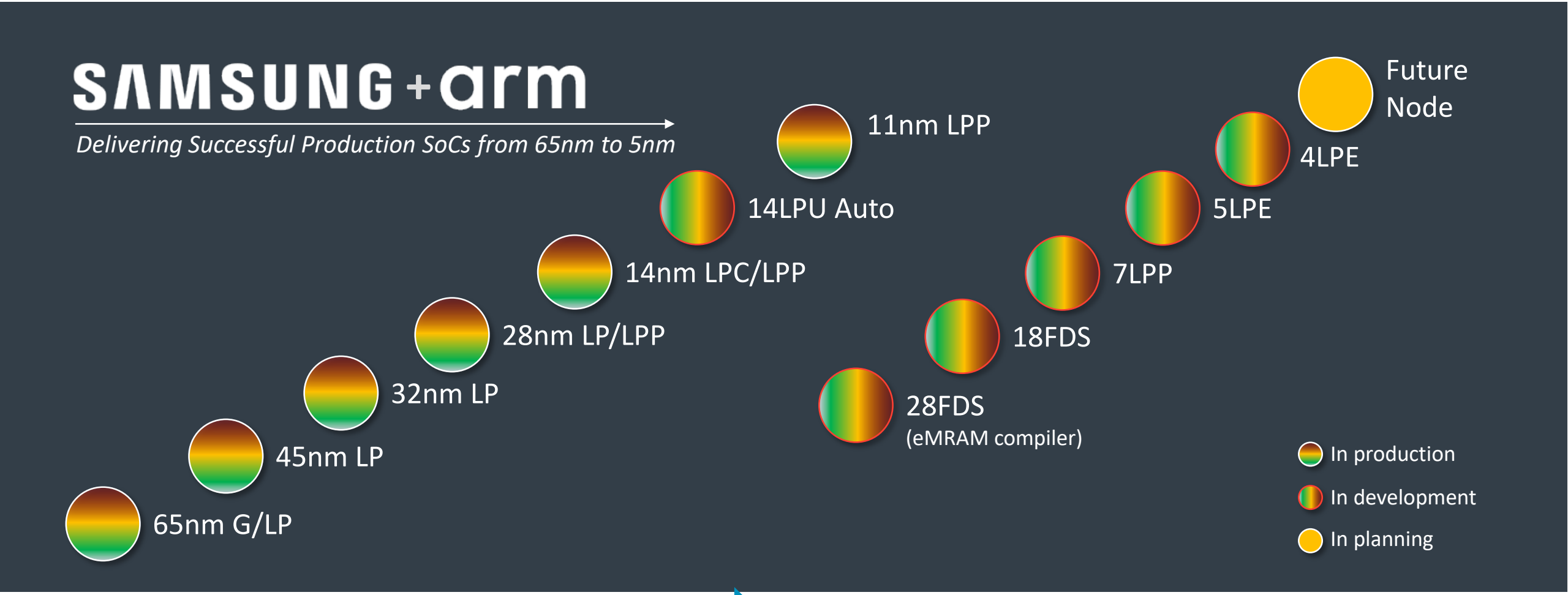
Arm Artisan Physical IP and Samsung Foundry Partnership

Over 3 billion chips shipped with Arm Artisan Physical IP



Arm Artisan on Samsung Foundry 5LPE (EUV) Platform

Standard Cell
- Comprehensive cell set for broad application coverage
- 7.5 & 6 UHD Track Library
- Power management & ECO

Memory Compiler
- 8 memory compilers
- Low VDD assist features
- Multi periphery Vt options
- Extensive features set

GPIO
- GPIO 1.8V
- GPIO 3.3V

Architect
- Logic libraries
- Memory compiler

POP™ IP
- Cortex-A76
- Cortex-A55
- Hercules
- All POP with DynamIQ™

Complete Physical IP Platform

- **Foundry sponsored** foundation IP Support wide range of applications from mobile, consumer and automotive
- POP IP for “Hercules” CPU, Arm® Cortex®-A76 and Cortex-A55 based computing systems
- Design kits available

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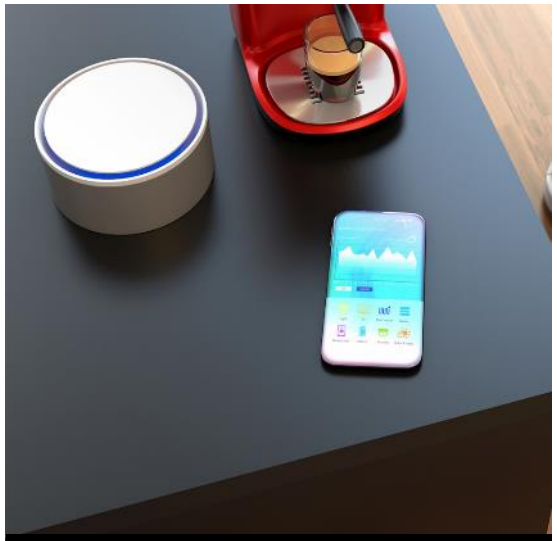
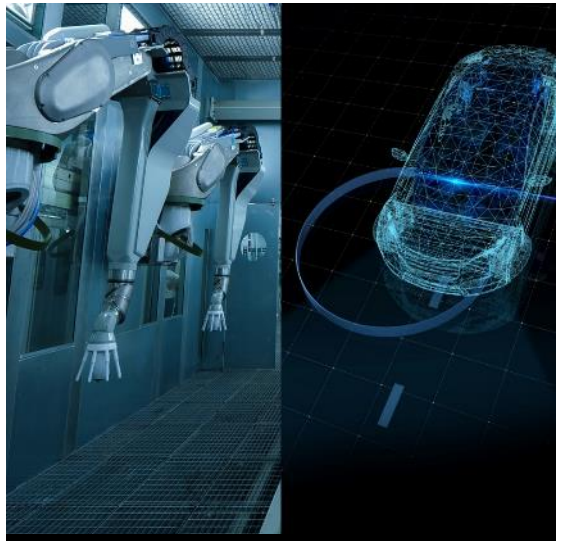
Technology Trends that Will Redefine All Industries



Artificial Intelligence in every device



Autonomous machines

Augmented reality

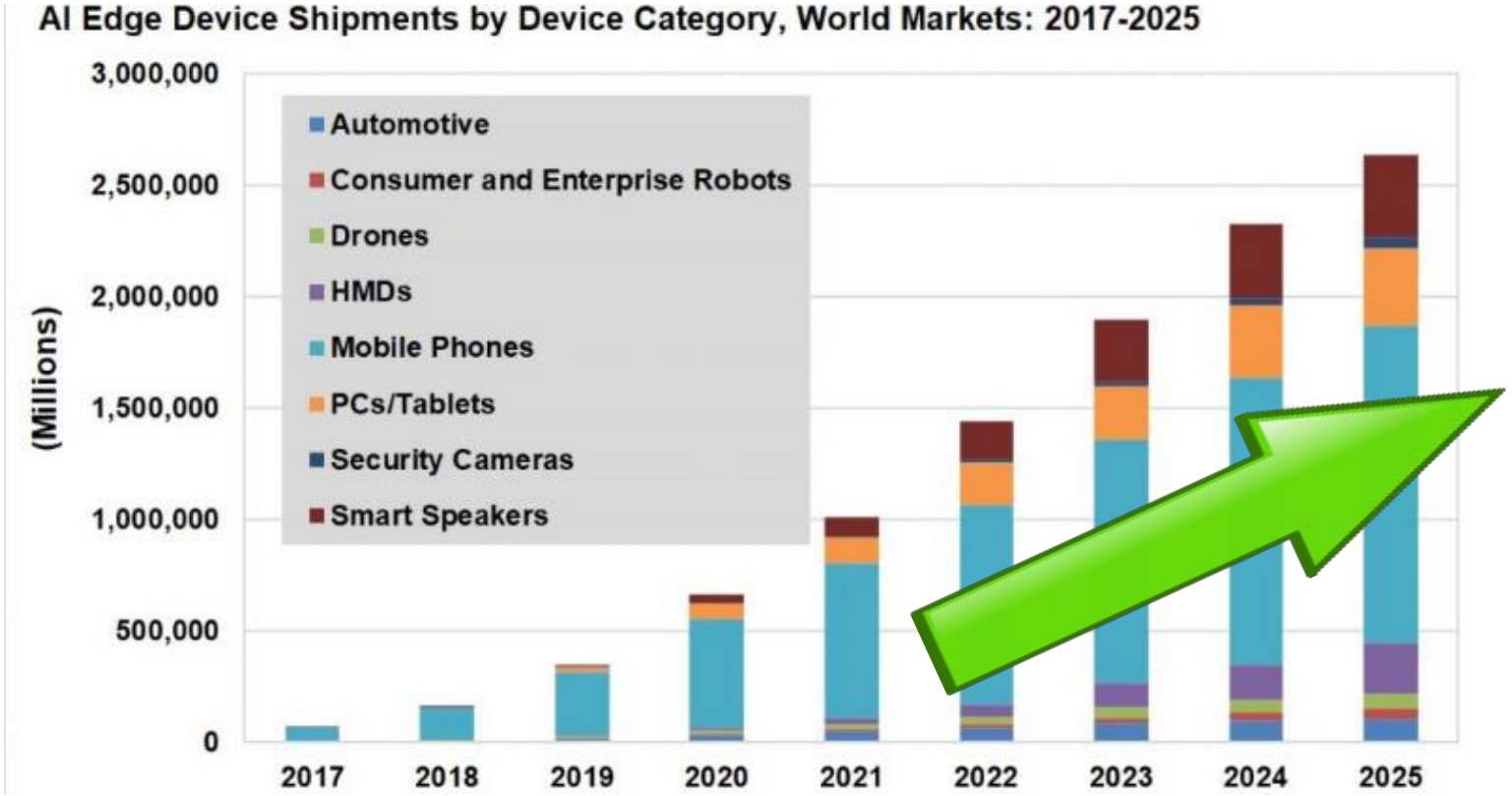
Hyperscale cloud and connectivity

Security and Privacy

AI is Everywhere

Industry landscape: What trends will drive the industry

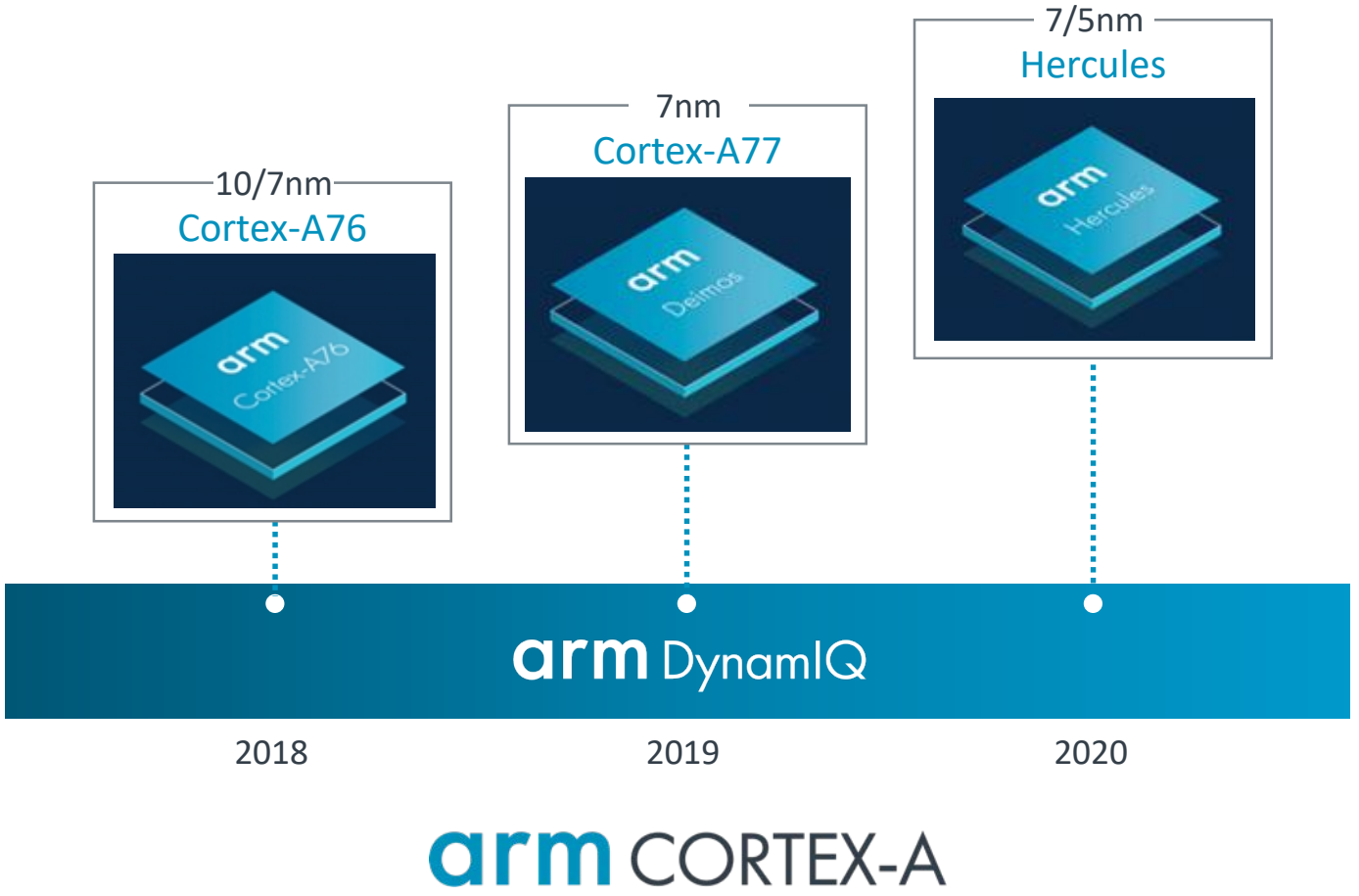
- AI cuts across applications spaces
- Projected continued growth across all applications



Source : Tractica (2018)

Breakthrough Performance for Always-On, Always-Connected

Continuing the trajectory of increased compute performance for AI, ML and premium mobile



- **Cortex-A76: High-performance implementation: 3+ GHz in 7nm**
- **Cortex-A77: Up to 20% improved IPC performance**
- **Hercules: Continuing performance and efficiency leadership**
- **Supports the flexibility of Arm DynamIQ big.LITTLE™**

Translating Arm RTL Benefits into Silicon

HOW TO

Translate the year-over-year **performance improvements of >15%** for compute through 2020 in silicon

?

Optimize implementation for new cores and advanced process nodes

?

Ensure **fast turn-around time** such that increased productivity of new Arm cores

?

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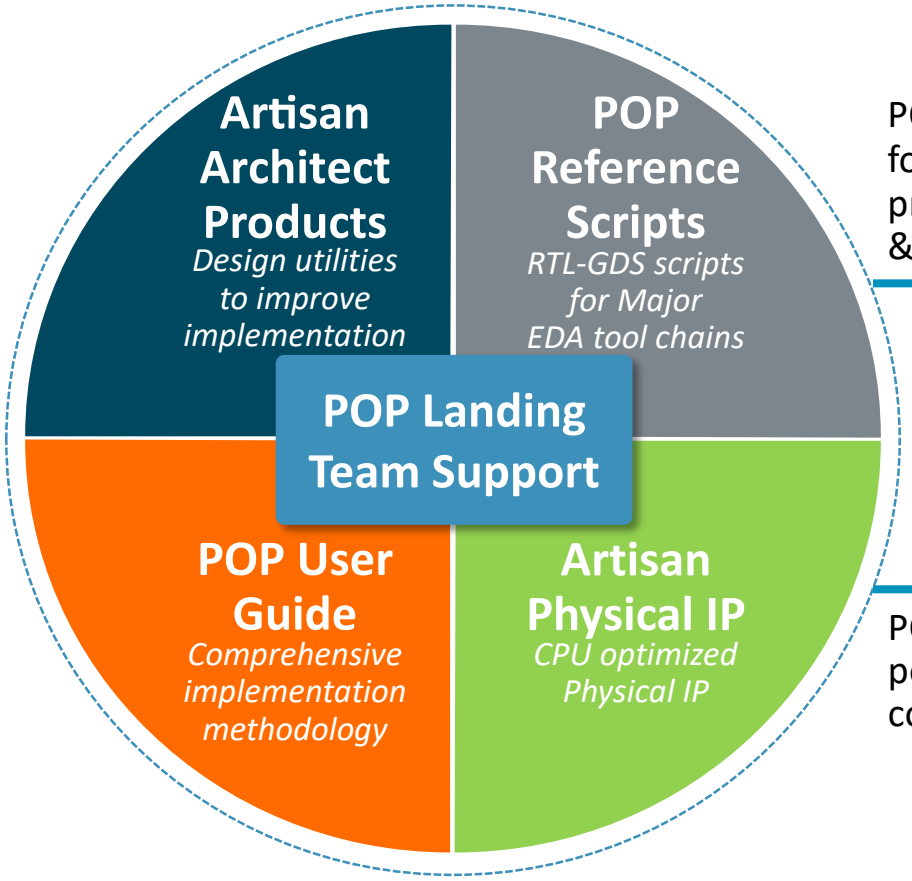
Arm POP IP is Optimized Arm Core Implementation

POP IP Components



POP is available for major foundries producing on 28nm & more advanced nodes

SAMSUNG FOUNDRY
and other foundries

POP achieves the best possible PPA for Arm cores

arm NEOVERSE
arm CORTEX-A
arm MALI
arm ARTISAN

Comprehensive support and services

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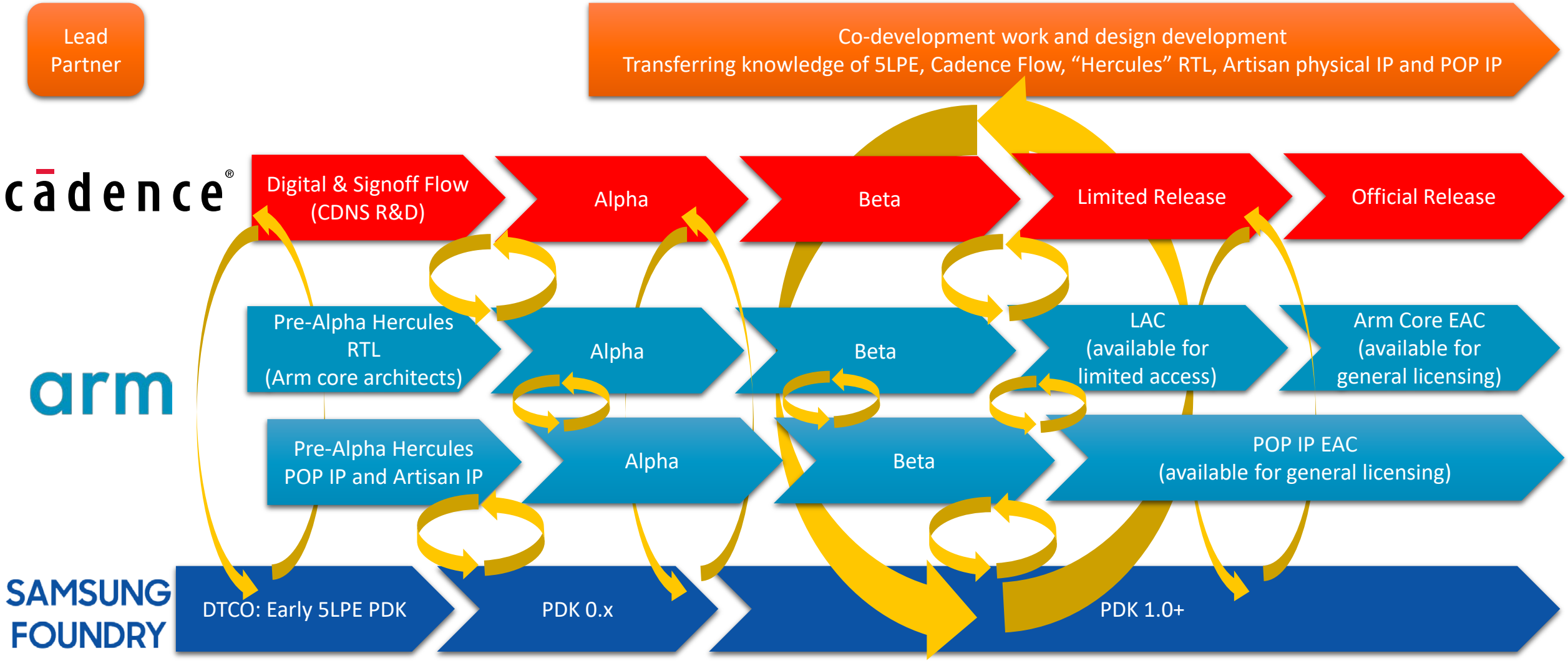
Design Technology Co-Optimization (DTCO) Benefits the Ecosystem

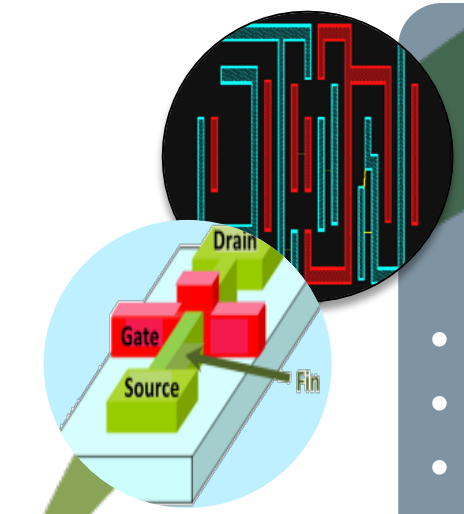


Alignment of Arm and Cadence product developments and process may vary by process maturity; iterative references may vary

Implementation Challenges

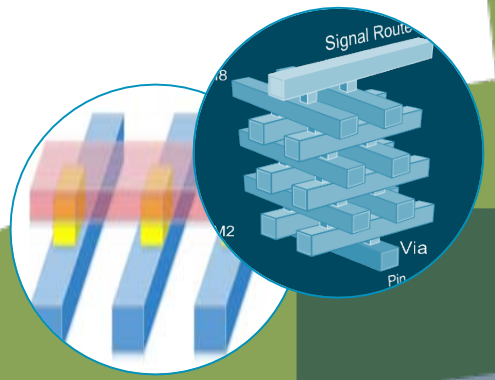
Challenges present for advanced nodes and cores

Advanced nodes



14nm

- FinFETs
- Placement rules
- DPT-aware colorless routing



5nm

- Via ladders
- New placement rules
- Power grid challenges
- Addressing variation

Latest Arm Cores

- Concurrent configuration of CPU with DynamIQ Shared Unit (DSU)
- Asynchronous configuration
- Long channels between DSU and CPU slaves
- Private L2 cache
- Architectural clock gating

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5LPE: Continued Enhancements for Artisan Logic IP

Performance

- New compressor cells
- New flip-flops: 30% performance gain per cell level

Power

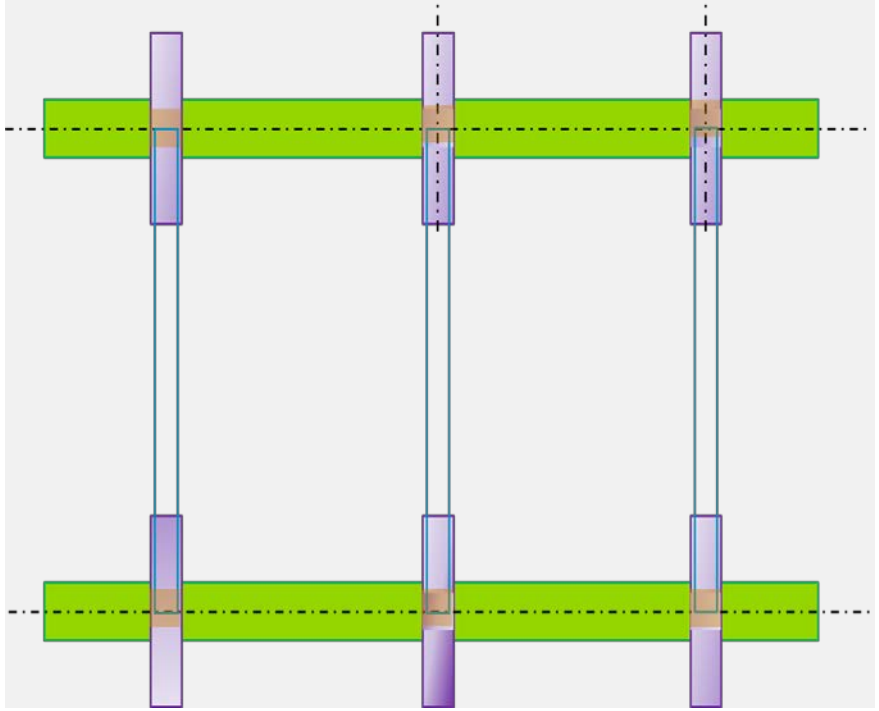
- New multi-bit functional cells
- Low power flip-flops

Density

- Key combinatorial cells: 5-10% area gains per cell level
- Flip-flops: 10+% area gains per cell level

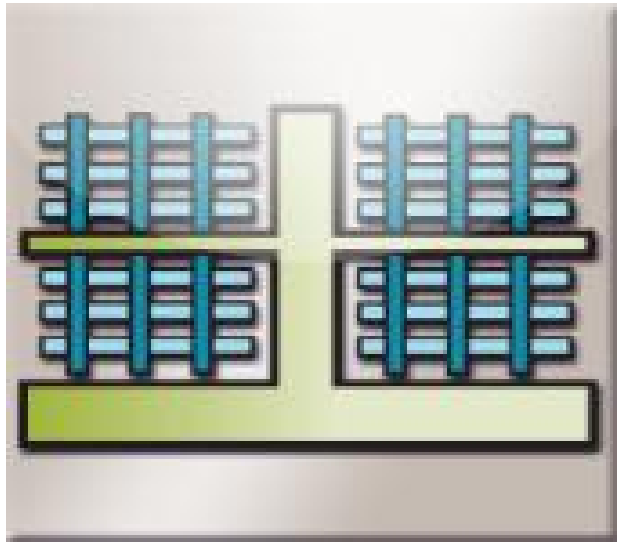
Implementation

- Cells crafted to enable flexible cell placement while maintaining a tight and regular lower grid
- Utilities included to ease power grid generation
- Post-route opportunistic M2 stitching supported to improve EM/IR drop
- Large clock drivers for ideal H-Tree implementation
- Power gate design ensures no break in grid regularity



Dependencies exists between standard cell architecture & power grid;
Proper grid required for optimization

5LPE: Continued Enhancements for Artisan Memory IP



Performance

- Special optimization for key compilers
- Bitcell selection to match 5LPE target markets
- Multiple level shifting options for optimized DVFS at SOC level
- Careful wireplaning to mitigate RC

Power

- Compile-time options for core and periphery separation, control, retention and power down
- Multiple architecture and micro architecture changes

Density

- Extensive MUX, bank and slice options
- Innovative assist scheme
- Newer topological options

Implementation

- Instance layout minimizes placement and abutment restrictions

High-Performance 5LPE Implementation Next-Generation Arm “Hercules” CPU

Edson Gomersall
Product Engineering Architect
Cadence

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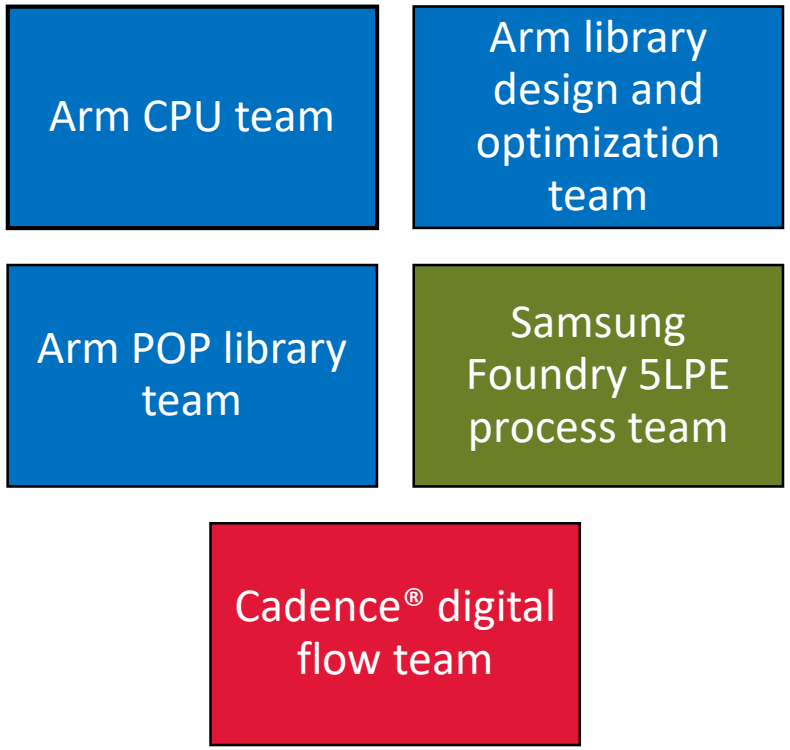
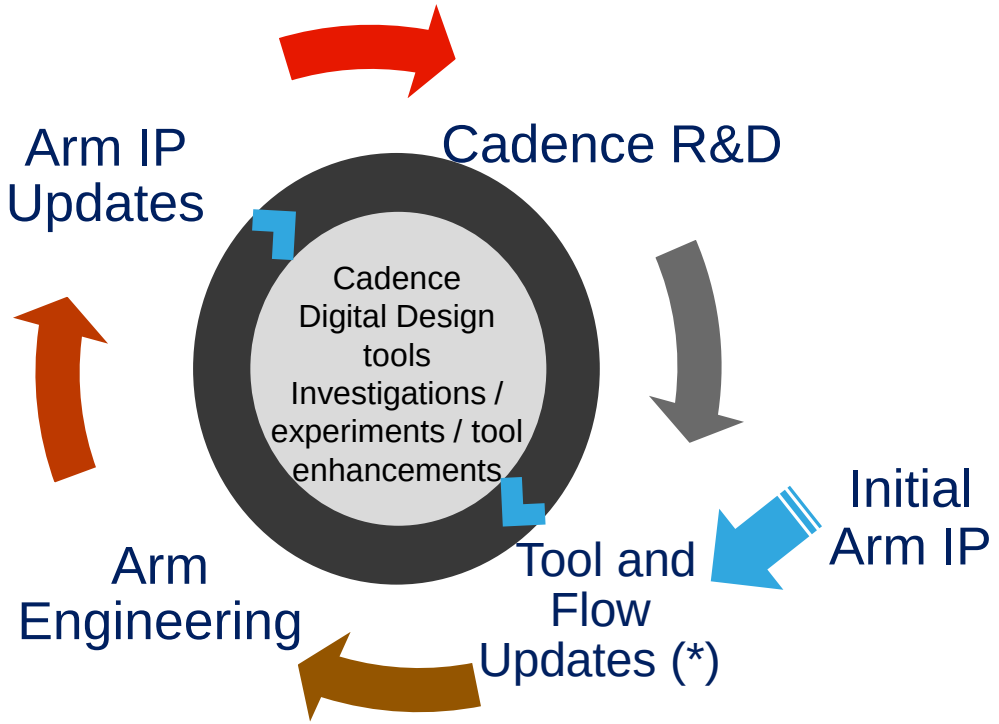
Cadence, Arm, and Samsung Foundry Collaboration

- Worldwide engineering relationship

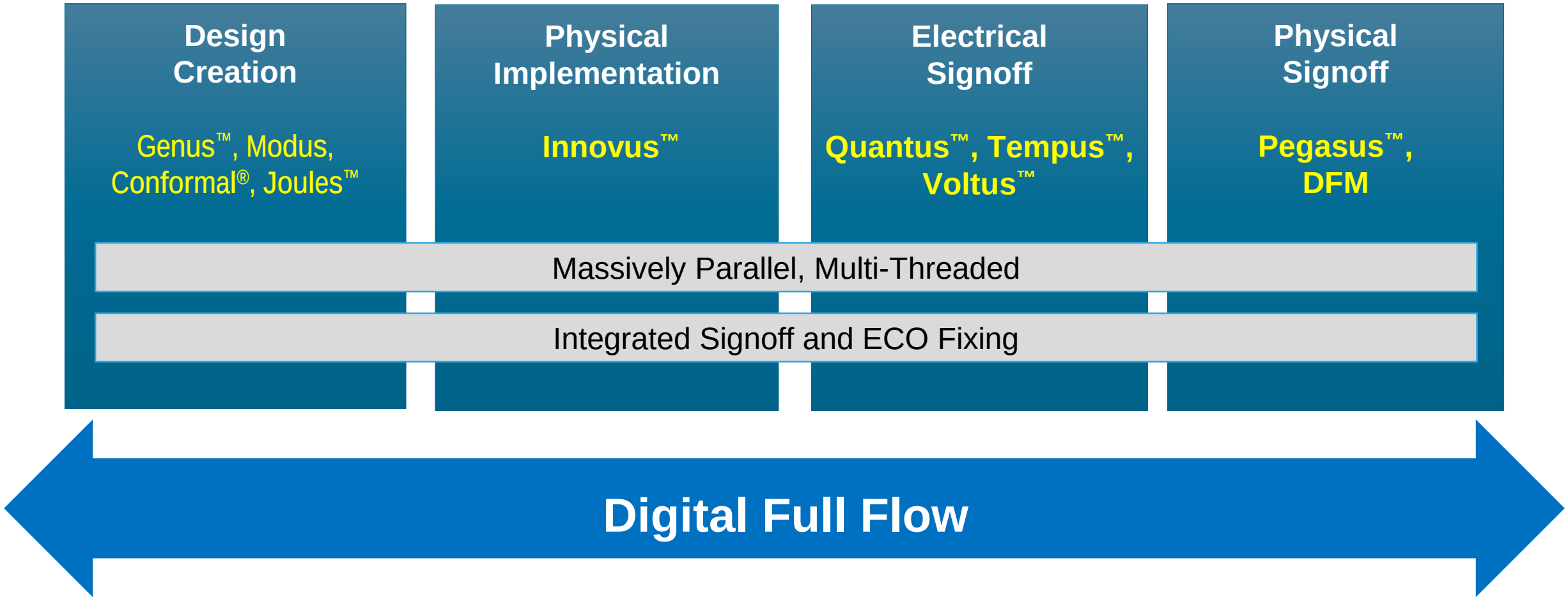




- Collaboration enables high-performance flow to be delivered

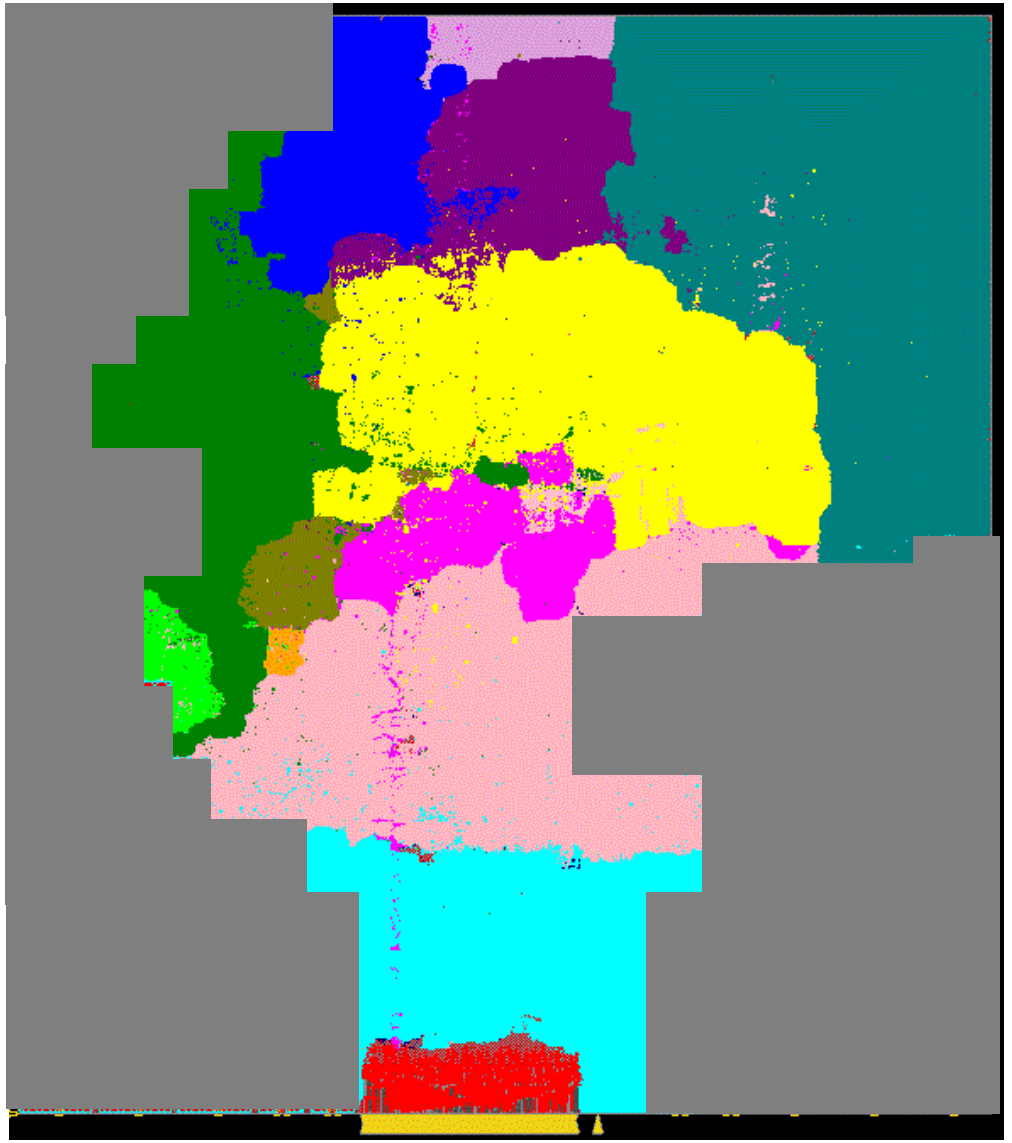
(*) Early collaboration ensures tool support in place

Arm CPU 5LPE Digital and Signoff Flow



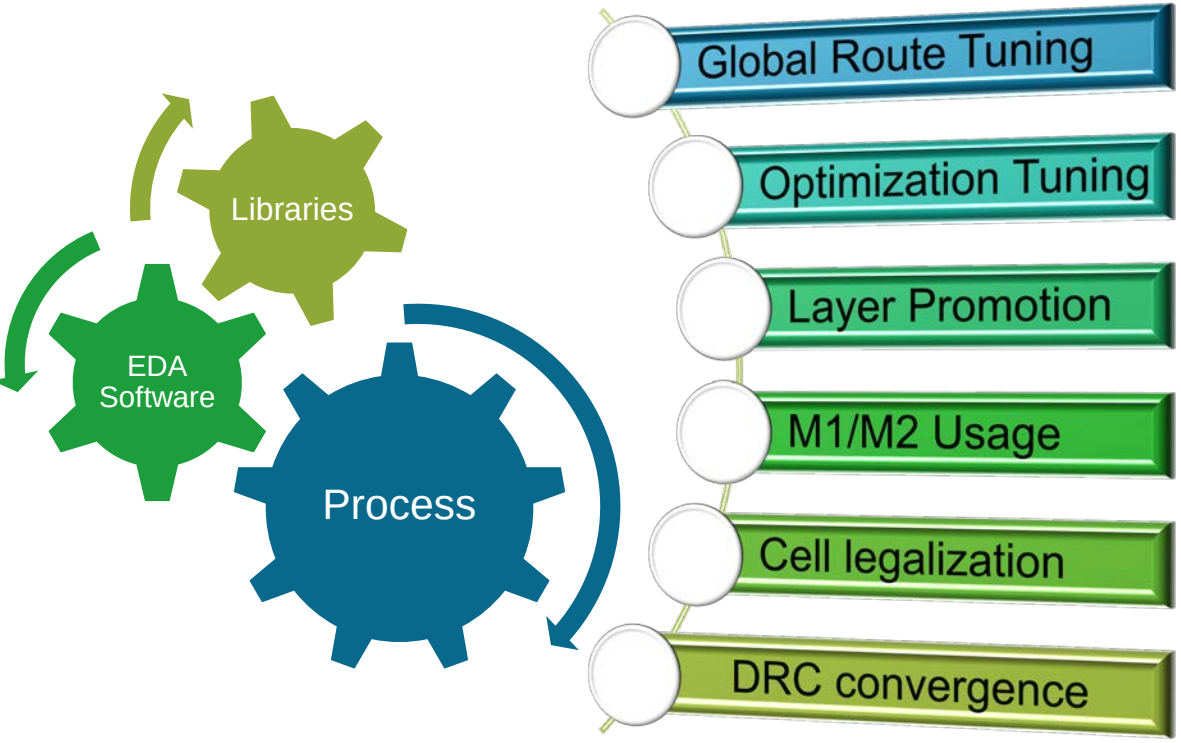
Arm CPU 5LPE Design Configuration

- Process
  - Samsung Foundry 5LPE
  - 13 Layer Metal stack
- CPU Core Overview
  - Arm CPU 5LPE POP 7.5T standard cells
  - Arm CPU 5LPE POP FCI memories
  - Arm CPU floorplan
- Multiple voltage islands



Cadence and Samsung Foundry 5LPE Co-Optimization

5LPE Process and Tool Co-Optimization



- One simple option to enable all 5LPE process support

```
setDesignMode -process 5 -node S5
```

Metric	After eGR tuning
Frequency	14% improvement
Utilization	7% improvement

Early Global Route Tuning

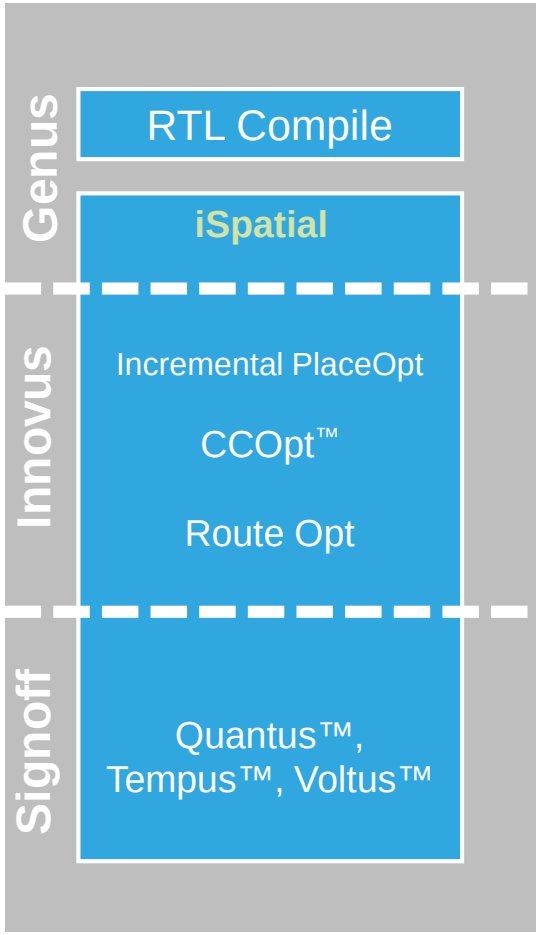
	M4	D5	D6	D7	D10
Before tuning	80.5	77.9	84.2	51.5	43.2
After tuning	81.4	79.7	85.5	52.7	61.3

Layer Promotion Adherence

Out-of-Box Better Full Flow PPA

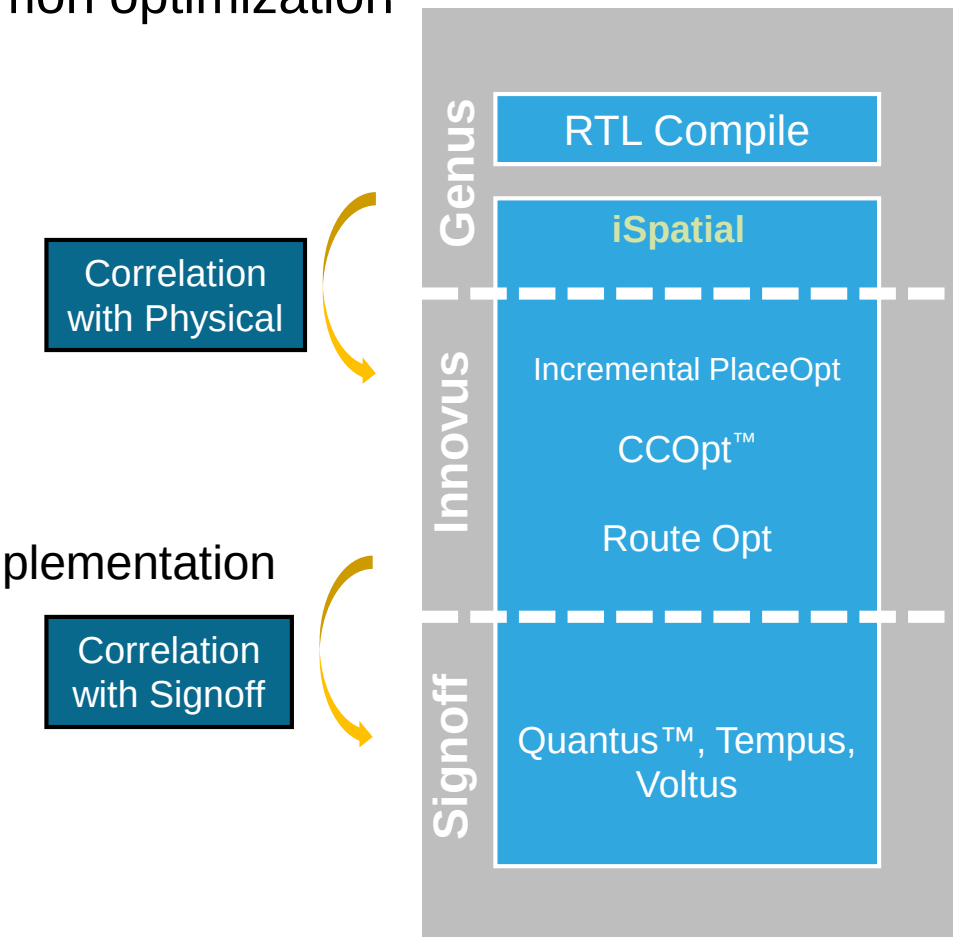
5LPE and CPU Characteristic Driven Features

5LPE-driven features	CPU-driven features
Early global route tuning	Floorplan regions/guides
Layer promotion	ICG placement optimization
NDRs for specific layers	Custom cost groups
Cell legalization	Strategic pre-skewing
Statistical Via support	Clock tuning



Cadence Digital Flow Benefits

- Combined Genus™ and Innovus™ solution with common optimization
  - **iSpatial** technology
  - **2x** TAT improvement, **5%** PPA benefit
- IR drop-aware flow
  - Integrated IR drop repair flow
- True signoff
  - Completely integrated with industry-leading Innovus Implementation System
  - **Tempus™** and **Voltus™** **solutions** combined is TRUE SIGNOFF
  - Via variation-aware timing signoff
- Stylus common UI
  - Usability and productivity enabler



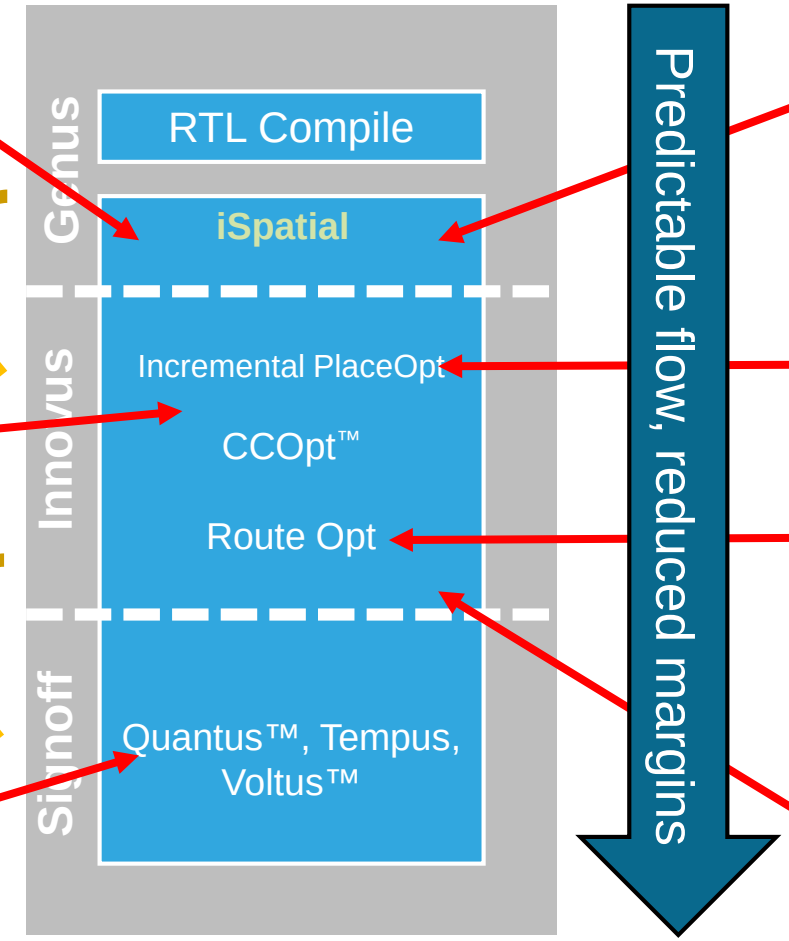
Arm CPU 5LPE iSpatial High-Performance Flow

Turn-around time and predictability benefits

- Placement regions/guides used in floorplan
- Custom cost groups

- Strategic global route layer promotion
- Extreme effort optimization

- Tempus ECO signoff-driven design closure
- Statistical Via modeling



Predictable flow, reduced margins

- Physically-aware synthesis
- Early clock tree during synthesis
- Multi-bit cell optimization

- IR-aware placement and optimization

- Timing- and power-driven routing

- Opportunistic via pillars and non-default-rules
- Post-route useful skew

Mesh and Flex-H clock distribution supported which can influence design performance

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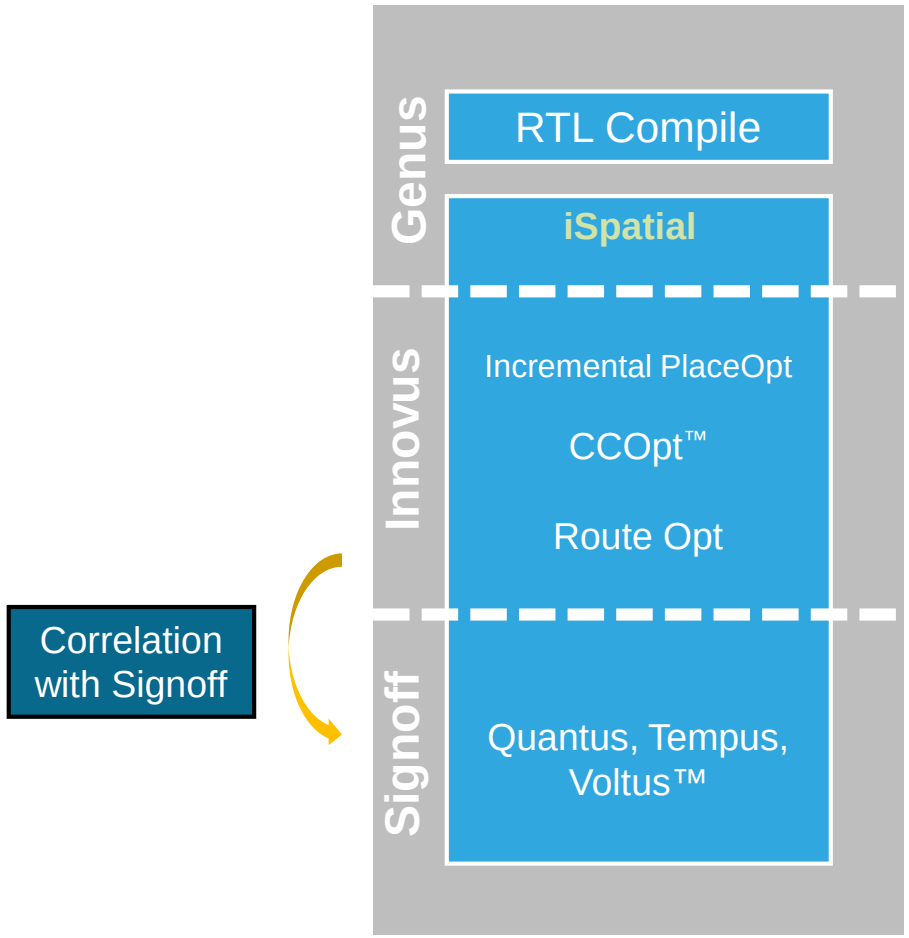
5LPE Statistical Via Timing Analysis and Optimization



- Exclusive feature used in 5LPE signoff flow
- Global Via resistance variation modelled in extraction technology files
- Local Via resistance variation is modelled statistically by the foundry
  - Samsung Foundry provides mean shift and standard deviation of via cut sizes
  - Quantus™ Extraction provides via resistance for each via
- Tempus™ delay calculation engine uses both global and local resistance variation to ensure timing convergence during the flow
  - Part of the Samsung Foundry 5LPE signoff requirements
- Tempus ECO optimization accounts for all Via resistance effects

Concurrent Timing, Power, and IR Drop Optimization

Innovus, Tempus, Voltus single data model integration

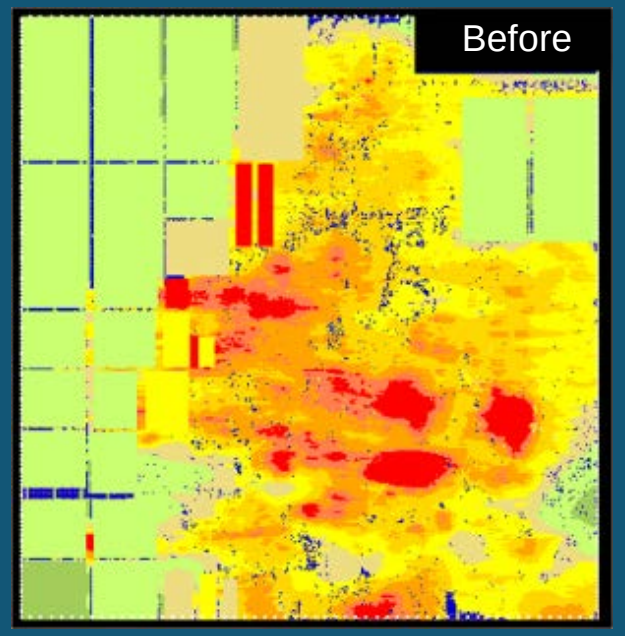
Multi-Stage IR Correction

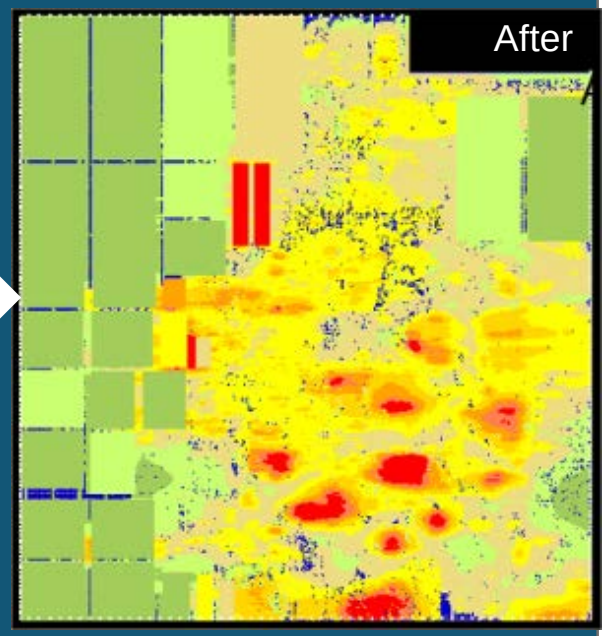
Genus
- RTL Compile
- iSpatial

Innovus
- Incremental PlaceOpt
- CCOpt™
- Route Opt

Signoff
- Quantus™, Tempus™, Voltus™

- **Early Rail Analysis**
- **IR Drop-Aware Placement**
- **Clock Useful Skew for Peak Power**
- **Power Routing and Via Optimization**
- **Timing And IR Drop-Aware ECO**





	IR drop victims	Peak IR drop voltage
Before	1334	110.5 mV
After	87	81.9 mV

93% fewer victims

No set-up/hold degradation

26% less peak IR

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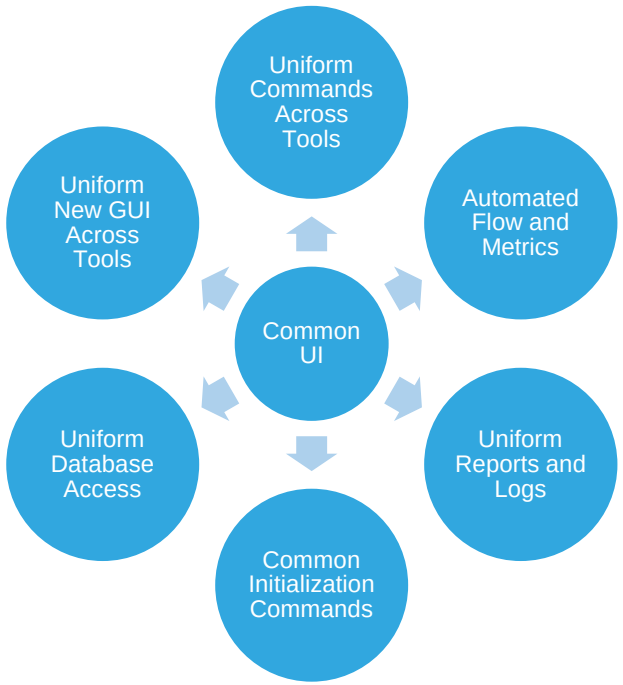
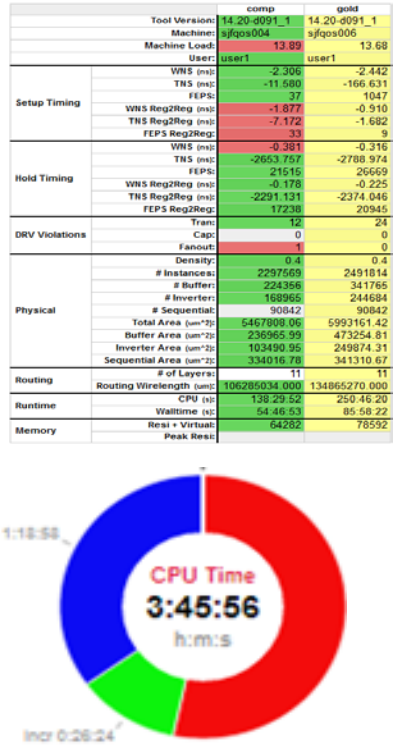
Full-Flow Unified Interface and Flow for Digital Implementation

Common User Interface

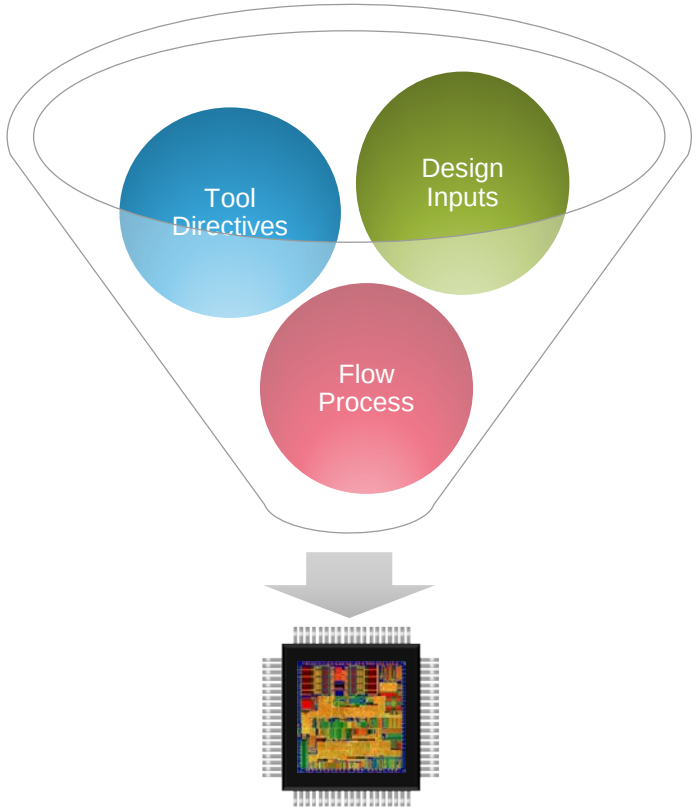


Unified Metrics



		comp	gold
	Tool Version:	14.20-d091_1	14.20-d091_1
	Machine:	sjfqos004	sjfqos006
	Machine Load:	13.89	13.68
	User:	user1	user1
Setup Timing	WNS (ns):	-2.306	-2.442
	TNS (ns):	-11.580	-166.631
	FEPS:	37	1047
	WNS Reg2Reg (ns):	-1.877	-0.910
	TNS Reg2Reg (ns):	-7.172	-1.682
	FEPS Reg2Reg:	33	9
Hold Timing	WNS (ns):	-0.381	-0.316
	TNS (ns):	-2653.757	-2788.974
	FEPS:	21515	26669
	WNS Reg2Reg (ns):	-0.178	-0.225
	TNS Reg2Reg (ns):	-2291.131	-2374.046
	FEPS Reg2Reg:	17238	20945
DRV Violations	Tran:	12	24
	Cap:	0	0
	Fanout:	1	0
Physical	Density:	0.4	0.4
	# Instances:	2297569	2491814
	# Buffer:	224356	341765
	# Inverter:	168965	244684
	# Sequential:	90842	90842
	Total Area (um^2):	5467808.06	5993161.42
	Buffer Area (um^2):	236965.99	473254.81
	Inverter Area (um^2):	103490.95	249874.31
	Sequential Area (um^2):	334016.78	341310.67
Routing	# of Layers:	11	11
	Routing Wirelength (um):	106285034.000	134865270.000
Runtime	CPU (s):	138:29:52	250:46:20
	Walltime (s):	54:46:53	85:58:22
Memory	Resi + Virtual:	64282	78592
	Peak Resi:		

Flow Capture and Automation



- Joules™ RTL Power Analysis
- Genus™ Synthesis
- Modus DFT
- Conformal LEC
- Innovus™ Implementation
- Quantus™ Extraction
- Tempus™ Timing
- Voltus™ Power
- Pegasus™ Verification

Improved ease of use and designer productivity

Consistent PPA reporting across the whole digital flow

Quickly capture digital flows and deploy to users

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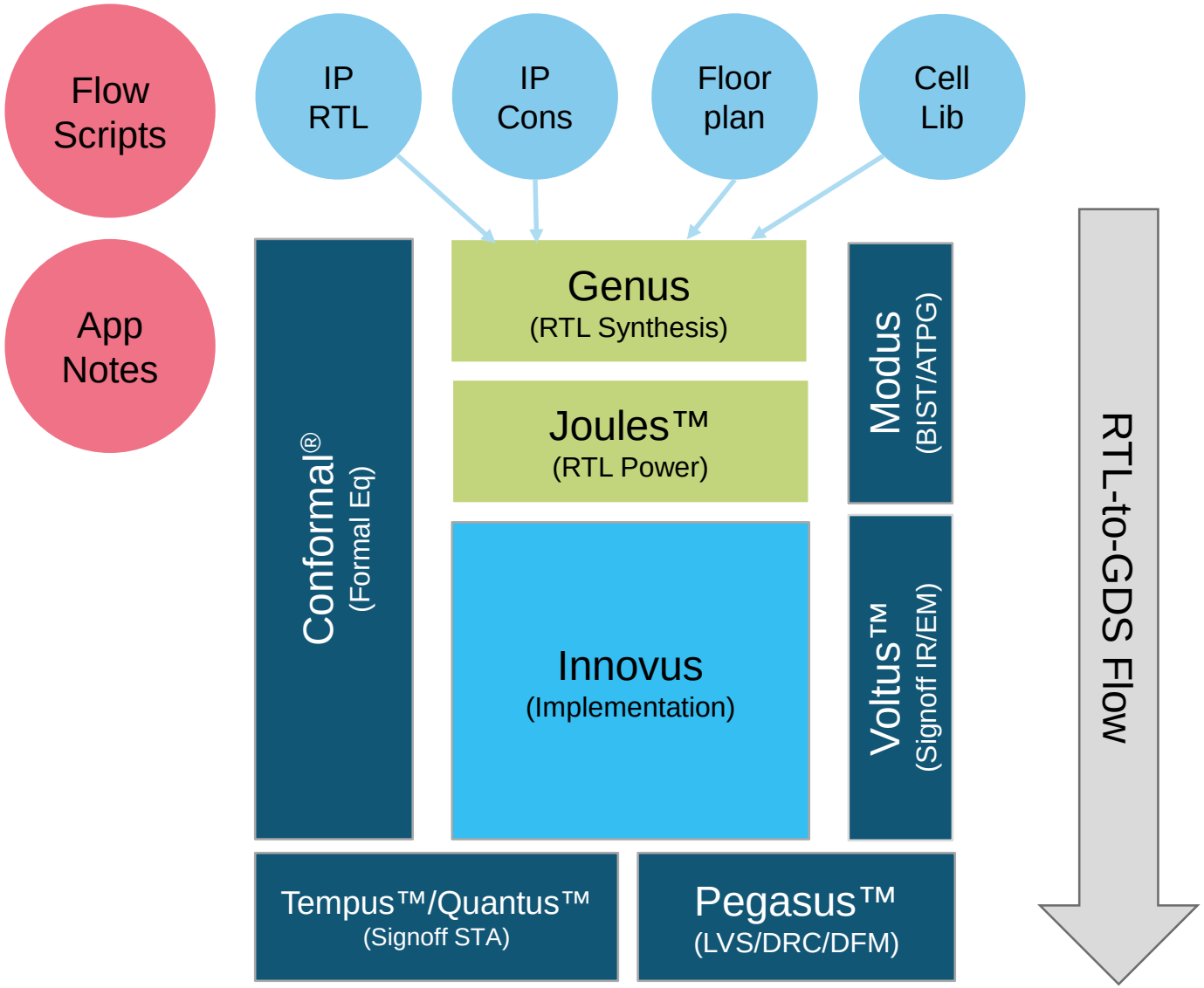
Arm CPU 5LPE High-Performance Rapid Adoption Kit



- Complete Cadence RTL-to-GDS digital implementation flow
  - Example flow scripts
  - Example floorplan
  - Application note explaining how to setup the RAK
  - Application notes showing how the flow works
- Customized for latest advanced Arm CPU and Samsung Foundry 5LPE process
- Available to customers enabling fast implementation of latest Arm CPU

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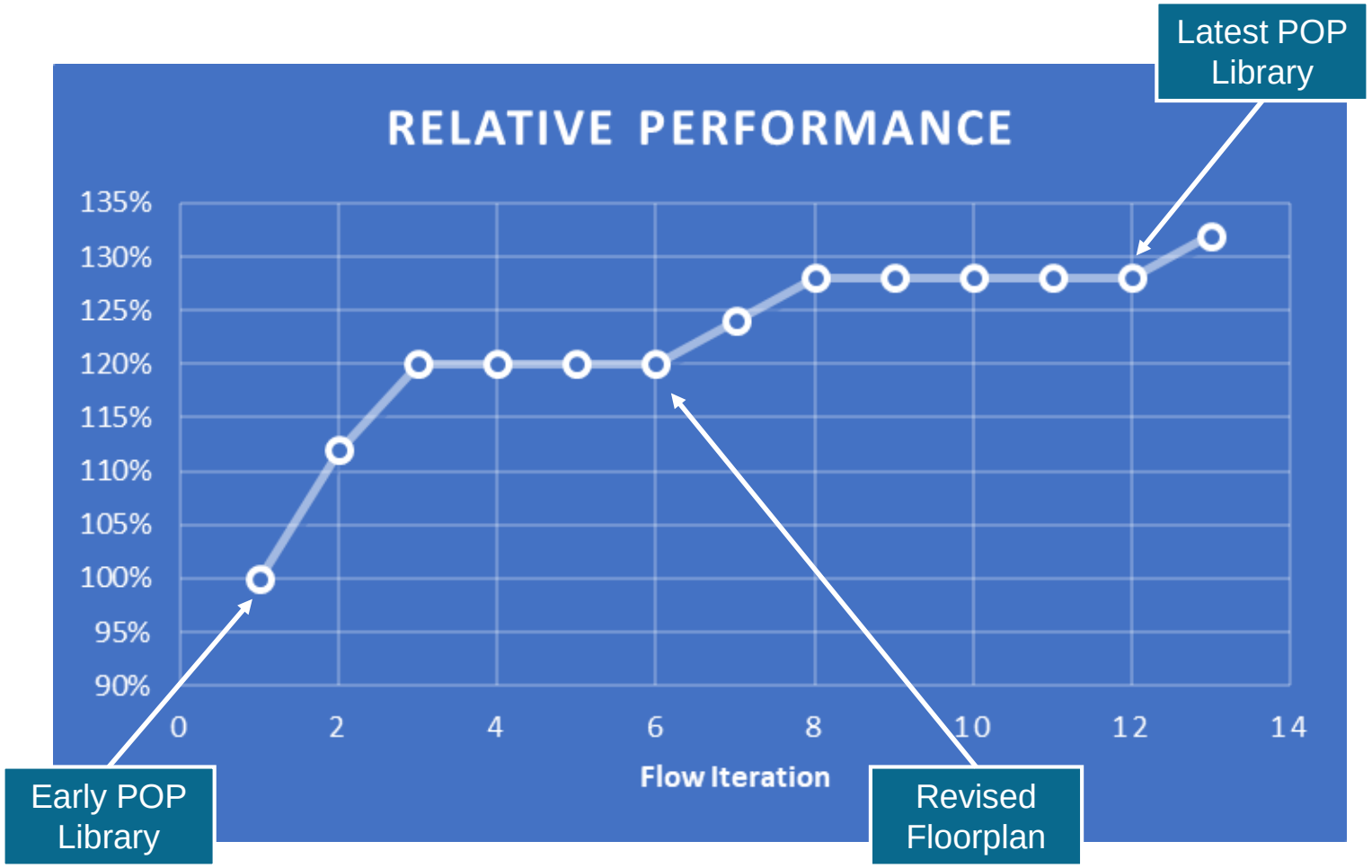
Arm Advanced CPU 5LPE High-Performance RAK Results



- Arm, Samsung Foundry, and Cadence working together have enabled over 30% performance improvements
- More to come as collaboration continues
- Customers have immediate access to improved results using RAK

Over 30% performance improvement achieved so far .. More to come

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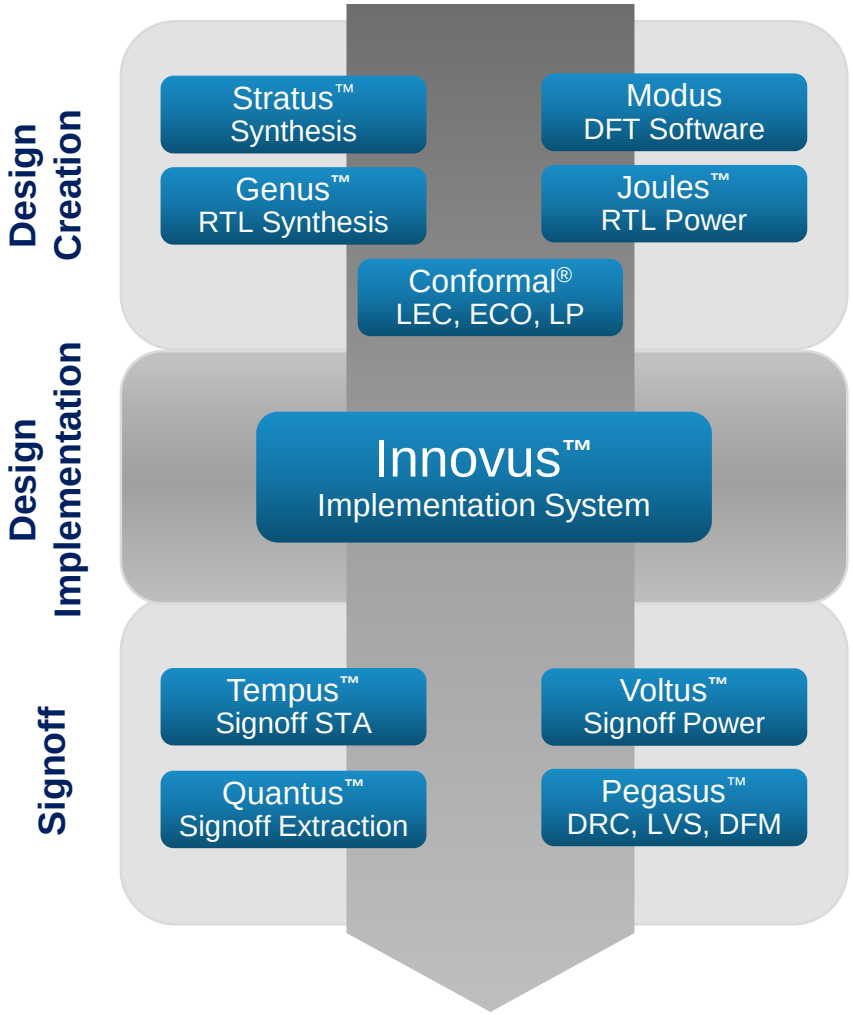
Delivering Design Excellence for 5LPE Arm CPU Implementation



- Complete Cadence high-performance digital implementation and signoff flow
- Fully qualified for Samsung Foundry 5LPE
  - 5LPE process and tool co-optimization
  - One simple command to enable 5LPE set-up
  - 5LPE Statistical Via Timing Analysis and Optimization
- Tuned and proven on Arm high-performance CPU and POP library for outstanding PPA
- Common user interface and FlowKit included as part of Rapid Adoption Kit

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