High Volume Semiconductor Manufacturing using Nanoimprint Lithography

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ABSTRACT

Nanoimprint lithography manufacturing equipment utilizes a patterning technology that involves the field-by-field deposition and exposure of a low viscosity resist deposited by jetting technology onto the substrate. The patterned mask is lowered into the fluid which then quickly flows into the relief patterns in the mask by capillary action. Following this filling step, the resist is crosslinked under UV radiation, and then the mask is removed, leaving a patterned resist on the substrate. The technology faithfully reproduces patterns with a higher resolution and greater uniformity compared to those produced by photolithography equipment. Additionally, as this technology does not require an array of wide-diameter lenses and the expensive light sources necessary for advanced photolithography equipment, NIL equipment achieves a simpler, more compact design, allowing for multiple units to be clustered together for increased productivity.

In this paper, we review the progress and status of the FPA-1200NZ2C wafer imprint system and FPA-1100NR2 mask replication system. To address high volume manufacturing concerns, an FPA-1200NZ2C four-station cluster tool is used in order to meet throughput and cost of ownership requirements (CoO). Throughputs of up to 90 wafers per hour were achieved by applying a multi-field dispense method. Mask life of up to 125 lots, using a contact hole test mask were demonstrated. A mix and match overlay of 3.4 nm has also been achieved and a single machine overlay across the wafer of 2.1nm in X, 1.9nm in Y was also demonstrated.

In addition, data is also presented on mask replication. Critical elements of a replication platform include image placement (IP) accuracy and critical dimension uniformity (CDU). Data is presented on both of these subjects. With respect to image placement, an IP accuracy (after removing correctables) of 0.8nm in X, 1.0nm in Y has been demonstrated.

Keywords: Nanoimprint Lithography, NIL, CoO, defectivity, throughput, overlay, image placement accuracy, mask replication

1. INTRODUCTION

Imprint lithography is an effective and well known technique for replication of nano-scale features.[1,2] Nanoimprint lithography (NIL) manufacturing equipment utilizes a patterning technology that involves the field-by-field deposition and exposure of a low viscosity resist deposited by jetting technology onto the substrate.[3-9] The patterned mask is lowered into the fluid which then quickly flows into the relief patterns in the mask by capillary action. Following this filling step, the resist is crosslinked under UV radiation, and then the mask is removed, leaving a patterned resist on the substrate. The technology faithfully reproduces patterns with a higher resolution and greater uniformity compared to those produced by photolithography equipment. Additionally, as this technology does not require an array of wide-diameter lenses and the expensive light sources necessary for advanced photolithography equipment, NIL equipment achieves a simpler, more compact design, allowing for multiple units to be clustered together for increased productivity.

Previous studies have demonstrated NIL resolution better than 10nm, making the technology suitable for the printing of several generations of critical memory levels with a single mask. In addition, resist is applied only where necessary, thereby eliminating material waste. Given that there are no complicated optics in the imprint system, the

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reduction in the cost of the tool, when combined with simple single level processing and zero waste leads to a cost model that is very compelling for semiconductor memory applications.

There are many other criteria besides resolution that determine whether a particular technology is ready for manufacturing. With respect to the imprint stepper, both critical dimension uniformity (CDU) and line edge roughness meet the criteria of 2nm. A collaboration partner achieved overlay of 10nm (with a target of 8nm) and defect levels ~ 5/cm^2 across a lot of 25 wafers.[10] Other criteria specific to any lithographic process include throughput, which plays a strong role in determining whether CoO requirements can be met. Recently, Takeishi and Sreenivasan reported that a throughput of 40 wafers per hour was achieved on a four-station imprint tool.[11]

On the mask side, there are stringent criteria for imprint mask defectivity, critical dimension uniformity (CDU), image placement (IP) and imprint defectivity. Semiconductor requirements dictate the need for a well-defined form factor for both master and replica masks which is also compatible with the existing mask infrastructure established for the 6025 semi standard, 6" x 6" x 0.25" photo masks. Complying with this standard provides the necessary tooling needed for mask fabrication processes, cleaning, metrology, and inspection. The master mask blank, which consists of a thin (< 10nm) layer of chromium on the 6" x 6" x 0.25" fused silica was recently reported to have a defectivity of only 0.04/cm^2 as measured by a Lasertec tool with 50 nm sensitivity.[12]

The replica form factor has additional features specific to imprinting such as a pre-patterned mesa. In 2012, an MR-5000 mask replication tool was developed specifically to pattern 6" x 6" x 0.25" replica masks from an e-beam written master. Previous work by Ichimura et al. using this tool, demonstrated that a CDU of less than 1.5nm 3-sigma can be achieved on both the master and replica masks.[13]

As the most aggressive features in advanced memory designs continue to shrink below 15 or 16 nm (towards 1Z nm), the cost of fabricating these devices increases because of the large number of additional deposition, etch and lithographic steps necessary when using immersion lithography.[14] NIL offers a more attractive CoO than competing technologies. Cost benefits can be realized by:

- Enabling direct printing of the features of interest, without the need for multiple patterning techniques.
- Improved mask life that allows a replica mask to be used for more than 2000 wafers.
- By improving the throughput of the NIL tool

In this review paper, we focus on improvements to both the wafer imprint tool (with an emphasis on particle control and mask life) and the mask replication tool.

2. Wafer Nanoimprint Tool

2.1 Throughput

There are several parameters that can impact resist filling. Key parameters include resist drop volume (smaller is better), system controls (which address drop spreading after jetting), Design for Imprint or DFI (to accelerate drop spreading) and material engineering (to promote wetting between the resist and underlying adhesion layer). In addition, it is mandatory to maintain fast filling, even for edge field imprinting. Previously, we have demonstrated that it is feasible to fill dense line/space patterns in only one second.

The resist properties have a large impact on fill time and the engineering of the resist is critical for meeting performance criteria and properties such as surface tension, viscosity and wetting. Surface wetting has a strong influence on fill time. To enhance drop spreading after dispense and achieve a throughput of 80 wafers per hour, a two component resist system is used to create a surface tension gradient to drive resist flow. The approach is similar to Marangoni flow, which is driven by surface tension gradients. For additional details on this process, the reader is referred to the paper by N. Khusnatdinov et al.[15]

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To further increase throughput, a multi-field dispense (MFD) method has been developed in which resist is jetted onto several fields in order to decrease the overhead resulting from a sequential dispense and imprint process flow. The improvement to 90 wafers per hour is shown in a graph of throughput (for a four-station cluster tool) as a function of year. The next target is > 100 wafers per hour.

2.2 Overlay

The alignment and overlay system consists of various factors, which can be categorized generally as alignment and distortion. Canon uses two key systems to address overlay (Figure 1):

- A through the mask (TTM) align system and a magnification actuator system which applies force through an array of piezo actuators to correct for magnification, skew and trap errors
- A High Order Distortion Control (HODC) system which locally varies the heat within a stepper field on the wafer to correct higher order distortions.

The system has now been used to correct distortion terms up to K30.[16]

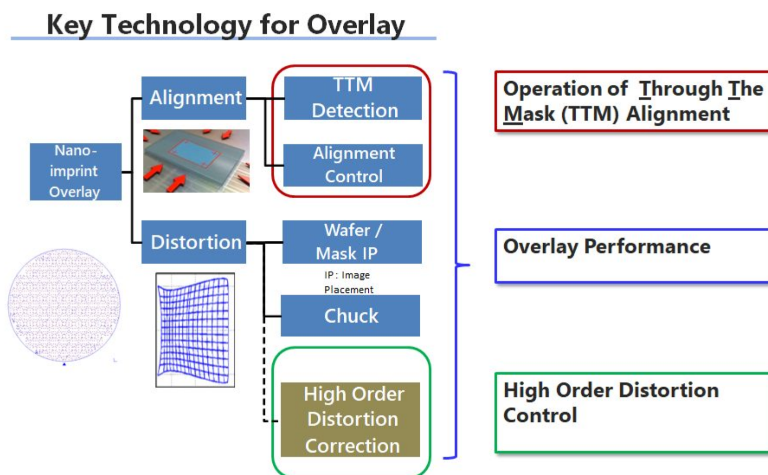

Figure 1. Schematic representation of the methodology for addressing overlay with a nanoimprint lithography tool. Key components include the TTM detection system and the HODC system.

As a final test, matched machine overlay (to an ASML ArFi scanner) and single machine overlay measurements (NZ2C to NZ2C) were done to characterize the NZ2C performance. Both tests were done by measuring the overlay of all 84 fields (including partial fields), 12 measurement points per field. The results are shown in Figures 2, respectively. For the MMO case, the average + 3 sigma was 3.4nm in both x and y. For the SMO case, the average + 3 sigma in x and y was 2.1nm and 1.9nm, respectively.

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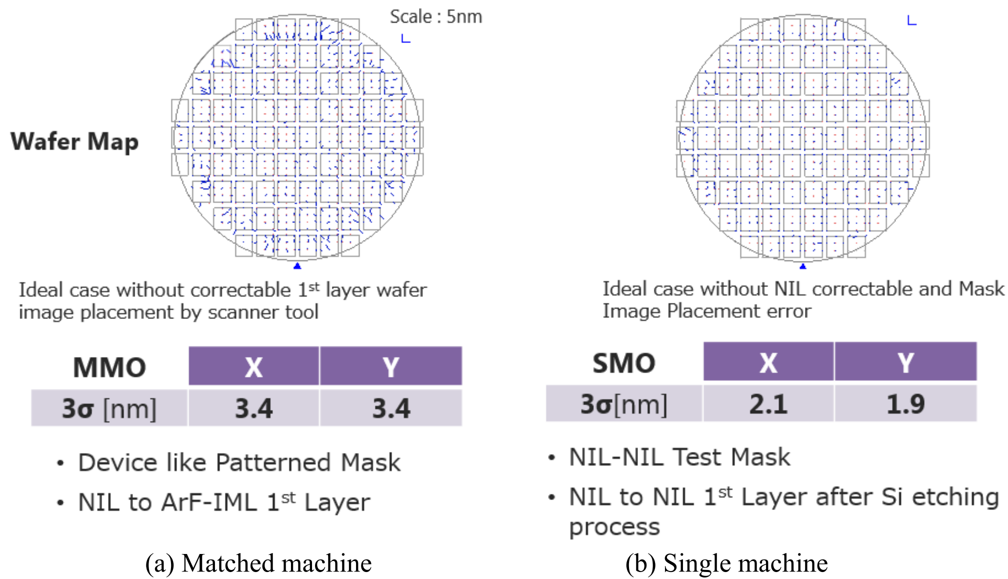

(a) Matched machine (b) Single machine

Figure 2. Overlay performance.

2.3 Particle Control and Mask Life

2.3.1 Background Information

Nanoimprint Lithography, like any lithographic approach requires that defect mechanisms be identified and eliminated in order to consistently yield a device. NIL does have defect mechanisms unique to the technology, and they include, liquid phase defects, solid phase defects and particle related defects.

Liquid phase defects can form, as an example, as the result of contamination to the underlying adhesion layer. The result of this contamination is incomplete filling in a small area, and is a type of non-fill defect. This defect type has been addressed in the past by applying the same sort of environmental filtering systems required, for example, for chemically amplified resists.

Solid phase defects can occur during the separation process. Shear forces imparted between the mask and wafer can tear features and potentially leave resist on the imprint mask. Another consequence of shear forces is line collapse and can be observed when the aspect ratio of sub-20nm features starts to grow well beyond 2:1. These defect types have also been overcome by careful attention to system controls during separation and are also no longer considered a priority.

More troublesome are particles that reside and adhere to either the mask or wafer surface. In the past we have described how the inkjet system can add to particle count and how liquid in-line filtrations systems addressed this issue.[17] These particles types were typically soft in nature and could be addressed by mask cleaning. Hard particles generated within the imprint tool are the biggest source of concern. Hard particles run the chance of creating a permanent defect in the mask, which cannot be corrected through a mask cleaning process. In summary,

- Liquid phase defects do not cause mask damage, do not require mask cleaning and can be addressed through environmental controls.
- Solid phase defects also do not damage the mask, but may require mask cleaning.

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- Particles, break down into two categories: soft and hard. Soft defects rarely damage the mask. Hard particles, however impact mask life.

To put this point in perspective, consider that in order to meet the CoO specs, the replica mask life must be sustained for better than 1000 wafers. If we conservatively assume that:

- Every hard particle adds a defect to the mask, and
- The mask defectivity limit from hard particles is 0.1 pieces per square centimeter,

then the number of particle adders per wafer path must be < 0.001. As a result, if we are to achieve this particle specification, an aggressive strategy is needed to remove particles adders to the wafer and mask. The purpose of this section is to review the measures being taken to reduce and control particles within the imprint tool and understand their impact to both particle adders and to mask life. Finally, we discuss additional methods that can further extend mask life and reduce NIL cost of ownership.

2.3.2 Strategy for Particle Mitigation

There are several countermeasures for particles that can be taken. In the past, countermeasures that have been discussed in detail include [18]

1. Particle source control: The minimization of particle generation from particle sources related to materials within the tool and the surface treatment of these materials.
2. Air curtain system: The reduction of particles that could potentially find their way onto the mask and wafer. These can be addressed by optimizing the airflow within the tool.

In this paper we examine:

- Particle test tool improvement
- Optimize cleaning and polishing
- In-situ particle removal
- Mask neutralization

By applying these techniques to a nanoimprint lithography system, as shown in Figure 3, it is possible to create an ultra-clean environment that is suitable for the nanoimprint process.

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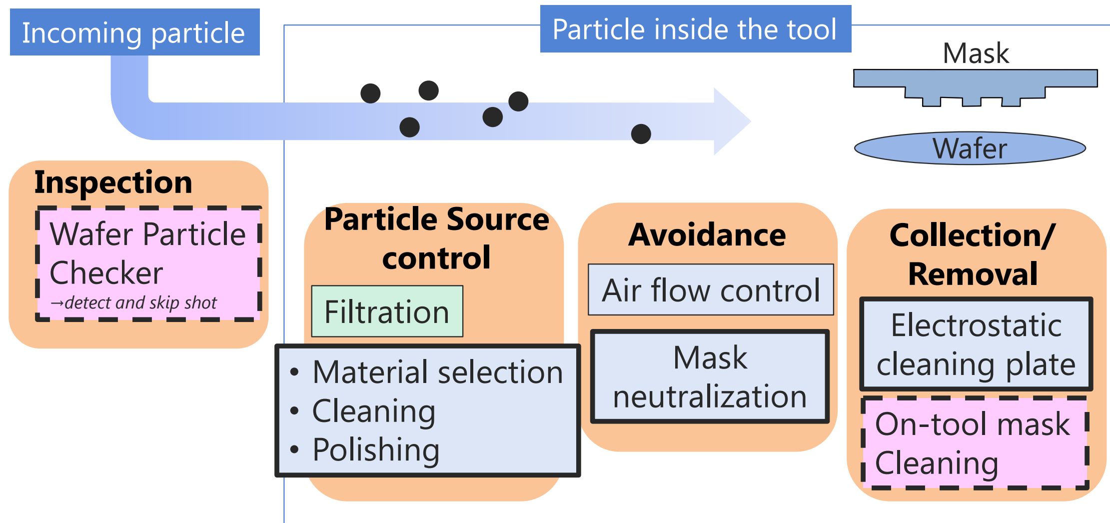

Figure 3. Canon's strategy for particle mitigation

2.3.3 Particle test tool improvement

The first step in improving particle source control required upgrades to the existing particle test tool used to qualify various parts. This test stand has been upgraded with new filtration and polished surfaces in order to reduce the background particles, thereby improving signal to noise the this system. The improvements and resulting data are shown in Figures 4 and 5. The resulting reduction in signal to noise allows more precise particle evaluation.

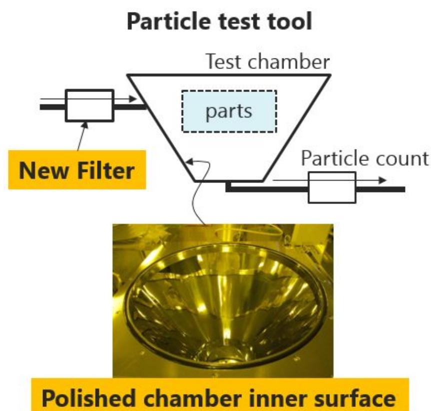

Figure 4. Particle test tool

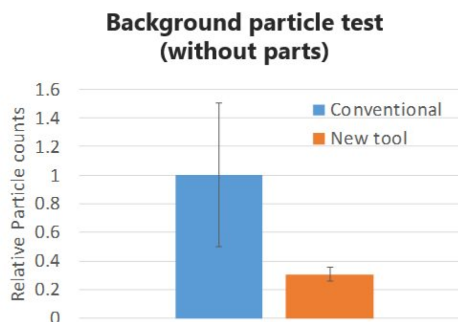

Figure 5. Background particle test

2.3.4 Optimization of cleaning and polishing

Materials have the potential to generate particles. As an example, gas delivery nozzles within the system often have rough surfaces that allow particles to detach from the surface during the operation of the nozzle. Mechanical and

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chemical polishing can reduce the roughness. In particular, it is important to optimize design, cleaning, polishing and drying before installation. Figure 6 shows the scheme used to minimize particles for these key parts.

To understand the efficacy of the process, we conducted an accelerated test using flow rates larger than the specific flow rate. Airborne particulates generated from key parts surfaces were measured using a TSI AeroTrak® Model 9110 Portable Particle Counter. The results of particle studies are shown below in Figure 7. Airborne particle counts were reduced significantly as a result of the polishing processes. It is clear that mechanical and chemical polishing improves surface quality and has the potential to greatly reduce defectivity.

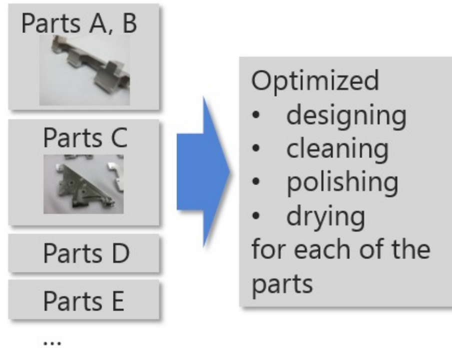

Figure 6. Scheme for minimizing particle generation

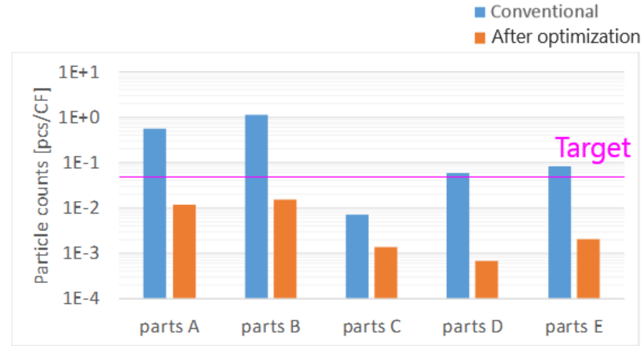

Figure 7. Particle evaluation result

2.3.5 Mask neutralization

A second method used to minimize particles on the mask surface works by the application of neutralization schemes. The mask and wafer separation step induces charging of the mask surface. We can take advantage of Paschen's law which describes the breakdown voltage needed to induce a discharge. Breakdown voltage is affected by pressure, which, in turn, is influenced by the mean free path between molecules. Since Noble gases, such as helium and neon have smaller diameters, mean free path is larger. As a result, by introducing helium gas between the mask and wafer as illustrated in Figure 8, we can reduce the electrostatic voltage at the mask surface. Neutralization tests were performed and we were able to reduce the electrostatic voltage by more than a factor of four, as shown in Figure 9.

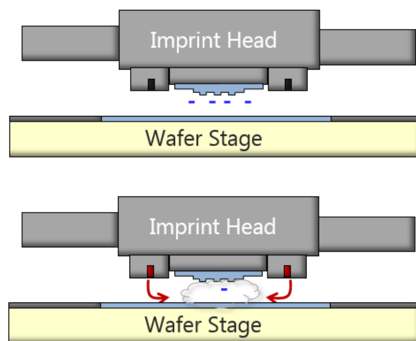

Figure 8. Introducing Helium gas on separation

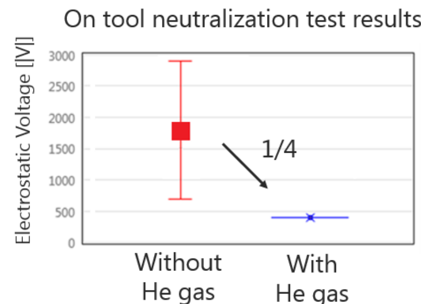

Figure 9. On tool neutralization test

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2.3.6 In situ particle removal

The remaining electrostatic charge still can attract particles to the surface of the mask. One method of further reducing the possibility of a particle event is to create a charged environment away from the mask in order to preferentially attract charged particles to the charged environment. An Electrostatic Cleaning Plate (ESCP) has been designed which is placed adjacent to the mask and operated at a voltage greater than the voltage generated on the imprint mask. The ESCP system was initially tested on an off-tool set up as shown in Figure 10a. In the configuration shown, two tests were run. In the first test (Figure 10b), particles were collected on a 100mm wafer over a five minute time period, and measured using a KLA-Tencor SFS6420 Surface Inspection System, with a detection limit of 120nm. Three particles were collected. In the second test (Figure 10c), the plate was set to 1kV. In this case, 25 adders were detected, confirming the efficacy of the ESCP.

As a follow up experiment, the ESCP was applied to an NZ2C nanoimprint tool, and found to be effective in attracting weakly attached particles on the wafer stage as shown in Figure 11.

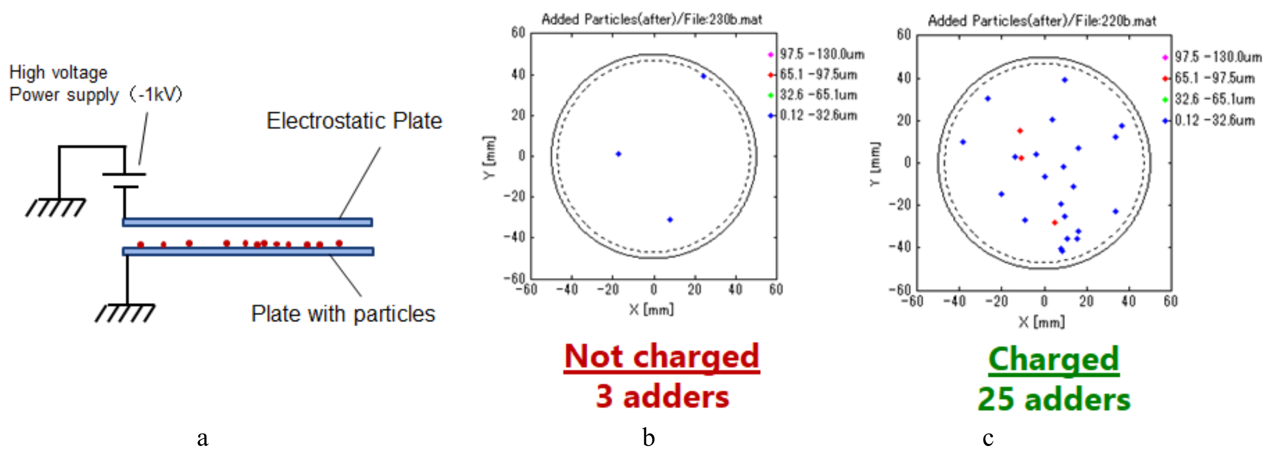

Figure 10. a. ESCP off-line test b. Particle adder test with no applied voltage c. Particle adder test with 1kV applied voltage

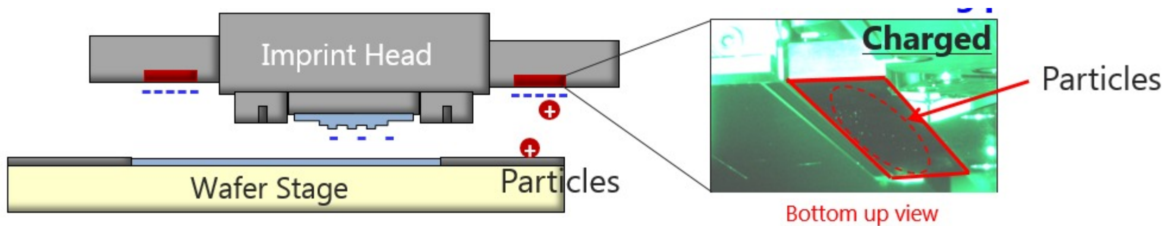

Figure 11. An ESCP was applied to an NZ2C nanoimprint tool and was effective in capturing weakly bound particles after applying a voltage to the plate.

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2.3.7 Mask Life Status

Particle reduction has been improved steadily. Over the last year, the inclusion of the ESCP, in addition to improvements in surface treatments and supply gas filtering has reduced particle adders to 0.0005 pcs/wafer, or 1 particle every 2000 wafers.

The correlation between particle adder reduction and mask life is apparent, as shown in Figure 12, which plots mask life as a function of year. Using the various methods described in this paper, a mask life of 125 lots (>3100 wafers) has been demonstrated.

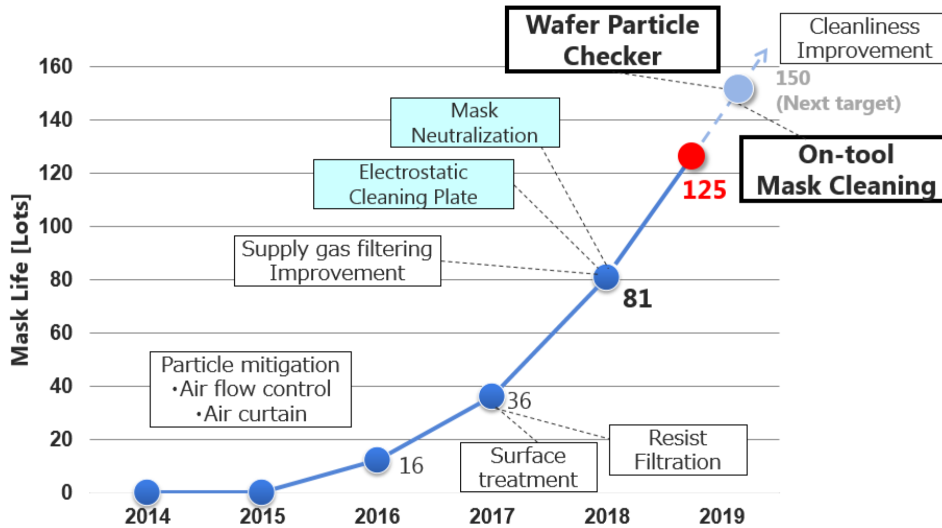

Figure 12. Mask life as a function of year. By applying a variety of particle reduction methods, a mask life of 125 lots has been demonstrated.

2.3.8 Solutions for Mask Life Extension

Extended mask life reduces cost of ownership. Therefore additional methods are being investigated as means of extending mask life beyond 150 lots. Figure 13 depicts a simple schematic of an imprint tool equipped with both a wafer particle checker (WPC) and an on-tool mask cleaning unit.

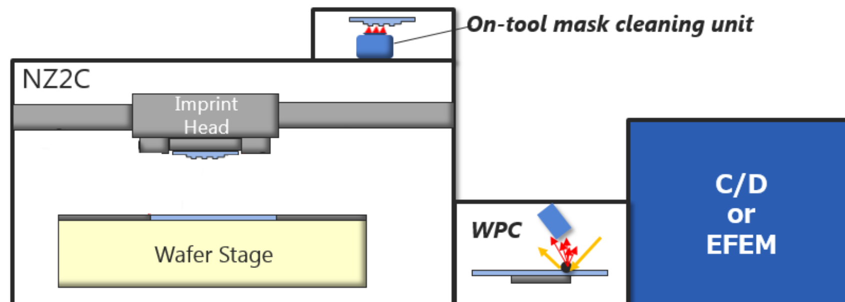

Figure 13. Schematic of an imprint tool equipped with both a wafer particle checker and an on-tool mask cleaning unit.

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Development has already started on the WPC as a means for screening wafers before they enter a nanoimprint station. The system is a compact scattered light detection system with nominal resolution of about 100nm on bare wafers and 300nm on patterned wafers. With an inspection time of 18 only seconds, the takt time of the WPC is 96 wafers per hour, consistent with the throughput of the NIL wafer tool.

An on-tool mask cleaning is also being developed. The system uses dry clean technology and scans the mask surface, removing any residual resist on the mask, thereby eliminating a mechanism for potential mask damage. Initial studies confirm that the system's ability to remove resist is comparable to off-line tolls currently used.

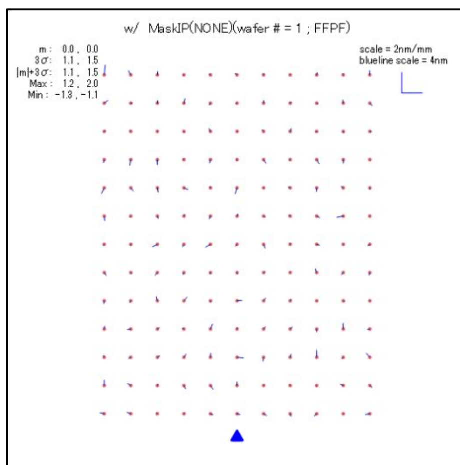
3. Mask Replication

In 2017, the new FPA-1100NR2 mask replication tool, which meets the target for the 1Z nm generation of devices, was shipped to a customer site. Target specifications are as follows. Throughput is 4 mask per hour, CD uniformity is 0.8 nm, Image placement is 1.0 nm, the particle adder spec is 0.002 pieces per mask.

To optimize image placement accuracy, we improved the accuracy of the pneumatics controls, chuck flatness, tilt control of the Master and Replica plate, and also optimized the imprint sequence. The pneumatic controls influence mask flatness during the mask replication process. We estimate that pressure accuracy needs to be around 10Pa for robust IP control. In addition, the dynamic range at high speed needs around 50kPa.[19]

We have been able to realize both of these conditions simultaneously with our high performance pneumatics, and the results are shown in Figure 14. The IP accuracy (after removing correctables) on the FPA-1100NR2 is 0.8nm in X, 1.0nm in Y.

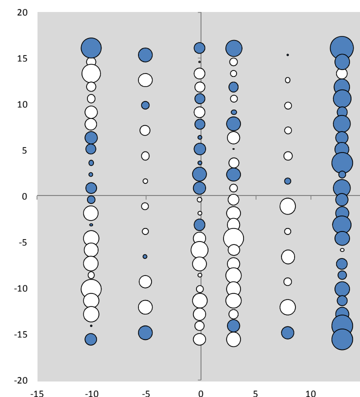
The mask replication process also requires good control of the critical features. Residual layer thickness (or RLT) plays a role in CDU, since variations in RLT can impact CDU after pattern transfer. As a result, we have worked to minimize RLT variation. Currently we can achieve with an RLT uniformity of 3.3nm. From a simple geometrical estimation, the impact on CDU on a replica mask after etching is 0.6 nm, and this value meets the 0.80nm specification. A map of the residual layer thickness uniformity across the 26 x 33mm field of an imprinted replica mask is shown in Figure 15.



3σX: 0.8nm

3σY: 1.0nm

Figure 14. IP accuracy (after removing correctables).



The RLT uniformity was 3.3nm, 3sigma.

Figure 15. RLT variation

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4. CONCLUSIONS

Great progress has been made in the field of NIL over the last four years. In this paper, to meet CoO requirements and to address yield issues, the progress on overlay, throughput, and particle was shown. 90 wafers per hour on a four-station cluster tool was achieved by applying a multi-field dispense (MFD) method in which resist is jetted onto several fields in order to decrease the overhead resulting from a sequential dispense and imprint process flow.

Refinement of the HODC system has enabled correction of higher order terms up to K30. The system was applied for both mix and match and single machine overlay tests. A mix and match overlay of 3.4 nm has been demonstrated and SMO across the wafer was 2.1nm.

A key factor for the insertion of nanoimprint lithography in a high volume manufacturing facility is mask life, which is influenced, in part, by the cleanliness of the nanoimprint tool. The continued reduction of particle adders extends both the life of the master mask and the replica mask. In this work, methods including optimize cleaning and polishing, in-situ particle removal and mask neutralization were discussed in detail. As a result of these methods, along with already developed techniques, particle counts on a wafer were reduced to only 0.0005 pieces per wafer path or a single particle over 2000 wafers, with a next target of 0.0001 pieces per wafer path. Particle adder reduction correlates directly with mask life, and a mask life of 125 lots (about 3100 wafers) was demonstrated. New methods are now under development to further extend mask and reduce cost of ownership. In this work on-tool wafer inspection and mask cleaning methods were introduced.

A new mask replication tool, the FPA-1100NR2 was also introduced and the means for improving the residual IP error in the tool to ~ 1 nm was presented. The combination of critical feature resolution and better IP will be used to address advanced devices with half pitch dimensions less than 15nm for the memory markets.

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