Highly Accelerated Thermal Shock Reliability Testing

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ABSTRACT
Thermal shock testing has long been the accepted method to check the reliability of plated-through holes and solder joint connections. Historically, thermal shock testing has been performed utilizing either dual chamber air-to-air systems or liquid-to-liquid systems. Both of these methods offer significant disadvantages in cost, time, and the fact that the samples must be transported between the hot and cold environments. Transportation of the samples between the temperature environments makes monitoring the resistance of the samples difficult and inaccurate due to the length and quantity of wires. The infrequent monitoring typically associated with traditional thermal shock methods also makes detection of glitch conditions marginal at best.

This paper introduces a new methodology that builds on the history of the models created for thermal shock testing while removing the disadvantages in cost, time and sample fixturing that are associated with traditional methods. This new technology attacks the main disadvantages of traditional tests while continuing to provide data that can be correlated to developed historical thermal shock test.

KEYWORDS: Via Reliability, Thermal Shock

INTRODUCTION
Thermal shock testing for to determine the reliability of electrical interconnects has been performed for many years. The fore father of today's thermal shock tests is MIL-STD-202 Method 107, which originated in the late 1950's and last updated in 1984.

For printed circuit boards and solder joints, the acceleration mechanism for reliability is a function of the thermal coefficient of expansion of the materials used in the device under test (DUT). Along with the difference between the temperature extremes (delta T) of the test environment, this coefficient determines the stresses introduced in the DUT and the reliability acceleration that is exhibited.

Thermal shock conditions are produced by rapidly moving the DUT between two temperature extremes, and typically require that the transition time between the extremes is less than 5 minutes, thereby creating a shock condition. The time the DUT must remain at a temperature extreme before reaching equilibrium can vary from a few minutes to an hour, depending on the method of producing the temperature extremes, the capacity for heat transmission, and the mass of the DUT. Considering that the number of cycles for a complete test can range from hundreds to thousands of cycles, this equilibrium time is very significant.

Historically, the two most used methodologies for producing thermal shock environments are air-to-air

and liquid-to-liquid. Air-to-air thermal shock systems utilize two separate chambers, each set to the opposite temperature extreme, and a mechanism to move the DUT between the two chambers. While these chambers are readily available, they are expensive to operate and provide a low heat exchange rate to the DUT.

Liquid-to-liquid chambers, each controlled to the opposite temperature extreme, utilize special liquids, and a mechanism to move the DUT between the two liquids. Unlike the air-to-air chambers, this very-expensive liquid provides an excellent heat exchange rate, and thus, is able to move the DUT rapidly between temperatures extremes.

Since both these methods physically move the DUT, cabling to the DUT must be capable of moving. It is very difficult to make electrical measurements during cycling, and the cabling is typically of lengths that do not allow for high accuracy measurements and limits the number of data points that can be monitored.

MIL-STD-202 Method 107

Almost all other thermal shock testing methods are based on MIL-STD-202 Method 107, which allows both liquid-to-liquid and air-to-air environments. Air-to-air conditions are broken into six categories based on delta T as detailed in Table 1, with dwell times at each extreme based on the mass of the DUT as shown in Table 2.

Category	Lower Temperature (C)	Upper Temperature (C)
A	-55	85
B	-65	125
C	-65	200
D	-65	350
E	-65	500
F	-65	150

Table 1. Air-to-Air Categories

Mass (g)	Dwell Time (minutes)
< 28	15
28 to 136	30
136 to 1,360	60
1,360 to 13,600	120
13,600 to 136,000	240
> 136,000	480

Table 2. Air-to-Air Dwell Times

Similarly, liquid-to-liquid conditions are broken into four categories based on delta T as detailed in Table 3, with dwell times at each extreme based on the mass of the DUT as shown in Table 4.

Category	Lower Temperature (C)	Upper Temperature (C)
AA	0	100
BB	-65	125
CC	-65	150
DD	-65	200

Table 3. Liquid-to-liquid Categories

Mass (g)	Dwell Time (minutes)
< 1.4	0.5
1.4 to 14	2
14 to 140	5

Table 4. Liquid-to-liquid Dwell Times

IPC-TM-650 2.6.7 Series of Test Methods

There are five IPC test methods for thermal shock that closely parallel MIL-STD-202 Method 107. They are all air-to-air methods intended for printed circuits, soldermasks and other coatings as shown below:

- 2.6.7A Thermal Shock and Continuity - Printed Board
- 2.6.7.1 Thermal Shock - Polymer Solder Mask Coatings
- 2.6.7.1A Thermal Shock - Conformal Coating
- 2.6.7.2A Thermal Shock, Continuity and Microsection - Printed Board
- 2.6.7.3 Thermal Shock - Solder Mask

These test methods use resistance measurements of a relatively small number of daisy-chained vias and microsection analysis to determine final acceptability.

Delphi Test

Delphi originated the thermal shock bare board reliability test as a sixty-minute, air-to-air cycle with a minimum and maximum temperature of –40C and 125C, respectively. The test temperature profile is specified by:

- Twenty-five minutes dwell at minimum temperature
- Less than five minutes transition time from minimum to maximum temperature
- Twenty-five minutes dwell at maximum temperature.

In 1995, Delphi expanded their test cycles to better represent possible locations on an automobile. Table 5 represents the four temperature classes currently specified by Delphi.

Class	Cycle	Operating Temperature	Typical Applications
A	-40 to 105C	85C	Passenger compartment
B	-40 to 125C	105C	Underhood Off-engine
C	-40 to 145C	125C	Underhood On-engine
D	-40 to 165C	145C	High performance/Chip-on-board/High dissipation components

Table 5. Delphi Reliability Classes

Like the IPC methods, the Delphi test uses resistance measurements of a relatively small number of daisy-chained vias and microsection analysis to determine final acceptability.

Interconnect Stress Test (IST)

The IST test approaches thermal shock from a very different perspective. The method uses the copper circuits (both traces and vias) integrated into the DUT as direct-current heating elements, and is cooled to ambient temperature with circulated air. Since the method does not include the cold portion of the thermal cycle, it can not replicate the traditional thermal shock methods.

Highly Accelerated Thermal Shock (HATS)

The HATS method was developed to emulate traditional air-to-air test methods, while significantly reducing the drawbacks of traditional methods. The test uses a single chamber in which high volume hot and cold air pass stationary samples. The high volume air flow provides rapid thermal transfer to the DUT, and reduces the time for the DUT to reach temperature equilibrium. This greatly reduces the time required for each cycle, and the stationary samples are easily fixtured to a high-speed precision resistance sampling network.

CAPABILITY, QUALITY AND RELIABILITY

The technology used to manufacture a printed circuit board is often determined early in the design process. The designer works within the constraints of overall size, thickness, weight, electrical performance, and thermal demands, but may have discretion on parameters such as layer count, feature sizes, and material properties to achieve the overall design objectives.

The interconnect technology and feature sizes selected by the designer can significantly impact the manufacturability, quality, performance, reliability, and cost of the printed circuit board. Capability and quality data can be used to optimize designs for manufacturability. By minimizing or eliminating features that are difficult to produce, the supply base will be able to manufacture designs at higher yields, lower costs, improved quality and reliability, and with minimal risk of shipment delays.

In this context, capability implies the ability to successfully form the vias and is quantified by metrics such as yield and defect density. Given that the vias are formed without defects, quality asserts the degree to which they conform to specification, and reliability affirms the ability of the vias to withstand operating and environmental conditions. Quality and reliability are quantified by statistical measures such as resistance coefficient of variation and percent change.

Prior to performing reliability studies, both capability and quality must be present in order to ensure the reliability results are valid. For example, a process which produces vias with a high defect density is of little interest since the supplier will never be able to consistently yield product. Additionally, if the process is producing vias of poor quality, then the reliability will be a function of the poor process – not of the operating and environmental conditions.

Experimental Details

The data reported in the study is from a Conductor Analysis Technologies, Inc. (CAT) process capability panels (Figure 1) produced by three large volume printed circuit suppliers as part of a Delphi advanced high density interconnect development project. The requirements were for forty 10.5 by 7.25 inch, 6-layer, 0.031-inch thick panels, each with outerlayer and innerlayer conductor and space features, via registration and daisy-chain features, and soldermask registration features. Additionally an IST coupon was incorporated into the panels in order to determine the reliability of the via structures.

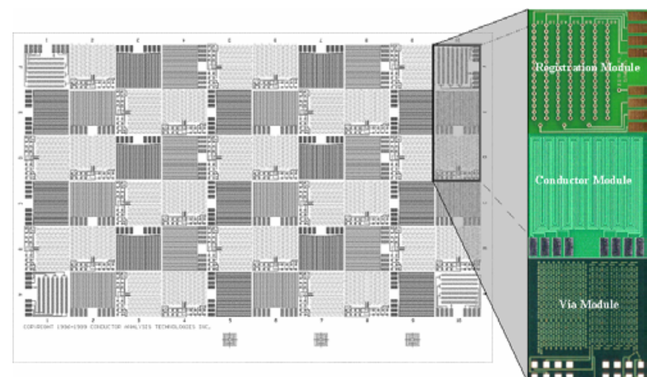

Figure 1. CAT Process Capability Panel

Stack-up and plating requirements were consistent among the suppliers, but some flexibility was given in the materials used in the construction of the panels to meet Delphi Class C requirements.

Table 6 details the designs features, aspect ratio, and interconnect sequence of the through-vias used in this study.

Hole (mils)	Land (mils)	Annular Ring (mils)	Aspect Ratio	Interconnect Sequence
8	14	3	3.8:1	1-4-2-5-3-6
8	20	6	3.8:1	1-4-2-5-3-6
10	16	3	3.1:1	1-4-2-5-3-6
10	22	6	3.1:1	1-4-2-5-3-6

Table 6. Through-Via Designs

Via Capability

A Poisson model was used to calculate via defect densities which are reported in defects per million vias. The equation used is:

$$\text{Defect Density} = -10^6 * (\ln Y) / n$$

where, Y is the number of good daisy-chains divided by the total number of daisy-chains, and n is the number of vias in each daisy-chain. In order for this equation to be meaningful, both the number of daisy-chains and the total number vias of should be large. Table 7 details the number of daisy-chains and the total number of vias measured in the determination of defect density for this study.

Via Hole / Land (mils)	Number of Chains	Number of Vias per Chain	Total Number of Vias
8 / 14	360	90	32,400
8 / 20	360	90	32,400
10 / 16	360	90	32,400
10 / 22	360	90	32,400

Table 7. Number of Vias per Design

High defect densities will translate directly to poor manufacturing yields, shipping delays and often poor quality vias. For the three suppliers in this study, the defect densities demonstrated for each of the four via design were low as detailed in Table 8.

Attribute	Via Hole / Land (mils)	Manufacturer		
		A	B	C
Defect per Million Vias	8 / 14	0	37	18
	8 / 20	18	18	0
	10 / 16	36	18	18
	10 / 22	0	18	18

Table 8. Via Defect Density

Via Quality

Once the vias have been manufactured successfully, the quality of the vias in the daisy-chain can be characterized by precision resistance measurements. Each daisy-chain is replicated over the surface of the panel and from panel-to-panel. Since the physical designs are identical, the resistance for each daisy-chain should have the same value. However, in practice even vias manufactured by high quality processes exhibit small variations resistance. These variations originate from mis-registration of the via hole to pads, plating differences between vias, the quality of the interfaces formed between the via barrels and innerlayer pads, and etching difference in the pads and conductors used to interconnect the vias in the daisy-chain.

Resistance Coefficient of Variation (CoV), expressed as a percentage, is used as a measure of quality for the via daisy-chains and is calculated by:

$$CoV = 100 * (\text{standard deviation} / \text{mean})$$

For the three suppliers in this study, the resistance coefficient of variation demonstrated is detailed in Table 9. Suppliers A and C demonstrated low coefficient of variations, with supplier B having 2 to 3 times the variation of the others. While this variation for supplier B is of concern and indicates a need to investigate source or sources of the variation, it is not large enough to prohibit further investigations to determine the reliability of the vias.

Attribute	Via Hole / Land (mils)	Manufacturer		
		A	B	C
Via Net Resistance Coefficient of Variation (%)	8 / 14	3.3	9.3	4.1
	8 / 20	3.0	9.0	4.0
	10 / 16	3.1	9.0	4.4
	10 / 22	2.6	8.9	4.1

Table 9. Via Resistance Coefficient of Variation

Assembly Simulation

After initial testing of the via daisy-chains, ten of the 40 process capability panels were subjected to 6 passes (3 per side), using a temperature profile of 2 min. ambient-183C, 1 min 183-215C, 3 min 215C-ambient, through a convection reflow oven to simulate an assembly operation. The panels were then retested to determine any changes in resistance of the via daisy-chains. For all three suppliers, there were no significant changes in the resistance of the via daisy-chains.

Via Reliability

Both capability and quality must be satisfied before initiating reliability studies. If capability is marginal, defect levels will be too high to achieve acceptable manufacturing yields. Additionally, a well-controlled manufacturing process will form vias with low resistance coefficients of variation. While controlled manufacturing processes are not sufficient to guarantee reliability, they are essential prior to beginning reliability studies. Initiating reliability studies without knowing whether the manufacturing process is in control can lead to erroneous conclusions and very costly mistakes.

DELPHI RESULTS

Panels from each manufacturer were chosen for Delphi thermal shock testing per Class C specifications. This class was chosen to match the requirements for Delphi's most advanced engine control module (ECM). Prior to thermal cycling all panels received two exposures to a standard assembly simulation profile used for this ECM. Two daisy-chains were periodically tested for opens through the temperature cycling with the results summarized in Figurers 2-4 for each of the three suppliers.

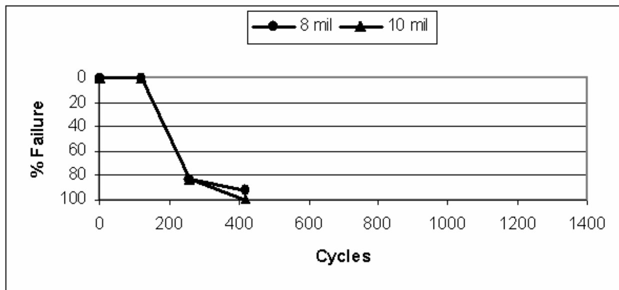

Figure 2. Delphi Via Reliability for Manufacturer A

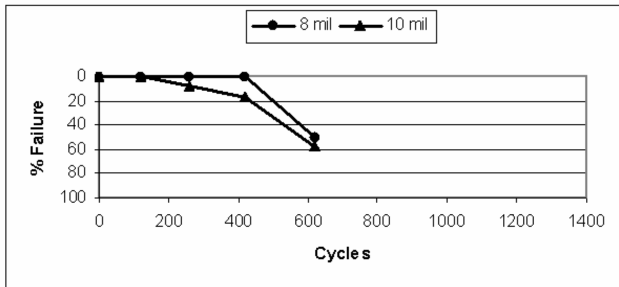

Figure 3. Delphi Via Reliability for Manufacturer B

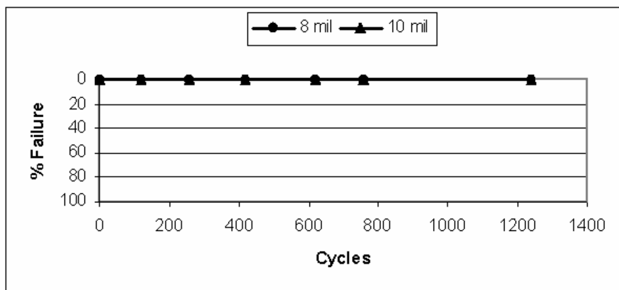

Figure 4. Delphi Via Reliability for Manufacturer C

A more complete end-point analysis was conducted on all through via daisy-chains as detailed in Table 10.

Attribute	Via Hole /	Manufacturer (Cycles)		
		A (420)	B (620)	C (1240)
Yield Loss	8 / 14	99.4	48.5	0
	8 / 20	100	65.8	0
	10 / 16	93.7	32.7	0
	10 / 22	98.9	66.1	0
Yield Loss (%) Threshold: 10% Change in Resistance	8 / 14	99.4	52.2	0.6
	8 / 20	100	75.2	0
	10 / 16	96.6	47.5	0
	10 / 22	99.4	74.1	0
Yield Loss (%) Threshold: 5% Change in Resistance	8 / 14	100	74.9	1.1
	8 / 20	100	83.9	0
	10 / 16	100	85.2	0
	10 / 22	100	86.4	0

Table 10. Via Reliability from Delphi Test

IST RESULTS

Coupons from each manufacturer were subjected to an interconnect stress test. Prior to the test the panels received two exposures to an assembly simulation profile. Based on prior work performed at Delphi, the upper temperature for the IST cycle was chosen at 170C to match Delphi Class C Specification. This was reported as a three minute heating stage from ambient to 170C and a two minute cooling stage to ambient for a total cycle time of five minutes. The IST results are shown in Figures 5-7.

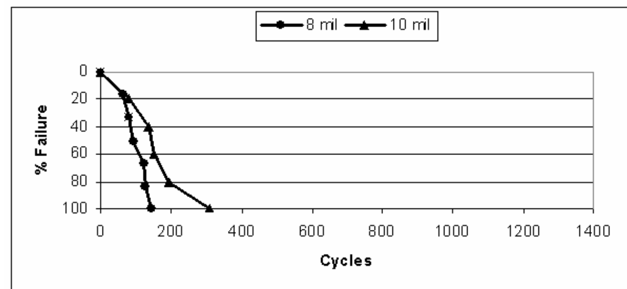

Figure 5. IST Via Reliability for Manufacturer A

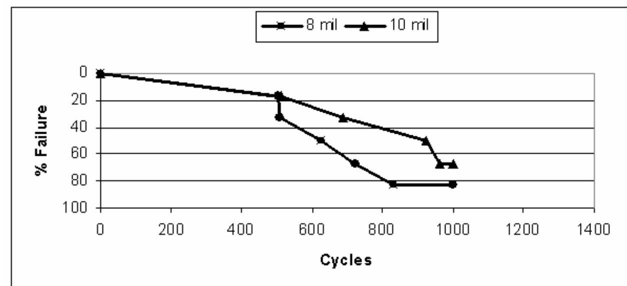

Figure 6. IST Via Reliability for Manufacturer B

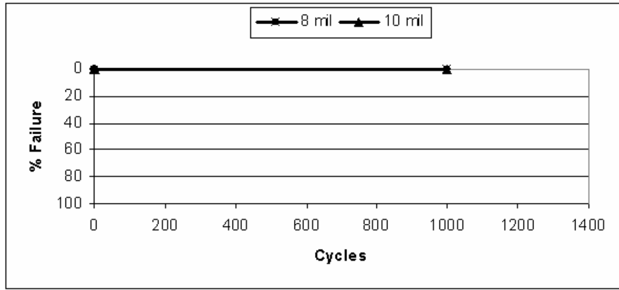

Figure 7. IST Via Reliability for Manufacturer C

HATS RESULTS

The HATS system has a maximum and minimum temperature capability of 160C and -55C, respectively. With a complete chamber load of thirty-six 0.62-inch thick coupons, the system has a temperature transition rate of 26C per minute. The system acquires precision resistance data from the test coupons. An example of this data is shown in Figure 8, which depicts the precision resistance of a net over the temperature extremes of the test and from cycle-to-cycle.

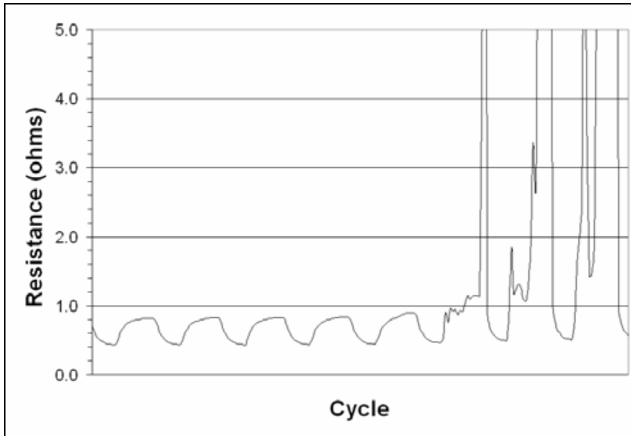

Figure 8. HATS Cycle Data

For this study coupons from each manufacturer were subjected to the Delphi Class C temperature specifications (-40 to +145C) in the HATS test system. Prior to the test, the coupons received two exposures to an assembly simulation profile. The HATS results are shown in Figures 9-11.

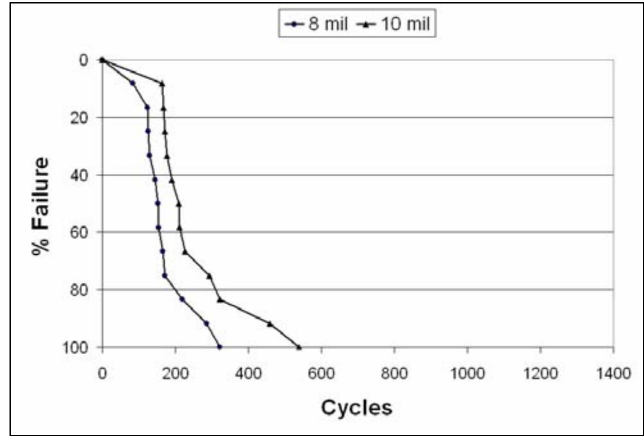

Figure 9. HATS Via Reliability for Manufacturer A

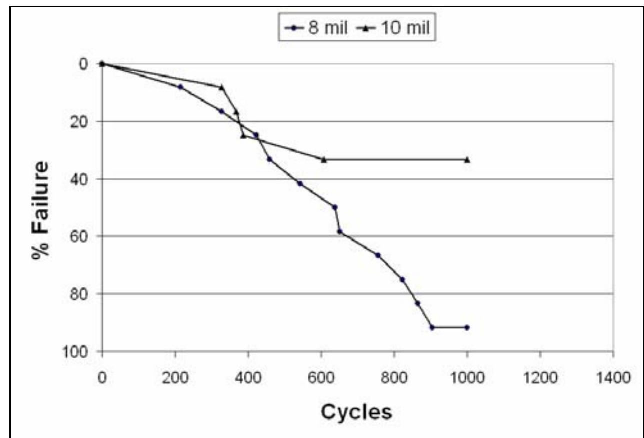

Figure 10. HATS Via Reliability for Manufacturer B

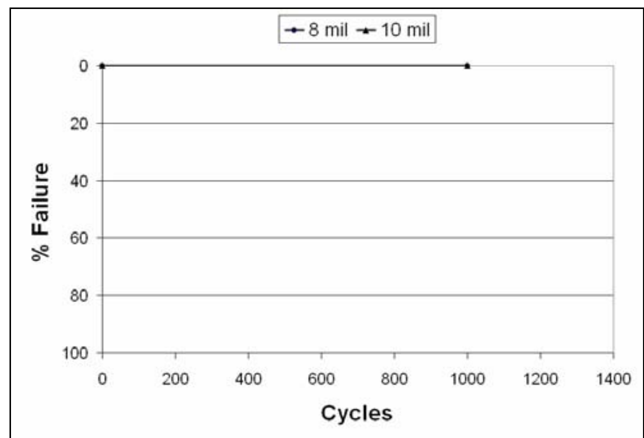

Figure 11. HATS Via Reliability for Manufacturer C

SUMMARY

The cycle parameters used for each of the three test methods used in this study are summarized in Table 11. The HATS cycle time is a factor of 4.3 times shorter than the Delphi method while maintaining the

same upper and lower temperatures. While the IST method provides the shortest cycle time, the upper and lower temperatures, and the delta T used was significantly different than the HATS and Delphi methods. Additionally, the IST method exceeded the glass-transition (T_g) of the substrate materials used in the manufacture of the test panels.

Test Method	Cycle Time	Lower Temp. (C)	Upper Temp. (C)	Delta T (C)
Delphi	60 min.	-40	145	185
HATS	14 min.	-40	145	185
IST	5 min.	30	170	150

Table 11. Test Method Parameters

In general, failure results from the three test methods provide the same conclusions in terms of the capabilities demonstrated by each of the three suppliers. However, there are differences in the results as shown in Table 12, which details the failure rates at the termination cycle of the Delphi test. Additionally, Table 13 details the number of cycles to the 62.4% failure point for the three methods.

Test Method	Via (mils)	Manufacturer (Cycles)		
		A (420)	B (620)	C (1000)
Delphi	8	92%	50%	0%
	10	100%	58%	0%
HATS	8	100%	50%	0%
	10	87%	33%	0%
IST	8	100%	50%	0%
	10	100%	33%	0%

Table 12. Percent Failure for Each Test Method

Test Method	Via (mils)	Manufacturer		
		A	B	C
Delphi	8	210	>620	>1000
	10	210	>620	>1000
HATS	8	160	700	>1000
	10	220	>1000	>1000
IST	8	110	700	>1000
	10	150	950	>1000

Table 13. Number of Cycles to 62.4% Failure