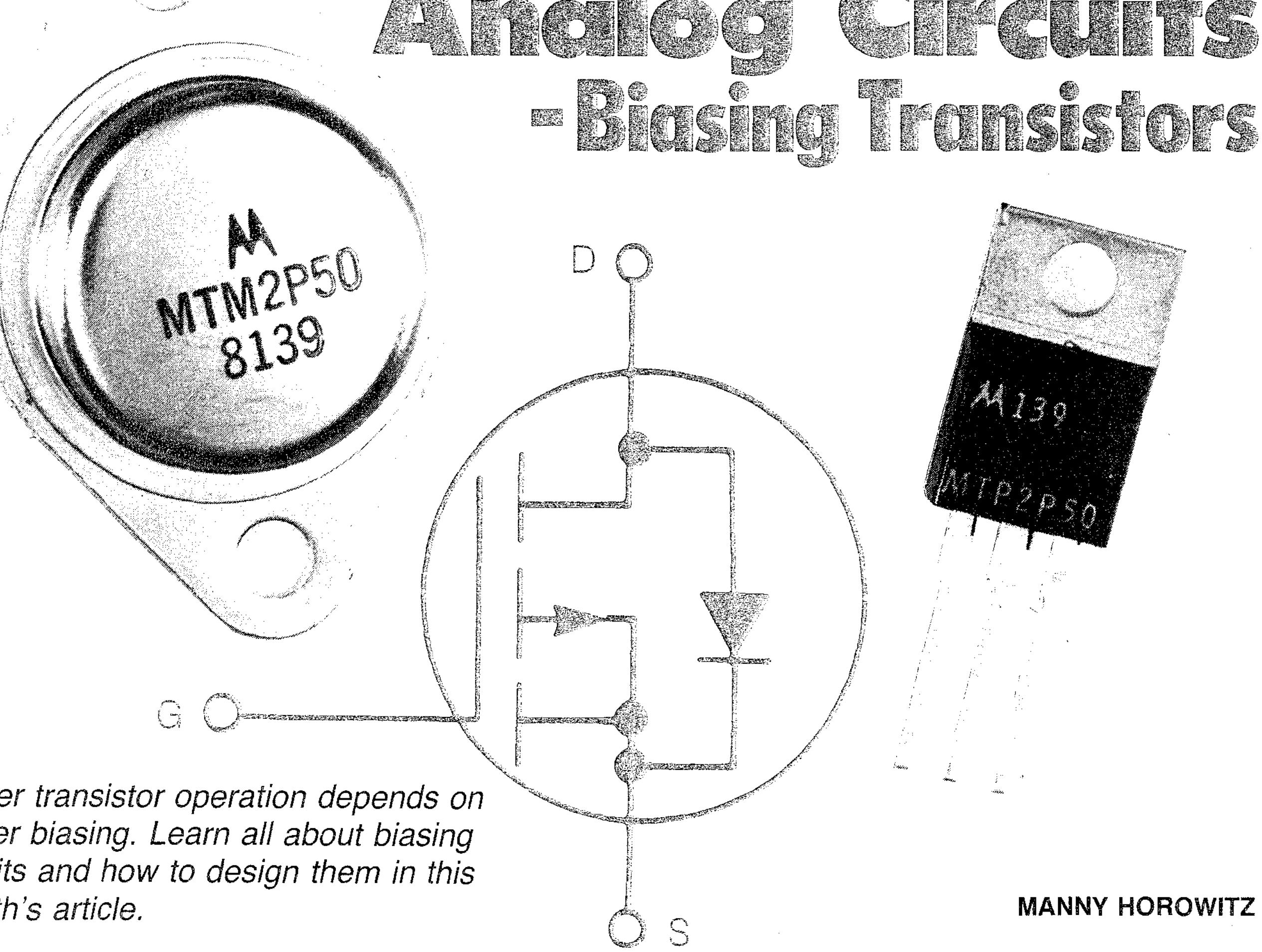
How to Design Analog Circuits - Biasing Transistors



Proper transistor operation depends on proper biasing. Learn all about biasing circuits and how to design them in this month's article.

MANNY HOROWITZ

Part 5 LAST MONTH, WE BEGAN our discussion of bipolar and FET transistors by looking at the structure of those devices and at some basic transistor circuits. One of the things we mentioned was that if a bipolar device were used in a Class A common-emitter circuit, for linear operation the collector voltage (with no input signal present), should be set at one half the supply voltage. The no-input-signal condition is commonly referred to as the quiescent operating point. (Similarly, in the case of an FET in a common-source circuit, the drain voltage should be one half the supply voltage). That, however, is merely an approximation: the actual operating point varies with the specific requirements of the circuit. In any event, once the proper operating point has been selected, the device must be *biased* for that point. Just how that is done is the topic of this month's article.

Bipolar transistors

There are essentially two types of bias circuits that are used with bipolar devices. Although there may appear to be many more, the others are simply variations of those two circuits. And even the two circuits are variations of each other.

But why do we need many bias circuits? They arose mainly because of the high leakage current, I_{CBO}, that flowed from the collector to the base in early germanium transistors. If that leakage current also flowed through the base-emitter junctions (as it normally did), it was multiplied by beta (β) to make it into a large undesirable leakage current, I_{CEO}, that flowed in the collector and emitter circuits. And to compound the problem, I_{CBO} and I_{CEO} doubled every time the temperature of the transistor increased by 10°C. Although those factors are still important in modern silicon transistors, the effect on the collector current is reduced considerably because the leakage current in silicon transistors is frequently low enough to be ignored.

In addition to leakage current, variations in the operating parameters from device to device, as well as with temperature, can cause problems. The value of β, for instance, will vary from device-to-device of the same type, as well as with temperature and collector current, I_C. In addition, the value of I_C at the operating point will vary with several parameters. Among those are V_{BE}, the voltage drop across the base-emitter junction, which itself varies with temperature; V_{BB}, the base supply-voltage; r_c, the collector-to-base resistance in a common-base circuit, and r_d the collector-to-base resistance in either a common-emitter or common-collector circuit.

But, once the operating point has been established for a circuit, ideally it should not be effected by differences in parameters from device-to-device, or by any external factors such as temperature. That is the reason for all of the bias-circuit variations—they are designed to help stabilize the operating point. In theory, if the proper bias circuit is used, the operating point will not change regardless of any change in any of the factors mentioned. However, theory and what really happens are not always the same. But even so, using the proper bias circuit will minimize any variations of the operating point sufficiently so that the circuit will still operate as intended.

To design a bias circuit properly, it is important to know how a variation in one variable will effect the other variables in the circuit. Because of that, three *stability factors* that relate the change of one factor to the change in another have been derived. They are:

$$S = \frac{\Delta I_C}{\Delta I_{CBO}} \quad (1)$$

which relates the change of collector current to the change in leakage current. The stability factor relating the change of collector current to the change in V_{BB} is:

$$S_E = \frac{\Delta I_C}{\Delta V_{BB}} \quad (2)$$

while the equation relating the collector current change to the change in β is:

$$S_\beta = \frac{\Delta I_C}{\Delta \beta} \quad (3)$$

Equations used to relate the various components in the circuit to the various stability factors, will be noted as each bias circuit is described. In each case, it is desirable that stability factors be as close to 1 (the perfect stability factor) as possible. Should more than one stability factor differ from 1, the effects of all variations must be taken into account when evaluating the design.

Bipolar transistor bias circuits

The simplest bias circuit to be described here is shown in Fig. 1. The base current, I_B, originates at V_{BB} and is delivered to the base through R_B. However, V_{BB} often does not exist as an independent supply; instead V_{CC} is used to supply both base and collector current. In that case, R_B is connected to V_{CC}, and that supply serves as both V_{CC} and V_{BB}.

In Fig. 1, all base current from V_{BB} flows through the base-emitter junction. If we consider the voltage across that junction, V_{BE}, as negligible when compared to V_{BB}, the base current due to the supply is V_{BB}/R_B. Collector current due to that base current is approximately equal to βI_B.

Next, let us add the effect of I_{CBO}, the leakage current that flows from the collector to the base. After flowing through the base-emitter junction, it is multiplied by beta. That βI_{CBO} flows in the collector and emitter circuits and substantially effects the collector and emitter currents. Collector current due to I_{CBO} is thus $\beta I_{CBO} = I_{CEO}$. (Note that in our discussions beta has been assumed to be much greater than 1. Thus only β is shown in formulas rather than $\beta + 1$.)

Finally, we have some collector current flowing due to r_d, the collector-to-

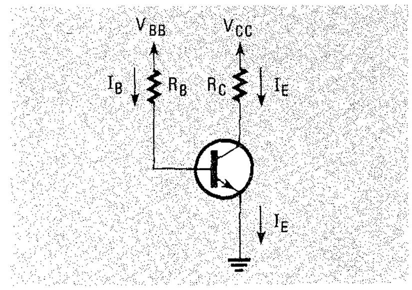


FIG. 1—A SIMPLE CIRCUIT for biasing bipolar transistors. Often there is no separate V_{BB} supply; instead V_{CC} is used to supply both the collector and base.

emitter resistance of the transistor. That resistance can be determined from the common-emitter collector-characteristics curve shown in Fig. 2. Using the procedure described in our last article (see the August 1982 issue of **Radio-Electronics**, draw the load line on the curve. The next step is to determine the operating or quiescent point needed to insure linear operation. If, for instance, you require that the collector current swing from 0 to $I_{C(MAX)}$, the collector current at the quiescent operating point, I_{CQ}, would be equal to $I_{C(MAX)}/2$. Find that point on the I_C axis. The voltage at the quiescent point, V_{CEQ}, is usually equal to about $V_{CC}/2$. Drawing a line perpendicular to the I_C axis at I_{CQ}, and a line perpendicular to the V_{CE} axis at V_{CEQ}, the point at which the two lines cross is the operating point. As drawn, that point falls on the $I_B = 100\ \mu A$ curve. Collector resistance, r_d, is the slope of that I_B curve around the operating point. The slope is found by noting two points that are equidistant from the operating point, and finding I_C and V_{CE} for those points. Assuming that the collector voltage and current at one point are V_{CE1} and I_{CE1}, and V_{CE2} and I_{CE2} at the other, then:

$$r_d = \frac{V_{CE2} - V_{CE1}}{I_{CE2} - I_{CE1}} \quad (4)$$

As indicated, r_d is the collector-emitter resistance of the transistor when it is used

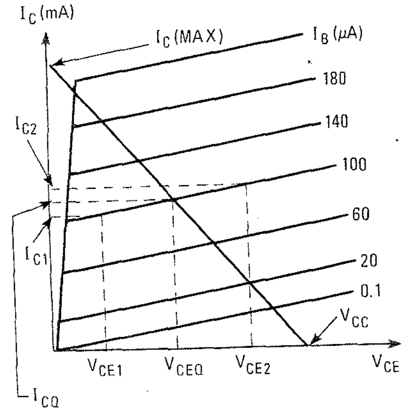


FIG. 2—ONCE THE QUIESCENT POINT has been found, the value of r_d is equal to the slope of the I_B curve around that point.

in a common-emitter or common-collector circuit. In a common-base circuit, that collector-emitter resistance is much higher and equal to βr_d; that quantity is called r_c.

A portion of the total collector current is due to the presence of r_d in the circuit. It is equal to the collector-emitter voltage, V_{CE}, divided by r_d. Obviously, V_{CE} is equal to the supply voltage less the voltage drop across the collector resistor, R_D, or $V_{CC} - I_C R_C$. Consequently, the total quiescent collector current flowing in the circuit of Fig. 1 is:

$$I_C = \beta I_B + I_{CEO} + \frac{V_{CC} - I_C R_C}{r_d}$$

which simplifies to:

$$I_C = \frac{\beta I_B + I_{CEO} + V_{CC}/r_d}{R_C/r_d + 1} \quad (5)$$

Should R_C be less than 10% of r_d, the effect of r_d becomes negligible, and all factors in the equation involving that term can be eliminated. We will then end up with the simple relationship:

$$I_C = \beta I_B + I_{CEO}$$

Finally, remembering that $I_B = V_{BB}/R_B$, we get:

$$I_C = \frac{\beta(V_{BB} + R_B I_{CBO})}{R_B} \quad (6)$$

You can usually use equation 6 and ignore r_d in most designs. But do not forget about r_d. It will be important later on when we discuss AC gain and the output impedance of transistor circuits.

The various stability factors for the circuit shown in Fig. 1 are:

$$S = \beta \quad (7)$$

$$S_E = \beta / R_B \quad (8)$$

$$S_\beta = \frac{I_{CBO} R_B + V_{BB}}{R_B} \quad (9)$$

Equation 9 indicates by how much the collector current will change for a specific change in β. Thus if a transistor with a β of 80 is substituted for one with a β of 40, the quiescent collector-current will double. To see how we came to that conclusion, let's digress a bit. First, as we saw in equation 3, $S_\beta = \Delta I_C / \Delta\beta$. Expanding further, equation 3 can be rewritten as $\Delta I_C = \Delta\beta(I_B)$. Secondly, since I_{CBO} is generally small enough to be ignored, and since V_{BB}/R_B is equal to I_B, in this case, the stability factor, $S\beta$, defined by equation 9 is approximately equal to I_B. Thus $\Delta I_C = \Delta\beta(I_B)$. Originally, I_C was equal to the inital β of 40 multiplied by I_B, or $40 I_B$. If $\Delta\beta = 40$, and $\Delta I_C = \Delta\beta I_B$, then

$\Delta I_C = 40I_B$. Finally, the total collector current when β is increased from 40 to 80 is $I_C + \Delta I_C$, or $40I_B + 40I_B = 80I_B$.

Improving stability

Stability can be improved by adding an emitter resistor, R_E, to the circuit in Fig. 1. If that is done, equations 7, 8, and 9 are modified to become:

$$S = \frac{\beta(R_E + R_B)}{\beta R_E + R_B} \qquad (10)$$

$$S_E = \frac{\beta}{\beta R_E + R_B} \qquad (11)$$

$$S_\beta = \frac{(R_E + R_B)\, V_{BB} + I_{CBO}\, R_B\, (R_E + R_B)}{(\beta R_E + R_B)^2} \qquad (12)$$

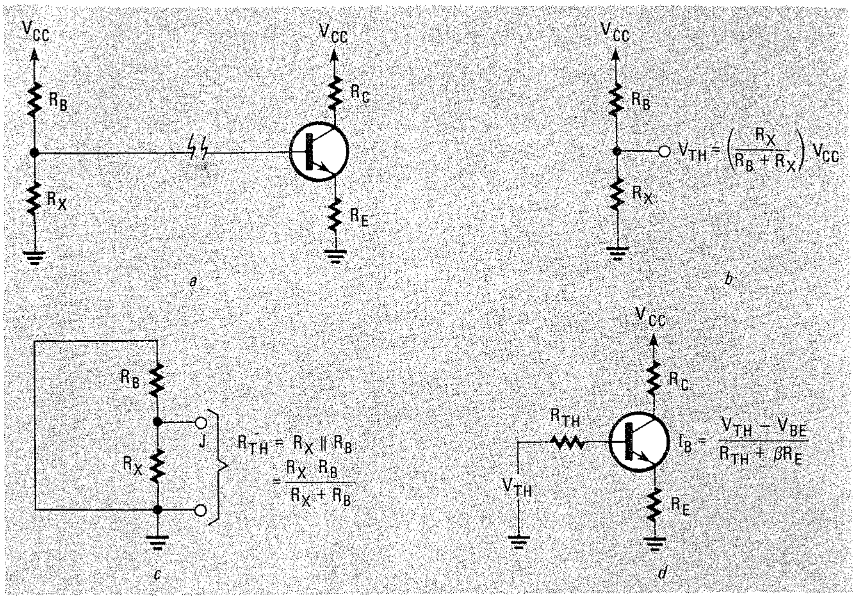


FIG. 4—TO EVALUATE THE BASE CURRENT of the circuit shown in Fig. 3, Thevenin's theorem must be used. The steps followed in applying that theorem are shown here.

In this arrangement, base current is less than it was when there was no emitter resistor. It is reduced because the emitter resistor, R_E, is reflected into the base circuit as a resistor equal to βR_E. Because of that, the base current becomes $(V_{BB}/(R_B + \beta R_E)) + I_{CBO}$. In addition, I_C becomes equal to βI_B.

The bias circuit shown in Fig. 3 is used when stability is a very important consideration. The circuit in Fig. 1, and the variation we created by adding an emitter resistor, are simplified versions of that circuit. In it, V_{BB} has been eliminated; instead, V_{CC} is used as both the collector and base supply.

Thevenin's theorem must be used in order to determine the base current in the circuit in Fig. 3. That theorem states, in part, that any network of voltage sources and resistances can be simplified to a single voltage source in series with a single resistance. Use the following steps to apply that theorem to the circuit. Those steps are shown in Fig. 4.

First, as shown in Fig. 4-a, separate the bias resistor circuit from the rest of the circuit.

The second step, as shown in Fig. 4-b, is to determine the voltage at the junction of R_B and R_X. That voltage is called the *Thevenin voltage*, V_{TH}, and, since R_B and R_X make up a simple voltage divider, is equal to $V_{CC}(R_X/(R_B + R_X))$.

The third step, as shown in Fig. 4-c, is to short the supply to ground and determine the *Thevenin resistance,* R_{TH}. That is the resistance seen when looking back toward R_X; in other words, the resistance between the junction "J" and ground. In this case, it is the parallel combination of R_X and R_B, which, of course, is equal to $R_X R_B/(R_X + R_B)$.

The fourth, and final step, shown in Fig. 4-d, is to reconstruct the original circuit, substituting V_{TH} for V_{CC}, and R_{TH} for R_B and R_X. The Thevenin voltage, V_{TH} and the Thevenin resistance, R_{TH}, are connected in series with the base of the transistor as shown. The base current can now be calculated from the formula:

$$I_B = \frac{V_{TH} - V_{BE}}{R_{TH} - \beta R_E}$$

The value of V_{BE} is usually .017-volt for a silicon transistor, and 0.2- to 0.3-volt for a germanium device. Once you've calculated I_B, the collector current is simply βI_B.

In this type of circuit, the effect of leakage current, I_{CBO}, is reduced because some of it is diverted from the base-emitter junction to R_X. A good rule of thumb to use when designing this type of circuit is to make R_X equal to less than ten times the size of R_E.

As we mentioned earlier, there are two basic types of bias circuits. So far, all of the circuits we've examined were variations of one type. Let's now turn our attention to the second type. It is shown in Fig. 5. Here, R_B is connected to the collector of the transistor being biased instead of to V_{CC}. In that circuit, negative feedback from the collector to the base acts to reduce the value of the stability factors, a desirable result. In determining the operating point, the simplest approach is to again use Thevenin's theorem. Just adapt the method described for the circuit in Fig. 3 to this circuit, using the value of V_{CE} that you are designing for instead of V_{CC}. A reasonably accurate formula for determining collector current is shown as equation 13. Note that R_C and I_{CBO} are included in the equation. Stability factors for this circuit are shown in equations 14, 15, and 16.

$$I_C = \frac{\beta[R_X V_{CC} + I_{CBO}(A + R_X R_B)]}{\beta A + R_X R_B} \qquad (13)$$

$$S = \frac{\beta(A + R_X R_B)}{\beta A + R_X R_B} \qquad (14)$$

$$S_E = \frac{\beta R_X}{\beta A + R_X R_B} \qquad (15)$$

$$S_\beta = \frac{(R_X V_{CC} + R_X R_B I_{CBO})(A + R_X R_B)}{(\beta A + R_B R_X)^2} \qquad (16)$$

Where $A = R_E R_C + R_E R_B + R_E R_X + R_X R_C$).

Those current and stability equations can be applied easily, with just slight modifications, to the circuit in Fig. 3. In equations 13 through 16, R_C is an important factor in determining the bias. It plays no part, however, in determining the stability and quiescent current for the circuit in Fig. 3. When applying those equations to that circuit, let R_C equal 0. That eliminates all terms containing R_C. If, in addition to setting R_C equal to 0, R_X was made infinite by removing it from the circuit and R_E was made equal to 0, or

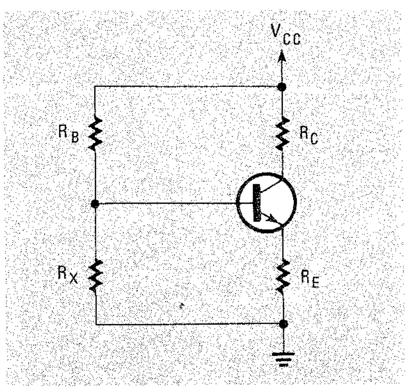


FIG. 3—IF BETTER STABILITY IS REQUIRED, the bias circuit shown here can be used.

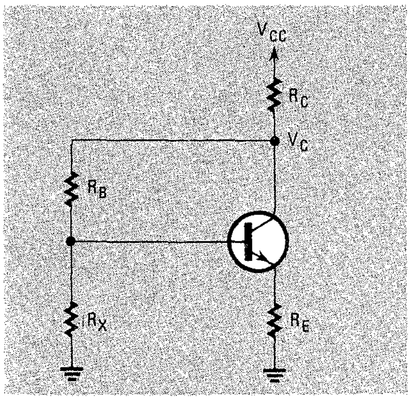


FIG. 5—THIS CIRCUIT is one of the many variations of the two basic bias circuits.

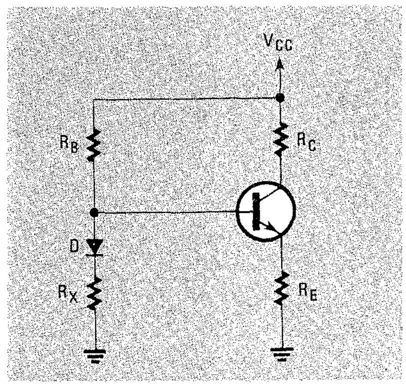


FIG. 6—TO COMPENSATE for variations caused by temperature, a diode can be placed in the base circuit as shown.

shorted, we end up with equations 6 through 9; those were, as you recall, used for the circuit shown in Fig. 1. Should R_E be left in the circuit, the equations will be identical to equations 10, 11, and 12, Thus, equations 6 through 12 are simply variations of equations 14, 15, and 16.

There are many variations of the simple circuits we have presented thus far. One of those is to remove R_X from the circuit of Fig. 5. That does reduce stability somewhat, however. Equations 13 through 16 still apply, but are modified by removing all terms containing the expression R_X.

Temperature compensation

Base-emitter voltage variation with temperature is an important consideration, especially in power circuits, because in those the temperature of the transistors tends to increase by a considerable amount. The circuit most-commonly used to compensate for that is shown in Fig. 6.

Diode D is placed into the circuit as shown so that it is always on. The diode used should have the same voltage/temperature characteristic as the forward biased base-emitter junction of the transistor. It should also be placed close to the transistor so that both of their temperatures will vary in a similar manner. With this configuration, the voltages across the diode and the base-emitter junction are always identical. Because of that, the voltage across R_E and R_X are also always identical, regardless of any changes in V_{BE} caused by temperature. Thus stability is improved.

The final variation we'll discuss here, is the one shown in Fig. 7. In most bias circuits, R_E is connected between the emitter and ground. Here, however, a battery or other voltage source, V_{EE}, is inserted between the emitter and ground. As a result, the base current, I_B is approximately equal to $V_{EE}/(R_X + \beta R_E)$; the collector current, as usual, is equal to βI_B. The stability factors for that circuit are essentially the same as those calculated using equations 10 through 12. When applying the equations here,

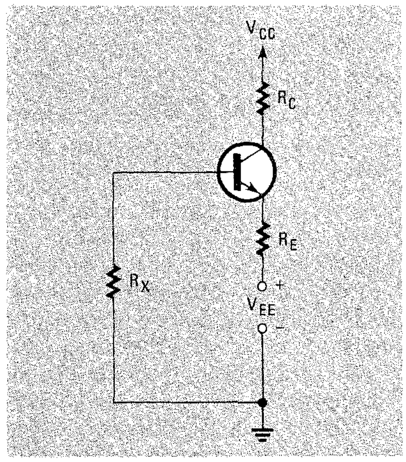


FIG. 7—IN THIS VARIATION, a battery or other voltage source is inserted between the emitter and ground.

however, substitute V_{EE} for V_{CC}, and R_X for R_B.

In summary, as a general procedure when designing bias circuits, first determine the ideal quiescent collector voltage and current. Divide the collector current by β to find approximately what the base current should be. Next design a base circuit to establish those conditions. Remember that those conditions should be relatively insensitive to temperature changes, as well as parameter variations from device to device. To make certain that they are, you must check the stability factors. Any of the circuits we've discussed, as well as many other variations, can be used when biasing bipolar transistors. You must determine how much operating point instability your design can tolerate. Start with the simplest circuit and calculate the stability factors. If collector current variations due to these factors are too great, increase the complexity one step at a time. Never go beyond the simplest circuit you can use to satisfy your requirements.

Biasing JFET's

Gates of n-channel JFET's are usually made negative with respect to the source. But, as no gate current flows if the gate is made just slightly positive with respect to the source of a JFET, up to +0.5 volt may be placed at the gate. Two arrangements used for establishing the proper bias voltage are shown in Fig. 8.

In Fig. 8-a, drain current, I_D, flows through R_D and R_S. Thus, the source current, I_S, and I_D are equal to each other. A voltage equal to $I_D R_S$ is developed across R_S. That voltage is called V_{RS} and has the polarity shown.

A leakage current, I_{GSS}, flows from the gate to the source. The value of I_{GSS} at 25°C is often found on the specification sheets of the device. That leakage current, however, increases with temperature—usually doubling with each increase of 10°C. The leakage current flows through R_G, developing a voltage, V_{RG} equal to $I_{GSS}R_G$. The polarity of that voltage is also shown in Fig. 8-a.

Voltage between the gate and source is equal to $V_{RS} - V_{RG}$. The value of V_{RS} is usually adjusted to be larger than the value of V_{RG} so that the gate will be biased negative with respect to the source. That's how the bias for the circuit shown in Fig. 8-a is established.

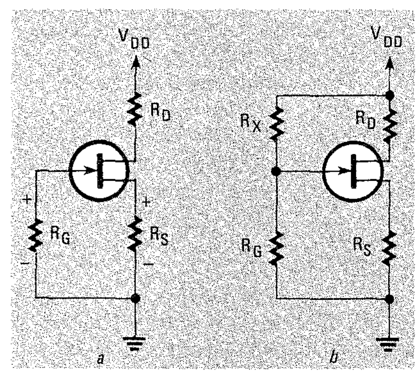


FIG. 8—EITHER OF THESE CIRCUITS can be used when biasing either JFET's or MOSFET's.

The source resistor is an important factor in enhancing the stability of the circuit as it is used to counteract any increase of I_{GSS} caused by a change in temperature. Circuit stability can be improved by increasing the size of R_S. But there is a limit to this. Should R_S be increased too much, the voltage developed across it can be high enough to bias the transistor near or at pinch-off. That is, of course, undesirable. The value of the source resistor must be chosen so that the proper bias point is established when the voltage developed across R_G is subtracted from the voltage developed across R_S.

A larger source resistor can be used with the circuit shown in Fig. 8-b. In that circuit, a sizable positive voltage can be developed across R_G due to the presence of $+V_{DD}$ and the action of the voltage divider made up of resistors R_X and R_G. That positive voltage is increased somewhat by the presence of leakage current I_{GSS}. To determine the gate-to-source bias voltage, subtract the voltage de-

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veloped across R_G from that developed across R_S. If it is desirable to make R_S very large, all you need do to compensate for the voltage, V_{RS}, that is developed across it, is to either increase R_G or reduce R_X. The larger voltage now developed across R_G, subtracted from the increased voltage developed across R_S due to its increased value, establishes a reasonable negative bias voltage.

Before calculating the values of R_X and R_G, we should know what values of I_D and R_S are desireable. That can readily be done by averaging values that are found on the JFET's specification sheet.

First determine the average pinch-off voltage, $\overline{V_P}$. It is midway between the maximum and minimum pinch-off voltages specified for the device.

In a similar fashion, calculate the average I_{DSS}, $\overline{I_{DSS}}$, the drain current when $V_{GS} = 0$.

Finally, choose a reasonable value for an average gate-to-source bias voltage, $\overline{V_{GS}}$. It frequently is equal to about $0.4 \times \overline{V_P}$.

All those factors are then substituted into the following equation to determine the average quiescent drain current, $\overline{I_D}$:

$$\overline{I_D} = \overline{I_{DSS}}\left(1 - \frac{|\overline{V_{GS}}|}{|\overline{V_P}|}\right) \qquad (17)$$

Absolute values of $\overline{V_{GS}}$ and $\overline{V_P}$ are used so that polarities can be ignored.

Now that we have determined $\overline{I_D}$, we can turn our attention to establishing a relationship between R_S and V_G, the voltage between the gate and ground. It is:

$$V_G = \overline{I_D}R_S - \overline{V_{GS}} \qquad (18)$$

We obviously want to make R_S as large as possible to improve stability, but there are some limitations. Voltages are developed across R_S and R_D due to the presence of I_D. When I_D is at its maximum, the sum of the voltages across R_S and R_D should be several volts less than V_{DD} if the transistor is to operate in the pinch-off region. Hence $(R_S + R_D)I_D$ must be less than V_{DD}. The value of R_D is usually determined by other circuit requirements, so that limits the value of R_S. Once the maximum value for R_S has been determined, the value of V_G is found from:

$$V_G = \left(\frac{R_G}{R_G + R_X}\right)V_{DD} \qquad (19)$$

But the values for R_G and R_X cannot be selected at random because of the presence of the leakage current, I_{GSS}. If ΔV_{GS} is the allowable bias voltage variation in the design, ΔI_D is the allowable drain

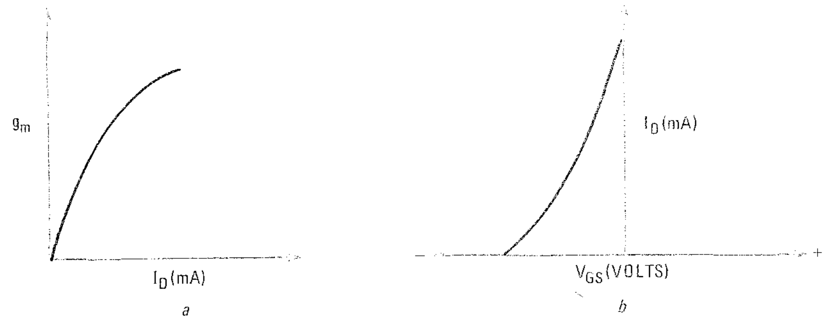

FIG. 9—THESE CURVES are extremely useful when designing MOSFET bias circuits. The curves for the device you are designing for can be found on that device's specification sheet.

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current variation, ΔI_{GSS} is the amount the leakage gate current changes over the operating temperature range, and R_S is the value of the source resistor, the parallel equivalent resistance, R_P, of R_G and R_X can be no larger than:

$$R_P = \frac{R_G R_X}{R_G + R_X} < \frac{\Delta I_D R_S - \Delta V_{GS}}{\Delta I_{GSS}} \qquad (20)$$

Once you've calculated R_P, you can find R_G and R_X from:

$$R_X = \frac{R_P V_{DD}}{V_{GS}} \qquad (21)$$

$$R_G = \frac{R_P V_{DD}}{V_{DD} - V_{GS}} \qquad (22)$$

Substituting that information into equation 19, we can determine V_G.

Biasing MOSFET's

MOSFET gates are insulated from their substrates and channels. Because of that, the leakage current is much lower than the I_{GSS} of a JFET. Furthermore, this leakage current remains constant regardless of the MOSFET's temperature.

Leakage current was a very important factor in bipolar device designs because it affected the output current. Collector current increased rapidly with leakage current and temperature causing the temperature and current to keep rising until the transistor, in many instances, destroyed itself. As for the MOSFET, that is not a problem because the output current here actually drops as the temperature of the transistor rises.

As for bias voltage, no gate current other than leakage current flows regardless of the gate's polarity with respect to the source. Despite that, n-channel enhancement\depletion-type MOSFET's are usually biased so that the gate is negative with respect to the source. But they could, if desired, be biased so that the gate is positive with respect to the source. Enhancement-type devices, however, MUST be biased so that the gate is positive with respect to the source.

The circuits we used to bias the JFET, shown in Fig. 8, can also be used for biasing MOSFET's. There is one additional consideration, however. Some MOSFET's have a lead from the substrate. If that should be the case connect that lead to the source of the transistor.

Two curves, a plot of g_m vs. I_D and a plot of I_D vs. V_{GS}, are useful when designing MOSFET bias circuits; a typical example of each of those is shown in Fig. 9-a and Fig. 9-b, respectively. Be aware that those curves will, of course, vary greatly among different types of MOSFET's; the curves for the specific device you are working with will be found on the device's specification sheet.

For a specific V_{DS}, calculating the values for the circuit shown in Fig. 8-a is relatively easy if you follow these steps.

1. Determine the g_m required for the circuit being designed.
2. Extend a line from that point on the vertical (g_m) axis of the plot of g_m vs. I_D found in the device's specification sheet to the curve itself. Drop a vertical line from the intersection point to the I_D axis. Where that line crosses the I_D axis is the desired value of I_D.
3. Following a procedure similar to the one in the last step, use the value of I_D to find the desired value of V_{GS} from the plot of I_D vs. V_{GS} found in the device's specification sheet. Once that is done, the values of I_D, V_{GS}, and V_{DS} are known.
4. Calculate R_S. For the circuit shown in Fig. 8-a, it is equal to V_{GS}/I_D.
5. As the voltage across R_D must be equal to $I_D R_D$, V_{DD} must be equal to $I_D R_D + V_{DS}$.

The design procedure is somewhat more complex when working on the bias network for the circuit shown in Fig. 8-b. Here, the bias voltage is the sum of the voltage across R_S, as just determined, and the voltage across R_G. If the voltage across R_G is to be positive with respect to ground, the voltage across the resistor can

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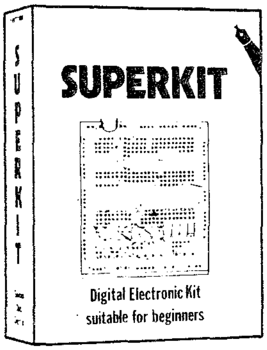

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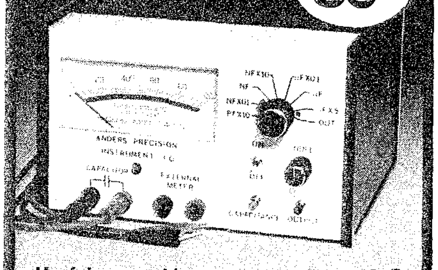

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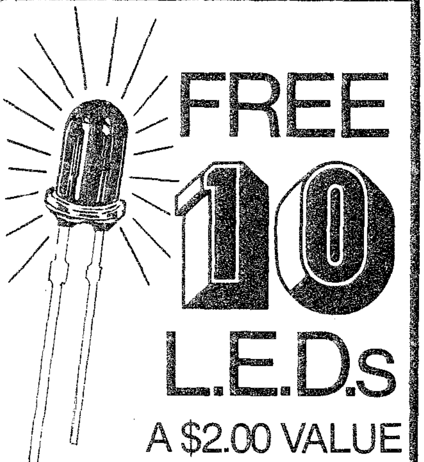

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COMMUNICATIONS CORNER

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the volume level: The loud sounds are clipped, while the soft sounds are allowed to pass through unprocessed.

Clipping the audio waveform causes distortion, and results in the generation of odd-order harmonics. For example, if the modulating signal is 1.5 kHz, clipping will produce substantial output at the third harmonic of 4.5 kHz and the fifth harmonic of 7.5 kHz, which are outside the upper narrow-band FM limit of 3 kHz. A low-pass filter consisting of R2/R3 and C2/C3/C4 strips out everything above 3 kHz before the signal gets to the next modulation amplifier.

The output from the amplifier is fed to a potentiometer, R4, which serves as a "deviation" (modulation level) adjustment, and then on to a varactor diode that's connected to the master oscillator. In that type of circuit it's necessary only to adjust the deviation control until the test equipment indicates the desired deviation.

Confusion sometimes sets in if a separate clipping adjustment is provided. Note that in the circuit shown, the clipping level in relation to the microphone signal is fixed; it's established by the preamplifier's gain and by diode D1. You will often find that there's a gain control for the preamp, or a level adjustment between the preamp's output and the clipper; either way, you can set the degree of clipping for a specific level into the microphone, or tailor the clipping level to the voice level of a specific user. Just remember that the transmitter's deviation—the modulation of the RF signal—is set with a single control. **R-E**

ANALOG DESIGN

continued from page 103

be found using equation 19. Complications arise if that voltage must be negative with respect to ground. Now the upper terminal of R_X should no longer be connected to $+V_{DD}$, but is instead connected to a negative supply. That supply is called $-V_{GG}$. Equation 19 still applies, except that $-V_{GG}$ is substituted for V_{DD}. The values of R_X, R_G, and R_S are still found as outlined above for the JFET.

Transistor applications

From here on, we will concentrate on designing practical circuits that use bipolar and FET transistors. We will start with small signal audio applications and continue our discussion detailing high frequency circuits, feedback, and so on. Regardless of what type of circuit you are designing, you will need to apply the material we've detailed over the past two months if you are to be successful. **R-E**

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