

• I2C Bus Arbitration.

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- I2C Clock Synchronisation.
- Serial Peripheral Interface (SPI)
- Controller Area Network (CAN)

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I2C Bus Arbitration.

- I2C is designed for multimaster purpose this means that more than one device can initiate transfers.
- Bus arbitration occurs when two or more masters start a transfer at the same time.

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I2C Bus Arbitration.

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• In the example below, The Master 1 issues a START sequence and sends an address, all slaves will listen, including Master 2 which at the time, is considered a slave as well.



• If the address does not match Master 2, then the Master 2 withholds its transactions until the bus becomes idle.



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- The Physical bus helps to handle the problem that can occur in the event that one of the master misses the start sequence and still thinks that the bus is Idle.
- The structure of the bus is wired-AND this means that if the device pulls the bus line low then the line stays low.



SDA

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• When Master 2 changes the state of the line to high then the line must go high, If the bus line does not go high then the bus is occupied already by some other device which has put the bus low such as Master1 here.







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• Thus, Master does not get its data on the bus. For as long as there has been no **STOP** sequence present on the bus, it won't touch the bus and leaves the **SCL And SDA** line alone.

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• A rule of thumb, If the Master can not make data line to go high then it looses the arbitration and needs to back off and wait until the stop sequence is seen.



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I2C Bus Arbitration.

• Later It can check the line and make another attempt when the line is free.



I2C Bus Arbitration.

Let see the timing diagram to elaborate.

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• In this example the two masters who have taken the control of the bus line have same speed and both are in the the right mode and want to address the same Slave.



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• The Slave acknowledges it and so far both the master are under the impression that It owns the bus because so far they have transmitted same data on the bus.

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slave.

0 0/1\0/ Data Master ' Clock Now each master wants to transmit its own data to the **0 1 1** 0/1 <u>\0</u>/ 1\0/ Data 0 / ... Master 2 Clock <mark>/∖0/1 ?</mark> 0 0/1\0 SDA Bus SCL ACK STOP START i Address R/W* ACK Data

I2C Bus Arbitration.

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The moment their data bits
do not match any more then
The Master 2 loses
arbitration and It must backs
Off because when Master 2
tries to move the SDA line
high the data on the bus
remains low due to wiredAND configuration (as
Master 1 already occupies it.)



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I2c Bus Arbitration.

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I2C Bus Arbitration.

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I2c Bus Arbitration.

Thus Master2 does not get its data on the bus as long as there has been no STOP sequence present on the bus till then it wont touch the bus.

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Clock Synchronization



• In serial communication, some people use the term "Clock Synchronization" merely refers to the matching of the speed for both the transmitter and receiver.

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- The I2c doens not synchronize the devices to the predefined baud rate.
- It is the master device which controls the clock speed.
- So the master device determines the clock speed.
- However the slave on the I2C may not cooperate with the clock speed given by the mster and might needs to slow down.



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- This is done using Clock Syncrhonization.
- Clock synchronization is perfomed using the wired-AND connection of the devices on the SCL line.







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Clock Synchronization

• Once the START sequence is initiated, the active slave and master start counting off their LOW periods of their own clocks



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- Once a device goes low, it holds the SCL line in that state indicating that it is not yet ready to process more data.
- However, the 0-1 transition of the master device's clock may not change the state of the SCL line of a slave device's clock that is still within its low period.



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- A master device pulls the SCL line low to begin a transaction.
- The master then sends clock pulses at a certain speed. But the slave can only work at this clock speed.
- So the master enters a HIGH wait-state (as indicated by the highlighted regions).
- It can be said that devices with shorter low periods enter a HGH wait-sate this time.
- When all devices have counted off their low period. The SLC line will be released and go HIGH.

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I2C Bus

Shortcomings(Limitations):

Electromagnetic Interference.

I2C is extremely sensitive to EMC



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I2C Bus

Limited Speed.

Shortcomings(Limitations):



Maximum possible speed of the I²C

400Kbits/sec

The connection of the Microcontroller with the memory chips requires a network type with fast speed so that data can be exachanged in quick fashion so I2C is really a bad option in that case because the Maximum it can provide is 400Kbits/sec





I2C Bus

Shortcomings(Limitations):

Long Distance Problem

• Being a protocol where one combines data and control lines it is very poor choice if you have longer lines (longer than few centimetres)



SPI--- Serial Peripheral Interface

The <u>SPI bus</u>

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The Serial Peripheral Interface (SPI) bus was developed by Motorola to provide **full-duplex synchronous** serial communication between master and slave devices.







SPI Basics

- A communication protocol using 4 wires
- Synchronized.
- SPI is a fully synchronous serial protocol. For every clock cycle one bit is transferred.

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Capabilities of SPI

- Always Full Duplex
 - Communicating in two directions at the same time
- Multiple Mbps transmission speed
- Transfers data in 4 to 16 bit characters
- Multiple slaves
SPI--- Serial Peripheral Interface

• SPI can be clocked up to 10 MHz.

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• The <u>SPI bus</u> is commonly used for communication with Flash memory, sensors, real-time clocks (RTCs), analog-to-digital converters, and more





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<u>SPI</u>

Physical Layer

Lets now look at the signal definitions and terminologies of the SPI.

- At the simplest level, SPI communications consists of a single bus master connected to a single bus slave.
- One device acts as Master and other as Slave.
- Two data transfer lines.



<u>SPI</u>

Physical Layer

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• In case of multiple slaves, master must provide the dedicated chip select Cs lines for each slave and this configuration is like the configuration depicted on the left.

• This configuration is often used in data acquisition systems where multiple analog-to-digital (ADCs) and digital-to-analog converters (DACs) must be accessed individually.



<u>SPI</u>

Physical Layer

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• Both the SPI master and Slave have a shift Register.



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<u>SPI</u>

Physical Layer

• When the master wants to send the data to the slave, First it loads the data into its Shift Register.



SS

MOSI

MISO

Shift register

з

5

6

0

Shift register

3

5 6 7

• The master then select the destination. This is done by selecting the SS or CS line associated with that slave.

Physical Layer

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• The serial Clock line is then enabled and one bit of the data is shifted on the MOSI line with each clock pulse.





<u>SPI</u>

<u>SPI</u>

Physical Layer

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- Since the SPI protocol uses full duplex synchronous serial data transfer method, it could transfer the data and at the same time receiving the slave data using its internal shift register.
- From the SPI master and slave interconnection diagram on the right side You can see that the SPI peripheral use the shift register to transfer and receive the data



SPI Master and Slave Interconection

Physical Layer

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• For example the master want to transfer **0b10001101(0x8E**) to the slave and at the same time the slave device also want to transfer the **0b00110010(0×32)** data to the master.

SPI

- By activating the CS (chip select) pin on the slave device, now the slave is ready to receive the data.
- Prior to a data exchange, the master and slave load their internal shift registers with memory data.
- Upon a clock signal, the master clocks out its shift register MSB first via MOSI line.
- At the same time the slave reads the first bit from the master at MOSI, stores it into memory, and clocks out its MSB via MISO.



SPI Master and Slave Data Transfer Diagram

Physical Layer

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• Continuously using the same principle for each bit, the complete data transfer between master and slave will be done in 8 clock cycle

SPI



SPI Master and Slave Data Transfer Diagram



<u>SPI</u>

- SPI interface allows to transmit and receive data simultaneously on two lines (MOSI and MISO).
- Clock polarity (CPOL) and clock phase (CPHA) are the main parameters that define a clock format to be used by the SPI bus.

<u>SPI</u>

• Idle (or First) State is 0 so the Polarity =0



• If Idle state is low then Clock Polarity=0.

Polarity determines the idle state of the clock.

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Clock Polarity

• If Idle state is high then Clock Polarity=1

• Idle (or First) State is 1 so the Polarity =1



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Clock Phase

<u>SPI</u>

Phase determines at which edge data read/write occurs

- If Clock Polarity=0 and data read/write occurs at rising edge then the Clock Phase=1
- If Clock Polarity=0 and data read/write occurs at rising edge then the Clock Phase=0.
- If Clock Polarity=1 and data read/write occurs at falling edge then the Clock Phase=1
- If Clock Polarity=1 and data read/write occurs at rising edge then the Clock Phase=0



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<u>SPI</u>

Modes in SPI

- The frame of the data exchange is described by two parameters, the clock polarity (CPOL) and the clock phase (CPHA).
- This diagram shows the four possible states for these parameters and the corresponding mode in SPI.

Mode	CPOL	СРНА
0	0	0
1	0	1
2	1	0
3	1	1

<u>SPI</u>

<u>Mode 0</u>

- The data must be available before the first clock signal rising.
- The clock idle state is zero.

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- The data on MISO and MOSI lines must be stable while the clock is high and can be changed when the clock is low.
- The data is captured on the clock's low-to-high transition and propagated on high-to-low clock transition.



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<u>SPI</u>

<u>Mode 1</u>

- The first clock signal rising can be used to prepare the data.
- The clock idle state is zero.
- The data on MISO and MOSI lines must be stable while the clock is low and can be changed when the clock is high.
- The data is captured on the clock's high-to-low transition and propagated on low-to-high clock transition.



<u>SPI</u>

<u>Mode 2</u>

- The data must be available before the first clock signal falling.
- The clock idle state is one.

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- The data on MISO and MOSI lines must be stable while the clock is low and can be changed when the clock is high.
- The data is captured on the clock's high-to-low transition and propagated on low-to-high clock transition.



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<u>SPI</u>

Mode 3

- The first clock signal falling can be used to prepare the data.
- The clock idle state is one.
- The data on MISO and MOSI lines must be stable while the clock is high and can be changed when the clock is low.
- The data is captured on the clock's low-to-high transition and propagated on high-to-low clock transition.



<u>SPI</u>

Why 4 modes why not only 1

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- SPI's predecessor had only one CPOL/CPHA mode.
- SCK(Clock) negative polarity is best when open-L type drivers with pullup are used.
- SCK(Clock) positive polarity is good when bus master is powered separately as SCK will not glitch when master is power up/down.
- CPHA=1 is useful when MISO is multiplexed with BUSY/READY and CPHA=0 require 1 less flipflop in a slave.



<u>SPI</u>

How to Select the Mode

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- You select the mode by configuring a bit in a configuring register. Your device manual will tell you which bit it is
- As for how to configure clock phase and polarity, it depends on the device you are working with.
- Typically the device has a register with bits corresponding to clock phase and polarity this bit can be manipulated to bring the device in the desired mode.



Advantages of SPI

- 1. Full duplex communication
- 2. Higher throughput than I²C protocol
- 3. Not limited to 8-bit words in the case of bit-transferring
- 4. Arbitrary choice of message size, contents, and purpose
- 5. Simple hardware interfacing
- 6. Typically lower power requirements than I²C due to less circuitry.



Disadvantages of SPI

- 1. Requires more pins on IC packages than I²C
- 2. No hardware flow control
- 3. No Acknowledgement Signal.

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Broadcasting.

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Broadcasting.





<u>Need for Broadcasting and Priority</u> for the Message.

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CAN Protocol

• The CAN Bus is an automotive bus developed by Robert Bosch.

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- It has quickly gained acceptance into the automotive and aerospace industries.
- CAN is a serial bus protocol to connect individual systems and sensors as an alternative to conventional multi-wire looms.



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CAN Protocol

• The Controller Area Network (CAN) is a serial communication way, which efficiently supports distributed real-time control with a very high level of security.

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• It allows automotive components to communicate on a dual-wire networked data bus up to 1Mbps.





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CAN Protocol

After CAN



As technology progressed, the vehicles became more complex as electronic components replaced mechanical systems and provided additional comforts, convenience, and safety features.

Up until the release of CAN Bus, vehicles contained enormous amounts of wiring which was necessary to interconnect all of the various electronic components.

Before CAN



CAN Protocol

CAN is based on the "broadcast communication mechanism", which is based on a message-oriented transmission protocol.

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It defines message contents rather than stations and station addresses.

Every message has a message identifier, which is unique within the whole network since it defines content and also the priority of the message.

This is important when several stations compete for bus access (bus arbitration).



CAN Protocol

• It provides the error process mechanisms and message priority concepts.

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- These features can improve the network reliability and transmission efficiency.
- Furthermore, CAN supplies the multi-master capabilities, and is especially suited for networking "intelligent" devices as well as sensors and actuators within a system or subsystem.
- The protocol's error management, fault isolation, and fault tolerance capabilities provide some nice benefits to design engineers building base transceiver station (BTS) and mobile switching center (MSC) equipment for emerging third-generation wireless networks.





CAN Protocol

Important Features.

Multi-master

When the bus is free any unit may start to transmit a message.

• The unit with the message of highest priority to be transmitted gains the bus access.

Safety *

In order to achieve the utmost safety of data transfer, powerful measures for error detection, signalling and self-checking are implemented in every CAN node.

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CAN Protocol

Speed & Distance

Baud (bit/sec)	Ideal Bus Length
1M	25
800K	50
500K	100
250K	250
125K	500
50K	1000
20K	2500
10K	5000

Arbitration

If two or more nodes start transmitting messages at the same time, the arbitration mechanism is applied to guarantee that one of these messages can be sent successfully according to the priority.

Priorities

The **CAN IDENTIFIER** defines a static message priority during bus access.

CAN Protocol

How CAN Communication Works

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- There is no master that controls when individual nodes have access to read and write data on the CAN bus.
- When a CAN node is ready to transmit data, it checks to see if the bus is busy and then simply writes a CAN frame onto the network.
- The CAN frames that are transmitted do not contain addresses of either the transmitting node or any of the intended receiving node(s). Instead, an arbitration ID that is unique throughout the network labels the frame.
- All nodes on the CAN network receive the CAN frame, and, depending on the arbitration ID of that transmitted frame, each CAN node on the network decides whether to accept the frame.



CAN Protocol

How CAN Communication Works

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CAN Network

• Physically a CAN bus consists of a pair of wires labelled CAN H and CAN L.

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- Each device on the bus "taps" off these two wires.
- These wires are twisted along their length and terminated at each end with terminating resistors.
- Twisting and terminating resistors are essential to ensure correct signal integrity on the bus.
- The following diagrams illustrates the minimum CAN bus:


CAN Protocol

How do CAN bus modules communicate?

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- CAN bus uses two dedicated wires for communication. The wires are called CAN high and CAN low.
- When the CAN bus is in idle mode, both lines carry 2.5V. When data bits are being transmitted, the CAN high line goes to 3.75V and the CAN low drops to 1.25V, thereby generating a 2.5V differential between the lines.
- The CAN bus has two states, one representing a logical 1, called the recessive state, and the other representing a logical 0, called the dominant state. When the bus is idle (no message traffic) the bus is in the recessive state. A device communicating on the bus will pull the bus to the dominant state.



CAN Protocol

Message on the CAN bus

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- CAN transmits signals on the CAN bus which consists of two wires, a CAN-High and CAN-Low.
- These 2 wires are operating in differential mode, that is they are carrying inverted voltages (to decrease noise interference) The voltage levels, as well as other characteristics of the physical layer, depend on which standard is being used.



CAN Protocol

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•SOF (start-of-frame) bit – indicates the beginning of a message with a dominant (logic 0) bit. and is used to synchronize the nodes on a bus after being idle.

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•Arbitration ID – identifies the message and indicates the message's priority

- This part sets the priority of the message in case of collision.
- The lower the binary value, the higher its priority

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- RTR-The single remote transmission request (RTR) bit is dominant when information is required from another node.
- All nodes receive the request, and the corresponding node replies and put the requested data on the bus..
- The responding data is also received by all nodes and used by any node interested.

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• **CTRL**—The 4-bit CTRL contains the number of bytes of data being transmitted.

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• Data field – Contains the actual information that is being transmitted. Can range from 0 to 64 bits (with 8 bit increments).

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CRC–The 16-bit (15 bits plus delimiter) cyclic redundancy check (CRC) contains the checksum (number of bits transmitted) of the preceeding application data for error detection.

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- Acknowledgement Field
- It is an acknowledgement of reception, securing at least one receiver has got the message OK
- The transmitter sets the ACK bit to 1
- Any receiver set the ACK bit to 0 when the message is found OK

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EOF–This end-of-frame (EOF), 7-bit field marks the end of a CAN frame (message)

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IFS–This 7-bit interframe space (IFS) contains the time required by the controller to move a correctly received frame to its proper position in a message buffer area

CAN Protocol

How the Bus Conflicts are Managed.

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Bus access conflicts are resolved by bit-wise arbitration of the identifiers involved by each station observing the bus level bit for bit.



Why we studied the Communication Protocol

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• To learn how to Analyse the Transmission protocol so that we are able to find and correct the Error in the Transmission.





