IBM System/360 Reference Data

MACHINE INSTRUCTIONS

NAME	MNEMONIC	OP CODE	FOR-MAT	OPERANDS
Add (c)	AR	1A	RR	R1,R2
Add (c)	A	5A	RX	R1,D2(X2,B2)
Add Decimal (c,d)	AP	FA	SS	D1(L1,B1),D2(L2,B2)
Add Halfword (c)	AH	4A	RX	R1,D2(X2,B2)
Add Logical (c)	ALR	1E	RR	R1,R2
Add Logical (c)	AL	5E	RX	R1,D2(X2,B2)
AND (c)	NR	14	RR	R1,R2
AND (c)	N	54	RX	R1,D2(X2,B2)
AND (c)	NI	94	SI	D1(B1),I2
AND (c)	NC	D4	SS	D1(L,B1),D2(B2)
Branch and Link	BALR	05	RR	R1,R2
Branch and Link	BAL	45	RX	R1,D2(X2,B2)
Branch and Store (e)	BASR	0D	RR	R1,R2
Branch and Store (e)	BAS	4D	RX	R1,D2(X2,B2)
Branch on Condition	BCR	07	RR	M1,R2
Branch on Condition	BC	47	RX	M1,D2(X2,B2)
Branch on Count	BCTR	06	RR	R1,R2
Branch on Count	BCT	46	RX	R1,D2(X2,B2)
Branch on Index High	BXH	86	RS	R1,R3,D2(B2)
Branch on Index Low or Equal	BXLE	87	RS	R1,R3,D2(B2)
Compare (c)	CR	19	RR	R1,R2
Compare (c)	C	59	RX	R1,D2(X2,B2)
Compare Decimal (c,d)	CP	F9	SS	D1(L1,B1),D2(L2,B2)
Compare Halfword (c)	CH	49	RX	R1,D2(X2,B2)
Compare Logical (c)	CLR	15	RR	R1,R2
Compare Logical (c)	CL	55	RX	R1,D2(X2,B2)
Compare Logical (c)	CLC	D5	SS	D1(L,B1),D2(B2)
Compare Logical (c)	CLI	95	SI	D1(B1),I2
Convert to Binary	CVB	4F	RX	R1,D2(X2,B2)
Convert to Decimal	CVD	4E	RX	R1,D2(X2,B2)
Diagnose (p)		83	SI	
Divide	DR	1D	RR	R1,R2
Divide	D	5D	RX	R1,D2(X2,B2)
Divide Decimal (d)	DP	FD	SS	D1(L1,B1),D2(L2,B2)
Edit (c,d)	ED	DE	SS	D1(L,B1),D2(B2)
Edit and Mark (c,d)	EDMK	DF	SS	D1(L,B1),D2(B2)
Exclusive OR (c)	XR	17	RR	R1,R2
Exclusive OR (c)	X	57	RX	R1,D2(X2,B2)
Exclusive OR (c)	XI	97	SI	D1(B1),I2
Exclusive OR (c)	XC	D7	SS	D1(L,B1),D2(B2)
Execute	EX	44	RX	R1,D2(X2,B2)
Halt I/O (c,p)	HIO	9E	SI	D1(B1)
Insert Character	IC	43	RX	R1,D2(X2,B2)
Insert Storage Key (a,p)	ISK	09	RR	R1,R2
Load	LR	18	RR	R1,R2
Load	L	58	RX	R1,D2(X2,B2)
Load Address	LA	41	RX	R1,D2(X2,B2)
Load and Test (c)	LTR	12	RR	R1,R2
Load Complement (c)	LCR	13	RR	R1,R2
Load Halfword	LH	48	RX	R1,D2(X2,B2)
Load Multiple	LM	98	RS	R1,R3,D2(B2)
Load Multiple Control (e,p)	LMC	B8	RS	R1,R3,D2(B2)
Load Negative (c)	LNR	11	RR	R1,R2
Load Positive (c)	LPR	10	RR	R1,R2
Load PSW (n,p)	LPSW	82	SI	D1(B1)
Load Real Address (c,e,p)	LRA	B1	RX	R1,D2(X2,B2)
Move	MVI	92	SI	D1(B1),I2
Move	MVC	D2	SS	D1(L,B1),D2(B2)
Move Numerics	MVN	D1	SS	D1(L,B1),D2(B2)
Move with Offset	MVO	F1	SS	D1(L1,B1),D2(L2,B2)
Move Zones	MVZ	D3	SS	D1(L,B1),D2(B2)
Multiply	MR	1C	RR	R1,R2
Multiply	M	5C	RX	R1,D2(X2,B2)
Multiply Decimal (d)	MP	FC	SS	D1(L1,B1),D2(L2,B2)
Multiply Halfword	MH	4C	RX	R1,D2(X2,B2)
OR (c)	OR	16	RR	R1,R2
OR (c)	O	56	RX	R1,D2(X2,B2)
OR (c)	OI	96	SI	D1(B1),I2

IBM System/360 Reference Data

MACHINE INSTRUCTIONS

NAME	MNEMONIC	OP CODE	FORMAT	OPERANDS
Add (c)	AR	1A	RR	R1,R2
Add (c)	A	5A	RX	R1,D2(X2,B2)
Add Decimal (c,d)	AP	FA	SS	D1(L1,B1),D2(L2,B2)
Add Halfword (c)	AH	4A	RX	R1,D2(X2,B2)
Add Logical (c)	ALR	1E	RR	R1,R2
Add Logical (c)	AL	5E	RX	R1,D2(X2,B2)
AND (c)	NR	14	RR	R1,R2
AND (c)	N	54	RX	R1,D2(X2,B2)
AND (c)	NI	94	SI	D1(B1),I2
AND (c)	NC	D4	SS	D1(L,B1),D2(B2)
Branch and Link	BALR	05	RR	R1,R2
Branch and Link	BAL	45	RX	R1,D2(X2,B2)
Branch and Store (e)	BASR	0D	RR	R1,R2
Branch and Store (e)	BAS	4D	RX	R1,D2(X2,B2)
Branch on Condition	BCR	07	RR	M1,R2
Branch on Condition	BC	47	RX	M1,D2(X2,B2)
Branch on Count	BCTR	06	RR	R1,R2
Branch on Count	BCT	46	RX	R1,D2(X2,B2)
Branch on Index High	BXH	86	RS	R1,R3,D2(B2)
Branch on Index Low or Equal	BXLE	87	RS	R1,R3,D2(B2)
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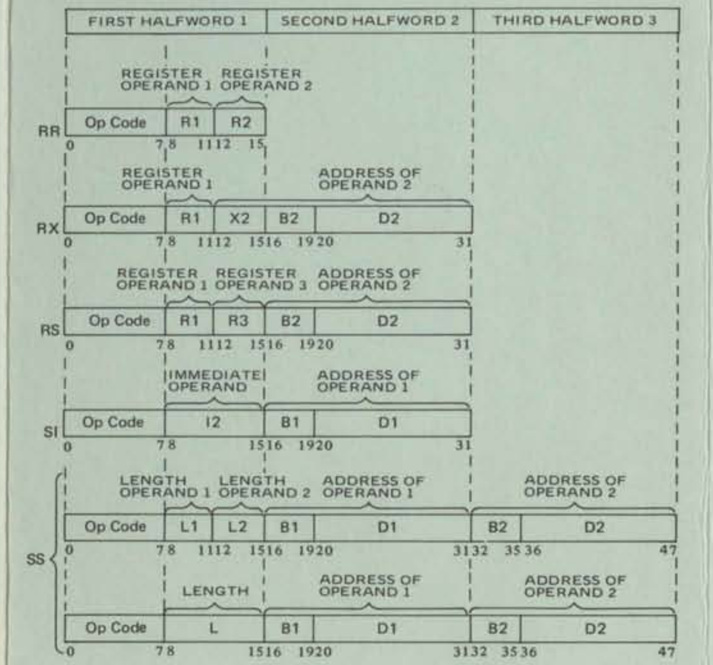
Compare (c)	C	59	RX	R1,D2(X2,B2)
Compare Decimal (c,d)	CP	F9	SS	D1(L1,B1),D2(L2,B2)
Compare Halfword (c)	CH	49	RX	R1,D2(X2,B2)
Compare Logical (c)	CLR	15	RR	R1,R2
Compare Logical (c)	CL	55	RX	R1,D2(X2,B2)
Compare Logical (c)	CLC	D5	SS	D1(L,B1),D2(B2)
Compare Logical (c)	CLI	95	SI	D1(B1),I2
Convert to Binary	CVB	4F	RX	R1,D2(X2,B2)
Convert to Decimal	CVD	4E	RX	R1,D2(X2,B2)
Diagnose (p)		83	SI	
Divide	DR	1D	RR	R1,R2
Divide	D	5D	RX	R1,D2(X2,B2)
Divide Decimal (d)	DP	FD	SS	D1(L1,B1),D2(L2,B2)
Edit (c,d)	ED	DE	SS	D1(L,B1),D2(B2)
Edit and Mark (c,d)	EDMK	DF	SS	D1(L,B1),D2(B2)
Exclusive OR (c)	XR	17	RR	R1,R2
Exclusive OR (c)	X	57	RX	R1,D2(X2,B2)
Exclusive OR (c)	XI	97	SI	D1(B1),I2
Exclusive OR (c)	XC	D7	SS	D1(L,B1),D2(B2)
Execute	EX	44	RX	R1,D2(X2,B2)
Halt I/O (c,p)	HIO	9E	SI	D1(B1)
Insert Character	IC	43	RX	R1,D2(X2,B2)
Insert Storage Key (a,p)	ISK	09	RR	R1,R2
Load	LR	18	RR	R1,R2
Load	L	58	RX	R1,D2(X2,B2)
Load Address	LA	41	RX	R1,D2(X2,B2)
Load and Test (c)	LTR	12	RR	R1,R2
Load Complement (c)	LCR	13	RR	R1,R2
Load Halfword	LH	48	RX	R1,D2(X2,B2)
Load Multiple	LM	98	RS	R1,R3,D2(B2)
Load Multiple Control (e,p)	LMC	B8	RS	R1,R3,D2(B2)
Load Negative (c)	LNR	11	RR	R1,R2
Load Positive (c)	LPR	10	RR	R1,R2
Load PSW (n,p)	LPSW	82	SI	D1(B1)
Load Real Address (c,e,p)	LRA	B1	RX	R1,D2(X2,B2)
Move	MVI	92	SI	D1(B1),I2
Move	MVC	D2	SS	D1(L,B1),D2(B2)
Move Numerics	MVN	D1	SS	D1(L,B1),D2(B2)
Move with Offset	MVO	F1	SS	D1(L1,B1),D2(L2,B2)
Move Zones	MVZ	D3	SS	D1(L,B1),D2(B2)
Multiply	MR	1C	RR	R1,R2
Multiply	M	5C	RX	R1,D2(X2,B2)
Multiply Decimal (d)	MP	FC	SS	D1(L1,B1),D2(L2,B2)
Multiply Halfword	MH	4C	RX	R1,D2(X2,B2)
OR (c)	OR	16	RR	R1,R2
OR (c)	O	56	RX	R1,D2(X2,B2)
OR (c)	OI	96	SI	D1(B1),I2
OR (c)	OC	D6	SS	D1(L,B1),D2(B2)
Pack	PACK	F2	SS	D1(L1,B1),D2(L2,B2)
Read Direct (b,p)	RDD	85	SI	D1(B1),I2
Set Program Mask (n)	SPM	04	RR	R1
Set Storage Key (a,p)	SSK	08	RR	R1,R2
Set System Mask (p)	SSM	80	SI	D1(B1)
Shift Left Double (c)	SLDA	8F	RS	R1,D2(B2)
Shift Left Double Logical	SLDL	8D	RS	R1,D2(B2)
Shift Left Single (c)	SLA	8B	RS	R1,D2(B2)
Shift Left Single Logical	SLL	89	RS	R1,D2(B2)
Shift Right Double (c)	SRDA	8E	RS	R1,D2(B2)
Shift Right Double Logical	SRDL	8C	RS	R1,D2(B2)
Shift Right Single (c)	SRA	8A	RS	R1,D2(B2)
Shift Right Single Logical	SRL	88	RS	R1,D2(B2)
Start I/O (c,p)	SIO	9C	SI	D1(B1)
Store	ST	50	RX	R1,D2(X2,B2)
Store Character	STC	42	RX	R1,D2(X2,B2)
Store Halfword	STH	40	RX	R1,D2(X2,B2)
Store Multiple	STM	90	RS	R1,R3,D2(B2)
Store Multiple Control (e,p)	STMC	B0	RS	R1,R3,D2(B2)
Subtract (c)	SR	1B	RR	R1,R2
Subtract (c)	S	5B	RX	R1,D2(X2,B2)
Subtract Decimal (c,d)	SP	FB	SS	D1(L1,B1),D2(L2,B2)
Subtract Halfword (c)	SH	4B	RX	R1,D2(X2,B2)
Subtract Logical (c)	SLR	1F	RR	R1,R2
Subtract Logical (c)	SL	5F	RX	R1,D2(X2,B2)
Supervisor Call	SVC	0A	RR	I
Test and Set (c)	TS	93	SI	D1(B1)
Test Channel (c,p)	TCH	9F	SI	D1(B1)
Test I/O (c,p)	TIO	9D	SI	D1(B1)
Test under Mask (c)	TM	91	SI	D1(B1),I2
Translate	TR	DC	SS	D1(L,B1),D2(B2)
Translate and Test (c)	TRT	DD	SS	D1(L,B1),D2(B2)
Unpack	UNPK	F3	SS	D1(L1,B1),D2(L2,B2)
Write Direct (b,p)	WRD	84	SI	D1(B1),I2
Zero and Add (c,d)	ZAP	F8	SS	D1(L1,B1),D2(L2,B2)

NOTES FOR PANELS 1-3

a. Protection feature
b. Direct control feature
c. Condition code is set
d. Decimal feature
e. Model 67
n. New condition code is loaded
p. Privileged instruction
x. Extended precision floating point feature

MACHINE FORMATS



FLOATING-POINT FEATURE INSTRUCTIONS

NAME	MNEMONIC	OP CODE	FORMAT	OPERANDS
Add Normalized, Extended (c,x)	AXR	36	RR	R1,R2
Add Normalized, Long (c)	ADR	2A	RR	R1,R2
Add Normalized, Long (c)	AD	6A	RX	R1,D2(X2,B2)
Add Normalized, Short (c)	AER	3A	RR	R1,R2
Add Normalized, Short (c)	AE	7A	RX	R1,D2(X2,B2)
Add Unnormalized, Long (c)	AWR	2E	RR	R1,R2
Add Unnormalized, Long (c)	AW	6E	RX	R1,D2(X2,B2)
Add Unnormalized, Short (c)	AUR	3E	RR	R1,R2
Add Unnormalized, Short (c)	AU	7E	RX	R1,D2(X2,B2)
Compare, Long (c)	CDR	29	RR	R1,R2
Compare, Long (c)	CD	69	RX	R1,D2(X2,B2)
Compare, Short (c)	CER	39	RR	R1,R2
Compare, Short (c)	CE	79	RX	R1,D2(X2,B2)
Divide, Long	DDR	2D	RR	R1,R2
Divide, Long	DD	6D	RX	R1,D2(X2,B2)
Divide, Short	DER	3D	RR	R1,R2
Divide, Short	DE	7D	RX	R1,D2(X2,B2)
Halve, Long	HDR	24	RR	R1,R2
Halve, Short	HER	34	RR	R1,R2
Load and Test, Long (c)	LTDR	22	RR	R1,R2
Load and Test, Short (c)	LTER	32	RR	R1,R2
Load Complement, Long (c)	LCDR	23	RR	R1,R2
Load Complement, Short (c)	LCER	33	RR	R1,R2
Load, Long	LDR	28	RR	R1,R2
Load, Long	LD	68	RX	R1,D2(X2,B2)
Load Negative, Long (c)	LNDR	21	RR	R1,R2
Load Negative, Short (c)	LNER	31	RR	R1,R2
Load Positive, Long (c)	LPDR	20	RR	R1,R2
Load Positive, Short (c)	LPER	30	RR	R1,R2
Load Rounded, Extended to Long (x)	LRDR	25	RR	R1,R2
Load Rounded, Long to Short (x)	LRER	35	RR	R1,R2
Load, Short	LER	38	RR	R1,R2
Load, Short	LE	78	RX	R1,D2(X2,B2)
Multiply, Extended (x)	MXR	26	RR	R1,R2
Multiply, Long	MDR	2C	RR	R1,R2
Multiply, Long	MD	6C	RX	R1,D2(X2,B2)
Multiply, Long/Extended (x)	MXDR	27	RR	R1,R2
Multiply, Long/Extended (x)	MXD	67	RX	R1,D2(X2,B2)
Multiply, Short	MER	3C	RR	R1,R2
Multiply, Short	ME	7C	RX	R1,D2(X2,B2)
Store, Long	STD	60	RX	R1,D2(X2,B2)
Store, Short	STE	70	RX	R1,D2(X2,B2)
Subtract Normalized, Extended (c,x)	SXR	37	RR	R1,R2
Subtract Normalized, Long (c)	SDR	2B	RR	R1,R2
Subtract Normalized, Long (c)	SD	6B	RX	R1,D2(X2,B2)
Subtract Normalized, Short (c)	SER	3B	RR	R1,R2
Subtract Normalized, Short (c)	SE	7B	RX	R1,D2(X2,B2)
Subtract Unnormalized, Long (c)	SWR	2F	RR	R1,R2
Subtract Unnormalized, Long (c)	SW	6F	RX	R1,D2(X2,B2)
Subtract Unnormalized, Short (c)	SUR	3F	RR	R1,R2
Subtract Unnormalized, Short (c)	SU	7F	RX	R1,D2(X2,B2)

SUMMARY OF CONSTANTS

TYPE	IMPLIED LENGTH, BYTES	ALIGNMENT	FORMAT	TRUNCATION/ PADDING
C	–	byte	characters	right
X	–	byte	hexadecimal digits	left
B	–	byte	binary digits	left
F	4	word	fixed-point binary	left
H	2	halfword	fixed-point binary	left
E	4	word	short floating-point	right
D	8	doubleword	long floating-point	right
L	16	doubleword	extended floating-point	right
P	–	byte	packed decimal	left
Z	–	byte	zoned decimal	left
A	4	word	value of address	left
Y	2	halfword	value of address	left
S	2	halfword	address in base-displacement form	–
V	4	word	externally defined address value	left
Q*	4	word	symbol naming a DXD or DSECT	left

*OS only

EXTENDED MNEMONIC INSTRUCTION CODES

GENERAL

Extended Code		Machine Instruction		Meaning
B	D2(X2,B2)	BC 15,	D2(X2,B2)	Branch Unconditionally
BR	R2	BCR 15,	R2	Branch Unconditionally
NOP	D2(X2,B2)	BC 0,	D2(X2,B2)	No Operation
NOPR	R2	BCR 0,	R2	No Operation (RR)

AFTER COMPARE INSTRUCTIONS (A:B)

BH	D2(X2,B2)	BC 2,	D2(X2,B2)	Branch on A High
BL	D2(X2,B2)	BC 4,	D2(X2,B2)	Branch on A Low
BE	D2(X2,B2)	BC 8,	D2(X2,B2)	Branch on Equal B
BNH	D2(X2,B2)	BC 13,	D2(X2,B2)	Branch on A Not High
BNL	D2(X2,B2)	BC 11,	D2(X2,B2)	Branch on A Not Low
BNE	D2(X2,B2)	BC 7,	D2(X2,B2)	Branch on A Not Equal B

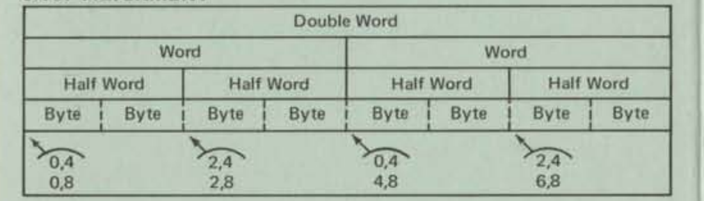
AFTER ARITHMETIC INSTRUCTIONS

BO	D2(X2,B2)	BC 1,	D2(X2,B2)	Branch on Overflow
BP	D2(X2,B2)	BC 2,	D2(X2,B2)	Branch on Plus
BM	D2(X2,B2)	BC 4,	D2(X2,B2)	Branch on Minus
BZ	D2(X2,B2)	BC 8,	D2(X2,B2)	Branch on Zero
BNP	D2(X2,B2)	BC 13,	D2(X2,B2)	Branch on Not Plus
BNM	D2(X2,B2)	BC 11,	D2(X2,B2)	Branch on Not Minus
BNZ	D2(X2,B2)	BC 7,	D2(X2,B2)	Branch on Not Zero

AFTER TEST UNDER MASK INSTRUCTIONS

BO	D2(X2,B2)	BC 1,	D2(X2,B2)	Branch if Ones
BM	D2(X2,B2)	BC 4,	D2(X2,B2)	Branch if Mixed
BZ	D2(X2,B2)	BC 8,	D2(X2,B2)	Branch if Zeros
BNO	D2(X2,B2)	BC 14,	D2(X2,B2)	Branch if Not Ones

CNOP ALIGNMENT



EDIT AND EDMK PATTERN CHARACTERS (in hex)

20–digit selector	40–blank	5C–asterisk
21–start of significance	4B–period	6B–comma
22–field separator	5B–dollar sign	C3D9–CR

PERMANENT STORAGE ASSIGNMENTS

ADDRESS DEC	HEX	LENGTH	PURPOSE
0	0	double word	Initial program loading PSW
8	8	double word	Initial program loading CCW1
16	10	double word	Initial program loading CCW2
24	18	double word	External old PSW
32	20	double word	Supervisor Call old PSW
40	28	double word	Program old PSW
48	30	double word	Machine-check old PSW
56	38	double word	Input/output old PSW
64	40	double word	Channel status word
72	48	word	Channel address word
76	4C	word	Unused
80	50	word	Timer (uses bytes 50, 51 & 52)
84	54	word	Unused
88	58	double word	External new PSW
96	60	double word	Supervisor Call new PSW
104	68	double word	Program new PSW
112	70	double word	Machine-check new PSW
120	78	double word	Input/output new PSW
128	80	(1)	Diagnostic scan-out area

(1) The size of the diagnostic scan-out area depends on the particular model and I/O channels; for models 30 through 75, maximum size is 256 bytes.

CONDITION CODES

Condition Code Setting	0	1	2	3
Mask Bit Position	8	4	2	1

FLOATING-POINT ARITHMETIC

Add Normalized S/L/E	zero	<zero	>zero	–
Add Unnormalized S/L	zero	<zero	>zero	–
Compare S/L (A:B)	equal	A low	A high	–
Load and Test S/L	zero	<zero	>zero	–
Load Complement S/L	zero	<zero	>zero	–
Load Negative S/L	zero	<zero	–	–
Load Positive S/L	zero	–	>zero	–
Subtract Normalized S/L/E	zero	<zero	>zero	–
Subtract Unnormalized S/L	zero	<zero	>zero	–

FIXED-POINT AND DECIMAL ARITHMETIC

Add H/F/Dec.	zero	<zero	>zero	overflow
Add Logical	zero, no carry	not zero, no carry	zero, carry	not zero, carry
Compare H/F/Dec. (A:B)	equal	A low	A high	–
Load and Test	zero	<zero	>zero	–
Load Complement	zero	<zero	>zero	overflow
Load Negative	zero	<zero	–	–
Load Positive	zero	–	>zero	overflow
Shift Left Single/Double	zero	<zero	>zero	overflow
Shift Right Single/Double	zero	<zero	>zero	–
Subtract H/F/Dec.	zero	<zero	>zero	overflow
Subtract Logical	–	not zero, no carry	zero, carry	not zero, carry
Zero and Add	zero	<zero	>zero	overflow

LOGICAL OPERATIONS

AND	zero	not zero	–	–
Compare Logical (A:B)	equal	A low	A high	–
Edit	zero	<zero	>zero	–
Edit and Mark	zero	<zero	>zero	–
Exclusive OR	zero	not zero	–	–
OR	zero	not zero	–	–
Test under Mask	zero	mixed	–	one
Translate and Test	zero	incomplete	complete	–

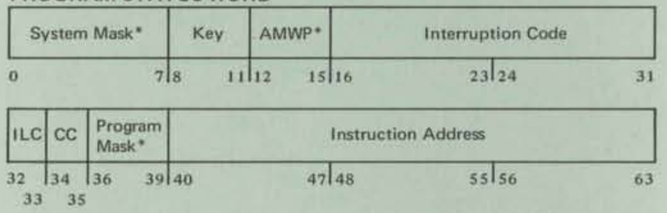
INPUT/OUTPUT OPERATIONS

Halt I/O	interruption pending	CSW stored	halted	not oper
Start I/O	started	CSW stored	busy	not oper
Test I/O	available	CSW stored	busy	not oper
Test Channel	available	interruption pending	burst mode	not oper

MISC. OPERATIONS

Test and Set	zero	one	–	–
Load Real Address (Mod. 67)	successful	segment unavailable	page unavailable	–

PROGRAM STATUS WORD



0 Multiplexer channel mask
1 Selector channel 1 mask
2 Selector channel 2 mask
3 Selector channel 3 mask
4 Selector channel 4 mask
5 Selector channel 5 mask
6 Selector channel 6 mask
7 External mask
12 ASCII-8 mode (A)
13 Machine check mask (M)
14 Wait state (W)
15 Problem state (P)
32-33 Instruction length code (ILC)
34-35 Condition code (CC)
36 Fixed-point overflow mask
37 Decimal overflow mask
38 Exponent underflow mask
39 Significance mask

*A one-bit equals on, and permits an interrupt.

CODES FOR PROGRAM INTERRUPTION

Interruption Code		Program Interruption Cause	Interruption Code		Program Interruption Cause
Dec	Hex		Dec	Hex	
1	0001	Operation	10	000A	Decimal overflow
2	0002	Privileged operation	11	000B	Decimal divide
3	0003	Execute	12	000C	Exponent overflow
4	0004	Protection	13	000D	Exponent underflow
5	0005	Addressing	14	000E	Significance
6	0006	Specification	15	000F	Floating-point divide
7	0007	Data	16*	0010	Segment translation
8	0008	Fixed-point overflow	17*	0011	Page translation
9	0009	Fixed-point divide			

*Model 67

HEXADECIMAL AND DECIMAL CONVERSION

From hex: locate each hex digit in its corresponding column position and note the decimal equivalents. Add these to obtain the decimal value.

From decimal: (1) locate the largest decimal value in the table that will fit into the decimal number to be converted, and (2) note its hex equivalent and hex column position. (3) Find the decimal remainder. Repeat the process on this and subsequent remainders.

HEXADECIMAL COLUMNS											
6		5		4		3		2		1	
HEX	= DEC	HEX	= DEC	HEX	= DEC	HEX	= DEC	HEX	= DEC	HEX	= DEC
0	0	0	0	0	0	0	0	0	0	0	0
1	1,048,576	1	65,536	1	4,096	1	256	1	16	1	1
2	2,097,152	2	131,072	2	8,192	2	512	2	32	2	2
3	3,145,728	3	196,608	3	12,288	3	768	3	48	3	3
4	4,194,304	4	262,144	4	16,384	4	1,024	4	64	4	4
5	5,242,880	5	327,680	5	20,480	5	1,280	5	80	5	5
6	6,291,456	6	393,216	6	24,576	6	1,536	6	96	6	6
7	7,340,032	7	458,752	7	28,672	7	1,792	7	112	7	7
8	8,388,608	8	524,288	8	32,768	8	2,048	8	128	8	8
9	9,437,184	9	589,824	9	36,864	9	2,304	9	144	9	9
A	10,485,760	A	655,360	A	40,960	A	2,560	A	160	A	10
B	11,534,336	B	720,896	B	45,056	B	2,816	B	176	B	11
C	12,582,912	C	786,432	C	49,152	C	3,072	C	192	C	12
D	13,631,488	D	851,968	D	53,248	D	3,328	D	208	D	13
E	14,680,064	E	917,504	E	57,344	E	3,584	E	224	E	14
F	15,728,640	F	983,040	F	61,440	F	3,840	F	240	F	15
0123		4567		0123		4567		0123		4567	
BYTE				BYTE				BYTE			

BINARY CONVERSION

Dec	= Hex	= Binary
0	0	0000
1	1	0001
2	2	0010
3	3	0011
4	4	0100
5	5	0101
6	6	0110
7	7	0111
8	8	1000
9	9	1001
10	A	1010
11	B	1011
12	C	1100
13	D	1101
14	E	1110
15	F	1111
16	10	0001 0000

POWERS OF 16 TABLE

16^n	n
1	0
16	1
256	2
4 096	3
65 536	4
1 048 576	5
16 777 216	6
268 435 456	7
4 294 967 296	8
68 719 476 736	9
1 099 511 627 776	10
17 592 186 044 416	11
281 474 976 710 656	12
4 503 599 627 370 496	13
72 057 594 037 927 936	14
1 152 921 504 606 846 976	15

Comments about this card may be sent to the Technical Publications Dept. at the White Plains address below. All comments and suggestions become the property of IBM.

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Decimal	Hexadecimal	Instruction Mnemonic (RR Format)	Graphic & Control Symbols BCDIC	Graphic & Control Symbols EBCDIC	7-Track Tape BCDIC	Punched Card Code	System/360 8-bit Code
0	00			NUL		12-0-1-8-9	0000 0000
1	01			SOH		12-1-9	0000 0001
2	02			STX		12-2-9	0000 0010
3	03			ETX		12-3-9	0000 0011
4	04	SPM		PF		12-4-9	0000 0100
5	05	BALR		HT		12-5-9	0000 0101
6	06	BCTR		LC		12-6-9	0000 0110
7	07	BCR		DEL		12-7-9	0000 0111
8	08	SSK				12-8-9	0000 1000
9	09	ISK				12-1-8-9	0000 1001
10	0A	SVC		SMM		12-2-8-9	0000 1010
11	0B			VT		12-3-8-9	0000 1011
12	0C			FF		12-4-8-9	0000 1100
13	0D	BASR (4)		CR		12-5-8-9	0000 1101
14	0E			SO		12-6-8-9	0000 1110
15	0F			SI		12-7-8-9	0000 1111
16	10	LPR		DLE		12-11-1-8-9	0001 0000
17	11	LNR		DC1		11-1-9	0001 0001
18	12	LTR		DC2		11-2-9	0001 0010
19	13	LCR		TM		11-3-9	0001 0011
20	14	NR		RES		11-4-9	0001 0100
21	15	CLR		NL		11-5-9	0001 0101
22	16	OR		BS		11-6-9	0001 0110
23	17	XR		IL		11-7-9	0001 0111
24	18	LR		CAN		11-8-9	0001 1000
25	19	CR		EM		11-1-8-9	0001 1001
26	1A	AR		CC		11-2-8-9	0001 1010
27	1B	SR		CU1		11-3-8-9	0001 1011
28	1C	MR		IFS		11-4-8-9	0001 1100
29	1D	DR		IGS		11-5-8-9	0001 1101
30	1E	ALR		IRS		11-6-8-9	0001 1110
31	1F	SLR		IUS		11-7-8-9	0001 1111
32	20	LPDR		DS		11-0-1-8-9	0010 0000
33	21	LNDR		SOS		0-1-9	0010 0001
34	22	LTDR		FS		0-2-9	0010 0010
35	23	LCDR				0-3-9	0010 0011
36	24	HDR		BYP		0-4-9	0010 0100
37	25	LRDR		LF		0-5-9	0010 0101
38	26	MXR		ETB		0-6-9	0010 0110
39	27	MXDR		ESC		0-7-9	0010 0111
40	28	LDR				0-8-9	0010 1000
41	29	CDR				0-1-8-9	0010 1001
42	2A	ADR		SM		0-2-8-9	0010 1010
43	2B	SDR		CU2		0-3-8-9	0010 1011
44	2C	MDR				0-4-8-9	0010 1100
45	2D	DDR		ENQ		0-5-8-9	0010 1101
46	2E	AWR		ACK		0-6-8-9	0010 1110
47	2F	SWR		BEL		0-7-8-9	0010 1111
48	30	LPER				12-11-0-1-8-9	0011 0000
49	31	LNER				1-9	0011 0001
50	32	LTER		SYN		2-9	0011 0010
51	33	LCER				3-9	0011 0011
52	34	HER		PN		4-9	0011 0100
53	35	LRER		RS		5-9	0011 0101
54	36	AXR		UC		6-9	0011 0110
55	37	SXR		EOT		7-9	0011 0111
56	38	LER				8-9	0011 1000
57	39	CER				1-8-9	0011 1001
58	3A	AER				2-8-9	0011 1010
59	3B	SER		CU3		3-8-9	0011 1011
60	3C	MER		DC4		4-8-9	0011 1100
61	3D	DER		NAK		5-8-9	0011 1101
62	3E	AUR				6-8-9	0011 1110
63	3F	SUR		SUB		7-8-9	0011 1111

NOTES FOR PANELS 7 - 10

1. Add C (check bit) for odd or even parity as needed, except as noted
2. For even parity use CA
3. Decimal feature
4. Model 67
5. EBCDIC code required for graphics) + (= and '

RR FORMAT

Op Code	R_1	R_2
0	7 8 11	12 15

Decimal	Hexadecimal	Instruction Mnemonic (RX Format)	Graphic & Control Symbols BCDIC	Graphic & Control Symbols EBCDIC	7-Track Tape BCDIC (1)	Punched Card Code	System/360 8-bit Code
64	40	STH		SP	(2)	no punches	0100 0000
65	41	LA				12-0-1-9	0100 0001
66	42	STC				12-0-2-9	0100 0010
67	43	IC				12-0-3-9	0100 0011
68	44	EX				12-0-4-9	0100 0100
69	45	BAL				12-0-5-9	0100 0101
70	46	BCT				12-0-6-9	0100 0110
71	47	BC				12-0-7-9	0100 0111
72	48	LH				12-0-8-9	0100 1000
73	49	CH				12-1-8	0100 1001
74	4A	AH		¢		12-2-8	0100 1010
75	4B	SH	.	.	B A 8 21	12-3-8	0100 1011
76	4C	MH	⌑)(5)	<	B A 8 4	12-4-8	0100 1100
77	4D	BAS (4)	[	(	B A 8 4 1	12-5-8	0100 1101
78	4E	CVD	<	+	B A 8 4 2	12-6-8	0100 1110
79	4F	CVB	ǂ	|	B A 8 4 2 1	12-7-8	0100 1111
80	50	ST	& + (5)	&	B A	12	0101 0000
81	51					12-11-1-9	0101 0001
82	52					12-11-2-9	0101 0010
83	53					12-11-3-9	0101 0011
84	54	N				12-11-4-9	0101 0100
85	55	CL				12-11-5-9	0101 0101
86	56	O				12-11-6-9	0101 0110
87	57	X				12-11-7-9	0101 0111
88	58	L				12-11-8-9	0101 1000
89	59	C				11-1-8	0101 1001
90	5A	A		!		11-2-8	0101 1010
91	5B	S	$	$	B 8 21	11-3-8	0101 1011
92	5C	M	*	*	B 8 4	11-4-8	0101 1100
93	5D	D	]	)	B 8 4 1	11-5-8	0101 1101
94	5E	AL	;	;	B 8 4 2	11-6-8	0101 1110
95	5F	SL	Δ	¬	B 8 4 2 1	11-7-8	0101 1111
96	60	STD	-		B	11	0110 0000
97	61		/	/	A 1	0-1	0110 0001
98	62					11-0-2-9	0110 0010
99	63					11-0-3-9	0110 0011
100	64					11-0-4-9	0110 0100
101	65					11-0-5-9	0110 0101
102	66					11-0-6-9	0110 0110
103	67	MXD				11-0-7-9	0110 0111
104	68	LD				11-0-8-9	0110 1000
105	69	CD				0-1-8	0110 1001
106	6A	AD				12-11	0110 1010
107	6B	SD	,	,	A 8 21	0-3-8	0110 1011
108	6C	MD	% ((5)	%	A 8 4	0-4-8	0110 1100
109	6D	DD	⋎	_	A 8 4 1	0-5-8	0110 1101
110	6E	AW	\	>	A 8 4 2	0-6-8	0110 1110
111	6F	SW	⧻	?	A 8 4 2 1	0-7-8	0110 1111
112	70	STE				12-11-0	0111 0000
113	71					12-11-0-1-9	0111 0001
114	72					12-11-0-2-9	0111 0010
115	73					12-11-0-3-9	0111 0011
116	74					12-11-0-4-9	0111 0100
117	75					12-11-0-5-9	0111 0101
118	76					12-11-0-6-9	0111 0110
119	77					12-11-0-7-9	0111 0111
120	78	LE				12-11-0-8-9	0111 1000
121	79	CE				1-8	0111 1001
122	7A	AE	ƀ	:	A	2-8	0111 1010
123	7B	SE	# = (5)	#	8 21	3-8	0111 1011
124	7C	ME	@ ' (5)	@	8 4	4-8	0111 1100
125	7D	DE	:	'	8 4 1	5-8	0111 1101
126	7E	AU	>	=	8 4 2	6-8	0111 1110
127	7F	SU	√	"	8 4 2 1	7-8	0111 1111

RX FORMAT

Op Code	R_1	X_2	B_2	D_2
0	7 8 11	12 15	16 19	20 31

R1, D2 (X2, B2) or R1, S2 (X2)
R1, D2 (0, B2) or R1, S2

Decimal	Hexadecimal	Instruction Mnemonic (Var. Formats)	Graphic & Control Symbols BCDIC	Graphic & Control Symbols EBCDIC	7-Track Tape BCDIC	Punched Card Code	System/360 8-bit Code
128	80	SSM				12-0-1-8	1000 0000
129	81			a		12-0-1	1000 0001
130	82	LPSW		b		12-0-2	1000 0010
131	83	(Diagnose)		c		12-0-3	1000 0011
132	84	WRD		d		12-0-4	1000 0100
133	85	RDD		e		12-0-5	1000 0101
134	86	BXH		f		12-0-6	1000 0110
135	87	BXLE		g		12-0-7	1000 0111
136	88	SRL		h		12-0-8	1000 1000
137	89	SLL		i		12-0-9	1000 1001
138	8A	SRA				12-0-2-8	1000 1010
139	8B	SLA				12-0-3-8	1000 1011
140	8C	SRDL				12-0-4-8	1000 1100
141	8D	SLDL				12-0-5-8	1000 1101
142	8E	SRDA				12-0-6-8	1000 1110
143	8F	SLDA				12-0-7-8	1000 1111
144	90	STM				12-11-1-8	1001 0000
145	91	TM		j		12-11-1	1001 0001
146	92	MVI		k		12-11-2	1001 0010
147	93	TS		l		12-11-3	1001 0011
148	94	NI		m		12-11-4	1001 0100
149	95	CLI		n		12-11-5	1001 0101
150	96	OI		o		12-11-6	1001 0110
151	97	XI		p		12-11-7	1001 0111
152	98	LM		q		12-11-8	1001 1000
153	99			r		12-11-9	1001 1001
154	9A					12-11-2-8	1001 1010
155	9B					12-11-3-8	1001 1011
156	9C	SIO				12-11-4-8	1001 1100
157	9D	TIO				12-11-5-8	1001 1101
158	9E	HIO				12-11-6-8	1001 1110
159	9F	TCH				12-11-7-8	1001 1111
160	A0					11-0-1-8	1010 0000
161	A1					11-0-1	1010 0001
162	A2			s		11-0-2	1010 0010
163	A3			t		11-0-3	1010 0011
164	A4			u		11-0-4	1010 0100
165	A5			v		11-0-5	1010 0101
166	A6			w		11-0-6	1010 0110
167	A7			x		11-0-7	1010 0111
168	A8			y		11-0-8	1010 1000
169	A9			z		11-0-9	1010 1001
170	AA					11-0-2-8	1010 1010
171	AB					11-0-3-8	1010 1011
172	AC					11-0-4-8	1010 1100
173	AD					11-0-5-8	1010 1101
174	AE					11-0-6-8	1010 1110
175	AF					11-0-7-8	1010 1111
176	B0	STMC (4)				12-11-0-1-8	1011 0000
177	B1	LRA (4)				12-11-0-1	1011 0001
178	B2					12-11-0-2	1011 0010
179	B3					12-11-0-3	1011 0011
180	B4					12-11-0-4	1011 0100
181	B5					12-11-0-5	1011 0101
182	B6					12-11-0-6	1011 0110
183	B7					12-11-0-7	1011 0111
184	B8	LMC (4)				12-11-0-8	1011 1000
185	B9					12-11-0-9	1011 1001
186	BA					12-11-0-2-8	1011 1010
187	BB					12-11-0-3-8	1011 1011
188	BC					12-11-0-4-8	1011 1100
189	BD					12-11-0-5-8	1011 1101
190	BE					12-11-0-6-8	1011 1110
191	BF					12-11-0-7-8	1011 1111

RS FORMAT

Op Code	R_1	R_3	B_2	D_2
0	7 8 11	12 15	16 19	20 31

R1, R3, D2 (B2) or R1, R3, S2: BXH, BXLE, LM, LMC, STM, STMC
R1, D2 (B2) or R1, S2: All shift instructions

SI FORMAT

OP Code	I_2	B_1	D_1
0	7 8 15	16 19	20 31

D1 (B1) or S1: LPSW, SSM, HIO, SIO, TIO, TCH, TS
D1 (B1) , I2 or S1, I2: MVI, CLI, NI, OI, XI, TM, WRD, RDD

Decimal	Hexadecimal	Instruction Mnemonic (SS Format)	Graphic & Control Symbols		7-Track Tape BCDIC (1)	Punched Card Code	System/360 8-bit Code
			BCDIC	EBCDIC			
192	C0		?		B A 8 2	12-0	1100 0000
193	C1		A	A	B A 1	12-1	1100 0001
194	C2		B	B	B A 2	12-2	1100 0010
195	C3		C	C	B A 2 1	12-3	1100 0011
196	C4		D	D	B A 4	12-4	1100 0100
197	C5		E	E	B A 4 1	12-5	1100 0101
198	C6		F	F	B A 4 2	12-6	1100 0110
199	C7		G	G	B A 4 2 1	12-7	1100 0111
200	C8		H	H	B A 8	12-8	1100 1000
201	C9		I	I	B A 8 1	12-9	1100 1001
202	CA					12-0-2-8-9	1100 1010
203	CB					12-0-3-8-9	1100 1011
204	CC					12-0-4-8-9	1100 1100
205	CD					12-0-5-8-9	1100 1101
206	CE					12-0-6-8-9	1100 1110
207	CF					12-0-7-8-9	1100 1111
208	D0		!		B 8 2	11-0	1101 0000
209	D1	MVN	J	J	B 1	11-1	1101 0001
210	D2	MVC	K	K	B 2	11-2	1101 0010
211	D3	MVZ	L	L	B 2 1	11-3	1101 0011
212	D4	NC	M	M	B 4	11-4	1101 0100
213	D5	CLC	N	N	B 4 1	11-5	1101 0101
214	D6	OC	O	O	B 4 2	11-6	1101 0110
215	D7	XC	P	P	B 4 2 1	11-7	1101 0111
216	D8		Q	Q	B 8	11-8	1101 1000
217	D9		R	R	B 8 1	11-9	1101 1001
218	DA					12-11-2-8-9	1101 1010
219	DB					12-11-3-8-9	1101 1011
220	DC	TR				12-11-4-8-9	1101 1100
221	DD	TRT				12-11-5-8-9	1101 1101
222	DE	ED (3)				12-11-6-8-9	1101 1110
223	DF	EDMK (3)				12-11-7-8-9	1101 1111
224	E0		‡		A 8 2	0-2-8	1110 0000
225	E1					11-0-1-9	1110 0001
226	E2		S	S	A 2	0-2	1110 0010
227	E3		T	T	A 2 1	0-3	1110 0011
228	E4		U	U	A 4	0-4	1110 0100
229	E5		V	V	A 4 1	0-5	1110 0101
230	E6		W	W	A 4 2	0-6	1110 0110
231	E7		X	X	A 4 2 1	0-7	1110 0111
232	E8		Y	Y	A 8	0-8	1110 1000
233	E9		Z	Z	A 8 1	0-9	1110 1001
234	EA					11-0-2-8-9	1110 1010
235	EB					11-0-3-8-9	1110 1011
236	EC					11-0-4-8-9	1110 1100
237	ED					11-0-5-8-9	1110 1101
238	EE					11-0-6-8-9	1110 1110
239	EF					11-0-7-8-9	1110 1111
240	F0		0	0	8 2	0	1111 0000
241	F1	MVO	1	1	1	1	1111 0001
242	F2	PACK	2	2	2	2	1111 0010
243	F3	UNPK	3	3	2 1	3	1111 0011
244	F4		4	4	4	4	1111 0100
245	F5		5	5	4 1	5	1111 0101
246	F6		6	6	4 2	6	1111 0110
247	F7		7	7	4 2 1	7	1111 0111
248	F8	ZAP (3)	8	8	8	8	1111 1000
249	F9	CP (3)	9	9	8 1	9	1111 1001
250	FA	AP (3)				12-11-0-2-8-9	1111 1010
251	FB	SP (3)				12-11-0-3-8-9	1111 1011
252	FC	MP (3)				12-11-0-4-8-9	1111 1100
253	FD	DP (3)				12-11-0-5-8-9	1111 1101
254	FE					12-11-0-6-8-9	1111 1110
255	FF					12-11-0-7-8-9	1111 1111

SS FORMAT

	L					
Op Code	L_1	L_2	B_1	D_1	B_2	D_2
0 7	8 11	12 15	16 19	20 31	32 35	36 47

D1 (L, B1), D2 (B2) or S1 (L), S2 } { NC, OC, XC, CLC, MVC, MVN MVZ, TR, TRT, ED, EDMK

D1 (L1, B1), D2 (L2, B2) or S1 (L1), S2 (L2) } { PACK, UNPK, MVO, AP CP, DP, MP, SP, ZAP

CHANNEL ADDRESS WORD

Key	0000	Command Address
0 3	4 7	8 15 16 23 24 31

CHANNEL COMMAND WORD

Command Code	Data Address
0 7	8 15 16 23 24 31

Flags	000	▨	Byte Count
32 36	37 39	40 47	48 55 56 63

CD Bit 32 (80) causes use of address portion of next CCW
CC Bit 33 (40) causes use of command code and data address of next CCW
SLI Bit 34 (20) causes suppression of possible incorrect length indication
SKIP Bit 35 (10) suppresses transfer of information to main storage
PCI Bit 36 (08) causes an interruption as Program Control Interrupt

CHANNEL STATUS WORD

Key	0000	Command Address
0 3	4 7	8 15 16 23 24 31

Status	Byte Count
32 39 40 47	48 55 56 63

32 (8000) Attention
33 (4000) Status modifier
34 (2000) Control unit end
35 (1000) Busy
36 (0800) Channel end
37 (0400) Device end
38 (0200) Unit check
39 (0100) Unit exception

40 (0080) Program-controlled interruption
41 (0040) Incorrect length
42 (0020) Program check
43 (0010) Protection check
44 (0008) Channel data check
45 (0004) Channel control check
46 (0002) Interface control check
47 (0001) Chaining check

Byte Count: bits 48-63 form the residual count for the last CCW used.

DASD CHANNEL COMMAND CODES (see GA26-5988 and GA26-3599)

Command for CCW		Count	M-T Off		M-T On	
			Hex	Dec	Hex	Dec
Control	No Op	Not Zero	03	03		
	Seek	6	07	07		
	Seek Cylinder	6	0B	11		
	Seek Head	6	1B	27		
	Set File Mask	1	1F	31		
	Space Count	Not Zero	0F	15		
	Transfer in Channel	X	X8			
	Recalibrate (Note 1)	Not Zero	13	19		
	Restore (2321 only)	X	17	23		
Sense	Sense I/O	6	04	04		
Switching	Release Device } (Note 2)	Not Zero	94	148		
	Reserve Device	Not Zero	B4	180		
Search†	Home Address EQ	4 (usually)	39	57	B9	185
	Identifier EQ	5 (usually)	31	49	B1	177
	Identifier HI	5 (usually)	51	81	D1	209
	Identifier EQ or HI	5 (usually)	71	131	F1	241
	Key EQ	1 to 255	29	41	A9	169
	Key HI	1 to 255	49	73	C9	201
	Key EQ or HI	1 to 255	69	105	E9	233
	Key & Data EQ	(Note 3)	2D	45	AD	173
	Key & Data HI		4D	77	CD	205
	Key & Data EQ or HI		6D	109	ED	237
Continue Scan	Search EQ		25	37	A5	165
	Search HI		45	69	C5	197
	Search HI or EQ		65	101	E5	229
	Set Status Modifier*		35	53	B5	181
	Set Status Modifier*		75	117	F5	245
	No Status Modifier		55	85	D5	213
Read†	Home Address	5	1A	26	9A	154
	Count	8	12	18	92	146
	Record R0	Number of bytes transferred	16	22	96	150
	Data		06	06	86	134
	Key & Data		0E	14	8E	142
	Count, Key & Data		1E	30	9E	158
	IPL		02	02		
Write	Home Address	5 (usually)	19	25		
	Record R0	8+KL+DL of R0	15	21		
	Count, Key & Data	8+KL+DL	1D	29		
	Special Count, Key & Data	8+KL+DL	01	01		
	Data	DL	05	05		
	Key & Data	KL+DL	0D	13		
	Erase	8+KL+DL	11	17		

X = not significant
Note 1. For 2311 or 2314 only.
Note 2. Two-channel switch required except for a 2314/2844 combination.
Note 3. Include mask bytes in search argument; these commands are a special feature on 2841.
*Sense byte determines command used.
†M-T On = M-T Off except during Search and Read, bit 0 = 1 in M-T On.

CHANNEL COMMAND CODES

Device	Command for CCW		8-Bit Code 0	1	2	3	4	5	6	7	Hex	Dec
1052	Read Inquiry BCD		0	0	0	0	1	0	1	0	0A	10
	Read Reader 2 BCD		0	0	0	0	0	0	1	0	02	02
	Write BCD, Auto Carriage Return		0	0	0	0	1	0	0	1	09	09
	Write BCD, No Auto Carriage Return		0	0	0	0	0	0	0	1	01	01
	No Op		0	0	0	0	0	0	1	1	03	03
	Sense		0	0	0	0	0	1	0	0	04	04
	Alarm		0	0	0	0	1	0	1	1	0B	11
2540	Read, Feed, Select Stacker SS	Type AA	S	S	D	0	0	0	1	0		
	Read	Type AB	1	1	D	0	0	0	1	0		
	Read, Feed (1400 compatability mode only)		1	1	D	1	0	0	1	0		
	Feed, Select Stacker SS	Type BA	S	S	1	0	0	0	1	1		
	PFR Punch, Feed, Select Stacker SS	Type BA	S	S	D	0	1	0	0	1		
	Punch, Feed, Select Stacker SS	Type BB	S	S	D	0	0	0	0	1		

SS	Stacker
00	R1
01	R2
10	RP3

D	Data Mode
0	EBCDIC
1	Column Binary

Device	Command for CCW	0	1	2	3	4	5	6	7
1442 N1	Read	M	M	M	0	0	0	1	0
	Write	M	M	M	0	0	0	0	1
	Control	M	M	0	0	0	0	1	1
	No Op	0	0	0	0	0	0	1	1
	Sense	0	0	M	M	0	1	0	0

	M	M	M	M	
Read	0	0	X		Eject and SS1
Read	1	0	X		Eject and SS1
Read	0	1	X		Eject and SS2
Read	1	1	X		Eject and SS2
Write	0	0	X		SS1
Write	1	0	X		Eject and SS1
Write	0	1	X		SS2
Write	1	1	X		Eject and SS2
Control	1	0			Eject and SS1
Control	0	1			SS2
Control	1	1			Eject and SS2
Sense			1	1	Punch diagnostic
Sense			0	1	Read diagnostic

X = 0 means EBCDIC mode
X = 1 means Column Binary Mode

Device	Command for CCW	0	1	2	3	4	5	6	7	Hex	Dec
1403 or 1443	Write, No Space	0	0	0	0	0	0	0	1	01	01
	Write, Space 1 After Print	0	0	0	0	1	0	0	1	09	09
	Write, Space 2 After Print	0	0	0	1	0	0	0	1	11	17
	Write, Space 3 After Print	0	0	0	1	1	0	0	1	19	25
	Write, Skip To Channel N After Print	1	C	H	A	N	0	0	1		
	Diagnostic Read (1403)	0	0	0	0	0	0	1	0	02	02
	Diagnostic Read (1443)	0	0	0	0	0	1	1	0	06	06
	Sense	0	0	0	0	0	1	0	0	04	04
Carriage Control	Space 1 Line Immediately	0	0	0	0	1	0	1	1	0B	11
	Space 2 Line Immediately	0	0	0	1	0	0	1	1	13	19
	Space 3 Line Immediately	0	0	0	1	1	0	1	1	1B	27
	Skip To Channel N Immediately	1	C	H	A	N	0	1	1		
	No Op	0	0	0	0	0	0	1	1	03	03

C	H	A	N	Channel
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6

C	H	A	N	Channel
0	1	1	1	7
1	0	0	0	8
1	0	0	1	9
1	0	1	0	10
1	0	1	1	11
1	1	0	0	12

Device	Command for CCW	0	1	2	3	4	5	6	7	Hex	Dec
UCS	Allow buffer loading	1	1	1	0	1	0	1	1	EB	235
	Load buffer (no folding)	1	1	1	1	1	0	1	1	FB	251
	Load buffer (folding)	1	1	1	1	0	0	1	1	F3	243
	Block data check latch	0	1	1	1	0	0	1	1	73	115
	Reset block data check latch	0	1	1	1	1	0	1	1	7B	123
2400 Tape*	Read Backward (Overrides Data Converter On)	0	0	0	0	1	1	0	0	0C	12
	Sense	0	0	0	0	0	1	0	0	04	04
	Write	0	0	0	0	0	0	0	1	01	01
	Read	0	0	0	0	0	0	1	0	02	02
	Control	0	0	C	C	C	1	1	1		
		D	D	M	M	M	0	1	1		
		1	1	N	N	N	0	1	1		

N	N	N	
0	0	0	1600 bpi P.E. **
0	0	1	800 bpi NRZI

C	C	C	Control Codes	Hex	Dec
0	0	0	REW	7	7
0	0	1	RUN	0F	15
0	1	0	ERG	17	23
0	1	1	WTM	1F	31
1	0	0	BSR	27	39
1	0	1	BSF	2F	47
1	1	0	FSR	37	55
1	1	1	FSF	3F	63

D	D	7 Track Density
0	0	200
0	1	556
1	0	800**
1	1	***

} 7 Track

M	M	M	(Mode Modifiers)	Set Density	Set Odd Parity	Set Even Parity	Data Converter On	Data Converter Off	Translator On	Translator Off	Request TIE (Track in Error)
0	0	0	No Op								
0	0	1	Not Used								
0	1	0	Reset Condition	X	X		X			X	
0	1	1	Nine-track only								X
1	0	0		X		X		X		X	
1	0	1		X		X		X	X		
1	1	0	Reset Condition	X	X			X		X	
1	1	1		X	X			X	X		

*9 track op. forces 800 BPI and odd parity; also, it overrides 7 track but does not reset 7 track. Load/Sys Reset forces 7 track to 800 BPI, odd parity, data converter on, translator off.

** Reset condition

*** Set 9 Track mode, Models 4-6