iC-MHM

14-BIT ABSOLUTE ANGLE HALL ENCODER

preliminary

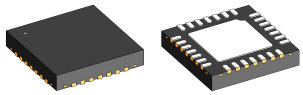
FEATURES

- Selectable resolution and tracking rate (e.g. 12 bit at up to 80 000 rpm and 14 bit at up to 10 000 rpm)
- Quad Hall sensors as array for fault-tolerant assembly
- Signal level control for optimum operating point
- 14-bit interpolation for a resolution of 0.02 °
- Programmable resolution, zero position, code direction
- Diff. 1 Vpp sin/cos output signals, current-limited
- BiSS interface for absolute position and programming
- BiSS Profile conform (BP1, BP3)
- SSI compatible data output
- Serial RS422 transceiver (5 V) for data rates of up to 10 Mbit/s
- LVDS compatibility for higher data rates
- Signal monitoring via BiSS error/warning bits (loss-of-magnet)
- I^2C multimaster interface for configuration from external EEPROM
- Serial multiturn interface (SSI)
- Extended temperature range from -40 to +125 °C
- Pin-selectable SPI operation

APPLICATIONS

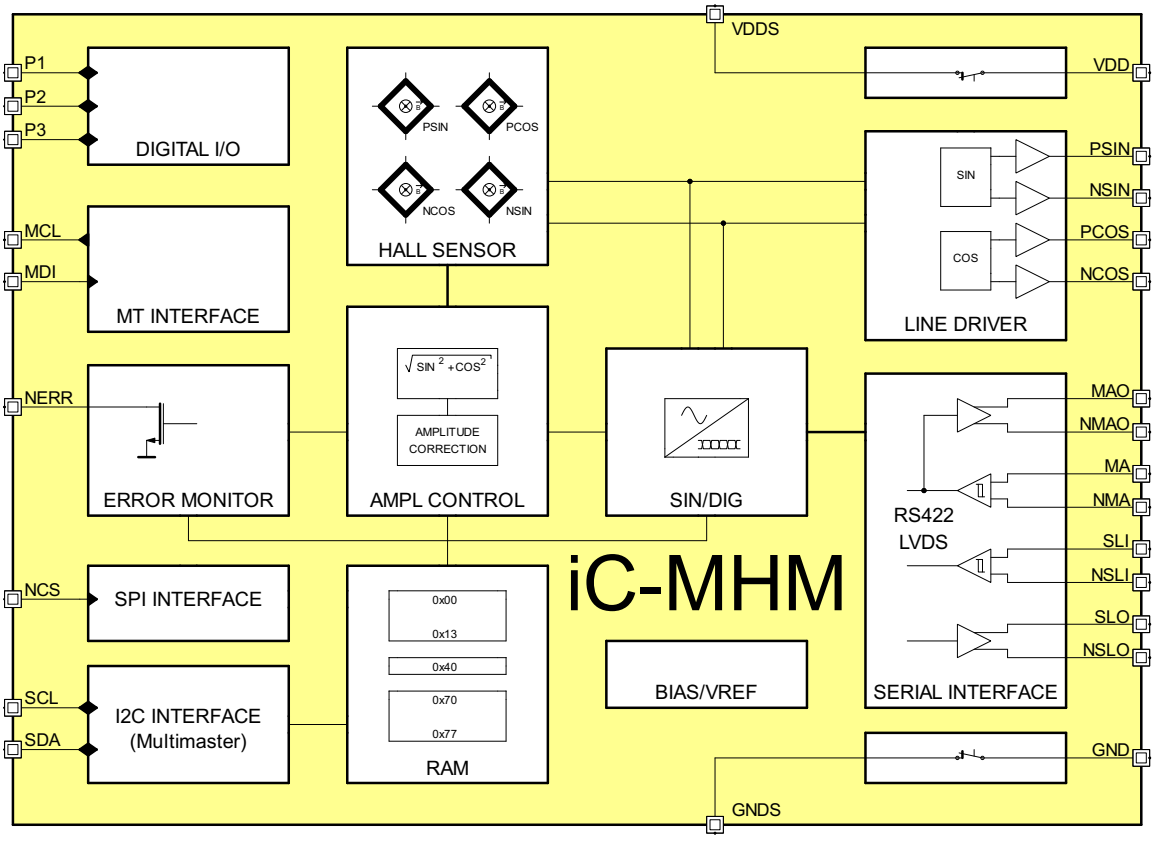
- Digital angular sensors over 360 °
- Absolute position encoders
- Brushless motors
- Motor feedback

PACKAGES



QFN28
5 mm x 5 mm x 0.9 mm
RoHS compliant

BLOCK DIAGRAM



DESCRIPTION

The angular encoder iC-MHM is a position sensor with four integrated Hall sensors for scanning a diametral permanent magnet.

The Hall sensors provide differential sine and cosine signals representing the angle position of the magnet. These signals can be calibrated with respect to amplitude ratio and offset. Before output, the signal can be amplified by a programmable factor or regulated to a constant amplitude of 1 Vpp.

The integrated sine/digital converter determines the angle position of the permanent magnet at 4 096 angular increments per rotation. Data from an external multiturn sensor can also be read in and synchronized.

External access is through the BiSS interface with BiSS C or SSI protocol and the integrated line drivers.

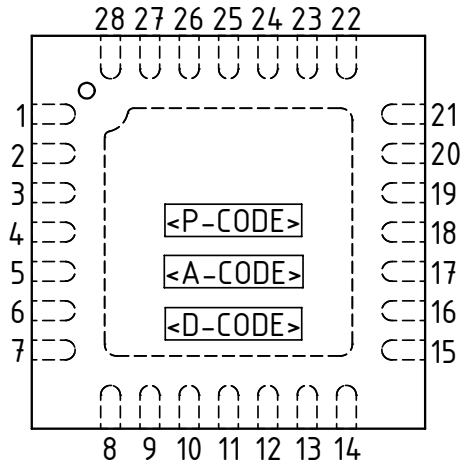
The configuration parameters are secured with a CRC and stored in an external EEPROM. These parameters are read in through the I^2C multimaster interface after the device has been switched on.

The device described here is a multifunctional iC that contains integrated BiSS C interface components. The BiSS C process is protected by patent DE 10310622 B4 owned by iC-Haus GmbH and its application requires the conclusion of a license (free of charge).
Download the license at www.biss-interface.com/bua

CONTENTS

PACKAGING INFORMATION

PIN CONFIGURATION
QFN28 5 mm x 5 mm x 0.9 mm
(according to JEDEC Standard MO-220)

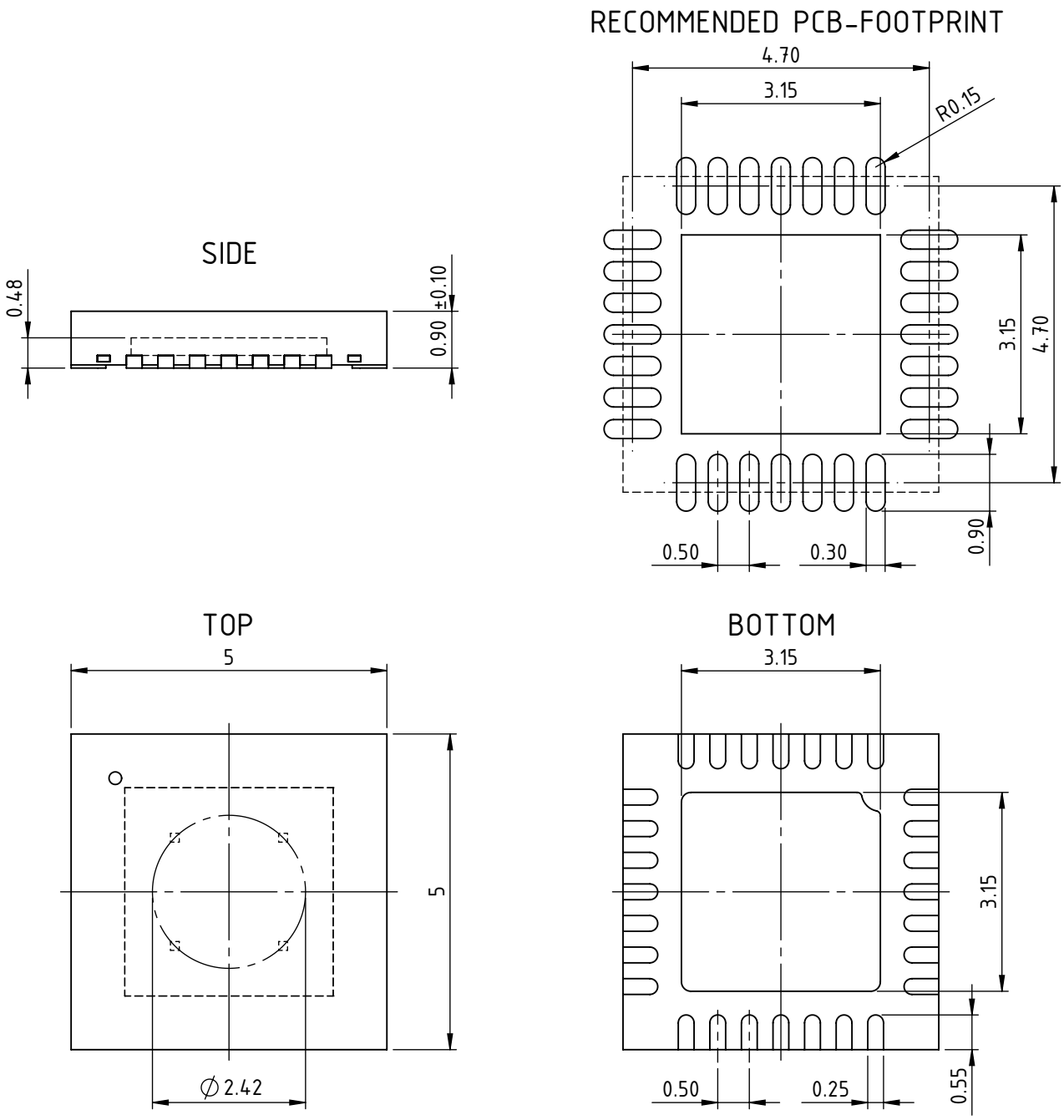


PIN FUNCTIONS

No.	Name	Function
1	MA	BiSS / SSI Clock Input SPI Clock Input (SCLK)
2	NMA	BiSS / SSI Clock Input, inverted
3	NSIN	Analog Sine Output, inverted
4	PSIN	Analog Sine Output
5	P1	Digital I/O Port 1
6	P2	Digital I/O Port 2
7	P3	Digital I/O Port 3
8	n.c.[1]	
9	NCS	SPI Enable and Chip Select Input, low active
10	MCL	Multiturn SSI Clock Output
11	MDI	Multiturn SSI Data Input
12	NERR	Error Mes. Input / Output, low active
13	SCL	I^2C Clock Line
14	SDA	I^2C Data Line
15	n.c.[1]	
16	GNDS	Switched GND (polarity protected)
17	VDDS	Switched VDD (polarity protected)
18	PCOS	Analog Cosine Output
19	NCOS	Analog Cosine Output, inverted
20	NSLI	BiSS Data Input, inverted
21	SLI	BiSS Data Input SPI Data Input (MOSI)
22	NSLO	BiSS / SSI Data Output, inverted
23	SLO	BiSS / SSI Data Output SPI Data Output (MISO)
24	VDD	+5 V Supply Voltage (line in)
25	n.c.[1]	
26	GND	Ground (line in)
27	NMAO	BiSS Clock Output, inverted (multislave)
28	MAO	BiSS Clock Output (multislave)
	BP[2]	Backside Paddle

IC top marking: <P-CODE> = product code, <A-CODE> = assembly code (subject to changes), <D-CODE> = date code (subject to changes);
1) Pin numbers marked n.c. are not connected.
2) Connecting the backside paddle is recommended by a single link to GNDS. A current flow across the paddle is not permissible.

PACKAGE DIMENSIONS



All dimensions given in mm.
Tolerances of form and position according to JEDEC MO-220.
Tolerance of sensor pattern: ±0.10mm / ±1° (with respect to center of backside pad). dra_qfn28-5x5-2_mhm_pack_1, 10:1

ABSOLUTE MAXIMUM RATINGS

These ratings do not imply operating conditions; functional operation is not guaranteed. Beyond these ratings device damage may occur.

Item No.	Symbol	Parameter	Conditions	Min.	Max.	Unit
G001	V()	Voltage at VDD, GND, PSIN, NSIN, PCOS, NCOS, MAO, NMAO, MA, NMA, SLI, NSLI, SLO, NSLO		-6	6	V
G002	V()	Pin-Pin-Voltage between VDD, GND, PSIN, NSIN, PCOS, NCOS, MAO, NMAO, MA, NMA, SLI, NSLI, SLO, NSLO			6	V
G003	V()	Voltage at P1, P2, P3, MCL, MDI, NERR, NCS, SCL, SDA, VDDS, GNDS		-0.3	6	V
G004	I()	Current in VDD, GND		-50	50	mA
G005	I()	Current in VDDS, GNDS		-25	25	mA
G006	I()	Current in PSIN, NSIN, PCOS, NCOS, MAO, NMAO, MA, NMA, SLI, NSLI, SLO, NSLO, P1, P2, P3, MCL, MDI, NERR, NCS, SCL, SDA		-20	20	mA
G007	Vd()	ESD Susceptibility at all pins	HBM, 100 pF discharged through 1.5 kΩ		2	kV
G008	Ts	Storage Temperature		-40	150	°C
G009	Tj	Junction Temperature		-40	150	°C

THERMAL DATA

Operating conditions: VDD = VDDS = 5 V ±10 %

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
T01	Ta	Operating Ambient Temperature Range		-40		125	°C
T02	Rthja	Thermal Resistance Chip to Ambient	package mounted on PCB, *thermal pad* at approx. 2 cm² cooling area		40		K/W

All voltages are referenced to Pin GNDS unless otherwise stated.
All currents flowing into the device pins are positive; all currents flowing out of the device pins are negative.

ELECTRICAL CHARACTERISTICS

Operating conditions: VDD = VDDS = 5 V ±10 %, Tj = -40...125 °C, CIBM adjusted to 200 µA, 4 mm NdFeB magnet, unless otherwise noted

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
General							
001	VDD	Permissible Supply Voltage	versus GND	4.5		5.5	V
002	I(VDD)	Supply Current in VDD	without load		25	32	mA
003	I(VDDS)	Permissible Load Current in VDDS		-25		0	mA
004	Vc()hi	Clamp-Voltage hi at P1, P2, P3, MCL, MDI, NERR, NCS, SCL, SDA	Vc()hi = V() − VDDS, I() = 1 mA	0.4		1.5	V
005	Vc()lo	Clamp-Voltage lo at all pins	I() = -1 mA	-1.5		-0.3	V
Hall Sensors and Signal Conditioning							
101	Hext	Permissible Magnetic Field Strength	at chip surface	20		100	kA/m
102	fmag	Operating Magnetic Field Frequency	CFGFLT = 0x00, R_ST ≥ 0x04, MTD = 0x01			1.4	kHz
103	rpm	Rotating Speed of Magnet	see Item No. 102			84000	rpm
104	dsens	Diameter of Hall Sensor Circle			2.42		mm
105	xdis	Permissible Lateral Displacement of Magnet Axis to Center of Hall Sensors				0.2	mm
106	xpac	Displacement Chip Center to Package Center	package QFN28	-0.2		0.2	mm
107	ϕpac	Angular Alignment of Chip vs. Package	package QFN28	-3		+3	Deg
108	hpac	Distance of Chip Surface to Package Surface	package QFN28		0.4		mm
109	Vos	Trimming Range of Output Offset Voltage	VOSS or VOSC = 0x7F	-37.5	-31.5	-27.5	mV
110	Vos	Trimming Range of Output Offset Voltage	VOSS or VOSC = 0x3F	27.5	31.5	37.5	mV
111	Vopt	Optimal Differential Output Voltage	Vopt = Vpp(PSIN) − Vpp(NSIN), ENAC = 0x0, see Figure 9		1		Vpp
Amplitude Control							
201	Vampl	Differential Output Amplitude	Vampl = Vpp(PSIN) − Vpp(NSIN), ENAC = 0x1, see Figure 9	0.8		1.2	Vpp
202	Vratio	Amplitude Ratio	Vratio = Vpp(PSIN) / Vpp(PCOS)	1.09			
203	Vratio	Amplitude Ratio	Vratio = Vpp(PSIN) / Vpp(PCOS)			0.92	
204	tampl	Settling Time of Amplitude Control	to final setpoint ±10 %			300	µs
205	Vae()lo	Amplitude Error Threshold for ERR_AMIN	$(V(PSIN-NSIN))^2 + (V(PCOS-NCOS))^2$ < Vae()lo	0.3		0.7	Vpp
206	Vae()hi	Amplitude Error Threshold for ERR_AMAX	$(V(PSIN-NSIN))^2 + (V(PCOS-NCOS))^2$ > Vae()hi	1.20		1.45	Vpp
Bandgap Reference							
401	Vbg	Bandgap Reference Voltage	at pin PCOS with mode TEST = 0x19	1.17	1.24	1.32	V
402	Vref	Reference Voltage	at pin PSIN with mode TEST = 0x19	45	50	55	%VDDS
403	Iibm	Bias Current	at pin NSIN with mode TEST = 0x19 CIBM = 0x0 CIBM = 0xF bias current adjusted	 -370 -220	 -200	 -100 -180	 µA µA µA
404	VDDon	Turn-on Threshold VDD (Power-Up-Enable)	increasing voltage	3.65	4.0	4.3	V
405	VDDoff	Turn-off Threshold VDD (Power-Down-Reset)	decreasing voltage	3	3.5	3.8	V
406	VDDhys	Turn-on Threshhold Hysteresis		0.3			V

ELECTRICAL CHARACTERISTICS

Operating conditions: VDD = VDDS = 5 V ±10 %, Tj = -40...125 °C, CIBM adjusted to 200 µA, 4 mm NdFeB magnet, unless otherwise noted

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
407	Vosr	Reference Voltage Offset Compensation	at pin NCOS in test mode TEST = 0x19	470	500	530	mV
Clock Generation							
501	f()sys	System Clock	bias current adjusted; measured at pin SCL with division factor 256	11.5	14	16	MHz
Sin/Digital Converter							
601	RESsdc	Converter Resolution			12		bit
602	AAabs	Absolute Angular Accuracy	calibrated signals	-0.35		0.35	Deg
603	AArel	Relative Angular Accuracy	with reference to one output period at A(P1), B(P2), with R_ST = 0x06, MTD > 0x00, see Figure 1	-15		15	%
Digital I/O, MT Interface, ERROR Monitor, SPI Interface, I²C Interface: P1, P2, P3, MCL, MDI, NERR, NCS, SCL, SDA							
701	Vs()hi	Saturation Voltage hi at P1, P2, P3, MCL	Vs()hi = V(VDDS) − V(), I() = -1.6 mA			0.4	V
702	Vs()lo	Saturation Voltage lo at P1, P2, P3, MCL, SCL, SDA, NERR	I() = 1.6 mA			0.4	V
703	Isc()hi	Short-Circuit Current hi at P1, P2, P3, MCL	V() = V(GNDS), Tj = 25 °C	-90	-50		mA
704	Isc()lo	Short-Circuit Current lo at P1, P2, P3, MCL, SCL, SDA, NERR	V() = V(VDDS), Tj = 25 °C		50	80	mA
705	tr()	Rise Time at P1, P2, P3, MCL	CL = 50 pF, rise 10 % to 90 %			60	ns
706	tf()	Fall Time at P1, P2, P3, MCL, SCL, SDA, NERR	CL = 50 pF, fall 90 % to 10 %			60	ns
707	Vt()hi	Threshold Voltage hi at P1, P2, P3, MDI, NERR, NCS, SCL, SDA				2	V
708	Vt()lo	Threshold Voltage lo at P1, P2, P3, MDI, NERR, NCS, SCL, SDA		0.8			V
709	Vt()hys	Threshold Hysteresis at P1, P2, P3, MDI, NERR, NCS, SCL, SDA		150	250		mV
710	Ipd()	Pull-down Current at P1, P2, P3	V() = 1 V...V(VDDS)	6	30	60	µA
711	Ipu()	Pull-up Current at MDI, NCS	V() = 0 V...V(VDDS) − 1 V	-60	-30	-6	µA
712	Ipu()	Pull-up Current at SCL, SDA, NERR	V() = 0 V...V(VDDS) − 1 V	-800	-300	-60	µA
713	fc()	Clock Frequency at MCL	F_MTI = 0x0 F_MTI = 0x1		1.75 0.44		MHz MHz
Line Driver Analog Signals PSIN, NSIN, PCOS, NCOS							
801	Isc()	Short-Circuit Current	short-circuit vs. VDD vs. GND	10 -50	30 -30	50 -10	mA mA
802	Ilk()	Leakage Current	reversed supply voltage	-1		1	µA
Serial Interface: General							
901	Rpu(MA)	Pull-up Resistor at MA			50		kΩ
902	Rpd(SLI)	Pull-down Resistor at SLI			50		kΩ
Serial Interface: TTL Mode Outputs (CFGIF = 0x01)							
903	Vs()hi	Saturation Voltage hi at MAO, SLO	Vs()hi = V(VDD) − V(), I() = 4 mA			0.4	V
904	Vs()lo	Saturation Voltage lo at MAO, SLO	Vs()lo = V(GND) − V(), I() = 4 mA			0.4	V
905	Isc()hi	Short-Circuit Current hi at MAO, SLO	vs. GND	-90	-50		mA
906	Isc()lo	Short-Circuit Current lo at MAO, SLO	vs. VDD		50	120	mA
907	tr()	Rise Time at MAO, SLO	CL = 30 pF, rise 10 % to 90 %		4		ns
908	tf()	Fall Time at MAO, SLO	CL = 30 pF, fall 90 % to 10 %		2.8		ns
909	Rpd()	Pull-down Resistor at NMAO, NSLO		1	2	3	kΩ

ELECTRICAL CHARACTERISTICS

Operating conditions: VDD = VDDS = 5 V ±10 %, Tj = -40...125 °C, CIBM adjusted to 200 µA, 4 mm NdFeB magnet, unless otherwise noted

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Serial Interface: TTL Mode Inputs (CFGIF = 0x00 or 0x01)							
910	Vt()hi	Threshold Voltage hi at MA, SLI	referenced to GND			2	V
911	Vt()lo	Threshold Voltage lo at MA, SLI	referenced to GND	0.8			V
912	Vt()hys	Hysteresis at MA, SLI		150	300		mV
Serial Interface: LVDS Mode (CFGIF = 0x10)							
913	V()hi	Output Voltage hi at MAO, NMAO, SLO, NSLO	RL = 100 Ω	1.25		1.6	V
914	V()lo	Output Voltage lo at MAO, NMAO, SLO, NSLO	RL = 100 Ω	0.9		1.25	V
915	Vadiff()	Differential Output Voltage at MAO / NMAO, SLO / NSLO	Vadiff(MAO) = V(MAO) – V(NMAO), Vadiff(SLO) = V(SLO) – V(NSLO), RL = 100 Ω	250	350	450	mV
916	Vacm()	Common Mode Output Voltage at MAO, NMAO, SLO, NSLO	RL = 100 Ω	1.125	1.2	1.375	V
917	tr()	Rise Time at MAO, NMAO, SLO, NSLO	CL = 5 pF, rise 10 % to 90 %		2		ns
918	tf()	Fall Time at MAO, NMAO, SLO, NSLO	CL = 5 pF, fall 90 % to 10 %		2		ns
919	Vcom()	Input Voltage Range at MA, NMA, SLI, NSLI	referenced to GND	0.8		3.0	V
920	Vtdiff()	Differential Input Threshold at MA / NMA, SLI / NSLI	Vtdiff(MA) = V(MA) – V(NMA), Vtdiff(SLI) = V(SLI) – V(NSLI)	-180		180	mV
921	Vthys()	Differential Input Threshold at MA / NMA, SLI / NSLI	Vthys(MA) = V(MA) – V(NMA), Vthys(SLI) = V(SLI) – V(NSLI)	35	70		mV
Serial Interface: RS422 Mode Outputs (CFGIF = 0x00 or 0x11)							
922	Vs()hi	Saturation Voltage hi at MAO, NMAO, SLO, NSLO	Vs()hi = VDD – V(), I() = -50 mA			800	mV
923	Vs()lo	Saturation Voltage lo at MAO, NMAO, SLO, NSLO	Vs()lo = GND – V(), I() = 50 mA			800	mV
924	Isc()hi	Short-Circuit Current hi at MAO, NMAO, SLO, NSLO	V() = GND	-120		-50	mA
925	Isc()lo	Short-Circuit Current lo MAO, NMAO, SLO, NSLO	V() = VDD	50		120	mA
926	tr()	Rise-Time lo to hi at MAO, NMAO, SLO, NSLO	Cl = 30 pF, RL = 100 Ω , rise 10 % to 90 %		10		ns
927	tf()	Fall-Time hi to lo at MAO, NMAO, SLO, NSLO	Cl = 30 pF, RL = 100 Ω , fall 90 % to 10 %		10		ns
Serial Interface: RS422 Mode Inputs (CFGIF = 0x11)							
928	Vcom()	Input Voltage Range at MA, NMA, SLI, NSLI	referenced to GND	0		3	V
929	Vtdiff()	Differential Input Threshold at MA / NMA, SLI / NSLI	Vtdiff(MA) = V(MA) – V(NMA), Vtdiff(SLI) = V(SLI) – V(NSLI)	-300		300	mV
930	Vthys()	Differential Input Threshold at MA / NMA, SLI / NSLI	Vthys(MA) = V(MA) – V(NMA), Vthys(SLI) = V(SLI) – V(NSLI)	75	150		mV
Reverse Polarity Protection VDDS, GNDS							
C01	Vs()	Saturation Voltage VDDS vs. VDD	Vs(VDDS) = VDD – V(VDDS); I(VDDS) = -10 . . . 0 mA I(VDDS) = -25 . . . -10 mA			 150 300	 mV mV
C02	Vs()	Saturation Voltage GNDS vs. GND	Vs(GNDS) = V(GNDS) – GND; I(GNDS) = 0 . . . 10 mA I(GNDS) = 10 . . . 25 mA			 150 300	 mV mV

CHARACTERISTICS: Diagram

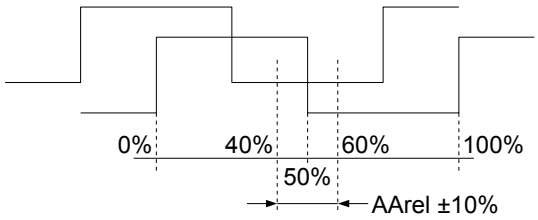


Figure 1: Definition of relative angular accuracy

OPERATING REQUIREMENTS: Multiturn Interface

Item No.	Symbol	Parameter	Conditions	Min.	Max.	Unit
Multiturn Interface: SSI (Figure 2)						
I001	t_{frame}	Clock Frame Repetition		250	40 000	ns
I002	t_C	Clock Period		25	40 000	ns
I003	t_{L1}, t_{L2}	Clock Signal hi/lo Level Duration		25	40 000	ns
I004	t_S	Setup Time: Data stable before clock edge lo → hi				
I005	t_H	Hold Time: Data stable after clock edge lo → hi				
I006	t_{out}	Permissible Slave Timeout				

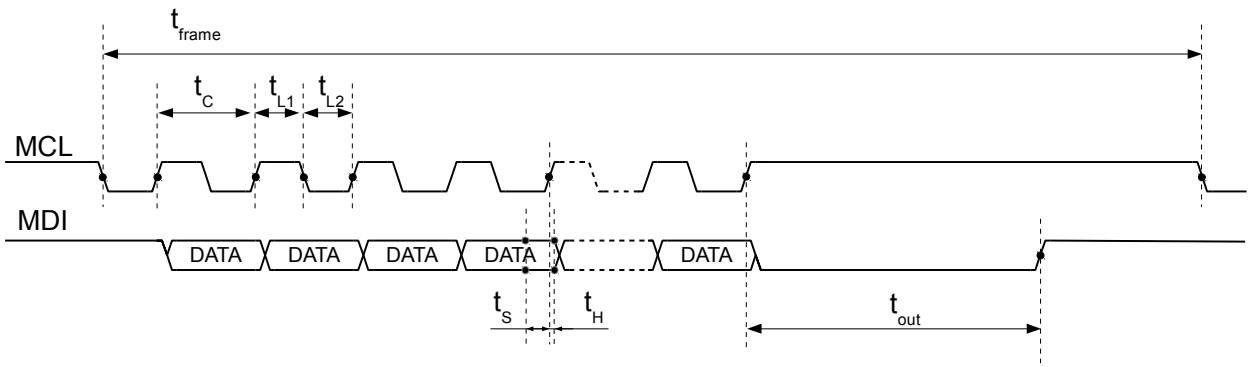


Figure 2: SSI Interface timing

OPERATING REQUIREMENTS: Serial Interface (BiSS, SSI)

Operating condition: VDD = VDDS = 5 V ±10 %, Tj = -40...125 °C, CIBM adjusted to 200 µA

Item No.	Symbol	Parameter	Conditions	Min.	Max.	Unit
Serial Interface: BiSS (Figure 3)						
I101	t_{frame}	Permissable Frame Repetition	CFGIF ≠ 0x10 (TTL or RS422)	100	40 000	ns
I102	t_C	Permissable Clock Period	CFGIF = 0x10 (LVDS)	12	40 000	ns
I103	t_{L1}	Clock Signal hi Level Duration	CFGIF ≠ 0x10 (TTL or RS422)	25	40 000	ns
I104	t_{L2}	Clock Signal lo Level Duration	CFGIF = 0x10 (LVDS)	6	40 000	ns
I105	t_{busy}	Processing Time w/o Start Bit Delay	CFGIF ≠ 0x10 (TTL or RS422)	25	40 000	ns
I106	t_{busy}	Processing Time with Start Bit Delay	CFGIF = 0x10 (LVDS)	6	40 000	ns
I107	t_{P3}	Output Propagation Delay				
I108	t_{out}	Adaptive Slave Timeout				
Serial Interface: SSI (Figure 4)						
I115	t_{frame}	Permissible Frame Repetition		100		ns
I116	t_C	Permissible Clock Period		50		ns
I117	t_{L1}	Clock Signal Hi-Level Duration		30		
I118	t_{L2}	Clock Signal Lo-Level Duration		30		
I119	t_{busy}	Processing Time w/o Start Bit Delay		30		ns
I120	t_{busy}	Processing Time with Start Bit Delay	DISBISS = 0x0	30		ns
I121	t_{P3}	Output Propagation Delay	DISBISS = 0x1	30		ns
I122	t_{out}	Adaptive Slave Timeout		500		

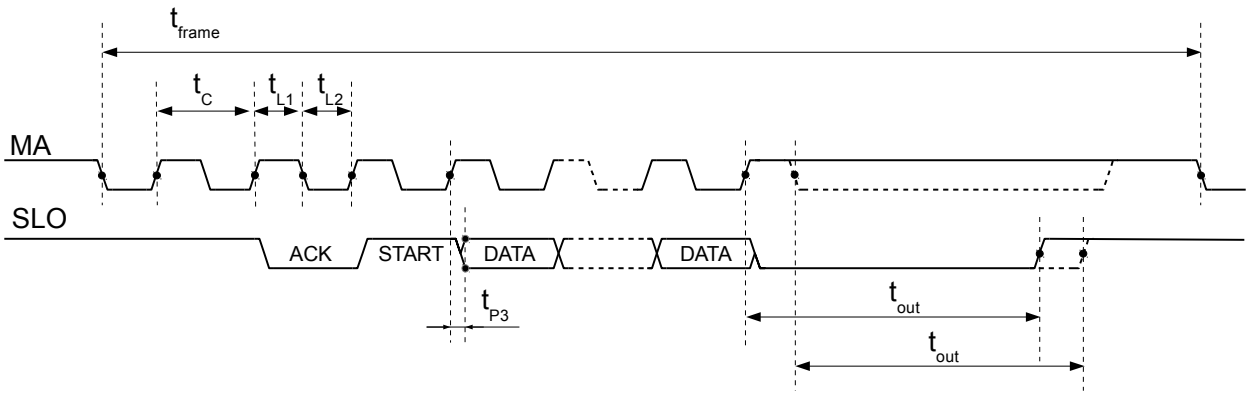


Figure 3: BiSS Interface timing

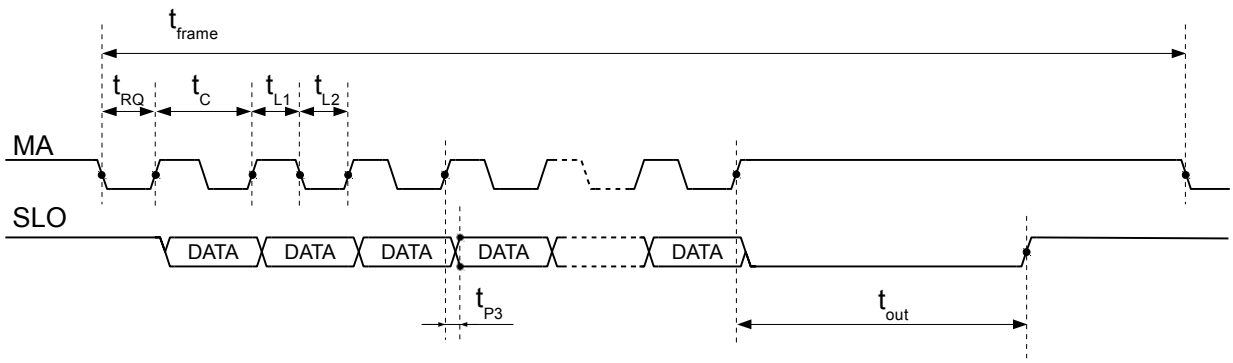


Figure 4: SSI Interface timing

OPERATING REQUIREMENTS: Serial Interface (SPI)

Item No.	Symbol	Parameter	Conditions	Min.	Max.	Unit
Serial Interface: SPI						
I201	t_{C1}	Permissible Clock Cycle Time		100		ns
I202	t_{D1}	Clock Signal lo Level Duration		30		ns
I203	t_{D2}	Clock Signal hi Level Duration		30		ns
I204	t_{S1}	Setup Time: NCS lo before MA lo → hi		50		ns
I205	t_{S2}	Setup Time: SLI stable before SCLK lo → hi		30		ns
I206	t_H	Hold Time: SLI stable after MA lo → hi		30		ns
I207	t_{P1}	Propagation Delay: SLO stable after MA hi → lo		30		ns
I208	t_{P2}	Propagation Delay: SLO hi after NCS		30		ns
I209	t_{P3}	Propagation Delay: SLO hi impedance after NCS lo → hi		30		ns
I210	t_W	Wait Time: between NCS lo → hi and NCS hi → lo		500		ns

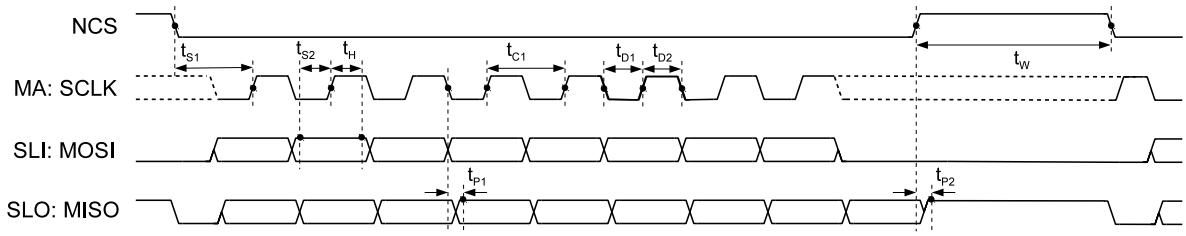


Figure 5: SPI Interface timing (DISBISS = 0x0)

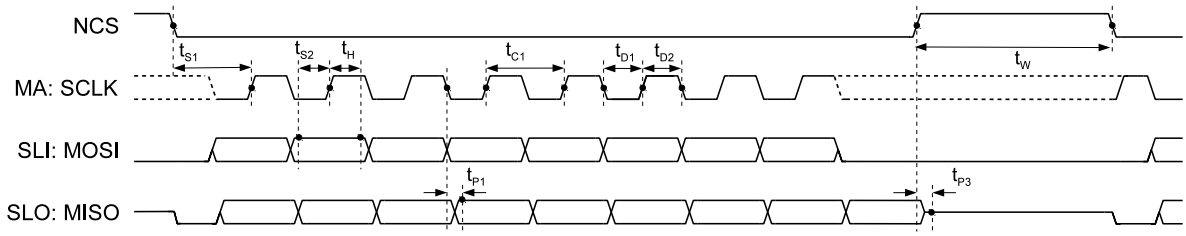


Figure 6: SPI Interface timing (DISBISS = 0x1)

CONFIGURATION PARAMETERS

REGISTER MAP: RAM

OVERVIEW								
Addr	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Sine/Digital Converter								
0x00	HYS(1:0)		ROT	MTD(2:0)			CFGFLT(1:0)	
Resolution								
0x01	0	R_ST(2:0)			0	R_MT(2:0)		
Multiturn Interface								
0x02	GET_MT	EBL_MTI(2:0)			SBL_MTI(2:0)			F_MTI
Serial Interface								
0x03	ENSSI	EXTSSI	BINSSI	CFGIF(1:0)		MT12	CFGDIO(1:0)	
Hall Signal Conditioning								
0x04	ENF	VOSS(6:0)						
0x05	HARMCAL(4)	VOSC(6:0)						
0x06	HARMCAL(3:0)				CIBM(3:0)			
0x07	0	0	DISBISS	TEST(4:0)				
0x08	GAING(1:0)		GAINF(5:0)					
0x09	ENAC	GCC(6:0)						
Safety								
0x0A	0	ENLC	CRC_ID(5:0)					
Enable								
0x0B	0	0	ENINST_2	ENPRES_I	ENROT_P	ENPRES_P	COMPROT	REGPROT
CRC								
0x0C	CRC_CFG(7:0)							
Output Offset								
0x0D	OFFSET_MT(31:24)							
0x0E	OFFSET_MT(23:16)							
0x0F	OFFSET_MT(15:8)							
0x10	OFFSET_MT(7:0)							
0x11	OFFSET_ST(15:8)							
0x12	OFFSET_ST(7:0)							
CRC								
0x13	CRC_OFF(7:0)							

Table 7: Register layout

REGISTER MAP: BiSS (RAM/EEPROM)

OVERVIEW								
Addr	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Configuration								
0x00 .. 0x0F	1. Configuration range (used by multiturn devices like iC-MV and iC-PV)							
0x10 .. 0x23	2. Configuration range (used by iC-MHM)							
0x24 .. 0x3F	reserved							
BiSS Defined Standard Register								
0x40	Bank selection							
0x41	EDS bank (EEPROM)							
0x42 0x43	BiSS Profile ID (EEPROM)							
0x44 .. 0x47	BiSS Device Serial number (EEPROM)							
Output Values After Preset (zero position setting)								
0x48	PRESET_MT(31:24)							
0x49	PRESET_MT(23:16)							
0x4A	PRESET_MT(15:8)							
0x4B	PRESET_MT(7:0)							
0x4C	PRESET_ST(15:8)							
0x4D	PRESET_ST(7:0)							
0x4E	CRC_PRST(7:0)							
0x4F	reserved							
User Range								
0x50 .. 0x6F	EEPROM							
Status Messages								
0x70	ERR_MT	ERR_MTI	ERR_AMAX	ERR_AMIN	ERR_EXT	ERR_ST	ERR_OFF	ERR_CFG
0x71	0	0	0	0	P3	P2	P1	P0(MDI)
0x72	GAIN							
0x73	reserved							
Command Register								
0x74	0	0	0	0	0	0	PRESET	RESET
0x75	0	0	0	0	P3	P2	P1	P0(MCL)
0x76	GAIN							
0x77	reserved							
BiSS Identifier								
0x78 .. 0x7D	BiSS Device Identifier (EEPROM)							
0x7E .. 0x7F	BiSS Device Manufacturer Identifier (EEPROM)							
Note: Reserved registers must be programmed to zero.								

Table 8: Register layout

STARTUP AND OPERATION

Startup
(shown redand yellow in Figure 7)
After power on the configuration data and output offset are read in from external EEPROM addresses 0x10. . . 0x23 by the I²C multimaster interface, and both check sums are verified. If data verification proves faulty, the read-in is repeated. After three failed attempts the device goes into error mode. During this phase the data output SLO remains high to allow error detection in the SSI output format. Registers can be written through the BiSS interface. An error state can be quit using the reset command.

Following successful configuration, amplitude control is initialized and the singleturn data, i.e. the angle information within one rotation is calculated. Then, if the synchronization bit length is greater than zero, the multiturn data is read in and synchronized with the singleturn data. This process is repeated infinitely if an error occurs. If there are no faults, the system is now ready for operation. The entire startup phase is signaled with a low at error output NERR.

Operation
(shown green in Figure 7)
During operation, singleturn data is constantly generated in real time. The multiturn data is also counted and read in by way of verification cyclically approx. every 1.3 ms from the external sensor. After every access through BiSS or SSI the validity of the configuration parameters and output offset are checked in the RAM by a CRC.

Preset Sequence
(shown orange in Figure 7)
The preset sequence calculates a new output offset from the current position and the preset values stored in the EEPROM so that the preset is output during further operation at the current position. Provided the relevant enable has been signaled, the sequence is initiated by a high at port P1 (ENPRES_P), by programming the command register, or by sending BiSS command 3. Following this the preset values (PRESET_ST, PRESET_MT) are loaded from the external EEPROM into the offset (OFFSET_ST, OFFSET_MT) register. The singleturn and multiturn data are recalculated and the current position is then stored in the EEPROM as an offset value. The device is then reset.

Note 1: The preset sequence is aborted when the check sum stored in the EEPROM with the preset is faulty.

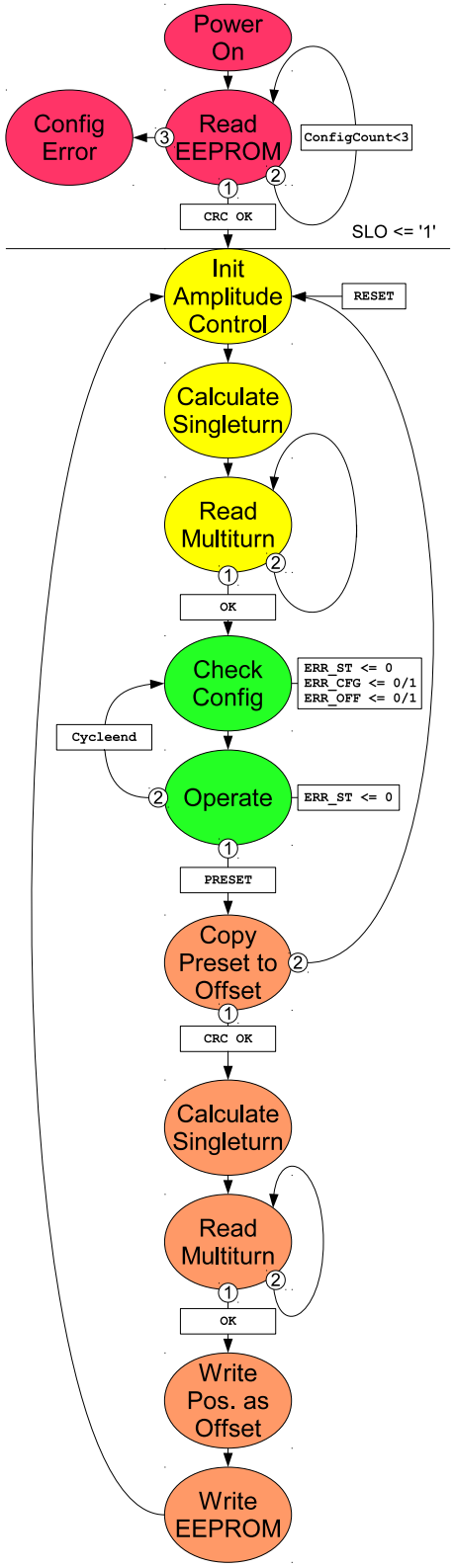


Figure 7: State diagram

Note 2: If an inverted direction of rotation is active with ROT, the two's complement of the preset value must be calculated and entered.

Note 3: Only in the states shown in green a valid measurement value is provided. In all other states the data value zero (error and warning active) is transmitted via BiSS or SSI.

PRESET	Addr. 0x48 - 0x4D;	
Addr.	Name	Description
0x48	PRESET_MT	Preset Multiturn (31:24)
0x49	PRESET_MT	Preset Multiturn (23:16)
0x4A	PRESET_MT	Preset Multiturn (15:8)
0x4B	PRESET_MT	Preset Multiturn (7:0)
0x4C	PRESET_ST	Preset Singleturn (15:8)
0x4D	PRESET_ST	Preset Singleturn (7:0)

Table 9: PRESET

SENSOR PRINCIPLE

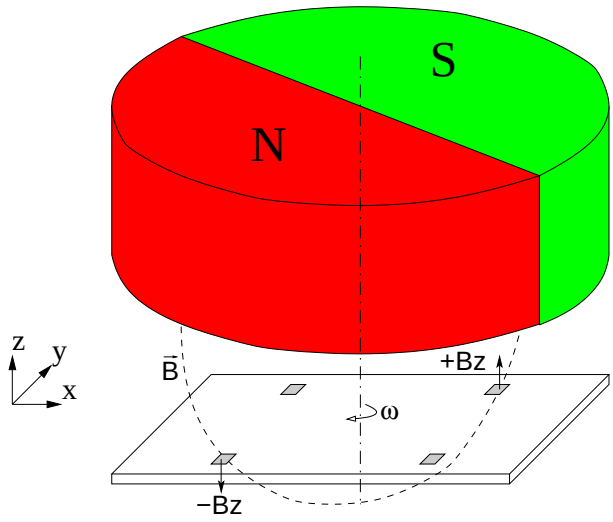


Figure 8: Sensor principle

Optimum sensor signals are generated by a diametrically magnetized, cylindrical permanent magnet (e.g. with a diameter of D = 4 mm and height of L = 4 mm).

Magnetic materials, such as neodymium iron boron (NdFeB) or samarium cobalt (SmCo), are very well suited to the sensor and are hardly influenced by external stray fields. As the length-to-diameter ratio of the magnet material magnetized to saturation has an effect on the resulting field strength, the magnet's body ratio should be within a range of 0.3 to 2.

iC-MHM has four Hall sensors adapted for angle determination which convert the magnetic field into measurable Hall voltages. Solely the magnetic field's z component is evaluated at which the field lines pass through two opposing sensors in opposite directions (see Figure 8). The arrangement of the Hall sensors has been specifically selected to allow a very tolerant assembly of iC-MHM to the magnet axis.

Differential Hall signals are generated by the combination of two Hall sensors each. When the magnet rotates around its longitudinal axis, sine and cosine voltages are generated which are used for angle determination.

HALL SIGNAL PROCESSING

GAING(1:0): Coarse Gain

Device iC-MHM has a signal calibration feature that can compensate for signal and adjustment errors. The Hall signals are amplified in two stages. The first amplifier stage can be roughly programmed to the following gains:

GAING(1:0)	Addr. 0x08; bit 7:6
Code	Description
0x00	5-fold
0x01	10-fold
0x10	14.5-fold
0x11	17.5-fold

Table 10: Coarse Gain

GAINF(5:0): Fine Gain

The second amplifier stage has a finer adjustment.

GAINF(5:0)	Addr. 0x08; bit 5:0
Code	Description
0x00	1.000
0x01	1.048
...	$exp(\frac{ln(20)}{64} \cdot GAINF)$
0x3F	19.08

Table 11: Fine Gain

ENAC: Amplitude Control

The integrated amplitude control unit can be activated using bit ENAC. In this case the differential signal amplitude is regulated to 1 Vpp; the values from GAING and GAINF only define the start value.

ENAC	Addr. 0x9; bit 7
Code	Description
0x0	Amplitude control deactivated
0x1	Amplitude control activated

Table 12: Activating Amplitude Control

After startup the gain is altered until the set amplitude is obtained. If the input amplitude is altered by the distance between the magnet and sensor being increased, or if there is a change in the supply voltage or temperature, the gain is automatically adjusted. The conversion of the sine signals thus always takes place at optimum amplitude. Amplitudes that are either too large or too small are recorded in the status register by ERR_AMIN or ERR_AMAX. This fault is also signaled at error output NERR and through BiSS.

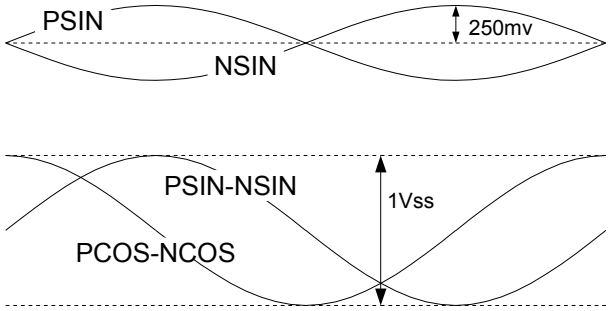


Figure 9: Definition of Differential Amplitude

GCC(6:0): Cosine Gain Correction

Register GCC enables the sensitivity of the sine channel in relation to the cosine channel to be corrected. The cosine amplitude can be corrected within a range of approx. ±10 %.

GCC(6:0)	Addr. 0x09; bit 6:0	
Code	Description	Effective Angle Corr.
0x00	1.000	0 °
0x01	1.0015	0.04 °
...	$exp(\frac{ln(20)}{2048} \cdot GCC)$	
0x3F	1.0965	2.7 °
0x40	0.9106	-2.7 °
...		
	$exp(-\frac{ln(20)}{2048} \cdot (128 - GCC))$	
0x7F	0.9985	-0.04 °

Table 13: Cosine Gain Correction

VOSS(6:0) and VOSC(6:0): Sine and Cosine Offset Calibration

If there is an offset in the sine or cosine signal, possibly caused by a magnet not being precisely adjusted, for instance, this can be corrected by registers VOSS and VOSC. The output voltage can be shifted in each case by ± 31.5 mV in order to calibrate the offset.

VOSS(6:0) Addr. 0x04; bit 6:0 **VOSC(6:0)** Addr. 0x05; bit 6:0		
Code	Description	Effective Angle Corr.
0x00	0 mV	0 °
0x01	0.5 mV	0.06 °
...	...	...
0x3F	31.5 mV	3.7 °
0x40	0 mV	0 °
0x41	-0.5 mV	-0.06 °
...	...	...
0x7F	-31.5 mV	-3.7 °

Table 14: Sine and Cosine Offset Calibration

ENF: Filter
The amplifier cutoff frequency can be programmed with ENF.

ENF	Addr. 0x04; bit 7
Code	Description
0x0	16 kHz cutoff frequency
0x1	3 kHz cutoff frequency

Table 15: Filter

CIBM(3:0): Bias Current Calibration
In test mode (TEST(4:0) = 0x19) the internal currents can be calibrated at pin NSIN. To this end the current must be measured referenced to GNDS, and register bits CIBM changed until the current is calibrated to 200 µA. All internal current sources are then calibrated.

CIBM(3:0)	Addr. 0x06; bit 3:0
Code	Description
0x08	50 %
0x09	56.25 %
...	...
0x0F	93.75 %
0x00 (±0)	100 %
0x01	106.25 %
...	...
0x07	143.75 %

Table 16: Bias Current Calibration

HARMCAL(4:0): Harmonic Calibration
After calibration of offset and gain a residual error with four times period remains. This error can be reduced with the calibration parameter HARMCAL.

HARMCAL(4:0)	Addr. 0x05; bit 7 Addr. 0x06; bit 7:4	
Code	Description	Effective Angle Corr.
0x00	0 LSB	0 °
0x01	1 LSB	0.05 °
...	...	...
0x0F	15 LSB	0.75 °
0x10	0 LSB	0 °
0x11	-1 LSB	-0.05 °
...	...	...
0x1F	-15 LSB	-0.75 °

Table 17: Harmonic Calibration

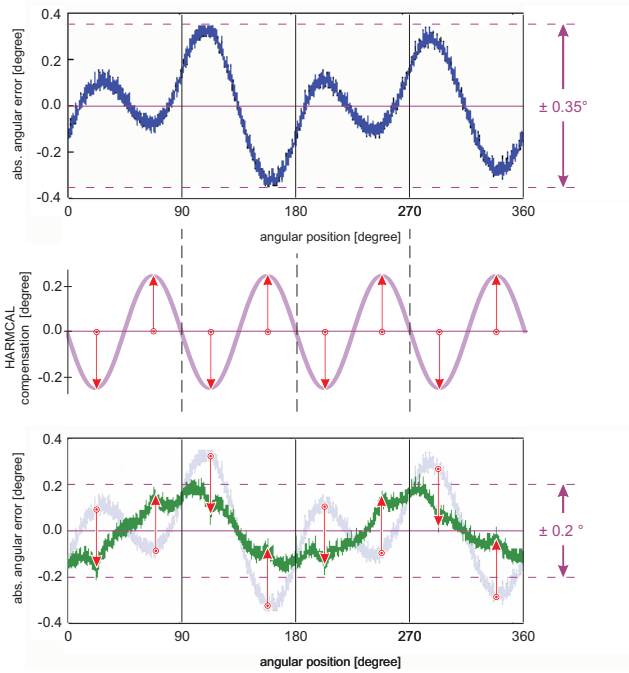


Figure 10: Harmonic Calibration

SINE/DIGITAL CONVERTER

The iC-MHM contains an real time A/D converter that transposes the sine/cosine Hall signals into angular position values which can be read out via the *BiSS*/SSI interface without delay. In addition, incremental signals are available at ports P1, P2 and P3.

Due to the converter tracking principle, the angular position value changes only with one LSB of the given resolution at a time. Therefore, with high input frequency, a phase mismatch will occur between the current mechanical position and its estimated angular value. A phase offset exceeding 90 ° will be recognized and results in a phase step at the output. This will be also signalled over *BiSS* as a warning and, if incremental signals are in use, results in an error output at pin NERR.

MTD(2:0): Permissible RPM Speed
The converter frequency automatically adjusts itself to the value required by the input frequency. This ranges from zero to a maximum dependent on the oscillator frequency, which can be programmed using register MTD.

A converter frequency of greater than 5 MHz reduces the level of accuracy; a lower converter frequency lowers the maximum input frequency. The converter frequency can be measured across the minimum edge distance of the incremental output.

MTD(2:0)	Addr. 0x00; bit 4:2	
Code	Converter Frequency (typ.)	Permissible RPM Speed
0x00	14 MHz	168 457 rpm
0x01	7 MHz	84 229 rpm
0x02	4.7 MHz	56 152 rpm
0x03	3.5 MHz	42 114 rpm
0x04	2.8 MHz	33 691 rpm
0x05	2.3 MHz	28 076 rpm
0x06	2 MHz	24 065 rpm
0x07	1.75 MHz	21 057 rpm
Note	Calculated for 12 bit resolution.	

Table 18: Permissible RPM Speed

The values in Table 18 have been computed with an oscillator frequency $f()sys$ = 11.5 MHz for a singleturn resolution of 12 bits. For using other resolutions the rpm values can be calculated:
Permissible RPM Speed = $\frac{f()sys}{Resolution\_ST * 60} / (MTD + 1)$

OFFSET
The zero position can be electrical adjusted with the parameter OFFSET.

OFFSET	Addr. 0x0D - 0x12;	
Addr.	Name	Description
0x0D	OFFSET_MT	Offset Multiturn (31:24)
0x0E	OFFSET_MT	Offset Multiturn (23:16)
0x0F	OFFSET_MT	Offset Multiturn (15:8)
0x10	OFFSET_MT	Offset Multiturn (7:0)
0x11	OFFSET_ST	Offset Singleturn (15:8)
0x12	OFFSET_ST	Offset Singleturn (7:0)

Table 19: OFFSET

HYS(1:0): Angle Hysteresis
If the rotational direction is reversed, an angular hysteresis prevents multiple switching of the converter at the reversal point. This is equivalent to a slip which exists between the two directions of rotation. The angular hysteresis can be set using parameter HYS.

HYS(1:0)	Addr. 0x00; bit 7:6
Code	Description
0x00	0°
0x01	0.17°
0x02	0.35°
0x03	0.70°

Table 20: Angle Hysteresis

ROT: Code Direction
The direction of rotation can be inverted by bit ROT.

ROT	Addr. 0x00; bit 5
Code	Description
0x0	Normal rotation (CCW)
0x1	Inverted rotation (CW)

Table 21: Code Direction

Normal rotation is counting up with magnet mounted on the top and turning counter clockwise.

CFGFLT(1:0): Digital Filtering
A digital averaging can be activated to enable resolutions above 12 bit. The maximum rotary frequency then is independent of the output resolution and limited dependend on CFGFLT.

CFGFLT(1:0) Addr. 0x00; bit 1:0			
Code	Filter	Latency (typ.)	Permissible RPM Speed
0x00	No digital averaging used		
0x01	Filter 1	1.2 µs	42 114 rpm
0x02	Filter 2	2.3 µs	21 057 rpm
0x03	Filter 3	4.6 µs	10 529 rpm

Table 22: Digital Filter

RESOLUTION

The output resolution can be set with R_ST according to the following Table:

R_ST(1:0) Addr. 0x01; bit 6:4	
Code	Resolution
0x00*	65536 (16 bit, not recommended)
0x01*	32768 (15 bit, not recommended)
0x02*	16384 (14 bit)
0x03*	8192 (13 bit)
0x04	4096 (12 bit)
0x05	2048 (11 bit)
0x06	1024 (10 bit)
0x07	512 (9 bit)
Note	*) Resolutions above 12 bit need digital filtering (CFGFLT ≠ 0x00)

Table 23: Singleturn Resolution

R_MT(4:0) Addr. 0x01; bit 2:0	
Code	Resolution
0x00	Multiturn not used
0x01	4
0x02	8
0x03	12
0x04	16
0x05	20
0x06	24
0x07	32

Table 24: Multiturn Bit Length

MULTITURN INTERFACE

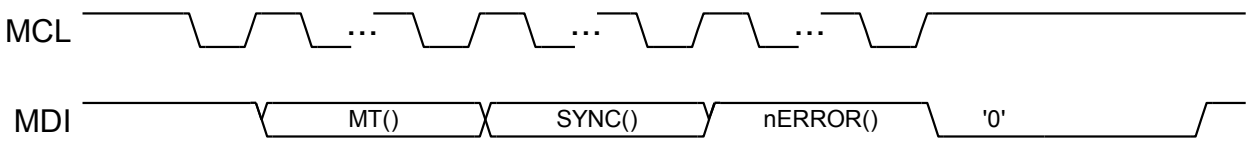


Figure 11: Multiturn Interface

An external multiturn sensor can be read in after power on and cyclically approx. every 1.3 ms. The multiturn data is synchronized with the singleturn data and assigned to the internal multiturn counter. For this purpose, the read-in value is decremented by one if necessary.

SBL_MTI(2:0): Synchronization Bit Length
The external multiturn sensor must therefore be mounted or programmed with an appropriate forward phase offset. The phase shift and synchronization range are dependent on the number of synchronization bits. Up to five synchronization bits are supported. The optimum phase shift is in the middle of the synchronization range. Table 25 gives the correlation.

SBL_MTI(2:0) Addr. 0x02; bit 3:1		
Code	Synchronization bits	phase shift range
0x00	No external multiturn sensor used	
0x01	1	0 ° ... 180 °
0x02	2	0 ° ... 270 °
0x03	3	0 ° ... 315 °
0x04	4	0 ° ... 337.5 °
0x05	5	0 ° ... 348.75 °

Table 25: Synchronization Bit Length

With setting SBL_MTI = 0x00 the multiturn interface is deactivated and only the internal counter is used. A counting error due to exceeding input rotation frequency or loss of signal can not be detected.

F_MTI: Clock Frequency at MCL
During operation, a change in singleturn position due to rotation of the permanent magnet reduces the available synchronization range. For example, with an input rotation frequency of 72 000 rpm and a read-in duration of 20 µs, the synchronization range reduces by an amount of 8.64 °. With parameter F_MTI, the clock frequency at MCL can be selected which determines the required read-in duration.

F_MTI Addr. 0x02; bit 0	
Code	Description
0x0	(f()sys* / 8)
0x1	(f()sys* / 32)
Note	*) see Item No. 501, 713

Table 26: Clock Frequency At MCL

EBL_MTI(1:0): Multiturn Error Bit Length
Should the multiturn counter value and the synchronized external multiturn data differ, the internal value is rejected and error **ERR_MT** (error in case of false internal multiturn data) generated. This error is stored until the next reset or preset.

The external multiturn sensor is read in in SSI format via pins MCL and MDI (see Figure 11).

After the data and synchronization bits, up to four error bits can be transmitted (Table 27). Data line MDI is then checked for a zero. If data transmission does not end in a zero, or if one of the error bits is set to zero, error

EBL_MTI(1:0) Addr. 0x02; bit 6:4	
Code	Error bits
0x00	Error bits not used
0x01	1
...	...
0x04	4

Table 27: Multiturn Error Bit Length

Direct Communication To Multiturn Sensor
Programming bit GET_MT connects MCL with MA, and MDI is activated in place of SLO. With this, the external sensor data can be read in directly for adjustment.

GET_MT Addr. 0x02; bit 7	
Code	Mode
0x0	disabled
0x1	Multiturn sensor communication enabled

Table 28: Enable multiturn sensor communication

SERIAL INTERFACE: General

Line Drivers
The line drivers can be configured as described in Table 29. In case of error (see Page 16), the configuration resets to the default value (first line: TTL - RS422).

CFGIF	Addr. 0x03; bit 4:3
Code	Function (Input - Output)
0x00	TTL - RS422
0x01	TTL - TTL
0x02	LVDS - LVDS
0x03	RS422 - RS422
Note	Recommended setting for operation with SPI is 0x00 or 0x01.

Table 29: Line Driver Inputs / Outputs

SERIAL INTERFACE: BiSS

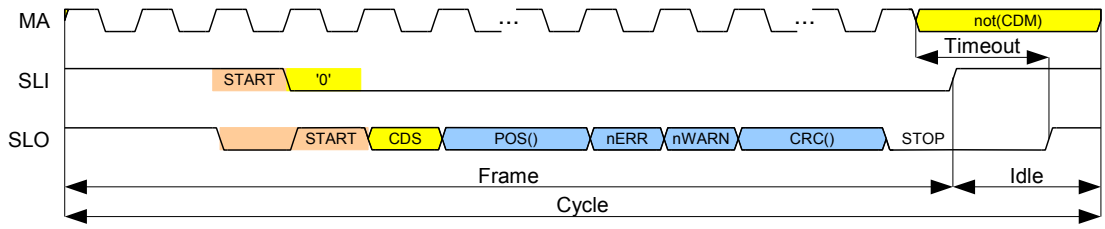


Figure 12: BiSS Protocol

The BiSS Interface is a serial, bidirectional interface which is used to read out the absolute position and to parameterize the device. For a detailed description of the protocol, please see the BiSS C protocol description. The singleturn data length is dependent on the output resolution. This is 16 bits for resolutions that are greater than 12; the data length is otherwise 12 bits. For compatibility to BiSS Profile BP1, the data length for multiturn can be set with MT12 to a multiple of 12 (Table 31).

Single Cycle Data(SCD)		
Bits	Typ.	Label
0 - 32	DATA	Angle data MT(31:0) (multiturn position)
12, 16	DATA	Angle data ST(11:0) or ST(15:0) (singleturn position)
1	ERROR	Error bit nE (low active)
1	ERROR	Warning bit nW (low active)
0, 6	LC	Sign-of-life counter (BiSS SCD cycle tracking)
6, 16	CRC	CRC polynomial 0x43 $x^6 + x^1 + x^0$ (inverted bit output)

Table 30: BiSS Single Cycle Data

The sensor data produced by iC-MHM contains the angle value (ST) with 3 to 13 bits, the multiturn (MT) with 0 to 32 bits, two error bits nERROR (nE) and nWARN (nW) and 6 or 16 CRC bits (CRC).

MT12	Addr. 0x03; bit 2	
Code	Function	Condition
0x0	As defined with R_MT	
0x1	0	R_MT = 0
	12	R_MT = 4 . . . 12
	24	R_MT = 16 . . . 24
	32	R_MT = 32

Table 31: Multiturn Data Length

The status register error messages are collated as an error bit and transmitted as low active. The warning bit nWARN is signalled with a zero indicating a phase shift of greater 90 °. The CRC is formed using the usual encoder generator polynomial $X^6 + X^1 + X^0$ and transmitted in its inverted state.

BiSS Timeout

The (automatic) BiSS timeout adaption is based on the BiSS MA clock period T_{MA} and the device specific internal sampling frequency $1/T_{CLK}$.

iC-MHM measures the 1.5 periods (from the first falling to the second rising edge) of MA each frame and calculates an adaptive timeout with $T_{CLK} = \frac{4}{3 * f()sys}$ (see El. Char., 501).

Symbol	Condition	Min.	Max.
timeout	$T_{CLK} \leq 1.5 * T_{MA}$	$1.5 * T_{MA}$	$1.5 * T_{MA} + 3.0 * T_{CLK}$
	$T_{CLK} \geq 1.5 * T_{MA}$	$1.0 * T_{CLK}$	$1.5 * T_{MA} + 3.0 * T_{CLK}$

Table 32: BiSS Adaptive Timeout

For more information please refer to the BiSS interface http://www.ichaus.de/BiSS_interface.

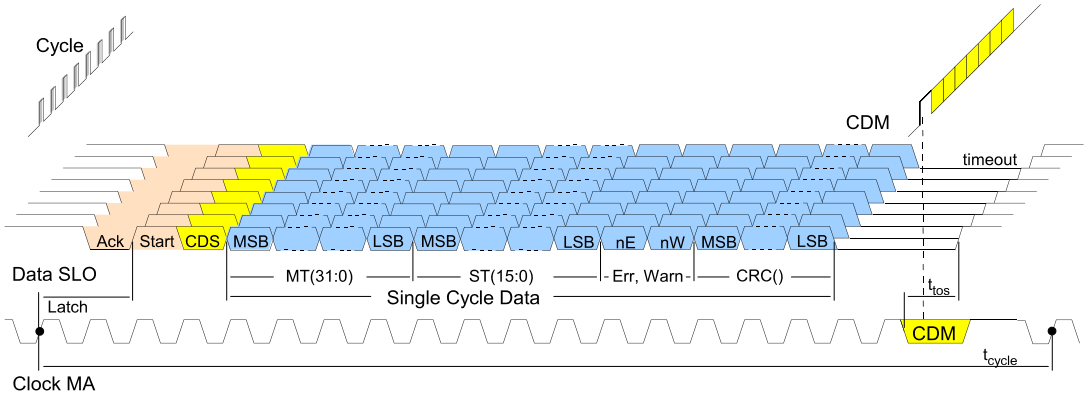


Figure 13: BiSS Protocol including Control Communication)

REGPROT	Addr. 0x0B; bit 0
Code	Description
0x0	No restriction for BiSS register access
0x1	Restriction for BiSS register access. For the type of restriction see Table 34

Table 33: Register Protection

COMPROT	Addr. 0x0B; bit 1
Code	Description
0x0	Writing in command register at address 0x74 allowed
0x1	Writing in command register at address 0x74 not possible

Table 34: Command Register Protection

BiSS Register Location, Content and Protection Type					
BANK No.	Address	Content	EEPROM	REGPROT	
				0	1
0	0x00 - 0x13	Configuration	RAM	R / W	n.a.
	0x14 - 0x3F	Not used	not used	n.a.	n.a.
1	0x00 - 0x0F	For MT devices	0x000 - 0x00F	R / W	n.a.
	0x10 - 0x23	iC-MHM Configuration	0x010 - 0x023	R / W	n.a.
	0x24 - 0x3F	Reserved	0x024 - 0x03F	R / W	n.a.
2 - 13	0x00 - 0x3F	EDS	0x080 - 0x37F	R / W	R
14 - 31	0x00 - 0x3F	USER DATA	0x380 - 0x7FF	R / W	R / W
X	0x40	Bank select	RAM	R / W	R / W
	0x41	ESD bank	0x041	R / W	R
	0x42 - 0x43	BiSS Profile ID	0x042 - 0x043	R / W	R
	0x44 - 0x47	Serial No.	0x044 - 0x047	R / W	R
	0x48 - 0x4F	Preset	0x048 - 0x04F	R / W	R / W
	0x50 - 0x6F	USER DATA	0x050 - 0x06F	R / W	R / W
	0x70 - 0x73	Status	RAM	R	R
	0x74 - 0x77	Command	RAM	W	W
	0x78 - 0x7F	BiSS ID	0x078 - 0x07F	R / W	R

Table 35: BiSS Register Location, Content and Protection Type

BiSS Command Mapping			
Opcode	Broadcast	Addressed	Condition
0	n.a.	n.a.	
1	n.a.	n.a.	
2	reset P3/MCL	set P3/MCL	ENINST_2 = 1
3	execute preset sequence	execute preset sequence	ENPRES_I = 1

Table 36: BiSS Command Mapping

Safety

For safety applications a sign of life (or life counter) can be transmitted in the sensor data. If the life counter has been activated, a 6-bit count is transmitted in the sensor data which is incremented on each new request for sensor data. The range of the life counter is 1 to 63.

ENLC	Addr. 0x0A; bit 6
Code	Function
0x0	Life counter not active, generator polynomial: $X^6 + X^1 + X^0$
0x1	Life counter active, generator polynomial: $X^{16} + X^{15} + X^{12} + X^7 + X^6 + X^4 + X^3 + X^0$

Table 37: Life Counter

In addition, with activated life counter, instead of using the standard 6 bit CRC, a 16 bit safety-CRC with the generator polynomial $X^{16} + X^{15} + X^{12} + X^7 + X^6 + X^4 + X^3 + X^0$ is used.

For the calculation of the checksum the starting value CRC_ID is used.

CRC_ID	Addr. 0x0A; bit 5:0
0x00	Default CRC start value used in non safety applications, e.g. BiSS Profile BP1 and BP3
0x01.. 0x3F	Unique CRC start value within all slaves of the BiSS channel

Table 38: CRC Start Value

SERIAL INTERFACE: SSI

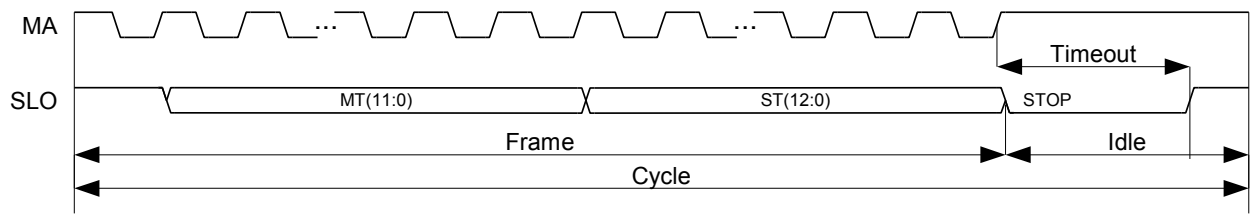


Figure 14: SSI Protocol

The interface can emulate the SSI protocol when ENSSI is set (Table 39).

ENSSI	Addr. 0x03; bit 7
Code	Protocol
0x0	BiSS C protocol
0x1	SSI protocol

Table 39: Activating SSI Output Protocol

For the SSI protocol, a standard and an extended format are distinguished (Table 40).

EXTSSI	Addr. 0x03; bit 6
Code	Protocol
0x0	Standard SSI Protocol
0x1	Extended SSI Protocol

Table 40: Activating Extended SSI Output Protocol

With the standard SSI protocol, the output provides a 13 bit singleturn data. With the extended SSI protocol, the output data consists of 12 bit singleturn, error, warning and, if also ENLC is activated, the lifetime counter data.

The position data can be output in either Gray or Binary code (Table 41).

BINSSI	Addr. 0x03; bit 5
Code	Description
0x0	Gray coded
0x1	Binary coded
Note	Binary or Gray coded data output starts with MSB.

Table 41: SSI Coding Gray / Binary

SERIAL INTERFACE: SPI

General Description

MA is used as clock input SCLK. SLI is the data input MOSI and SLO the output MISO. The SPI modes 0 and 3 are supported, i.e. idle level of SCLK low or high and acceptance of data on a rising edge. Data is sent in packages of 8 bits and with the MSB first (see Figure 15).

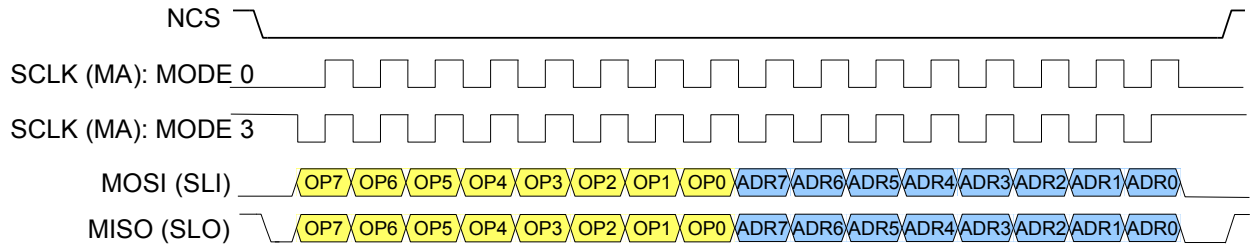


Figure 15: SPI Transmission SPI-Mode 0 and 3.

In the default configuration, the interface is switched from *BiSS* to SPI with a low level at NCS. Daisy chain is used to connect multiple devices to one controller (see Figure 16)

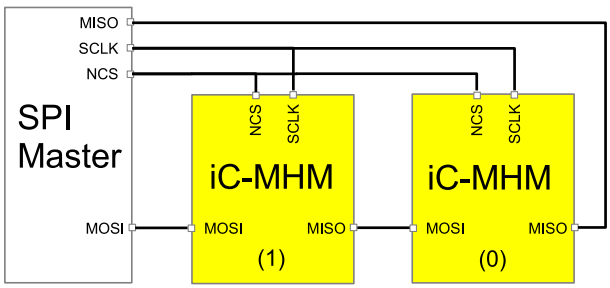


Figure 16: Daisy Chain Configuration with 2 Devices

The BiSS interface can completely deactivate per configuration with DISBISS. In this configuration MISO becomes high resistive, if the device is deselected with NCS. Figure 17 shows possible connections.

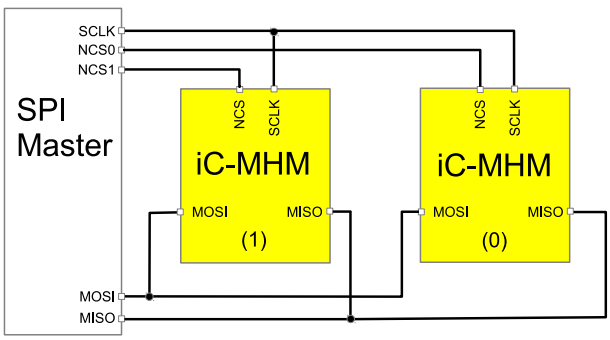


Figure 17: Parallel Configuration with 2 Devices

DISBISS	Addr. 0x07; bit 5
Code	Description
0x0	SLO always driving
0x1	SLO high resistive if deselected

Table 42: Disable BiSS Interface

Operation Codes

Each data transmission starts with the master sending an OPCODE (Table 43) to the device.

OPCODEs	
Code	Description
0xB0	ACTIVATE
0xA6	SDAD Transmission
0xF5	SDAD Status (no latch)
0x97	Read REGISTER (single)
0xD2	Write REGISTER (single)
0x8A	Read REGISTER (cont.)
0xCF	Write REGISTER (cont.)
0xAD	REGISTER Status/Data
0x9C	Read STATUS
0xD9	Write INSTRUCTION

Table 43: OPCODE Table

Reading Sensor Data

iC-MHM latches the absolute position on the first rising edge at SCLK, when NCS is at zero (REQ/LATCH). Because iC-MHM can output the sensor data (SD) immediately, the master can transmit the **SDAD Transmission** command directly.

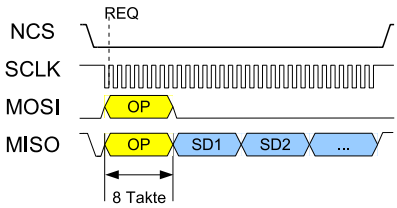


Figure 18: Sensor Data Transmission

The sensor data in SPI are byte aligned. First comes 0-4 byte multiturn depending on R_MT, second are two bytes singleturn and at last one status byte including one error bit, one warning bit and six bits sign-of-life counter.

R_MT(4:0)	Addr. 0x01; bit 2:0
Code	Description
0x00	Multiturn not used
0x02	8
0x04	16
0x06	24
0x07	32

Table 44: Multiturn Bit Length for SPI Interface

Sensor Data Format	
Code	Description
Multiturn	MT(31:0)
Singleturn	ST(15:0)
Status	nE(1), nW(1), LC(5:0)*

Table 45: Sensor Data Format

*) The sign-of-life counter LC only increments after BiSS access.

Register Data

Table 46 shows the register mapping used for SPI. An access to an external EEPROM is not possible.

Address	bit Content
0x00 .. 0x13	Ram
0x14 .. 0x6F	not used
0x70 .. 0x73	Status message
0x74 .. 0x77	Command register

Table 46: Register Mapping

Read REGISTER (cont.)

Reading data from internal registers the device does not need any processing time. These registers can be read out in continuous mode.

The master transmits the **Read REGISTER (cont.)** opcode. In the second byte the start address ADR is transmitted. The device immediately outputs the opcode, address and then transmits the DATA1 data. The internal address counter is incremented following each data packet.

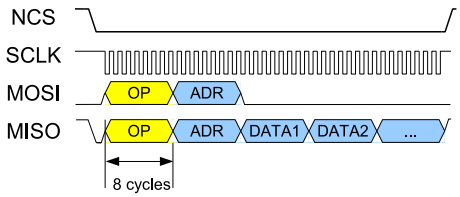


Figure 19: Read REGISTER (cont.)

Write REGISTER (cont.)

Writing data into internal registers the device does not need any processing time. These registers can be written in continuous mode.

The master transmits the **Write REGISTER (cont.)** opcode. In the second byte start address ADR is transmitted, followed by the DATA1 - DATAn data packets to be written. The device immediately outputs the opcode, address and data at MISO. The device increments its internal address counter following each data packet.

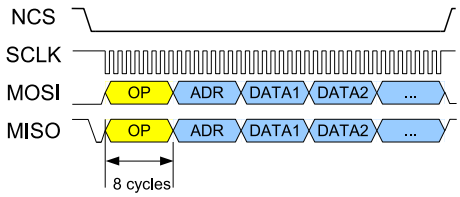


Figure 20: Write REGISTER (cont.)

Read STATUS

The command **Read STATUS** is designed to enable a fast readout of the internal, device specific status registers of a device (STAT1 - STATn). The opcode sets the address in the device to 0x70. The internal address counter is incremented following each STATUS byte. This command largely corresponds to the Read REGISTER (cont.) command, with the difference that here the addressing sequence is missing and the master does not need to know the device's exact STATUS address.

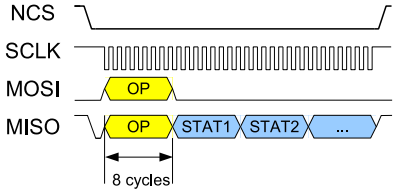


Figure 21: Read STATUS

Write INSTRUCTION
The command **Write INSTRUCTION** is designed to enable a fast setting of the internal, device-specific command registers. The opcode sets the address in the device to 0x74. The instruction data bytes (INST1 - INSTn) are send directly after the OPCODE byte. This command largely corresponds to the **Write REGISTER (cont.)** command, with the difference that here the addressing sequence is missing and the master does not need to know the devices's exact INSTRUCTION address.

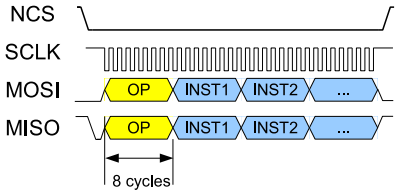


Figure 22: Write INSTRUCTION

ACTIVATE
Using the **ACTIVATE** command, the register and sensor/actuator data channels of the connected devices can be switched on and off. The command causes all devices to switch their RACTIVE and PACTIVE registers between MOSI and MISO and set them to low level. The register and sensor/actuator data channels can be switched on and off with data bytes following the OPCODE.

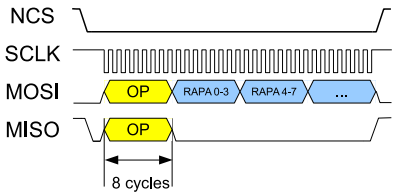


Figure 23: Set ACTIVATE: RACTIVE/PACTIVE (several devices)

The **ACTIVATE** command resets the bits FAIL, VALID, BUSY, and DISMISS in the STATUS byte (see Table 49).

RACTIVE	
Code	Description
0x0	Register communication deactivated
0x1	Register communication activated

Table 47: RACTIVE

If RACTIVE is not set, on commands **Read REGISTER (single), Write REGISTER (single), Read REGISTER (cont.), Write REGISTER (cont.), REGISTER Status/-Data, Read STATUS** and **Write INSTRUCTION** the ERROR bit is set in the STATUS byte (see Table 49) to indicate that the command has not been executed. At MISO the device immediately outputs the data transmitted by the master via MOSI.

PACTIVE	
Code	Description
0x0	Sensor/actuator data channel deactivated
0x1	Sensor/actuator data channel activated

Table 48: PACTIVE

If PACTIVE is not set, on commands **SDAD Status** and **SDAD Transmission** the ERROR bit is set in the STATUS byte (see Table 49) to indicate that the command has not been executed. At MISO the device immediately outputs the data transmitted by the master via MOSI.

If only one device is connected up with one register and one sensor data channel, it must be ensured that the RACTIVE and PACTIVE bits come last in the data byte.

Note: If the devices are connected in a chain (see Figure 16), using this command the master can determine the number of register and sensor data channels connected. To achieve this the master can transmit a high level after the opcode, which is repeated at MISO after the number of register/sensor data channels (see Figure 24).

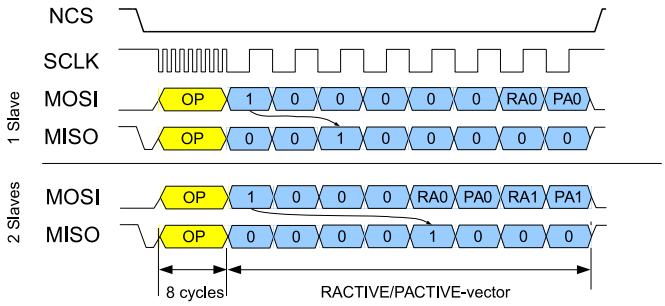


Figure 24: Set ACTIVATE: RACTIVE/PACTIVE (one device)

REGISTER Status/Data
The **REGISTER Status/Data** command can be used to request the status of the last register communication and/or the last data transmission. The STATUS byte contains the information summarized in Table 49.

All SPI status bits are updated with each register access. The exception to the rule is the ERROR bit; this bit indicates whether an error occurred during the last SPI communication with the device.

STATUS		
Bit	Name	Description of the status report
7	ERROR	Opcode not implemented, sensor data was invalid on readout
6..4	-	Reserved
Status bits of the register communication		
3	DISMISS	Address refused
2	FAIL	Data request has failed
1	BUSY	Device is busy with a request
0	VALID	DATA is valid
Note	Display logic: 1 = true, 0 = false	

Table 49: Communication Status Byte

The master transmits the **REGISTER Status/Data** opcode. The device immediately passes the opcode on to MISO. The device then transmits the STATUS byte and a DATA byte.

Following the commands **Read REGISTER (single)** and **Write REGISTER (single)**, the validity of the DATA byte is signaled with the VALID status bit.

The requested data byte is returned via DATA following the **Read REGISTER (single)** command. Following the **Write REGISTER (single)** command, the data to be written is repeated in the DATA byte. With all other OPCODES, the DATA byte is not defined.

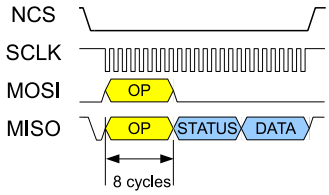


Figure 25: REGISTER Status/Data

I²C INTERFACE (Multimaster)

The serial EEPROM interface consists of the two pins SCL and SDA and enables read and write access to a serial EEPROM with I²C interface (with at least 128 bytes, 5 V function; e.g. 24C01, 24C02, 24C08 and maximal 24C16).

The configuration data in the EEPROM, of addresses 0x00 to 0x13, is secured by a CRC check.
The checksum of addressrange from 0x00 to 0x0B is located at address 0x0C (CRC_CFG) and between addressrange 0x0D and 0x12 the checksum is in address 0x13 (CRC_OFF). Additional the CRC_PRST at address 0x4E includes check sum of the preset values (0x48 ... 0x4D).
When the device is powered up, the address range from 0x00 to 0x13 is mapped onto iC-MHM's configuration RAM. The higher memory area contains BiSS C slave registers and optional memory banks available to the sensor system (see the following Table).

CRC	Addr. 0x0C, 0x13, 0x4E;	
Addr.	Name	Description
0x0C	CRC_CFG	Check sum for configuration data
0x13	CRC_OFF	Check sum for offset values
0x4E	CRC_PRST	Check sum for preset

Table 50: CRC

The register access to the configuration data and the memory banks 2 to 13 (intended for EDS) can be restricted by parameter REGPROT. As the size of the memory required for the activation configuration is slave-specific, the slave provides the bank number of the start of the freely available memory, which will be used for the electronic data sheet (EDS), in its register EDS bank at address 0x00 - 0x3F.

Example of CRC Calculation Routine

```
unsigned char Reg[20] = {0x44, 0x47, 0x10, 0x1A,
    0x80, 0x00, 0x10, 0x00, 0x03, 0x80, 0x00,
    0x00, 0x00, 0x00, 0x00, 0x00, 0x00, 0x00,
    0x00, 0x00};
int iCRCPoly = 0x11D; // CRC-Polynomial 100011101
unsigned char ucDataStream = 0;
unsigned char ucCRC;

// Calculate Config-CRC //
ucCRC = 2; // startvalue !!!
for (int iReg = 0 ; iReg<12; iReg ++) {
  ucDataStream = Reg[iReg];
  for (int i =0; i <=7; i ++) {
    if ( (ucCRC & 0x80) != (ucDataStream & 0x80))
      ucCRC = (ucCRC << 1 ) ^ iCRCPoly ;
    else
      ucCRC = (ucCRC << 1 ) ;
    ucDataStream = ucDataStream << 1 ;
  }
}
Reg[12] = ucCRC;

// Calculate Offset-CRC //
ucCRC = 2; // startvalue !!!
for (int iReg = 13 ; iReg<19; iReg ++) {
  ucDataStream = Reg[iReg];
  for (int i =0; i <=7; i ++) {
    if ( (ucCRC & 0x80) != (ucDataStream & 0x80))
      ucCRC = (ucCRC << 1 ) ^ iCRCPoly ;
    else
      ucCRC = (ucCRC << 1 ) ;
    ucDataStream = ucDataStream << 1 ;
  }
}
Reg[19] = ucCRC;
```

Programming Hint: After writing a byte to the EEPROM the same byte should be read back. iC-MHM does not output the start bit if the EEPROM is busy with its internal write procedure and so denies I²C access. Several read attempts may be required if the I²C interface is still blocked causing iC-MHM to refuse the read access. When writing to the EEPROM without reading the byte back, a waiting time of at least 4 ms must be allowed after each register.

DIGITAL I/O PORTS

The ports P0, P1, P2, and P3 can be read back by the Status Message at address 0x71 and set via Command Register at address 0x75. The pin function is set according to Table 51.

CFGDIO	Addr. 0x03; bit 1:0
Code	Function
0x00	Bidirectional ports
0x01	Reserved
0x02	Output - incremental signals
0x03	Output - calibration signals
Note	Required port setting for ABZ signals is 0x02.

Table 51: Port Direction / Function

For using P1, P2 or P3 as input, the corespondent bit in the Command Register must be reset to zero. The calibration signals are described in Section CALIBRATION PROCEDURE.

P0	Addr. 0x75; bit 0	
Code	Function	Condition
0x0	MCL drives low (strong)	SBL_MTI = 0x00
0x1	MCL drives high (strong)	SBL_MTI = 0x00
Note	P0 in status message belongs to pin MDI.	

P1	Addr. 0x75; bit 1	
Code	Function	Condition
0x0	P1 drives weak low	CFGDIO = 0x00; ENPRES_P = 0x0
0x1	P1 drives strong high	CFGDIO = 0x00; ENPRES_P = 0x0

P2	Addr. 0x75; bit 2	
Code	Function	Condition
0x0	P2 drives weak low	CFGDIO = 0x00; ENROT_P = 0x0
0x1	P2 drives strong high	CFGDIO = 0x00; ENROT_P = 0x0

P3	Addr. 0x75; bit 3	
Code	Function	Condition
0x0	P3 drives weak low	CFGDIO = 0x00; ENINST_2_P = 0x0
0x1	P3 drives strong high	CFGDIO = 0x00; ENINST_2_P = 0x0

Enable

Additional functions can be activated by configuration.

ENPRES_P	Addr. 0x0B; bit 2	
Code	Function	Condition
0x0	Preset sequence initialized via pin disabled	
0x1	Preset sequence initialized via pin P1	CFGDIO = 0x00
	Preset sequence initialized via pin MDI	CFGDIO ≠ 0x00; SBL_MTI = 0x00

ENROT_P	Addr. 0x0B; bit 3	
Code	Function	Condition
0x0	Inverted rotation via pin disabled	
0x1	Inverted rotation via pin P2	CFGDIO = 0x00
	Inverted rotation via pin MDI	CFGDIO ≠ 0x00; SBL_MTI = 0x00

ENPRES_I	Addr. 0x0B; bit 4
Code	Function
0x0	Preset sequence initialized via *BiSS* command disabled
0x1	Preset sequence initialized via addressed *BiSS* command with CDM = 0x3

ENINST_2	Addr. 0x0B; bit 5	
Code	Function	Condition
0x0	Pin access via *BiSS* command disabled	
0x1	P3 controllable via *BiSS* command	CFGDIO = 0x00
	MCL controllable via *BiSS* command	CFGDIO ≠ 0x00; SBL_MTI = 0x00
Note	An addressed command with CDM = 0x2 sets and a broadcast command resets the pin.	

Incremental Output

Any changes in angle are converted into incremental A QUAD B signals. The phasing is oriented to the assignment A = SIN and B = COS. The index Z is centered around the zero position and has a length of 180 °. It appears every period if no multiturn is used, otherwise only at multiturn overflow/underflow.

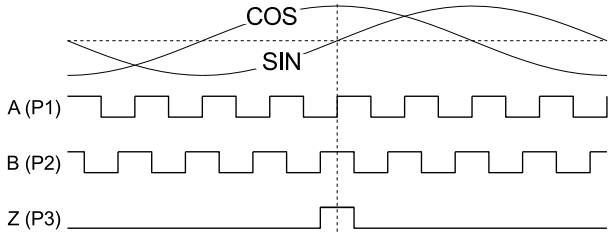


Figure 26: Incremental Output

DEVICE INITIALIZATION

Startup With A Configured EEPROM
After the supply has been turned on (power-on reset), iC-MHM reads the configuration data from the EEPROM. During this phase it actively keeps error pin NERR at a low signal (open drain output), and data output SLO at a high signal.

After a successful CRC the data output to SLO released and the error indication at pin NERR reset; an external pull-up resistor at pin NERR can supply a high signal. iC-MHM then switches to normal operation and determines the current angle position, providing that a magnet is mounted and there is no error.

Should the CRC prove unsuccessful due to a data error (disrupted transmission, no EEPROM or the EEPROM is not programmed), the configuration phase is automatically repeated. After a third failed attempt, the procedure is aborted and error pin NERR displays a permanent low; data output SLO remain at a high signal.

Startup Without An EEPROM
The configuration RAM contains zero values after startup; iC-MHM does not have a default configuration. Error pin NERR shows a low signal (open drain output); data output SLO indicate a high signal.

Initialization After Configuration Failure
So that it is always possible to communicate to iC-MHM via the I/O interface, iC-MHM first ignores the register values of CFGIF, GET_MT, DIS_BISS, REGPROT, COMPROT.

During this phase regular bidirectional BiSS register communication is not yet possible, as data output SLO is permanently kept at high. Writing the configuration to RAM must be executed without evaluating a reply. Data input SLI is ignored; iC-MHM always uses slave ID 0.

Each cycle transmits a single bit only and can be reduced to four clocks plus the timeout (CDM). The following figures each show a single cycle with CDM = 0x0 and CDM = 0x1. A wide range of 100 ns to 12.5 µs is permissible for clock period T(MA).

A complete write cycle requires 14 cycles at CDM = 0x0 and a sequence of 32 cycles calculated according to BiSS C register communication.

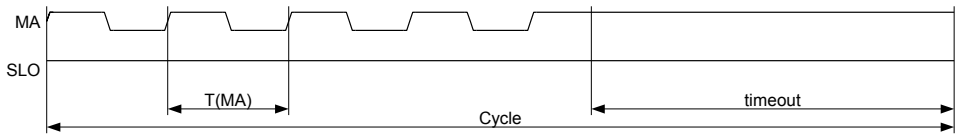


Figure 27: BiSS cycle at CDM = 0x0

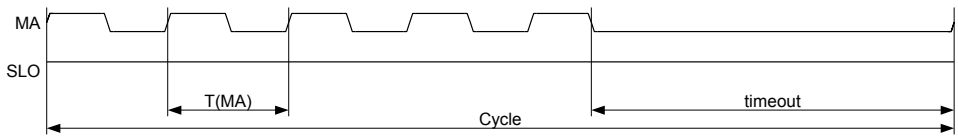


Figure 28: BiSS cycle at CDM = 0x1

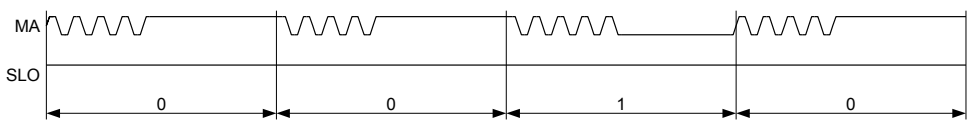


Figure 29: BiSS cycle extract for a CDM sequence of ’0010’.

Init Sequence
At least the following register bits need to be reset: address 0x02, 0x03, 0x05 and 0x0B. The following sequence gives an example of programming and subsequently executing a reset by programming address

0x74 with a value = 0x01.

"00000000000000"
"11000000001000000110000000011110"
"00000000000000"
"11000000001100110110000000011110"

"00000000000000"
"11000000010110010110000000011110"
"00000000000000"
"11000000010111000110000000011110"
"00000000000000"
"11000111010000100110000000111000"

REVERSE POLARITY PROTECTION

The line drivers in iC-MHM are short-circuit-proof and protected against reverse polarity. A defective connecting cable within the module or an incorrectly connected wire damages neither iC-MHM nor the devices protected against reverse polarity by VDDS and GNDS. The following pins are protected against reverse polarity: PSIN, NSIN, PCOS, NCOS, MAO, NMAO, MA, NMA, SLI, NSLI, SLO, and NSLO.

Boundary conditions: Pin GNDS may only be charged to VDDS. The maximum voltage difference between the pins must not exceed 6 V.

CALIBRATION PROCEDURE

The sensor can be adjusted to the magnet by observing the Hall signals of the individual Hall sensors. The sensor must be adjusted so that differential signals PSIN and NSIN, and PCOS and NCOS have the same amplitude and a phase shift of 180 °. Further calibration may not be necessary.

Another option is presented by the duty cycle at pins P1, P2, and P3 in calibration mode. The trimming is accurate if the duty cycle is 50 %. Recommended trimming order (after selecting GAIN): offset, amplitude ratio.

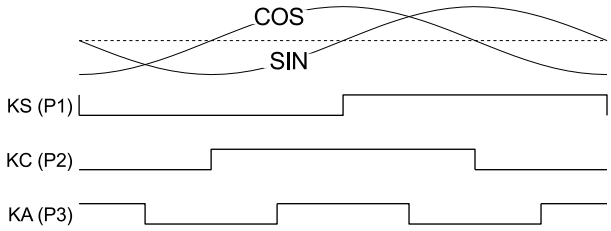


Figure 30: Calibration using incremental signals

STATUS MESSAGES

The status register reports 8 different errors. If an attempt is made to read the current position via the serial interface during startup, an error is signaled by ERR_ST as the actual position is not yet known. The ERR_AMAX signals if the amplitude is too high, while the ERR_AMIN signals if the amplitude is too low (for example, if the distance to the magnet is too large. If the NERR pin is pulled against GND from outside, a system error is also signaled via the serial interface. The ERR_EXT bit is then equal to high. The error bits are reset again after the status register is read out at the address 0x70. The error bit in the data word is then also read in the next cycle as low.

Status	Addr. 0x70; bit 7:0	
Bit	Name	Description
0	ERR_CFG	Configuration data check sum error
1	ERR_OFF	Output offset check sum error
2	ERR_ST	Singleturn data not available
3	ERR_EXT	External error
4	ERR_AMIN	Low amplitude error
5	ERR_AMAX	High amplitude error
6	ERR_MTI	Multiturn data error
7	ERR_MT	Internal multiturn data error false

Table 52: Status Messages

GAIN	Addr. 0x72; bit 7:0
Code	Description
0x00 .. 0xFF	GAING * GAINF

Table 53: Actual Gain Value Of Amplitude Control

APPLICATION NOTES: Circuit Example with iC-MV

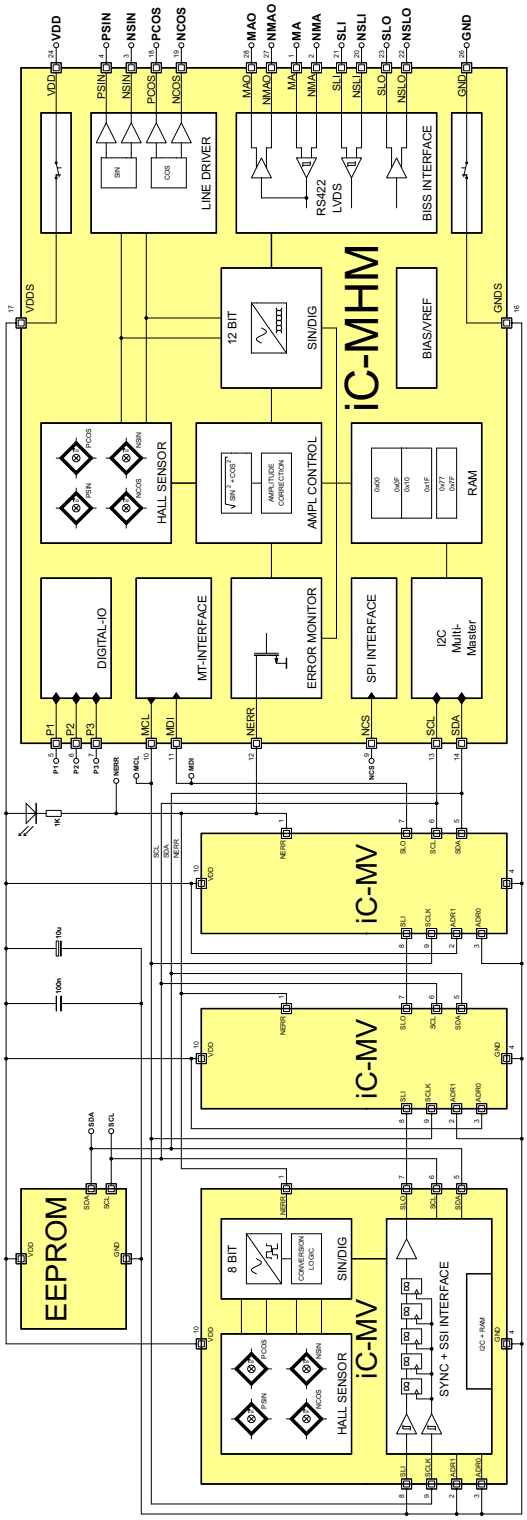


Figure 31: Multiturn encoder using three iC-MV together with iC-MHM

APPLICATION NOTES: Circuit Example with iC-PV

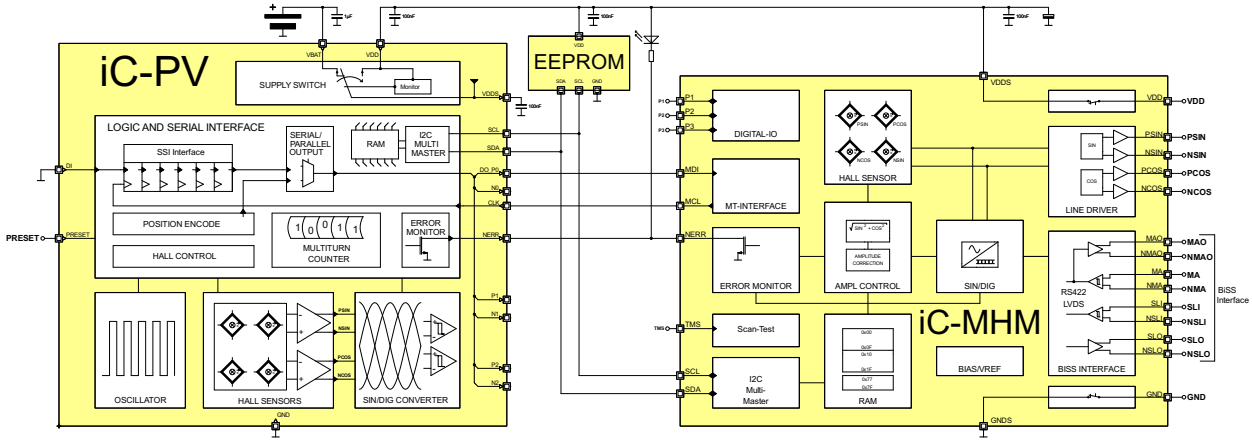


Figure 32: Magnetic absolute encoder with battery-buffered multiturn sensor. The devices are sharing a single EEPROM configured via the BiSS interface of iC-MHM.

DESIGN REVIEW: Notes On Chip Functions

iC-MHM X2		
No.	Function, Parameter/Code	Description and Application Hints
	ROT	Digital Filtering functionality requires ROT = 0 (normal rotation) for configuration.

Table 54: Notes on chip functions regarding iC-MHM chip release X2.

REVISION HISTORY

Rel	Rel.Date	Chapter	Modification	Page
A1	13-11-25	All	Initial release	All

Rel	Rel.Date	Chapter	Modification	Page
B1	14-10-11	All	Global update	All

Rel	Rel.Date	Chapter	Modification	Page
B2	15-04-17	DESIGN REVIEW	Design Review correction	36

ORDERING INFORMATION

Type	Package	Order Designation
iC-MHM	28-pin QFN, 5 mm x 5 mm x 0.9 mm, RoHS compliant	iC-MHM QFN28-5x5
MHM1D Evaluation board		iC-MHM EVAL MHM1D

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