MULTICORE/MANY-CORE SYSTEMS-ON-CHIP

IEEE 10th International Symposium on Embedded Multicore/Many-core Systems-on-Chip (MCSoC-16)

Lyon Congress Center, Lyon, France, September 21-23, 2016

Day 1: Wednesday, September 21st 2016 room Saint Clair 3 A	
8:00	Welcome
9:00	Opening comments
9:15	Keynote: Benoît Dupont de Dinechin, Kalray (FR)
10:00	Coffee break
10:30	Keynote: Pascal Vivet, CEA-LETI (FR)
11:15	Programming models and methods for heterogeneous parallel embedded systems
12:30	Lunch
13:30	Keynote: Andreas Hansson, ARM (UK)
14:15	Approaches and Frameworks for Predictable Multi-Core Processing
15:55	Coffee break
16:30	S1: Architectures
18:10	End of Day 1

Day 2: Thursday, September 22nd 2016	room Saint Clair 3 A	room Saint Clair 3 B
8:00	Welcome	
8:45	Keynote: Hoi-Jun Yoo, KAIST (KR)	
9:30	S2 Interconnect Networks (NoCs) I	S3: Energy efficiency
10:45	Coffee break	
11:00	S4: Benchmarks	Auto-Tuning for Multicore and GPU (ATMG) I
12:40	Lunch	
13:45	S5: Interconnect Networks (NoCs) II	S6: Design I
15:00	S7: Emerging Technologies and Paradigms	S8: Reconfigurable and parallel computing
16:15	Coffee break	
16:30	S9: Design II	Auto-Tuning for Multicore and GPU (ATMG) II
18:10	End of Day 2	
20:00	Gala Diner at Brasserie Le Sud	

Day 3: Friday, September 23rd 2016 room Saint Clair 3 A	
8:00	Welcome
8:45	Keynote: David Atienza, EPFL (CH)
9:30	S10: Interconnect Networks (NoCs) III
10:45	Coffee break
11:00	S11: Programming
11:50	Closing remarks
12:00	Lunch
13:00	End of IEEE-MCSoC 2016
14:00	visit around Lyon (2 hours)

keynote
special session
technical session

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TCMM IEEE Technical Committee on Microprocessors and Microcomputers

IEEE MCSoC-2016 Day 1: Wednesday, September 21st 2016 - Saint Clair 3 A	
8:00	**Welcome**
9:00	**Opening comments**
9:15	**Keynote**
	Engineering a Manycore Processor Platform for Mission-Critical Applications
	Presenter: Benoît Dupont de Dinechin, Kalray (FR)
10:00	**Coffee break**
10:30	**Keynote**
	From 3D technology to 2.5D and 3D many-core architectures
	Presenter: Pascal Vivet, CEA-LETI (FR)
11:15	**Special session on Programming models and methods for heterogeneous parallel embedded systems**
	Organizer: Jeronimo Castrillon, TU Dresden (DE)
	Chairman: Jeronimo Castrillon, TU Dresden (DE)
11:15	Supporting Static Binding in Stream Rewriting for Heterogeneous Many-Core Architectures
	Lars Middendorf; Christian Haubelt
11:40	Why Comparing System-level MPSoC Mapping Approaches is Difficult: a Case Study
	Andres Goens; Robert Khasanov; Jeronimo Castrillon; Simon Polstra; Andy Pimentel
12:05	Exploration of SW/HW co-designs space by synthesis of dataflow programs
	Simone Casale Brunet; Endri Bezati; Marco Mattavelli
12:30	**Lunch**
13:30	**Keynote**
	Mind the gap
	Presenter: Andreas Hansson, ARM (UK)
14:15	**Special Session on Approaches and Frameworks for Predictable Multi-Core Processing**
	Organizer: Jürgen Teich, Friedrich-Alexander-Universität Erlangen-Nürnberg (DE)
	Chairman: Davide Bertozzi, University of Ferrara (IT)
14:15	The ForeC Synchronous Deterministic Parallel Programming Language for Multicores
	Eugene Yip; Alain Girault; Partha Roop; Morteza Biglari-Abhari
14:40	Portable Multicore Resource Management for Applications with Performance Constraints
	Connor Imes; David Kim; Martina Maggio; Hank Hoffmann
15:05	Language/Compilation of Parallel Programs for Predictable MPSoC Execution using Invasive Computing
	Jürgen Teich; Michael Glaß; Sascha Roloff; Wolfgang Schroeder Preikschat; Gregor Snelting; Andreas Weichslgartner; Stefan Wildermann
15:30	Constructing Time-Predictable MPSoCs: Avoid Conflicts in Temporal Control
	Peter Puschner; Bekim Cilku; Daniel Prokesch
15:55	**Coffee break**
16:30	**Session 1: Architectures**
	Chairman: Gilles Sassatelli, CNRS-LIRMM (FR)
16:30	AFFORDe: Automatic Allocation and Floorplanning FOR SPMD Architecture
	Wissem Chouchene; Rabie Ben Atitallah; Jean-Luc Dekeyser
16:55	Acceleration of Full-PIC simulation on a CPU-FPGA tightly coupled environment
	Ryotaro Sakai
17:20	Improvement of Line Coding Overhead Targeting Both Run-Length and DC-Balance
	Sarat Yoowattana; Tomohiro Yoneda
17:45	Data and commands communication protocol for neuromorphic platform configuration
	Alessandro Siino; Francesco Barchi; Sergio Davies; Gianvito Urgese; Andrea Acquaviva
18:10	**End of IEEE-MCSoC 2016 Day 1**

IEEE MCSoC-2016 Day 2: Thursday, September 22nd 2016 - Saint Clair 3 A	
8:00	**Welcome**
8:45	**Keynote**
	Brain-Inspired Intelligent SoCs and Applications
	Presenter: Hoi-Jun Hoo, KAIST (KR)
9:30	**Session 2: Interconnect Networks (NoCs) I**
	Chairman: Y. Bouchebaba, ONERA (FR)
9:30	Adaptive VC Organization and Arbitration for Efficient NoC Design
	Masoud Oveis Gharan; Gul N. Khan
9:55	Heuristic based Routing Algorithm for Network on Chip
	Asma Benmessaoud Gabis; Marc Sevaux; Pierre Bomel; Mouloud Koudil; Karima Benatchba
10:20	A scalability analysis of many cores and on-chip mesh networks on the TILE-Gx platform
	Ye Liu; Hiroshi Sasaki; Shinpei Kato; Masato Edahiro
10:45	**Coffee break**
11:00	**Session 4: Benchmarks**
	Chairman: Jürgen Teich, Friedrich-Alexander-Universität Erlangen-Nürnberg (DE)
11:00	A Robust Methodology for Performance Analysis on Hybrid Embedded Multicore Architectures
	Romain Saussard; Boubker Bouzid; Marius Vasiliu; Roger Reynaud
11:25	A Data Locality and Memory Contention Analysis Method in Embedded NUMA Multi-core Systems
	Lin Li; Markus Fussenegger; Gordon Cichon
11:50	Going beyond mean and median program performances
	Julien Worms; Sid Touati
12:15	High-Precision Performance Estimation of Dynamic Dataflow Programs
	Malgorzata Michalska; Simone Casale Brunet; Endri Bezati; Marco Mattavelli
12:40	**Lunch**
13:45	**Session 5: Interconnect Networks (NoCs) II**
	Chairman: Yves Durand, CEA-LETI (FR)
13:45	Power Management Controller for Online Power Saving in Network-on-Chips
	Stephanie Friederich; Marco Neber; Juergen Becker
14:10	Time-Triggered and Rate-Constrained On-Chip Communication in Mixed-Criticality Systems
	Hamidreza Ahmadian; Roman Obermaisser; Mohammed Abuteir
14:35	A Beneš Based NoC Switching Architecture for Mixed Criticality Embedded Systems
	Steve Kerrison; David May; Kerstin Eder
15:00	**Session 7: Emerging Technologies and Paradigms**
	Chairman: Ian O'Connor, Lyon Institute of Nanotechnology (FR)
15:00	Dynamic Ring-based Multicast with Wavelength Reuse for Optical Network on Chips
	Feiyang Liu; Haibo Zhang; Yawen Chen; Zhiyi Huang; Gu Huaxi
15:25	Impact of on-chip power distribution on Temperature-Induced Faults in Optical NoCs
	Melika Tinati; Somayyeh Koohi; Shaahin Hessabi
15:50	Pushing the Limits of Online Auto-tuning: Machine Code Optimization in Short-Running Kernels
	Fernando Endo; Damien Couroussé; Henri-Pierre Charles
16:15	**Coffee break**
16:30	**Session 9: Design II**
	Chairman: Hiroshi Saito, University of Aizu (JP)
16:30	High-Precision Power Modelling of the Tegra K1 big.Little Processor Architecture
	Kristoffer Stokke; Pål Halvorsen; Carsten Griwodz; Håkon K Stensland
16:55	Full-System Simulation of big.LITTLE Multicore Architecture for Performance and Energy Exploration
	Anastasiia Butko; Florent Bruguier; Abdoulaye Gamatié; Gilles Sassatelli; David Novo; Lionel Torres; Michel Robert
17:20	Communication-Based Power Modelling for Heterogeneous Multiprocessor Architecture
	Baptiste Roux; Matthieu Gautier; Olivier Sentieys; Steven Derrien
17:45	Design Space Exploration Problem Formulation for Dataflow Programs on Heterogeneous Architectures
	Malgorzata Michalska; Nicolas Zufferey; Endri Bezati; Marco Mattavelli
18:10	**End of IEEE-MCSoC 2016 Day 2**

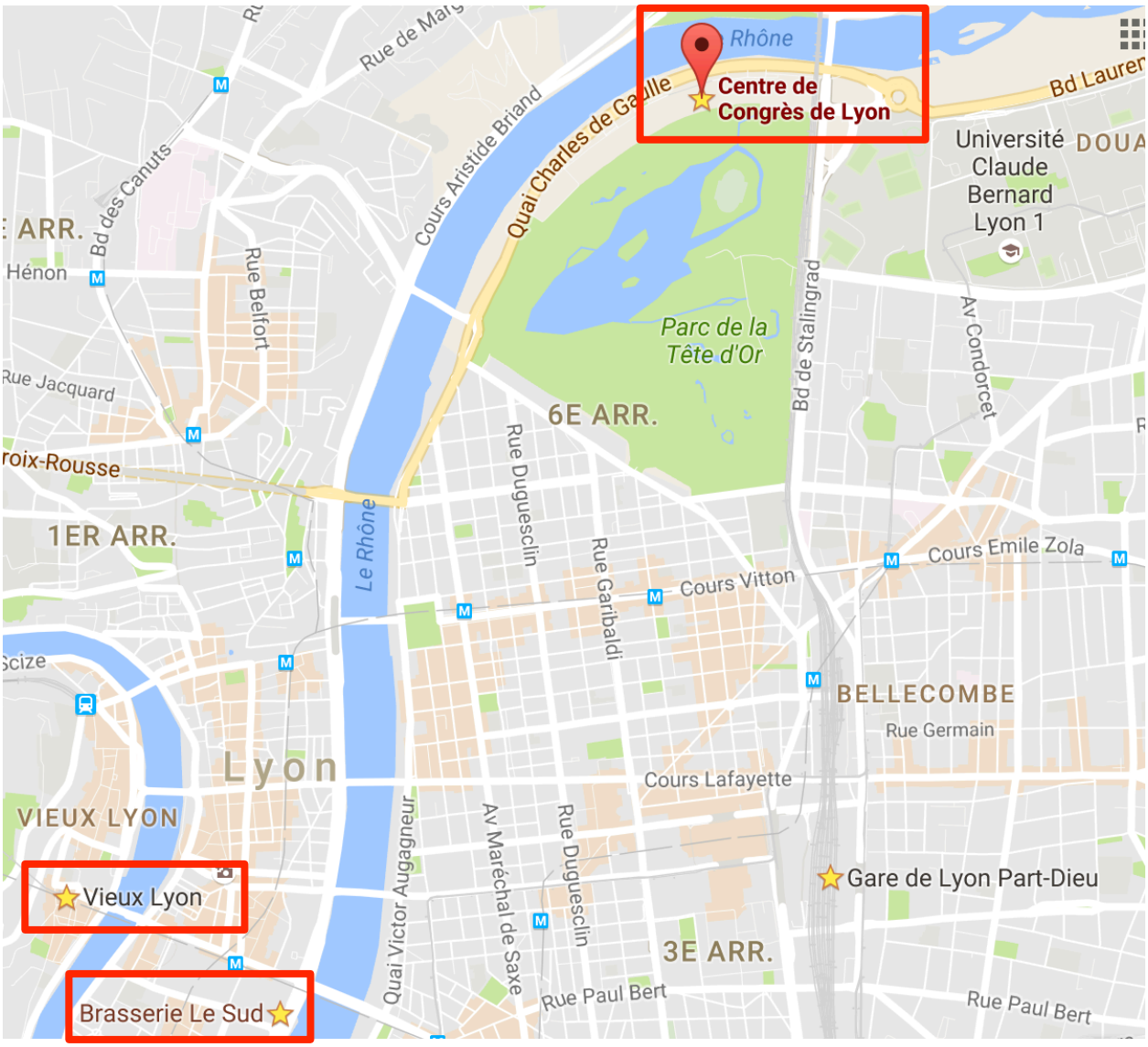
IEEE MCSoC-2016 Day 2: Thursday, September 22nd 2016 - Room Saint Clair 3 B	
8:00	**Welcome**
8:45	**Keynote held in room Saint Clair 3 A**
9:30	**Session 3: Energy efficiency**
	Chairman: Steve Kerrison, University of Bristol (UK)
9:30	The Role of Self-Awareness and Hierarchical Agents in Resource Management for Many-Core Systems *Maximilian Götzinger; Amir M. Rahmani; Martin Pongratz; Pasi Liljeberg; Axel Jantsch; Hannu Tenhunen*
9:55	Exploiting large memory using 32-bit energy-efficient manycore architectures *Mohamed Lamine Karaoui; Pierre-Yves Péneau; Quentin Meunier; Franck Wajsburt; Alain Greiner*
10:20	2-Step Power Scheduling with Adaptive Interval for Network Intrusion Detection Systems on Multicores *Tuong Phi Lau; Keiji Kimura*
10:45	**Coffee break**
11:00	**Special session on Auto-Tuning for Multicore and GPU (ATMG) I**
	Organizer: Satoshi Ohshima, University of Tokyo (JP)
	Chairman: Toshiyuki Imamura, RIKEN Advanced Institute for Computational Science (JP)
11:00	Faster method for tuning the tile size for tile matrix decomposition *Tomohiro Suzuki*
11:25	Auto-Tuning TRSM with an Asynchronous Task Assignment Model on Multicore and Multi-GPU Systems *Murilo Boratto; Pedro Alonso; Domingo Gimenez*
11:50	On constructing cost models for online automatic tuning using ATMathCoreLib *Seiji Nagashima; Takeshi Fukaya; Yusaku Yamamoto*
12:15	Autotuning of a Cut-off for Task Parallel Programs *Shintaro Iwasaki; Kenjiro Taura*
12:40	**Lunch**
13:45	**Session 6: Design I**
	Chairman: Christian Haubelt, University of Rostock (DE)
13:45	A Task Allocation Method for the DTTR Scheme based on the Parallelism of Tasks *Hiroshi Saito; Masashi Imai; Tomohiro Yoneda*
14:10	Accelerating Multicore Architecture Simulation using Application Profile *Keiji Kimura; Gakuho Taguchi; Hironori Kasahara*
14:35	Performance Prediction of Application Mapping in Manycore Systems with Artificial Neural Networks *Abdoulaye Gamatié; Roman Ursu; Manuel Selva; Gilles Sassatelli*
15:00	**Session 8: Reconfigurable and parallel computing**
	Chairman: Kenji Kise, Tokyo Tech (JP)
15:00	NoC based virtualized accelerators for cloud computing *Hiliwi Leake Kidane; El-Bay Bourennane; Gilberto Ochoa-Ruiz*
15:25	cReComp: Automated Design Tool for ROS-Compliant FPGA Component *Kazushi Yamashina; Hitomi Kimura; Takeshi Ohkawa; Kanemitsu Ootsu; Takashi Yokota*
15:50	Network on chip and parallel computing in embedded systems *Dihia Belkacemi; Youcef Bouchebaba; Mehammed Daoui*
16:15	**Coffee break**
16:30	**Special session on Auto-Tuning for Multicore and GPU (ATMG) II**
	Organizer: Satoshi Ohshima, University of Tokyo (JP)
	Chairman: Satoshi Ohshima, University of Tokyo (JP)
16:30	A Performance Model and Efficiency-Based Assignment of Buffering Strategies for Automatic GPU Stencil Code Generation *Yue Hu; David Koppelman; Steven Brandt*
16:55	Meta-Programming and Multi-Stage programming for GPGPUs *Ian Masliah; Marc Baboulin; Joel Falcou*
17:20	Automatic Thread-Block Size Adjustment for Memory-Bound BLAS Kernels on GPUs *Daichi Mukunoki; Toshiyuki Imamura; Daisuke Takahashi*
17:45	A Code Selection Mechanism Using Deep Learning *Hang Cui; Shoichi Hirasawa; Hiroyuki Takizawa; Hiroaki Kobayashi*
18:10	**End of IEEE-MCSoC 2016 Day 2**

IEEE MCSoC-2016 Day 3: Friday, September 23rd 2016 - Saint Clair 3 A	
8:00	**Welcome**
8:45	**Keynote**
	Towards Smart Wearable Systems in the Internet-of-Things Era
	Presenter: David Atienza, EPFL (CH)
9:30	**Session 10: Interconnect Networks (NoCs) III**
	Chairman: Gul Khan, Ryerson University (CA)
9:30	Distributed Dynamic Rate Adaptation on a Network on Chip with Traffic Distortion
	Yves Durand; Christian Bernard; Fabien Clermidy
9:55	Optimizing Latencies and Customizing NoC of Time-Predictable Heterogeneous Multi-Core Processor
	Zoran Salcic; Muhammad Nadeem; HeeJong Park; Juergen Teich
10:20	Increasing the Efficiency of Latency-Driven DVFS with a Smart NoC Congestion Management Strategy
	José Vicente Escamilla López; Mario Roberto Casu; Jose Flich
10:45	**Coffee break**
11:00	**Session 11: Programming**
	Chairman: Sid Touati, University Nice Sophia Antipolis (FR)
11:00	Network Contention-aware Method to Evaluate Data Coherency Protocols within a Compilation Toolchain
	Loïc Cudennec; Safae Dahmani; Guy Gogniat; Cédric Maignan; Martha Johanna Sepulveda Florez
11:25	Dual-Engine Cross-ISA DBTO Technique utilising MultiThreaded Support for Multicore Processor System
	Joo On Ooi; Fawnizu Azmadi Hussin; Mohamed Nordin Zakaria
11:50	**Closing remarks**
	lunch
12:30	**End of IEEE-MCSoC 2016**

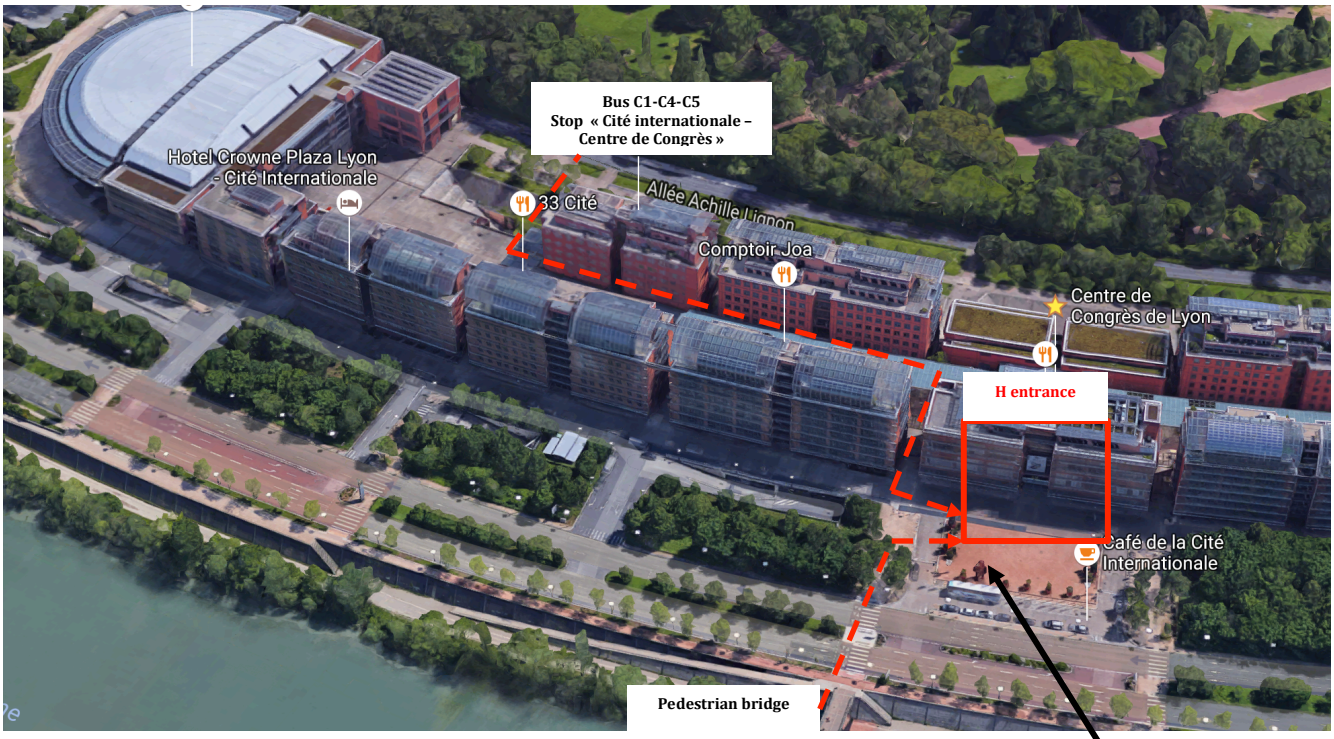
Conference places

Place	Activity	Address	Location	Website
Lyon convention center	All sessions, lunches and coffee breaks	50 Quai Charles de Gaulle 69463 Lyon cedex 06	By bus, take line C1 (10min from TGV Part-Dieu train station), C4 (20min from Jean Macé metro station) or C5 and get off at "Cité internationale – Centre de Congrès". Walk 5 min to **entrance H**. The event is located on the second floor, **St Clair level**.	http://www.ccc-lyon.com
Brasserie Le Sud	Gala Diner	11 Place Antonin Poncet 69002 Lyon	Nearest subway stop: Bellecour (metro lines A and D)	http://www.nordsudbrasseries.com/le-sud.html
Vieux Lyon	2 hour tour guide	Vieux Lyon metro station, line D	14:00: meeting point at street level, Av. Adolphe Max, 69005 Lyon	http://www.tcl.fr/en

Bus line C1 : http://www.tcl.fr/Me-deplacer/Toutes-les-lignes/C1
Bus line C4 : http://www.tcl.fr/Me-deplacer/Toutes-les-lignes/C4
Bus line C5: http://www.tcl.fr/Me-deplacer/Toutes-les-lignes/C5



Conference venue



Entrance H is located behind the bear