IEEE Heterogeneous Integration Roadmap: Aerospace and Defense (HIR-A/D)

Aerospace & Defense TWG Co-Chairs:
Tim Lee (Boeing)
Jeff Demmin (Keysight)

IEEE EPS Webinar
October 21, 2020

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Semiconductor and Defense
Project Manager
Keysight Technologies

Heterogeneous Integration Roadmap (HIR)
Driving Force and Enabling Technology for Systems of the Future
http://eps.ieee.org/technology/heterogeneous-integration-roadmap.html

Introduction to Heterogeneous Integration Roadmap

Lesson from our Industry's Foremost Prophet:

"Cramming more Components onto Integrated Circuits"
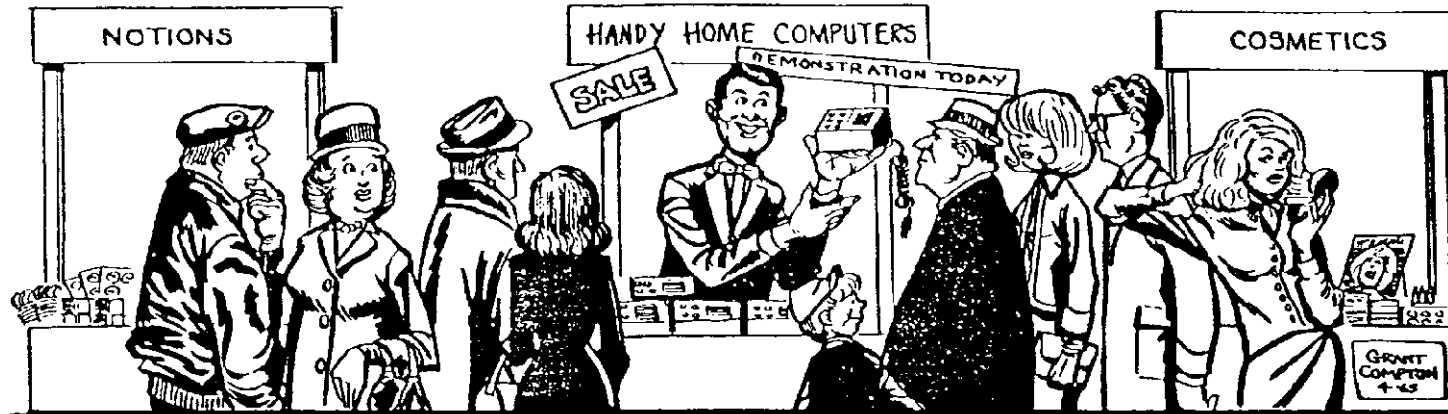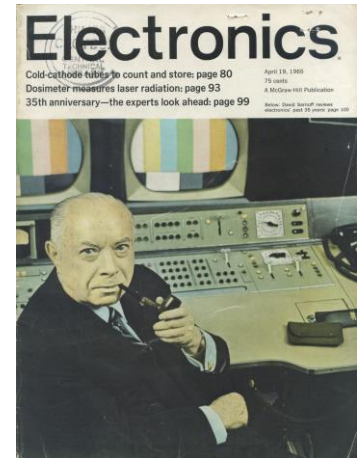Gordon Moore, pp. 114-117, *Electronics*, April 19, 1965 ⟶

Figure 1. Cartoon from Moore's paper illustrating his market vision [1]

"**Day of Reckoning.......**It may prove to be more economical to build large systems out of smaller functions, which are **separately packaged and interconnected**. The availability of large functions, combined with functional design and construction, should allow the manufacturer of large systems to design and construct a considerable variety of equipment both **rapidly and economically**."
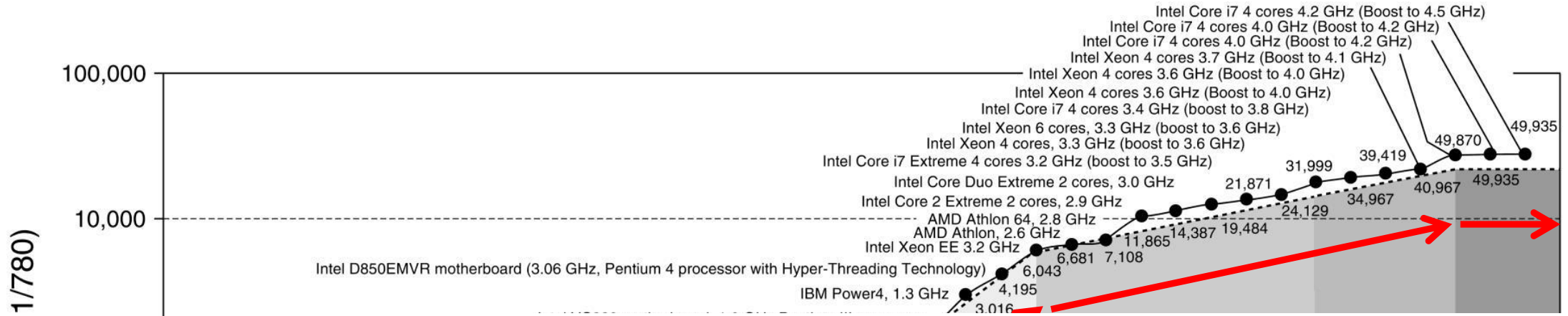
40 Years Of Progress In Computing

Source: John Hennessy (Chairman Alphabet) Plenary presentation at DARPA ERI Conference July 23 2018
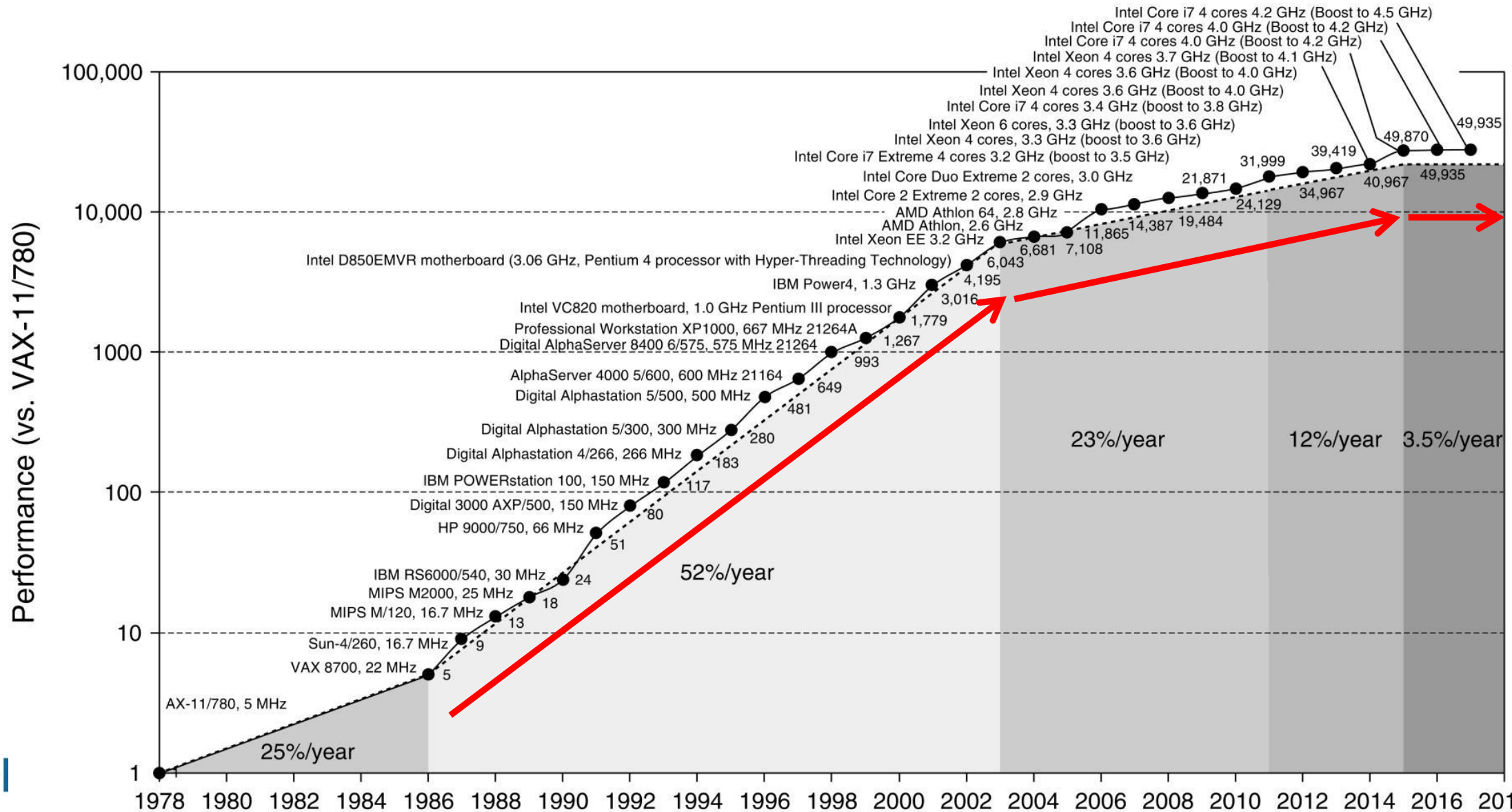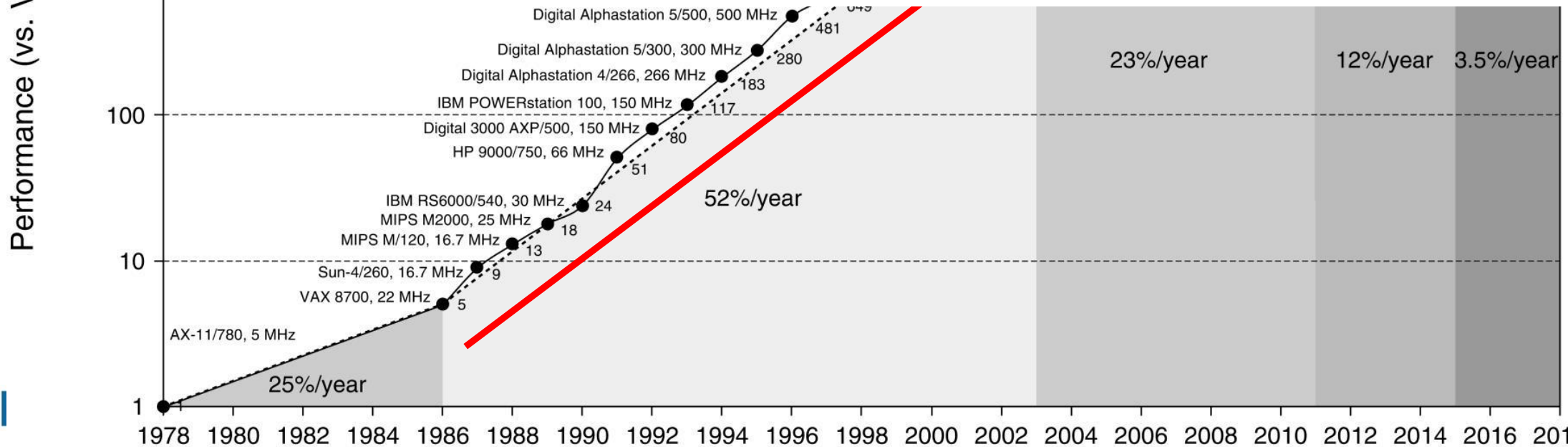
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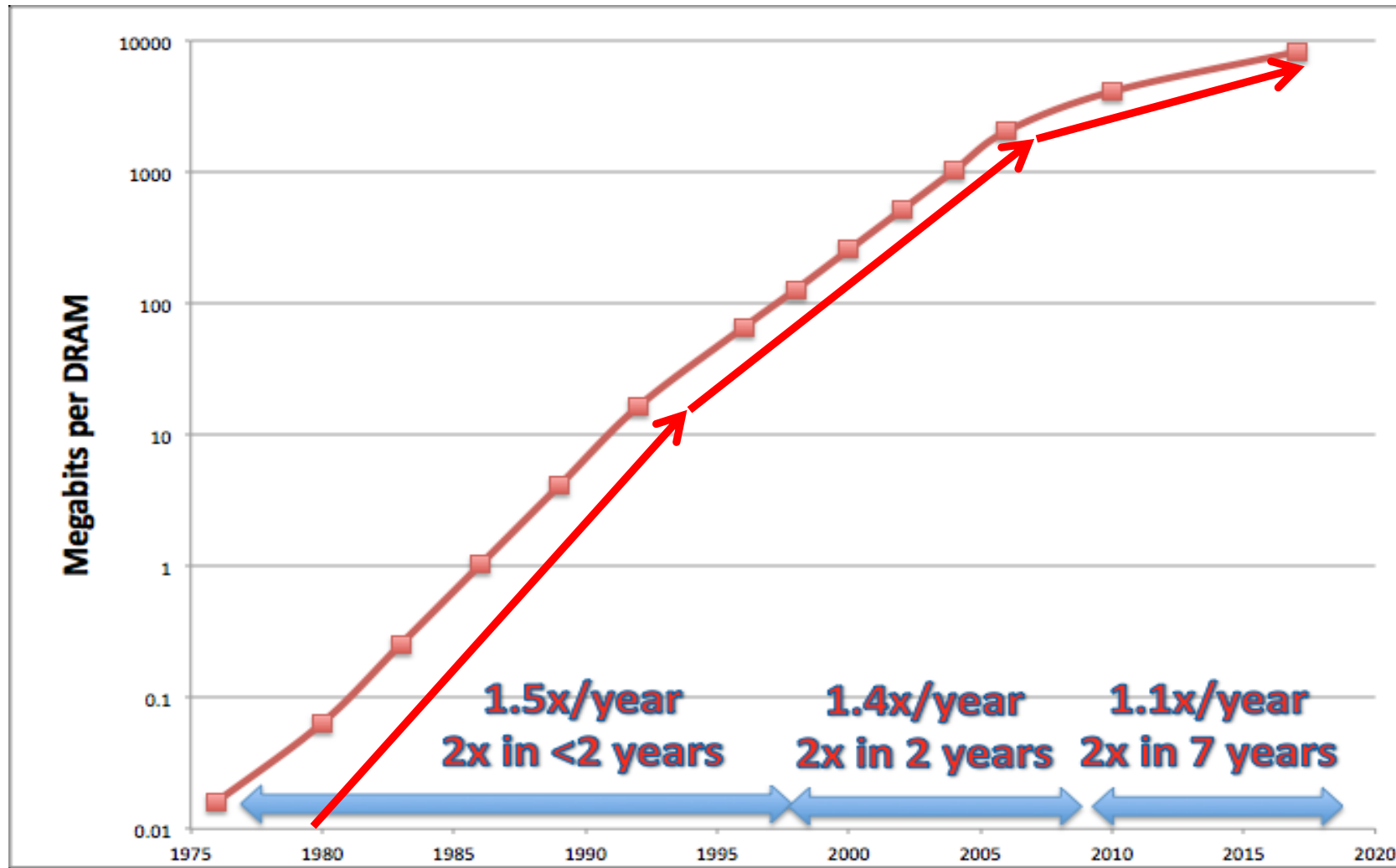**Progress in processor performance has slowed**

5

40 Year DRAM Memory Capacity Increase

Source: John Hennessy (Chairman Alphabet) Plenary presentation
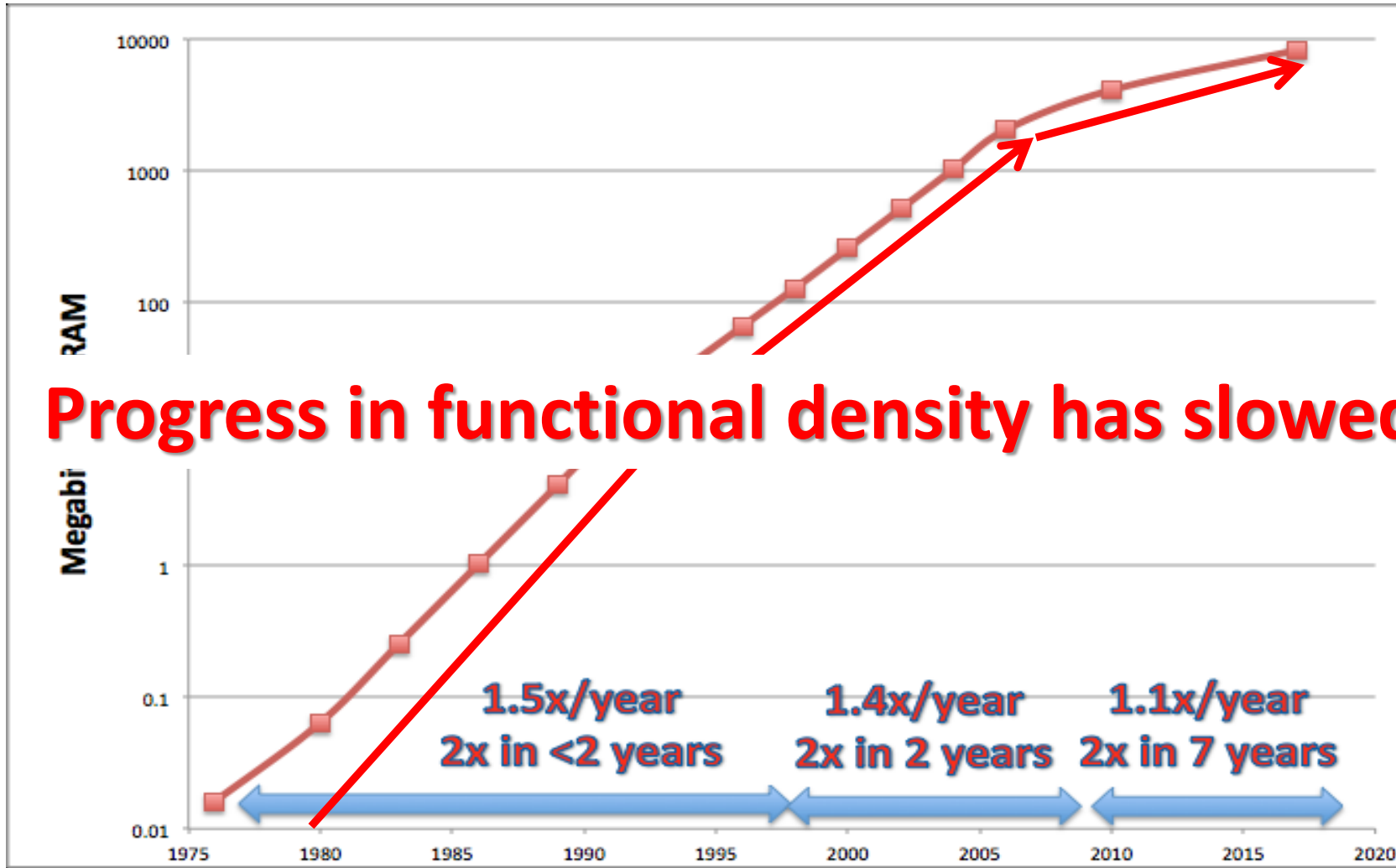"End of Moore's Law , a New Golden Age" at DARPA ERI Conference July 23 2018

40 Year DRAM Memory Capacity Increase

Source: John Hennessy (Chairman Alphabet) Plenary presentation
"End of Moore's Law , a New Golden Age" at DARPA ERI Conference July 23 2018

Moore's Law Economics Meeting Headwinds

Source : AMD Lisa Su "Delivering Future of High Performance Computing" Plenary Presentation DARPA ERI Conference July 15, 2019.

Semiconductor Technology Roadmap History

1991: World's first Open Source Technology Roadmap, the National Technology Roadmap for Semiconductors (NTRS) sponsored by the US Semiconductor Industry Association (SIA).

1998: NTRS expanded forming the first Global Technology Roadmap. Europe, Japan, Taiwan, and Korea joined. It was renamed International Roadmap for Semiconductors (ITRS).

2014: The benefits of Moore's Law scaling diminish and decision was made to end ITRS.

2015: The ITRS Heterogeneous Integration Focus Team signed an MOU with the IEEE CPMT Society initiating the formation of the Heterogeneous Integration Roadmap. HIR was founded with initiative from three IEEE Societies (Electronics Packaging Society, Electron Devices Society, Photonics Society) together with SEMI and ASME EPPD.

2016: The last edition of the ITRS was published July 8, 2016.

Packaging Roadmap Metrics: Slow Progress in ITRS
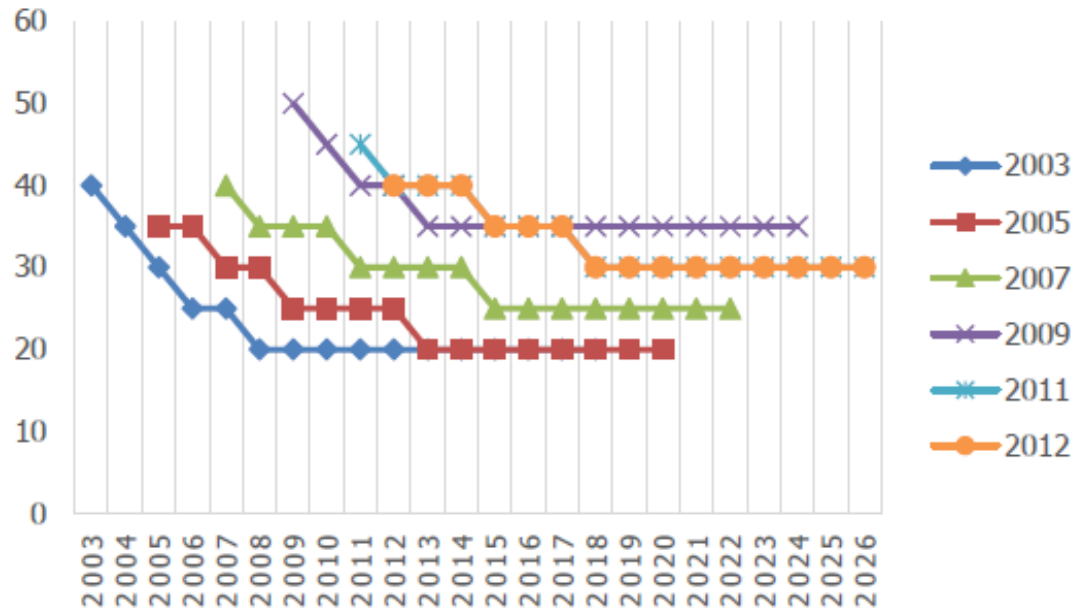
Wire bond pitch *increased* on the roadmap with shift from Au to Cu to decrease cost

PCB solder ball pitch roadmap just *pushed out laterally* for years

The Definition of Heterogeneous Integration
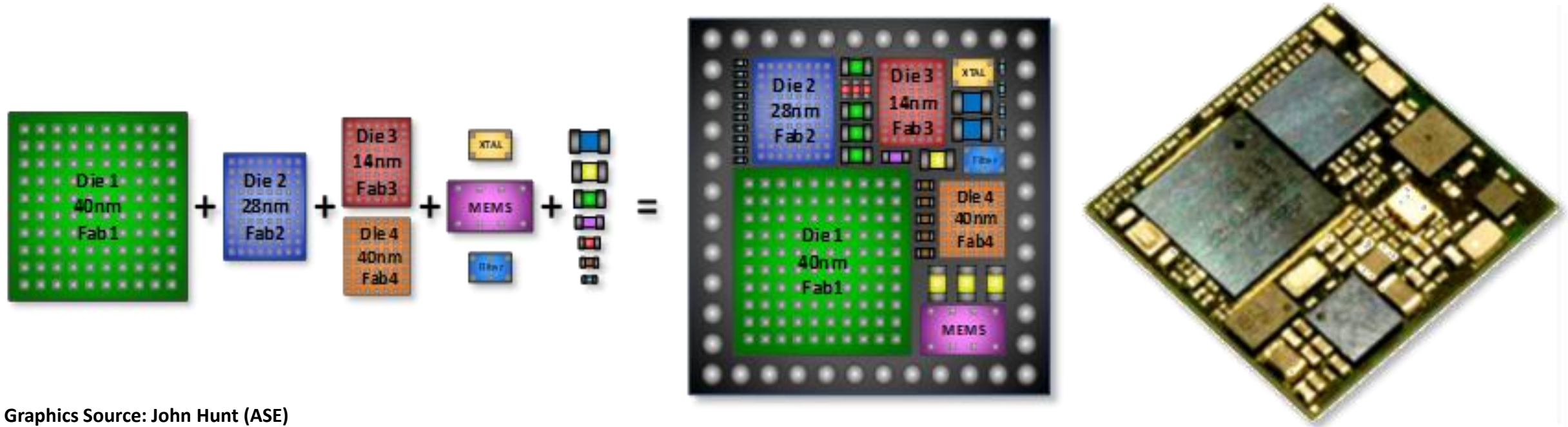
Graphics Source: John Hunt (ASE)

Heterogeneous by material, component type, circuit type, node, bonding/interconnect method, and sources

Homogeneous Integration to Heterogeneous Integration

1st and 2nd Generations of the AMD EPYC Processors

Source : AMD Lisa Su "Delivering Future of High Performance Computing" DARPA ERI Conference July 15, 2019
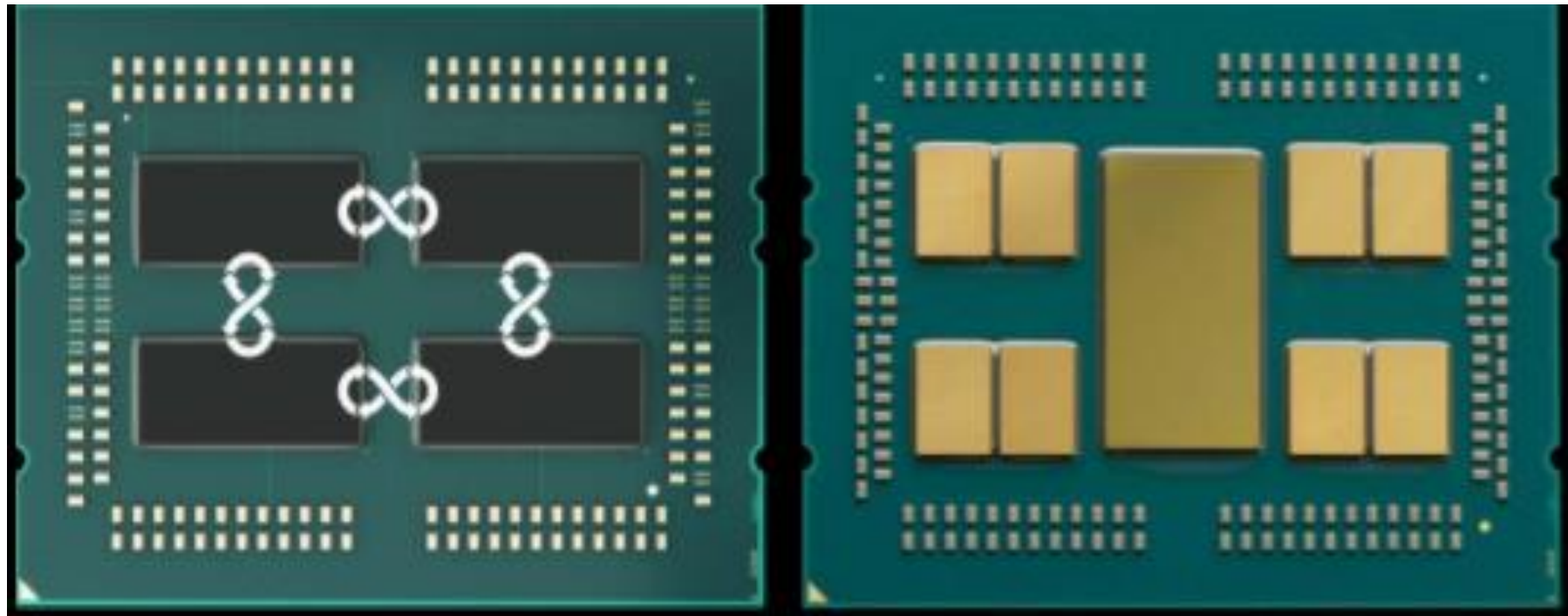
Left is large die split into 4 "chiplets" die (14nm) tightly coupled on an organic substrate

Right are 4 groups of 2 "chiplets" (7nm) on each side of larger I/O die (14nm) tightly coupled on an organic substrate

HIR International Roadmap Committee

- William (Bill) Chen, ASE Fellow & Senior Technical Advisor, (Chair)
- W. R. (Bill) Bottoms, Chairman 3MTS (Co-Chair representing EPS)
- Subramanian Iyer, Distinguished Professor UCLA (representing EDS)
- Amr Helmy, Chair Professor, U. of Toronto (Representing Photonics)
- Tom Salmon, VP SEMI Collaboration Platform (Representing SEMI)
- Ravi Mahajan, Intel Fellow (Representing ASME EPPD)
- Gamal Refai-Ahmed, Distinguished Engineer Xilinx (ASME EPPD alternate)

HIR Global Advisory Council

- Ajit Manocha: President and CEO of SEMI. Former CEO of GlobalFoundries and served as chair of SIA. Also served in executive roles at Philips/NXP & Spansion.

- Nicky Lu: Founder and Chairman of Etron Technology in Taiwan. Served as chair of TSIA and WSC and is a member of the US National Academy of Engineering.

- Babak Sabi: Intel Corporation Corporate Vice President, General Manager, Assembly Test Technology Development.

- Hubert Lakner: Board of Directors Chairman, Fraunhofer Microelectronics Group and Founding Director of Fraunhofer Institute of Photonic Microsystems (IPMS) in Dresden.

Heterogeneous Integration Roadmap
Technical Working Groups

HI Market Applications

- High Performance Computing & Data Center
- Mobile
- Medical, Health & Wearables
- Automotive
- IoT
- Aerospace & Defense

Heterogeneous Integration Components

- Single Chip and Multi Chip Integration
- Integrated Photonics
- Integrated Power Electronics
- MEMS & Sensor Integration
- 5G RF and Analog Mixed Signal

Cross-Cutting Topics

- Materials & Emerging Research Materials
- Emerging Research Devices
- Test
- Supply Chain
- Security
- Thermal Management

Integration Processes

- SiP
- 3D + 2D & Interconnect
- WLP (fan in and fan out)

Design

- Co-Design & Simulation – Tools & Practice

Download HIR Chapters: http://eps.ieee.org/hir

Mission Statement for HIR – Aerospace / Defense (A/D)

- The mission of **Heterogeneous Integration Roadmap for Aerospace and Defense** is to provide guidance and recommend solutions to the profession, industry, academia and government to identify key technical challenges with sufficient lead time that they do not become roadblocks preventing the continued progress in **Aerospace and Defense** electronics.

- There is the need to address heterogeneous integration technologies for new capabilities for embedded high-speed computing, cyber, sensors, C4ISR and RF/analog for **unique sets of requirements**, production volumes and lifecycle timelines.

- That progress is essential to the future growth of the industry and the realization of the promise of continued impact on aerospace, defense and security applications.

- The approach is to identify the requirements for heterogeneous integration in the **A-D** electronics industry with 5-, 10- and 15-year horizons, determine the difficult challenges that must be overcome to meet these requirements and, where possible, identify potential solutions and **synergies between the greater commercial sectors and the smaller A-D community.**

HIR: Initial Roadmap Press Release
Oct. 10, 2019

PISCATAWAY, N.J.--([BUSINESS WIRE](#))--IEEE, the world's largest technical professional organization dedicated to advancing technology for humanity, today announced the 2019 release of the **Heterogeneous Integration Roadmap (HIR), a roadmap to the future of electronics identifying technology requirements and potential solutions. The primary objective is to stimulate pre-competitive collaboration among industry, academia and government to accelerate progress. The roadmap offers professionals, industry, academia and research institutes a comprehensive, strategic forecast of technology over the next 15 years.** The HIR also delivers a 25-year projection for heterogeneous integration of emerging devices and materials with longer research-and-development timelines.

Download HIR Chapters:
http://eps.ieee.org/hir

Backdrop to A & D Electronics

Future Warfighting Systems

System of Systems

Autonomous and collaborative

Miniature and swarming

Cyber and social

Human and robot collaboration

| Diverse protected links | Decentralized systems | Human and autonomous systems | Information microsystems | Leverage global technology and infrastructure |

HIR
HETEROGENEOUS INTEGRATION ROADMAP

ASD(R&E)

IEEE

ELECTRON DEVICES SOCIETY
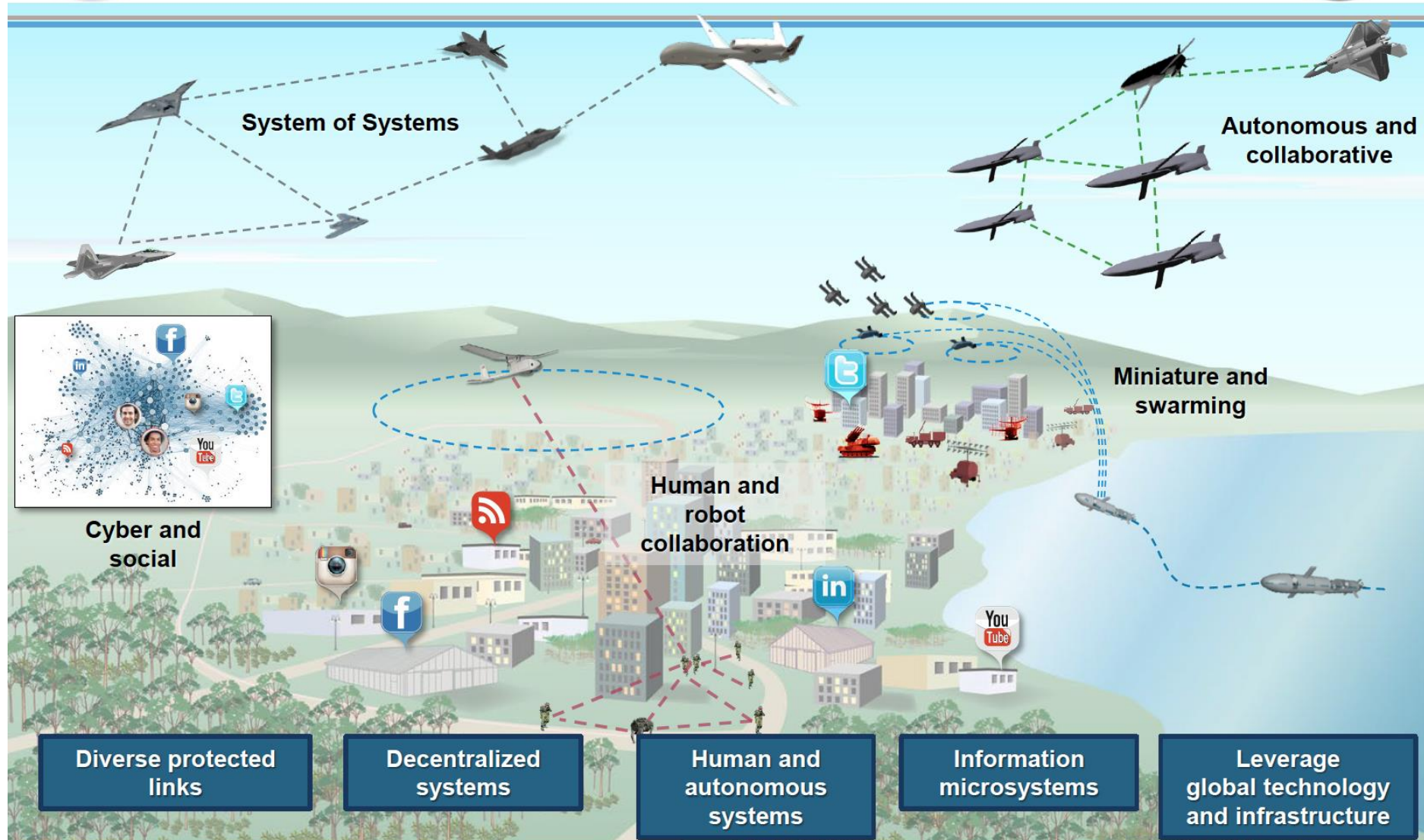
Future Warfighting Systems
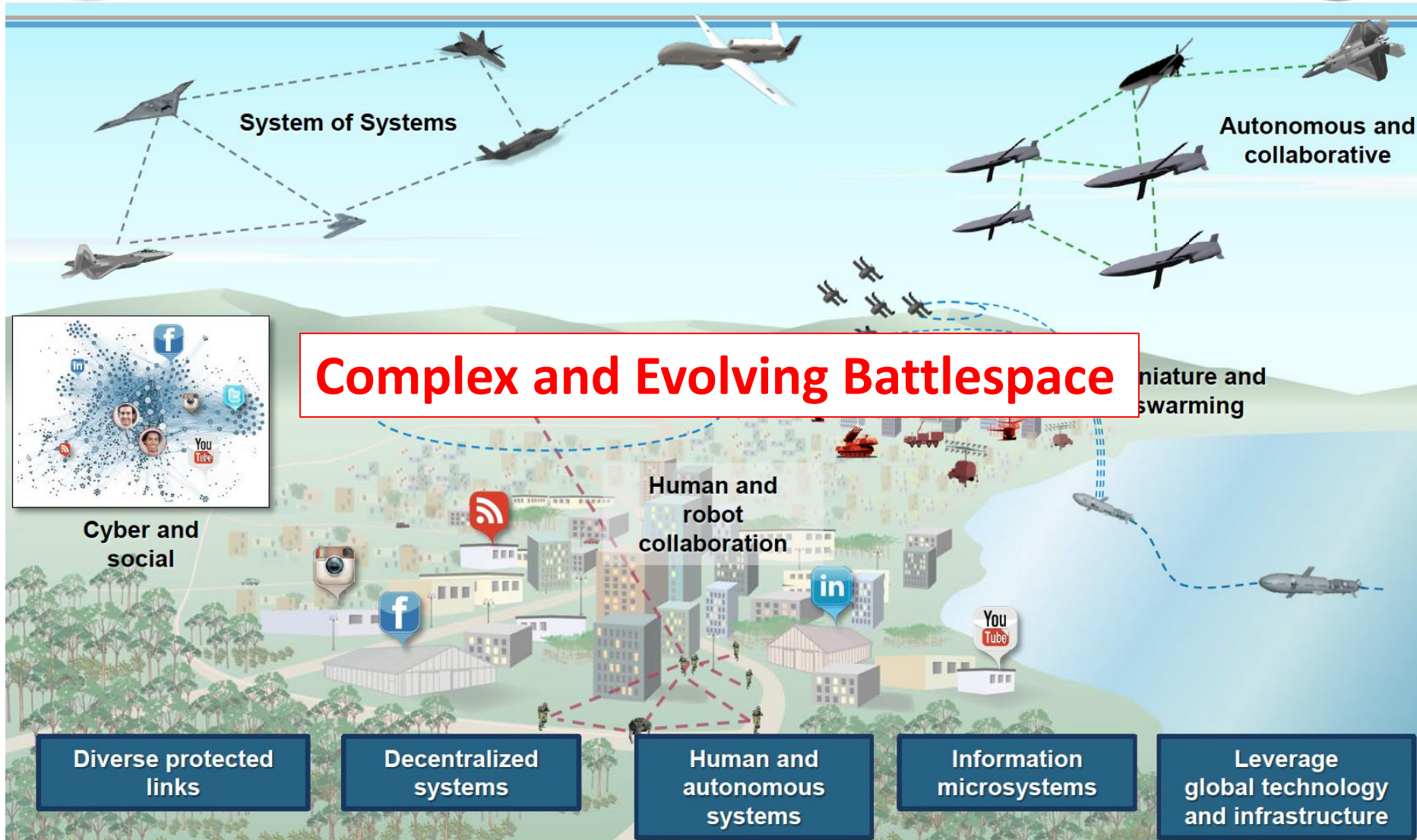
Complex and Evolving Battlespace
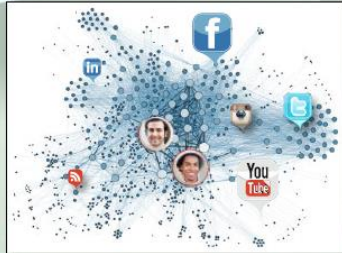
System of Systems

Autonomous and collaborative

Miniature and swarming

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Human and robot collaboration

| Diverse protected links | Decentralized systems | Human and autonomous systems | Information microsystems | Leverage global technology and infrastructure |

National Defense Strategy (2018):
Emphasis on Speed and Commercial Technology

- National Defense Strategy: "Platform electronics and software must be designed for routine replacement instead of static configurations that last more than a decade ... **Deliver performance at the speed of relevance.**"

- **New commercial technology** will change society and, ultimately, the character of war. The fact that many technological developments will come from the commercial sector means that state competitors and non-state actors will also have access to them, a fact that risks eroding the conventional overmatch to which our Nation has grown accustomed.

https://dod.defense.gov/Portals/1/Documents/pubs/2018-National-Defense-Strategy-Summary.pdf

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Roadmaps help both the pace of progress and cross-pollination of innovations.

https://dod.defense.gov/Portals/1/Documents/pubs/2018-National-Defense-Strategy-Summary.pdf

DoD Funding Historical Perspective

Fig. 1 – Defense Topline – A Historical Funding Picture

https://www.semiwiki.com/forum/content/7368-meeting-challenges-national-defense-strategy.html
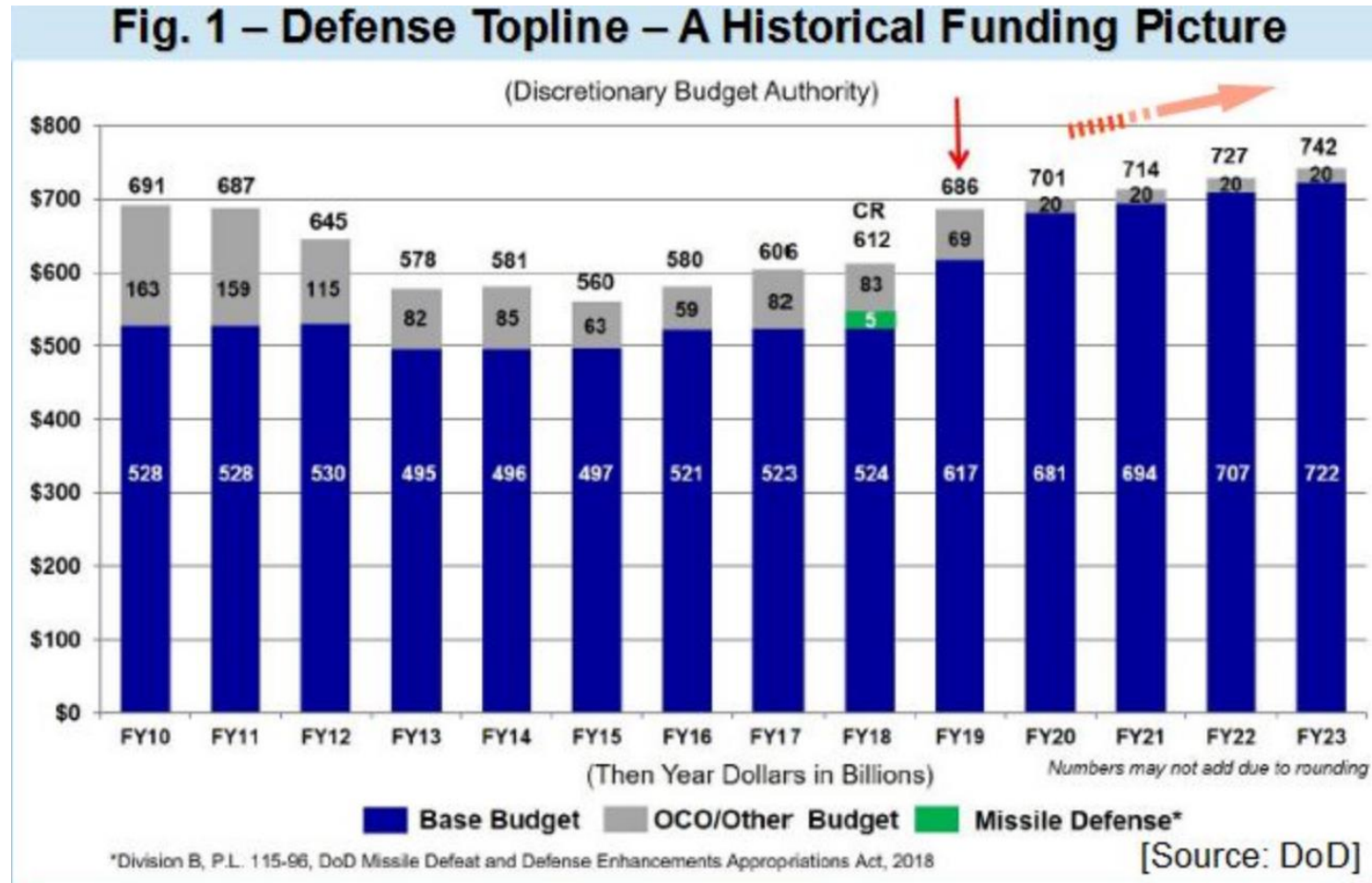
US Defense R&D Trend

Trends in Defense R&D, 1976-2020
Budget authority in billions of FY 2020 dollars

Legend:
- 2020 COVID-19 Spending
- 2009 Recovery Act
- DHS Defense-Related Activities
- DOE Atomic Defense
- DOD Science & Technology
- DOD Weapons + Other
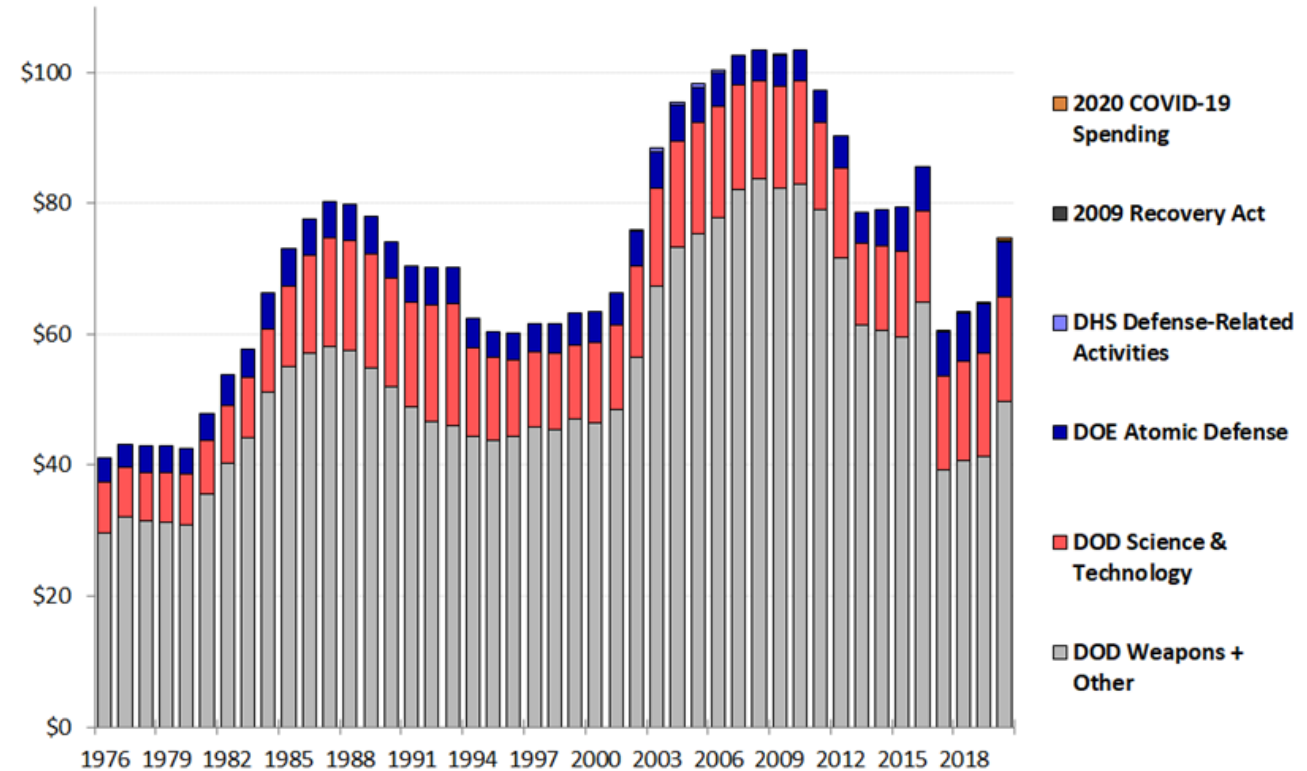
Note: Beginning in FY 2017, federal agencies have revised what they consider R&D. Late-stage development, testing, and evaluation programs, primarily within the Defense Department, are no longer counted as R&D. Source: AAAS Research & Development series and agency budget documents. © 2020 AAAS

https://www.aaas.org/programs/r-d-budget-and-policy/historical-trends-federal-rd

IC Manufacturing in a Globalized Independent Supply Chain
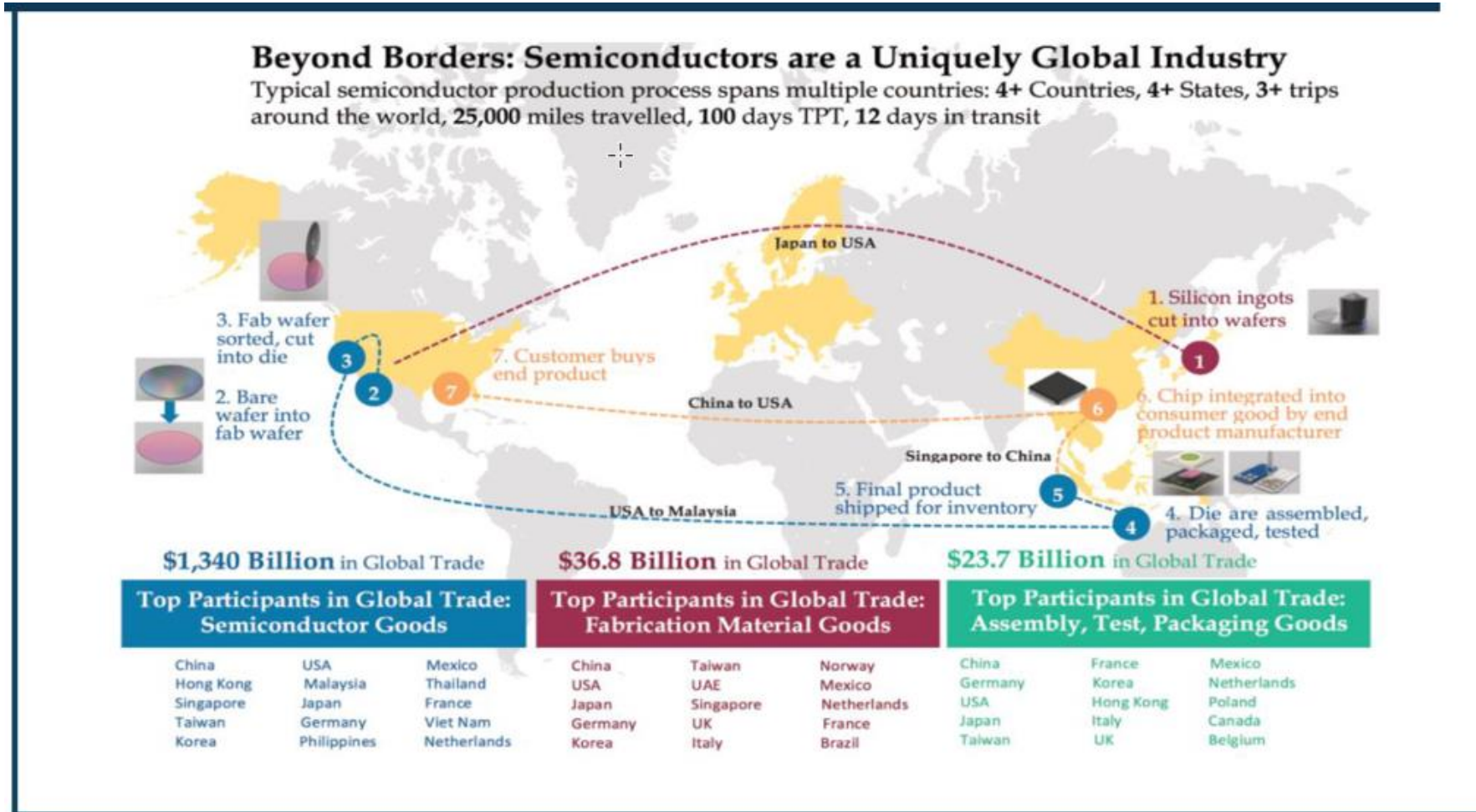
Recent Government HI Programs

"Creating Helpful Incentives to Produce Semiconductors (CHIPS) for America Act"*

- Creates a **40-percent refundable investment tax credit (ITC) for qualified semiconductor equipment** (placed in service) or any qualified semiconductor manufacturing facility investment expenditures through 2024. The ITC is reduced to 30 percent in 2025, 20 percent in 2026, and phases out in 2027.

- Directs the Secretary of Commerce to create a **$10 billion federal match program that matches state and local incentives** offered to a company for the purposes of building semiconductor fabs with advanced manufacturing capabilities.

- Creates a **new NIST Semiconductor Program** to support advanced manufacturing in America. The program's funds will also support STEM workforce development, ecosystem clustering, U.S. 5G leadership, and advanced assembly and test.

- Authorizes funding for DOD to execute research, development, workforce training, test, and evaluation for programs, projects, and activities in connection with semiconductor technologies and direct the implementation of a plan to utilize **Defense Production Act Title III** funding to establish and enhance a domestic semiconductor production capability.

*S.3933 and H.R. 7178

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Clear focus on manufacturing not just R&D

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"Creating Helpful Incentives to Produce Semiconductors (CHIPS) for America Act"

- Creates new R&D streams to ensure U.S. leadership in semiconductor technology and innovation is critical to American economic growth and national security:
  - $2 billion to implement the Electronics Resurgence Initiative at DARPA.
  - $3 billion to implement semiconductor basic research programs at NSF.
  - $2 billion to implement semiconductor basic research programs at the DoE.
  - $5 billion to establish an **Advanced Packaging National Manufacturing Institute** under the Department of Commerce to establish U.S. leadership in advanced microelectronic packaging and, in coordination with the private sector, to promote standards development, foster private-public partnerships, create R&D programs to advance technology, create an investment fund ($500M) to support domestic advanced microelectronic packaging ecosystem.
- Broad reach: DARPA, NSF, DoE, DoC

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National security is not just defense.

DARPA'S HISTORY OF INTEGRATION INNOVATION

ASEM

VISA

3D-IC

3D FPA Stack

COSMOS

CHIPS

DAHI

E-PHI

MOABB
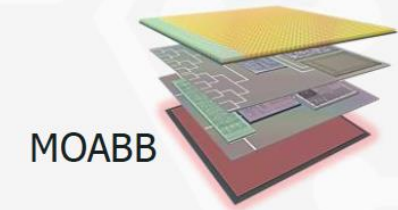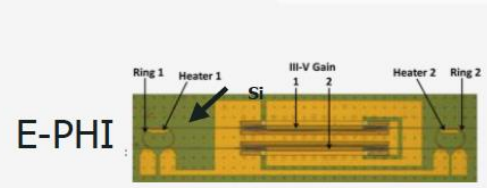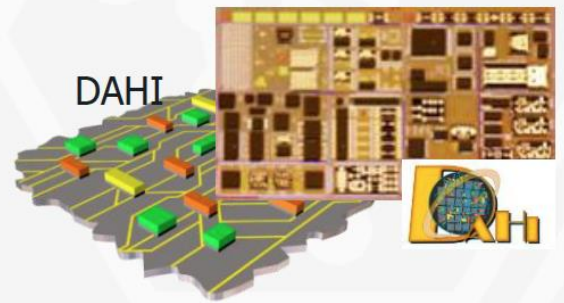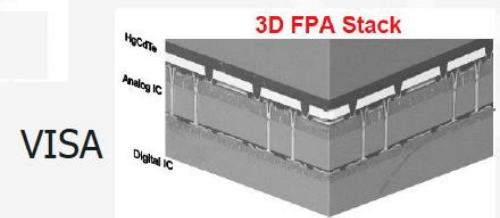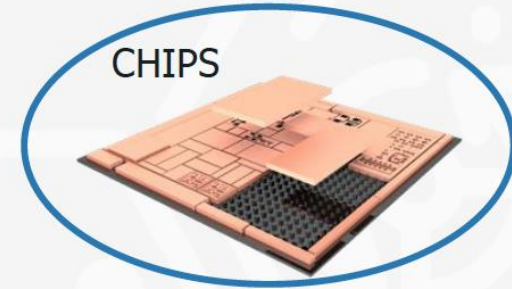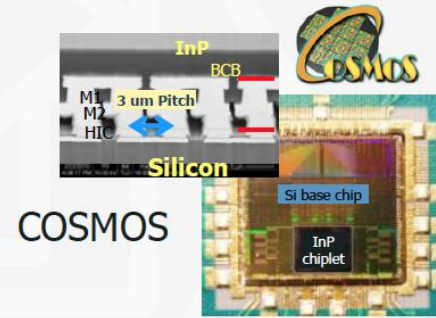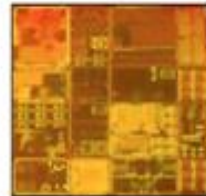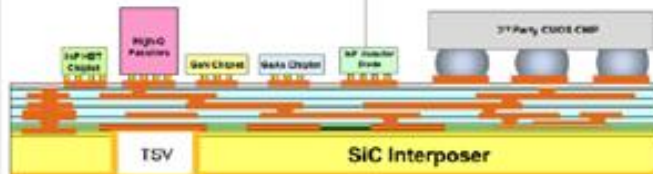
ASEM: Application Specific Electronic Modules
E-PHI: Electronic-Photonic Heterogeneous Integration
VISA: Vertically Integrated Sensor Arrays
COSMOS: Compound Semiconductor Materials on Silicon
DAHI: Diverse Accessible Heterogeneous Integration
MOABB: Modular Optical Aperture Building Blocks
CHIPS: Common Heterogeneous Integration and IP Reuse Strategies

1990s   2000s   2010s   2020s

Sources: DARPA, Smithsonian Chips

DARPA's DAHI Program Illuminated Path Forward

Technology	MPW0	MPW1	MPW2	MPW3	Future MPWs
CMOS	IBM 65nm	GF 45 nm	GF 45 nm	GF 45 nm	GF 45 nm
InP HBT	TF4 (2 metals)	TF4 (3 metals)	TF4 (4 metals)	TF4 (4 metals)	TF4 (4 metals)
		TF5 (3 metals)	TF5 (4 metals)	TF5 (4 metals)	TF5 (4 metals)
InP Varactor Diode					AD1
GaN HEMT	GaN20	GaN20	GaN20	GaN20	GaN20
	T3 (HRL)	T3 (HRL)	T3 (HRL)	T3 (HRL)	T3 (HRL)
GaAs HEMT				P3K6	P3K6
Passive Components		PolyStrata (Nuvotronics)	PolyStrata (Nuvotronics)	PolyStrata (Nuvotronics)	PolyStrata (Nuvotronics)
Base Substrate	CMOS	CMOS	CMOS	CMOS	CMOS
				SiC Interposer (IWP5)	SiC Interposer (IWP5)

DAHI = Diverse

8

Emergence of Chiplets as the Evolution of Moore's Law

- Chiplets (smaller pieces of silicon) will enable their silicon architects to design and fabricate silicon systems more quickly
  - Shorter time to market to mix and match modular pieces linked by shorter data interconnections instead of complex SOC design
  - Lower design costs and risks

- Industry leaders like Intel and AMD are implementing chiplet strategies
  - Ramune Nagisetty, a senior principal engineer at Intel calls it "an evolution of Moore's law."
  - AMD's Papermaster: "I think the whole industry is going to be moving in this direction"

- DARPA jump-started the development of "chiplet" ecosystem via the CHIPS program
  - CHIPS = Common Heterogeneous Integration and IP Reuse Strategies
  - Numerous organizations are now pursuing a range of approaches: ODSA, OCP, CHIPS Alliance, etc.

https://www.wired.com/story/keep-pace-moores-law-chipmakers-turn-chiplets/

The CHIPS Program in a Nutshell

DESIGN

Today: Monolithic → Tomorrow: Pseudolithic + Heterogeneous
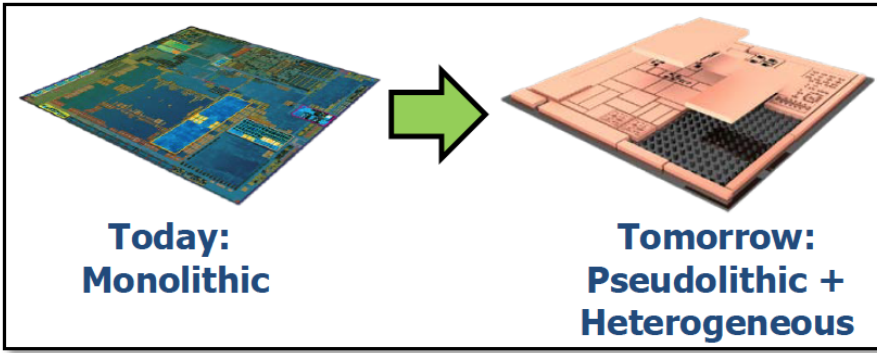
Image source: Intel

TECHNOLOGY

✓ A universal CHIPS interface standard

✓ SOTA manufacturing for DoD

✓ A critical set of IP chiplets

CHIPS END STATE

IP Blocks | CAD tools | Architecture | Design | Verification | Fabrication | Pkg / Test | Systems

ARM Cadence TSMC | Cadence Mentor Synopsys | Raytheon Northrop Lockheed Boeing BAE | CHIPS → | Raytheon Northrop Lockheed Boeing BAE

Raytheon Northrop Lockheed Boeing BAE

Design specs

Chiplets

Commercial | Raytheon Northrop HRL — Defense | Jariet Intrisix ? — Emerging | Mouser Digi-Key ? — Distributor

Source: DARPA

CHIPS Program Step #1: Agree on a Standard Interface
Intel Advanced Interface Bus (AIB) Enables Modular Design
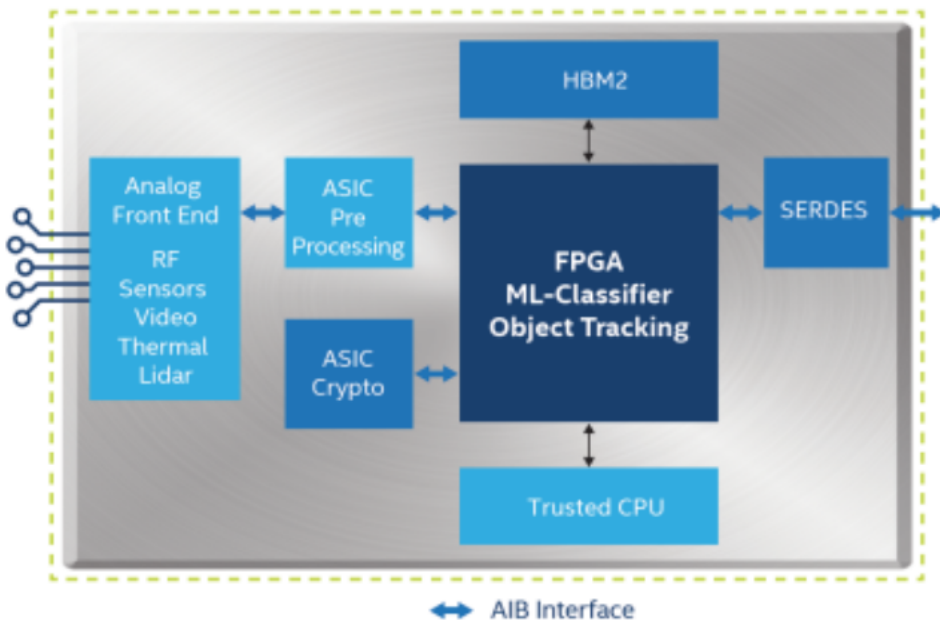
AIB Interface

Intel's Advanced Interface Bus (AIB) is a die-to-die PHY level standard that enables a modular approach to system design with a library of chiplet intellectual property (IP) blocks.

AIB uses a clock forwarded parallel data transfer mechanism similar to DDR DRAM interfaces. AIB is process and packaging technology agnostic—Intel's Embedded Multi-Die Interconnect Bridge (EMIB) or TSMC's CoWoS* for example.

Intel now provides the AIB interface license royalty-free to enable a broad ecosystem of chiplets, design methodologies or service providers, foundries, packaging, and system vendors.

- AIB was supported by the DARPA CHIPS program.
- AIB specification is now available to the electronics community

Figure: example of a possible heterogeneous system in package (SiP) that combines sensors, proprietary ASIC, FPGA, CPU, Memory and I/O using AIB as the chiplet interface.

https://www.intel.com/content/www/us/en/architecture-and-technology/programmable/heterogeneous-integration/overview.html

CHImPS Demonstration

- Heterogeneous Integration (EMIB)
- Standard Interface (AIB)
- IP Reuse
- Leading Edge Devices
  - Intel FPGA
  - Jariet converters
  - U of Michigan ASIC
  - Intel SERDES
  - Ayar Labs optical

DARPA CHIPS FPGA Module

Image: Intel
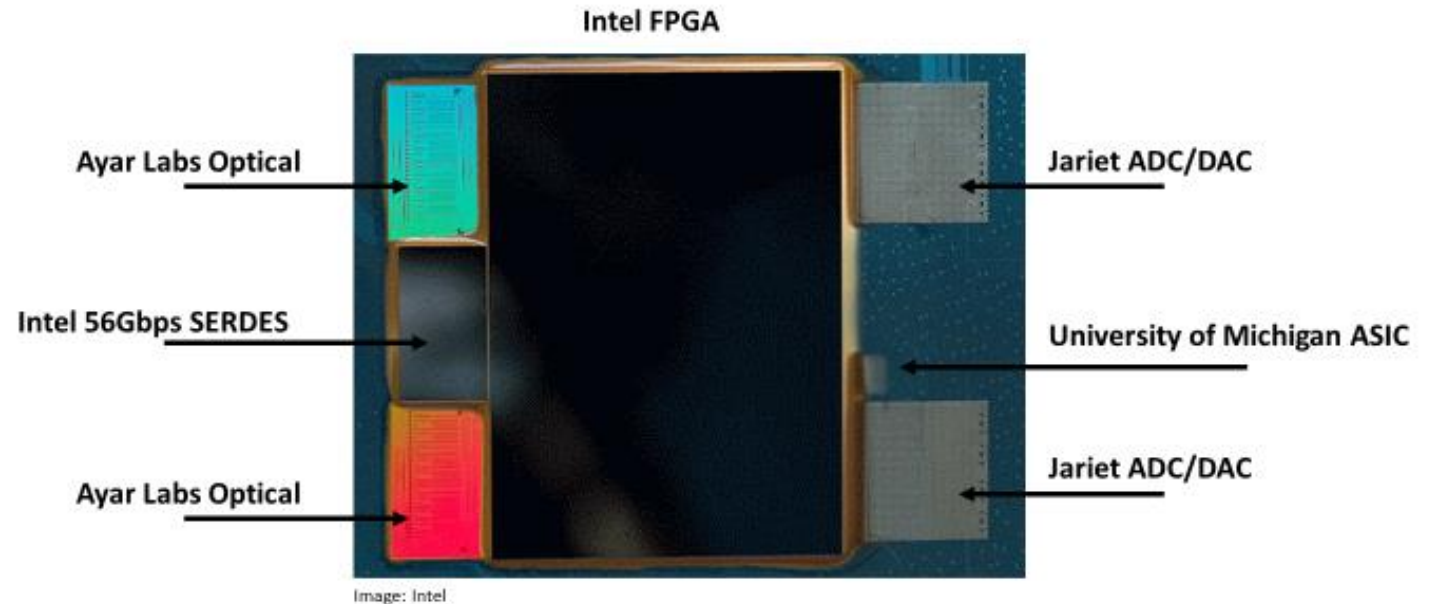
DARPA CHIPS Clarified Requirements for HI Manufacturing

CHIPS Manufacturing Wishlist

		Target Value
Dense Interconnect	Metallization material	Copper
	Front end metal layers	4 – 6
	Front end metal wiring density	~0.5 µm line/space
	Size (full reticle)	26 x 33 mm²
	Stitching (strongly desired)	6" x 6"?
TSVs	Depth	100-200 µm
	Diameter	25 µm
	Pitch	150 µm
Assembly	Back side bump pitch	150 µm C4
	Back side RDL	Needed, C4 on via?
	Front end bump pitch	55 µm Cu (10 µm roadmap)
	Chiplets supported	7nm to 180nm
	Chiplets assembled	2 - 100

Potential Engagement Path

2018 2019 2020 2021 2022 2023 2024 2025

Stand up a National Capability for 2.5D/3D Integration

Manufacturing ramp
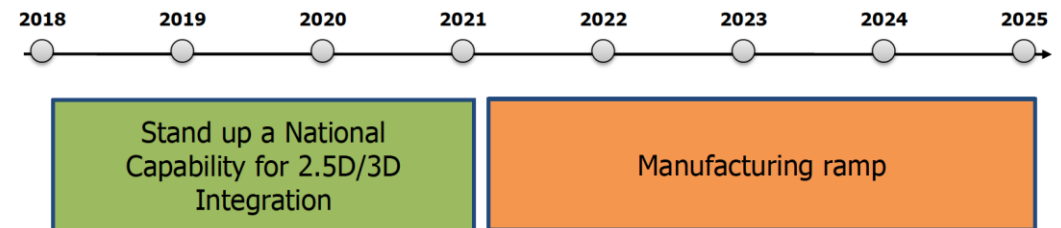
- Commercial **on-shore** manufacturing
  - (See previous slide)
  - Si interposer w/ TSVs
  - Organic package substrates
  - Copper bumping (<=55 µm)
  - C4 bumping (150 µm)
  - 2.5D assembly
  - 3D assembly
  - Flip Chip Assembly
  - SOTA automation
- Assemble all silicon sources!
- Turnkey model

- "MOSIS for 2.5D"
- Agile PDK development
- Yield ramping
- Manufacturing cost optimization
- NPI cost optimization "zero" target
- Long Term Goals:
  - ~$20 turnkey packaging cost
  - 2 week assembly turn
  - Standard fab turns
  - Zero email order

Source: DARPA

"SHIP": SOTA Heterogeneous Integrated Packaging

- Brett Hamilton, Distinguished Scientist for Trusted Microelectronics at NSWC Crane, is the Principal Technical Lead for the SHIP project.
  - SHIP gives us the ability to leverage state-of-the-art commercial processing power needed for modern weapon systems such as autonomous systems where artificial intelligence and real-time sensor data processing is critical
  - For these types of applications, SHIP significantly reduces size, weight, and power, while increasing performance.

- By having a secure SHIP design, assemble and test facility, DoD will greatly lower supply chain risk while enabling the ability to better protect the DoD's intellectual property (IP). In such an environment, DoD can integrate more robust security mechanisms, critical in lowering cyber security risks.

https://www.navsea.navy.mil/Media/News/Article/2005099/nswc-crane-leverages-ota-to-ensure-that-the-us-government-has-access-to-secure/

SHIP Requirements

SHIP Vision of Secure HI
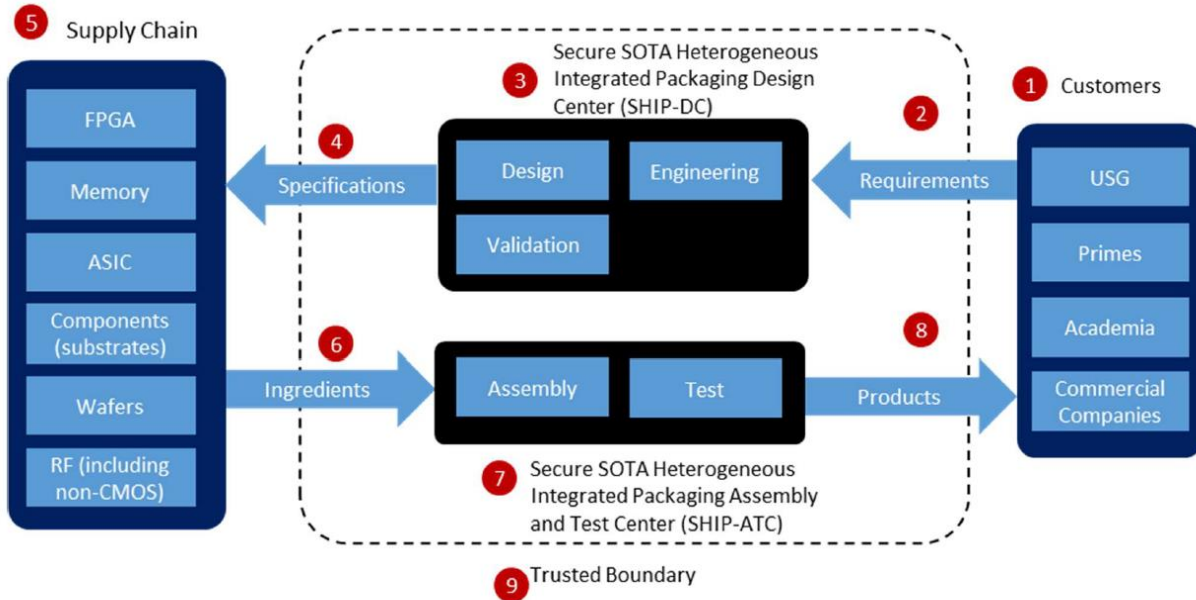
Figure 1 Notional design and prototype manufacturing flow

SHIP General Specifications

Table 3 General Capacity and Capability for the SHIP-ATC

Category	IOC	FOC	Scale
Capacity: Volume (annual)	1k+	10k+	100k
Silicon interposer	Required	Required	Required
Organic interposer	Preferred	Required	Required
Utilize SOTA COTS FPGA[1] and programmable devices	Required	Required	Required
Structured ASIC	Preferred	Preferred	Required
Security	ITAR	ITAR	Classified
Number of Chips/Package[2]	4	8	12+
Supply Chain target	>50% US	>75% US	>90% US
Can process singulated die	Required	Required	Required
Can process up to 300mm wafers	Preferred	Required	Required
Can process 200mm wafers	Preferred	Preferred	Required

[1] Must include ability to integrate and test SOTA FPGA (<14nm), not required for RF centric applications

[2] Could include, but not limited to, memory, ADC/DAC, transceivers, optical couplers, ASIC, structured ASICs, etc.

SHIP Assembly Specifications

Table 6 Advanced Microelectronics Assembly Specifications

		IOC	Final State
		IOC	**FOC**
Chip on Chip	Silicon Interposer Sizes	(22 x 33) mm	(22 x 33) mm
	Top Chip Process	All leading processes from 180nm to 7nm	
	Chip Size Range	(2 x 2) mm to (21 x 32) mm	(1 x 1) mm to (21 x 32) mm
	Chips Placed Per Interposer	20	
	Chip Spacing	100 μm	100 μm
	Chip Bump Pitch	50 μm	36 μm
	Total Connections		
	Number of chips in 3D stack	21 (estimate only)	> 21 (estimate only)
Chip on Substrate	Max Organic Substrate Sizes	(76 x 74) mm	(100 x 100) mm
	Substrate C4 Bump Pitch	55 μm	45 μm
	Chips Placed Per Substrate	7	12
	Chip Spacing	100 μm	100 μm
Packaging	Features	• High performance polymer and solder thermal interface materials integrated with Cu heat spreaders for improved thermal performance • Package substrates that are optimized for low loss high speed signaling	
		• Integration of high-performance passives (capacitors, inductors and resistors) to optimize power delivery networks and high speed signaling • Flip-chip packages at a minimum pitch of 100 μm	

Table 7 RF Centric Specifications

		IOC	Final State
		IOC	**FOC**
TSV's	Depth	100 μm	100 − 200μm
	Diameter	25 μm	10 μm
	Pitch	150 μm	50 μm
Dense Interconnect	Size (full reticle)	(26x33) mm	(26x33) mm
	Stitching	5.5"x5.5"	5.5"x5.5"
	Front end metal wiring density	0.5 μm line/space	0.5 μm line/space
	Front end metal layers	4 − 6 (copper)	4 − 6 (copper)
RF Performance	RF Output Power	A[1]	A + 5dBm
	RF Sensitivity	B	B + 5dB
	Increase Detection Range	C	C + 30%
SWaP	Array Size and Weight	D	D − 40%
	Prime Power	E	E − 30%
Assembly	Back side bump pitch	150 μm C4	50 μm C4
	Front end pitch	55 μm	10 μm
	Component thickness	800 − 300 μm	800 − 100 μm
	Chiplets supported	Down to 7nm	Down to 7nm
	Chiplets assemble	2 - 100	2 - 100
Packaging	Features	• High performance polymer and solder thermal interface materials integrated with Cu heat spreaders and/or heat pipes for improved thermal performance • Package substrates that are optimized for low RF loss, low latency data rates, high speed signaling • Integration of high-performance passives (capacitors, inductors and resistors) and	
		• matching networks to minimize prime power consumption and maximize high speed signaling • Flip-chip packages at a minimum pitch of 150 μm	

[1] Values A, B, C, D & E are classified. For the purpose of this proposal list best achievable.

SHIP Application Targets

Type	Attributes	Schematic
Radiation Hard – Safety Critical	• On-orbit Data Processing • Autonomous Vehicles	
Extremely High Performance	• Cognitive EW • AI - Radar Detection and Classification • Sensor fusion for tracking and targeting • Commercial applications - AI/ML, test & measurement, remote sensing, signal processing	
Ultra Low Power	• UAV, UUV • Remote Sensors • Robotics • IoT – cloud edge computing, AI enabled "Smart Operation"	

| RF | • RF performance frequency
• Efficiency – lower parasitic
• Increased power density
• Much smaller form factor | |

Table 1 Notional heterogeneous integration configurations that are of interest to the Government.

NAVY SHIP Phase 1 Awards:
~$25M Total for SHIP Foundry Planning

- SHIP-Digital Phase 1 Awarded to:
  - Intel Federal, LLC
  - Xilinx

- SHIP-RF Phase 1 Awarded to:
  - GE Research
  - Keysight Technologies
  - Northrop Grumman Aerospace Systems
  - Qorvo

https://nstxl.org/opportunity/state-of-the-art-heterogeneous-integrated-packaging-ship-prototype-project/

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  - Keysight Technologies
  - Northrop Grumman Aerospace Systems
  - **Qorvo**

Phase 2 Winners

https://nstxl.org/opportunity/state-of-the-art-heterogeneous-integrated-packaging-ship-prototype-project/

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DARPA PIPES - Photonics in the Package for Extreme Scalability

DARPA Applications Limited by Connectivity at All Length Scales

RF Phased Arrays — Radar & 5G
Improved Performance and System Scalability
Source: Comsol

sensors, edge, DoD

PIPES Ecosystem
Establish sustained DoD access to domestic design, fabrication, and packaging capabilities

Digital Sensors — Imaging
Scaling Pixel Array Size, Frame Rate, and Power
Source: DARPA.mil

Machine Learning & Simulation
Large-scale Modeling and Artificial Intelligence
Source: DARPA.mil

cloud, data center, HPC & AI

Computing & Data Analysis
Advanced Parallel Systems
Shutterstock

Facilitating DoD Access: Create an ecosystem for package-level optical signaling, enabling disruptive advances for artificial intelligence, phased arrays, sensors and processing.

Unique Nature of A & D Roadmap

Challenges of Aerospace and Defense Electronics Systems

The Aerospace / Defense market segment has unique challenges:

- High Performance – Access to leading nodes and advanced packaging technologies
- High Reliability – harsh environments, human safety
- Long Product Lifecycles – parts obsolescence & upgradability
- Low Volumes – high product mix, affordability
- Need domestic supply chain
- **How can heterogeneous integration help to achieve system performance objectives?**

Commercial vs. DoD Business Models

Commercial

Source: iFixit

- Product last ~2 years (until new one is out) – Revenue Based
- Systems are complex, but differing scale and complexity from DoD Systems
- Requires assured access to components for 2-3 years.

Military

- Product Lifecycles are Decades
- Systems are much more complex, and therefore risk managed
- Consequences are Different
- Requires Assured Access to components for Decades
- Capabilities that are not needed Commercially (RadHard)

Timelines and Complexities Are very different for DoD Modern Semiconductor Processes

NDIA: Trusted Microelectronics Joint Working Group: Future Needs & System Impact of Microelectronics Technologies, http://www.ndia.org/divisions/working-groups/tmejwg/final-team-reports

Aerospace and Defense Drivers

- **What are system drivers?**
  - **NRE costs and schedules**
  - **Qualification / Reliability for harsh environments**
  - **RF Convergence & Autonomy**
- **What are technical drivers?**
  - **Digitization over wide bandwidths and at high dynamic range to enable new capabilities**
  - **Common DSP HW/SW to reduce required equipment, reduce power consumption and improve sustainability / upgradability**
  - **Integration of RF/analog and digital functions is required**
- **What are the supply chain issues?**
  - **Access to the most advanced technology but on-shore in low volumes**
  - **Parts obsolescence, security, industry support**
  - **Possible solutions: standardized interfaces, IP-Reuse ecosystem**

What are Some Metrics to Consider?

- **Performance:** data rate, latency, throughput, TFLOPs, insertion loss, isolation, dynamic range, etc.
- **Energy/Power:** pJ/bit, throughput per Joule, TFLOPS/Joule, Leakage power, etc.
- **Interfaces:** signaling protocols, error correction, interconnect lengths, ESD, etc.
- **Thermal:** Maximum junction temperature, number and location of hot spots, power densities of hot spots
- **Electrical:** Power distribution losses to components inside package, losses in conversion, peak inductive noise, harmonic noise, etc.
- **Reliability/Availability:** MTBF, radiation hardness, metric related to graceful degradation on component failures, lifetime ranges, etc.
- **Others:** PLEASE SUGGEST!

HIR A&D Rev 0.1

Area	Metric	SOTA 2020	2025	2030	2035	comment
Performance	Frequency					
	Power					
	Thermal					
Design	Tools	Point solutions				
	Interfaces	CHIPS AIB (early traction)	Broad adoption + roadmap			
	IP reuse	Chiplets (broad interest)	Business model adoption			
Integration	RF + digital	Separate solutions (e.g., SHIP)	RF + FPGA/GPU/CPU in production			
	3D	HBM, 3D layered NAND	True HI in 3D			
	Photonics	R&D (e.g. DARPA PIPES)				
Reliability	HI standards	DoD discussions				
Supply Chain	Components	International ad hoc	"Zero trust" solutions			
	Assembly	US-only, lagging and/or proprietary tech	On-shore HVM-like interposers, FOWLP	Flow accommodates any volume, price, TAT		
	Security	Trusted facilities	"Zero trust" (data-based; need metrics)			
	Obsolescence	Lifetime buys				

Seeking more inputs to the proposed framework, metrics, and content in the table(s)

New Edition of HI Roadmap in 2021: A&D TWG Focus

- Track developments in industry and government

- Upgrade / populate roadmap table

- Increase linkages to other HIR chapters (photonics, design, thermal,…)

- Broaden scope internationally

- Address aerospace challenges that differ from defense

Name	Affiliation	Role
Tim Lee	Boeing	Co-chair
Jeff Demmin	Keysight Technologies	Co-chair
Tom Kazior	DARPA	Member
Dan Blass	Lockheed Martin	Member
Susan Trulli	Raytheon	Member
Kenji Miyake	Minimal Fab	Member

Summary

The TWG for Developing the Heterogeneous Integration Roadmap for Aerospace and Defense

- Goal: develop a **roadmap for heterogeneously integrated components for applications in Aerospace and Defense**

- **Specific goals:**

  - Identify the A-D specific challenges in the next 5, 10 and 15 year horizons

  - Identify promising solutions and technologies

  - Identify any unaddressed challenges and the types of solution / technologies needed

  - Document all of these as a chapter in the overall HIR document

    - Reports will be freely available on the IEEE EPS and SEMI websites

    - 2020 update to inaugural 2019 version complete; devising 2021 update plan

We invite you all to consider joining in the
Heterogeneous Integration Roadmap Development and
participate in contributing to the Aerospace and
Defense Technical Working Group.

Tim Lee, tt.lee@ieee.org
Jeffrey Demmin, jeffrey.demmin@keysight.com

Thank you

Additional Content

Silicon Manufacturing Largely Offshore

Foundries concentrated in Asia

Table: Ranking of the Global Top 10 Foundries by Revenue, 1Q20 (Unit: Million USD)

Ranking	Company	1Q20E	1Q19	YoY	M/S
1	TSMC	10,200	7,096	43.7%	54.1%
2	Samsung	2,996	2,586	15.9%	15.9%
3	GlobalFoundries	1,452	1,256	15.6%	7.7%
4	UMC	1,397	1,057	32.2%	7.4%
5	SMIC	848	669	26.8%	4.5%
6	TowerJazz	300	310	-3.3%	1.6%
7	VIS	258	224	14.9%	1.4%
8	PSMC	251	178	41.2%	1.3%
9	Hua Hong	200	221	-9.4%	1.1%
10	DB HiTek	158	139	13.8%	0.8%
Top 10 Total		18,060	13,737	31.5%	95.7%

Notes:
1. Samsung's revenue includes revenues from its System LSI unit and its foundry business
2. GlobalFoundries' revenue includes revenue generated by the chip manufacturing unit that it acquired from IBM
3. PSMC's revenue includes its foundry revenue only
4. Hua Hong's revenue includes figures from its publicly disclosed revenue only

Source: TrendForce compiled this table with data from the respective foundries, Mar. 2020

US companies have 25% of WW wafer capacity, but majority of it is offshore
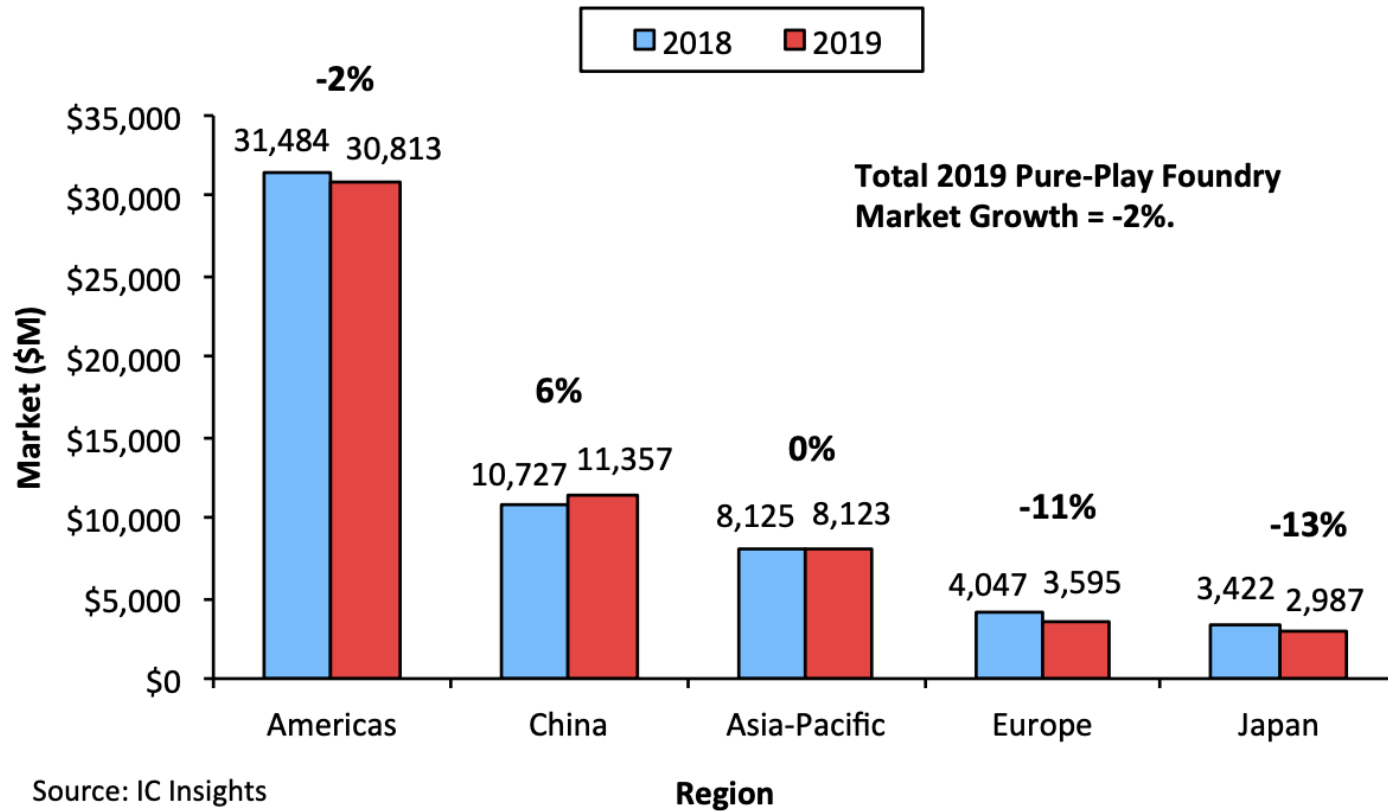

Comparing 300mm Wafer Capacity Based on Fab Location and HQ Location (6.2M* Wafers, Dec-2019)
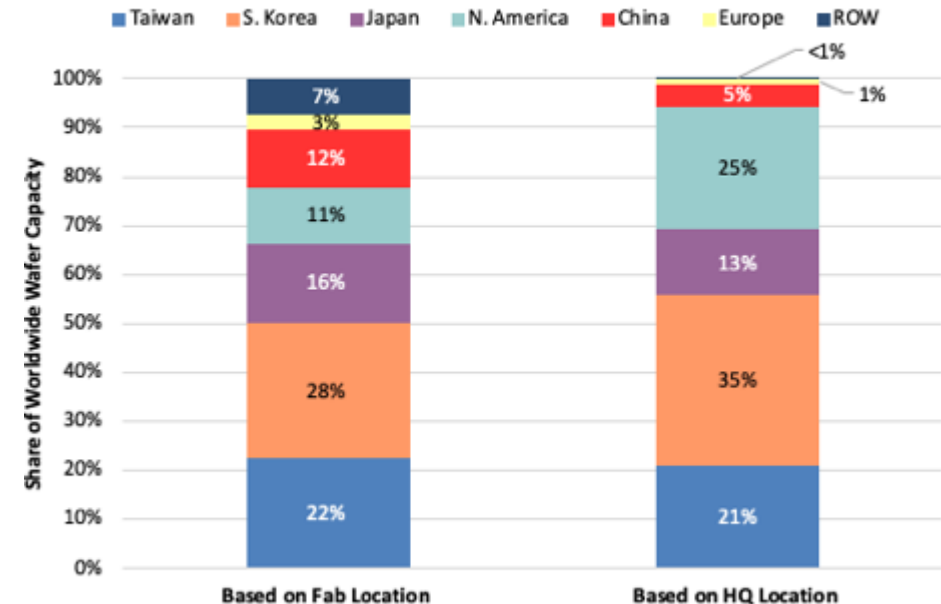
*Includes 300mm capacity for O-S-D devices from Sony, Infineon, Samsung, SK Hynix, and Alpha & Omega
Source: IC Insights

Nearly all foundry growth in 2019 driven by customers in China

Pure-Play Foundry Market by Region

Legend: ☐ 2018   ☐ 2019

Total 2019 Pure-Play Foundry Market Growth = -2%.

Y-axis: Market ($M) — $0, $5,000, $10,000, $15,000, $20,000, $25,000, $30,000, $35,000

Region	2018	2019	Growth
Americas	31,484	30,813	-2%
China	10,727	11,357	6%
Asia-Pacific	8,125	8,123	0%
Europe	4,047	3,595	-11%
Japan	3,422	2,987	-13%

X-axis: Region

Source: IC Insights