Integrated Cold Start of a Boost Converter at 57 mV Using Cross-Coupled Complementary Charge Pumps and Ultra-Low-Voltage Ring Oscillator

Soumya Bose, *Student Member, IEEE*, Tejasvi Anand, *Member, IEEE*, and Matthew L. Johnston, *Member, IEEE*

***Abstract*— This paper demonstrates an on-chip electrical cold-start technique to achieve low-voltage and fast start-up of a boost converter for autonomous thermal energy harvesting from human body heat. An improved charge transfer through high gate-boosted switches by means of cross-coupled complementary charge pumps enables voltage multiplication of the low input voltage during cold start. The start-up voltage multiplier operates with an on-chip clock generated by an ultra-low-voltage ring oscillator. The proposed cold-start scheme implemented in a general-purpose 0.18-μm CMOS process assists an inductive boost converter to start operation with a minimum input voltage of 57 mV in 135 ms while consuming only 90 nJ of energy from the harvesting source, without using additional sources of energy or additional off-chip components.**

***Index Terms*— Charge pump, dc–dc converter, integrated cold start, ring oscillator, thermoelectric energy harvesting.**

I. Introduction

THERMAL energy from human body heat is a ubiquitous source of energy, and unlike solar power, it can be harnessed irrespective of illumination conditions. As such, body heat is an ideal energy source for self-powered wearable devices [1]. Thermal energy can be converted to electrical energy using thermoelectric generators (TEG), the solid-state devices that generate a voltage from an applied temperature gradient (ΔT) using the Seebeck effect [2]. A wearable form factor requires small-area TEGs, which generate only tens of millivolts from the small ΔT value (∼1 °C–2 °C) between the skin and the ambient environment. A dc–dc step-up converter is needed to boost this small voltage to power electronics. While the low-voltage dc–dc converters have been demonstrated, initial start-up of the power converter at low input voltage is challenging without using additional energy sources, such as batteries [3], mechanical vibrations [4], or RF sources [5].

Over the past decade, research efforts focused on the low-voltage electrical cold start of thermoelectric energy harvesters have demonstrated fully battery-less operation. Transformers are used in [6] and [7] to kick-start the boost converter at 21 and 40 mV, respectively. Inductor-based LC oscillators [8] or Colpitts oscillators [9] have also demonstrated start-up from 50- and 40-mV input voltages. All these approaches accomplished low-voltage cold-start but required additional off-chip magnetic components that limit device miniaturization.

Fully integrated electrical cold start at low input voltage is challenging due to the high threshold voltage of transistors in sub-micrometer CMOS processes. The integrated self-start in [10] requires an input voltage of at least 330 mV to start the converter, and a capacitor pass-on scheme together with post-fabrication threshold-trimming of on-chip oscillator transistors in [11] achieves 95-mV cold start. Alternatively, Schmitt trigger oscillators are used in [12] to achieve integrated cold start at 70 mV, but reliance on a conventional charge pump and a large storage capacitor (1 nF) results in a slow start-up (1.5 s) and prevents further reduction of the cold-start voltage. An integrated oscillator reported in [13] successfully generates start-up clock at an input voltage of 45 mV, although converter cold start is limited to 210 mV.

In each of these implementations, a voltage multiplier boosts the low input voltage with the assistance of a start-up clock to power control the circuits of an inductive converter during start-up. Although primarily limited by the minimum supply needed for the clock, cold-start voltage is also highly dependent on the boosting ability and output power of the start-up voltage multiplier.

In this paper, we demonstrate an alternative integrated start-up mechanism, in which a one-shot pulse triggers the inductive converter to start operation. A start-up voltage multiplier is proposed that enables an efficient voltage multiplication of the small input voltage by means of a high-gate-boosting scheme, implemented using cross-coupled complementary charge pumps. The multiplier operates with a start-up clock generated by an on-chip ring oscillator using a unique stacked-inverter delay element for ultra-low-voltage operation. The proposed start-up mechanism is implemented in a 0.18-μm CMOS process and achieves the cold start of an inductive boost converter at an input voltage as low as 57 mV, which is the lowest cold-start voltage reported to date using a fully integrated electrical circuit [14]. This paper describes the detailed circuit architectures of the key

Manuscript received March 28, 2019; revised June 12, 2019; accepted July 10, 2019. This paper was approved by Associate Editor Pui-In Mak. This work was supported in part by the National Institutes of Health under Award R21DE027170. *(Corresponding author: Matthew Johnston.)*

The authors are with the School of Electrical Engineering and Computer Science, Oregon State University, Corvallis, OR 97331 USA (e-mail: matthew.johnston@oregonstate.edu).

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/JSSC.2019.2930911

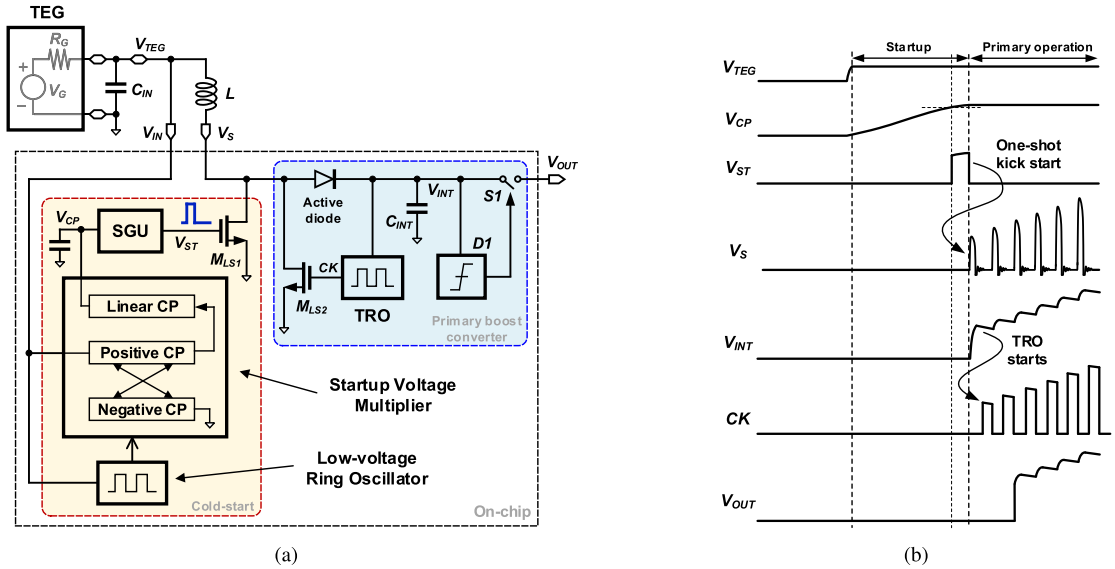


Fig. 1. (a) Proposed integrated cold-start architecture. (b) Timing diagram of the cold-start sequence utilizing a fast-falling edge of a strobe pulse for quick triggering of the primary inductive boost converter.

building blocks of the proposed start-up regime, including ultra-low-voltage clock generation, start-up voltage multiplier, and strobe generation, as well as low-voltage design challenges and extended block-level electrical characterization of the IC.

The rest of this paper is organized as follows. Section II describes the cold-start architecture. Section III elaborates the design of the ultra-low-voltage ring oscillator. Section IV explains the circuit details and operation of the proposed start-up voltage multiplier, and the generation of the strobe pulse is described in Section V. Section VI presents the measured results from the fabricated IC, and Section VII provides a brief conclusion.

II. Proposed One-Shot Cold-Start Operation

Limited on-chip capacitance constrained by silicon area and low input voltage reduce charge transfer ($Q = \mathrm{CV}$) through a charge-pump-based voltage multiplier. This is exacerbated by the low start-up clock frequency at low supply voltage, which results in low output current. As such, charging a large storage capacitor with the diminished output power of a charge pump is not prudent for low-voltage cold start. However, while a TEG provides low output voltage, it can provide a moderate amount of current due to its low source impedance (typically a few ohms); charging an inductor with this current can generate higher energy per cycle. To exploit this, rather than relying solely on a start-up charge pump, power transfer is quickly handed over to the inductive converter to achieve a low-voltage and fast cold-start operation.

The proposed cold-start architecture is shown in Fig. 1(a). A start-up voltage multiplier initially boosts the input voltage to power a strobe generation unit (SGU). The voltage boosting ability of the multiplier is improved by using the cross-coupled complementary charge pumps to enhance the gate drive of the charge transfer switches (CTSs). A low-voltage, on-chip ring oscillator generates the start-up clock for the operation of the charge pumps. A strobe signal V_{ST} from the SGU turns on an auxiliary low-side (LS) switch M_{LS1} and charges the inductor with current from the TEG. As shown in Fig. 1(b), a sharp falling edge of the one-shot pulse V_{ST} forces the voltage V_S to rise and forward-bias an active diode. The inductor current immediately charges a small on-chip storage capacitor C_{INT} (350 pF) to a voltage $V_{\mathrm{INT}} > 400$ mV in the strobe-cycle itself.

A thyristor-based ring oscillator (TRO) designed to start oscillation with low supply (400 mV) is powered immediately by V_{INT} and takes over control to operate the inductive converter. A wider LS switch M_{LS2} is now used to charge the inductor with a higher current per cycle. V_{INT} is not connected to the output until it crosses a voltage threshold detected by the voltage detector D1. This ensures that all inductor energy is used to start the TRO during start-up. M_{LS1} is disabled during primary operation as V_{ST} goes low.

The proposed start-up scheme reduces the power burden on the voltage multiplier and achieves low-voltage start-up. In addition, the one-shot kick-start mechanism quickly hands over the power transfer process to a more efficient current-mode inductive boost converter and, thereby, speeds up the start-up process.

III. Ultra-Low-Voltage Ring Oscillator

An oscillator is required for the operation of the start-up voltage multiplier. Ring oscillators comprising a series of delay stages in a closed loop are easy to integrate and have been used to generate start-up clocks [10]–[12]. To create sustained oscillation, required gain (A) of each delay stage and total number of stages (n) can be derived from the Barkhausen criteria for oscillation as follows:

$$A \geq \sqrt{1 + \left(\frac{\omega_o}{\omega_p}\right)^2} \quad \text{and} \quad n = \pi / \tan^{-1}\left(\frac{\omega_0}{\omega_p}\right) \tag{1}$$

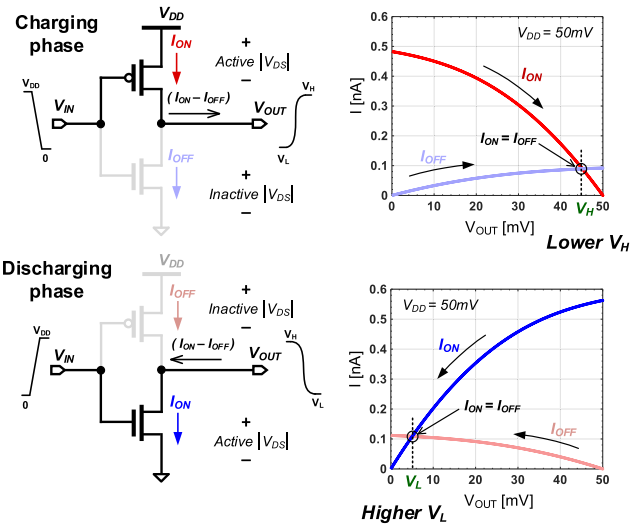


Fig. 2. Low output voltage rail of a CMOS inverter at low supply.

where ω_0 is the frequency of oscillation and ω_p is the pole frequency contributed by each stage. As such, a smaller gain (A) requires a higher number of delay stages (n) for oscillation and results in a low output frequency (ω_o) of the ring oscillator.

A. Limitations of CMOS Inverter as Delay Element

At very low supply voltage, CMOS inverters suffer from low dc gain due to the significant deterioration of transconductance of the transistors. From Meindl's limit [15], minimum supply required for an inverter in a 0.18-μm bulk CMOS process to achieve dc gain greater than unity is 48 mV at 300 °K [16]. Hence, this sets the theoretical limiting supply voltage for the operation of a CMOS inverter-based ring oscillator.

Low supply voltage also degrades the output voltage rails of an inverter. As shown in Fig. 2, during an output transition, the difference current ($I_{\rm ON} - I_{\rm OFF}$) between the active and inactive transistors charges or discharges the output. As $V_{\rm OUT}$ changes, $|V_{DS}|$ of the active transistor decreases and $I_{\rm ON}$ falls, whereas $|V_{\rm DS}|$ of the inactive transistor increases. Finally, $V_{\rm OUT}$ settles to V_H or V_L when $I_{\rm ON} = I_{\rm OFF}$. For a transistor in sub-threshold operation with device width W and length L, drain current I_D is given by

$$I_D = I_0.\frac{W}{L}.e^{\left(\frac{|V_{\rm GS}|-|V_{\rm th}|}{\eta V_T}\right)}.\left(1-e^{-\frac{|V_{\rm DS}|}{V_T}}\right) \qquad (2)$$

where I_0 ($= \mu_0.C_{\rm ox}.(\eta-1).V_T^2$) is constant, η is the sub-threshold swing factor, $V_{\rm th}$ is the threshold voltage, and V_T is the thermal voltage [17]. At very low supply, when $|V_{\rm GS}| << |V_{\rm th}|$ and $V_{\rm DS} \sim V_T$, I_D strongly depends on $|V_{\rm DS}|$. Thus, an increase in $|V_{\rm DS}|$ of the inactive transistor during $V_{\rm OUT}$ transition results in a significant increase of $I_{\rm OFF}$. Thereby, the difference current vanishes well before $V_{\rm OUT}$ reaches the supply rail ($V_{\rm DD}$ or GND) and reduces the output voltage rail ($V_H - V_L$) of the inverter (see Fig. 2); simulated output rail is 20% lower than supply rail (50 mV) in 0.18-μm CMOS. As a consequence, the output clock of a CMOS inverter-based ring oscillator exhibits degraded voltage swing at low supply.

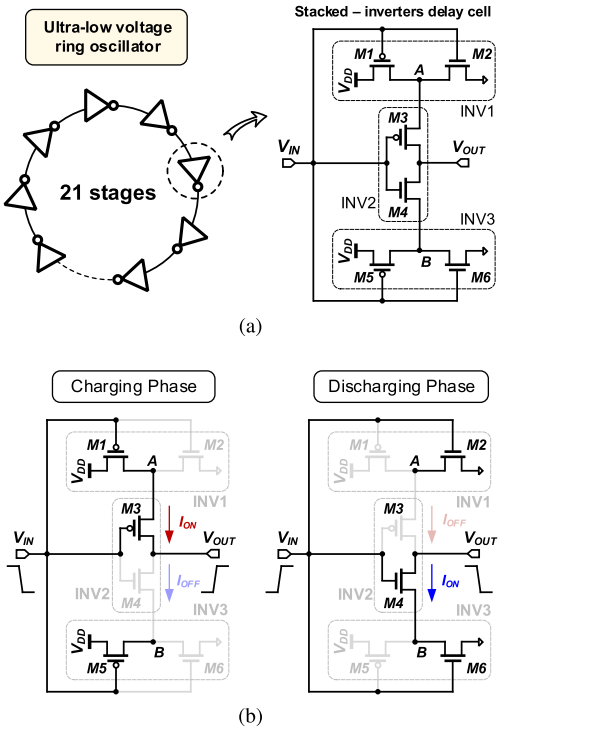


Fig. 3. (a) Ultra low-voltage ring oscillator comprising the proposed stacked-inverters-based delay cells. (b) Leakage current suppression in the delay cell in charging and discharging phases.

B. Proposed Delay Element

Dynamic reduction of the leakage current $I_{\rm OFF}$ can improve output voltage swing at low supply. To achieve this, a delay element is proposed [18] comprising of three inverters, arranged as shown in Fig. 3(a). The outputs of INV1 and INV3 are connected to the sources of PMOS and NMOS transistors of INV2, respectively.

During the charging phase, a high-to-low transition of $V_{\rm IN}$ causes INV3 to pull node B to $V_{\rm DD}$, as shown in Fig. 3(b). This reduces $V_{\rm DS}$ and $V_{\rm GS}$ across the NMOS transistor M4 of INV2 and suppresses the leakage current $I_{\rm OFF}$. During the discharging phase, as $V_{\rm IN}$ transitions from low to high, INV1 pulls node A down to GND and suppresses $I_{\rm OFF}$ through the PMOS transistor M3 of INV2 by reducing both $V_{\rm SD}$ and $V_{\rm SG}$ across it. However, $|V_{\rm DS}|$ drop across M1 or M6 in the path of $I_{\rm ON}$ will reduce effective $|V_{\rm GS}|$ across the active transistors, M3 and M4, respectively, in the corresponding phases. This would reduce effective $I_{\rm ON}$ and nullify the effect of lowering $I_{\rm OFF}$. To alleviate, M1 and M6 are sized three times the width of M3 and M4, respectively, while M2 and M5 are of the same dimensions as M4 and M3.

Compared with other leakage suppression techniques, such as Schmitt trigger logic [19], the proposed stacked-inverter delay cell provides more effective leakage current bypassing at low supply by applying maximum $|V_{\rm GS}|$ to M5 and M2 in the respective phases. It also yields faster pull-up and pull-down actions of M5 and M2; with the transition of $V_{\rm IN}$, $I_{\rm OFF}$ is blocked at the onset of the $V_{\rm OUT}$ transition. A similar leakage

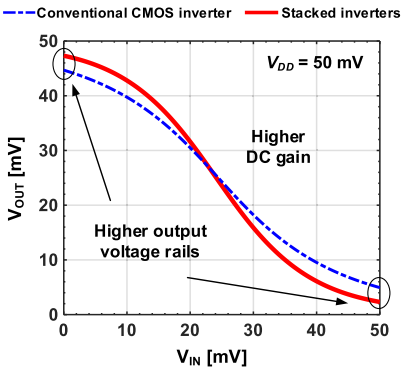


Fig. 4. Simulated VTC of the proposed delay cell shows improvement of dc gain and output voltage rails over the conventional CMOS inverter.

bypassing technique adopted for designing a low-voltage ring oscillator in recent work [13] also demonstrates the effectiveness of the technique. It is important to note that, although the leakage current I_{OFF} is suppressed from the output in both the phases, additional leakage currents through the bypass transistors, M2 and M5, increases total current consumption of the delay block compared with a simple CMOS inverter. However, the increase in power consumption is negligible compared with other blocks when used in a complete energy harvester architecture.

Low-V_{th} transistors are used to increase conduction at the low supply voltage. The simulated voltage transfer characteristic (VTC) of the stacked-inverter delay block in a 0.18-μm CMOS process is shown in Fig. 4, which demonstrates a 13.3% improvement in output voltage rails and 32.5% higher dc gain compared with those of a CMOS inverter (INV2 alone) at a supply of 50 mV. The enhanced gain is due to the higher output impedance R_o at the final output of the delay element, which can be expressed as

$$R_o = [r_{o3} + (1 + g_{m3}r_{o3})R_{o1}]||[r_{o4} + (1 + g_{m4}r_{o4})R_{o3}] \quad (3)$$

where R_{o1} and R_{o3} are the output impedances of INV1 and INV3, respectively, at the dc operating point. While the cascading effects of M3 and M4 are small due to the small intrinsic gains, $g_{m3}r_{o3}$ and $g_{m4}r_{o4}$, at the low supply voltage, R_o of the stacked-inverter delay cell is still higher than the output impedance ($r_{o3}||r_{o4}$) of INV2 alone. g_m of M1–M6 together contributes to the delay cell transconductance.

A ring oscillator was implemented using 21 stages of the stacked inverter delay element to generate the start-up clock. At a supply of 50 mV, the simulated frequency of the clock is 9.4 kHz at the typical corner; the frequency ranges between 2 and 38 kHz across process corners.

IV. Start-Up Voltage Multiplier

A voltage multiplier is required during start-up to boost the input voltage and power the cold-start control circuits. Low swing and low frequency of the pumping clock make designing such a multiplier, especially challenging at low voltage.

A. Limitation of Conventional Charge Pumps

On-chip voltage multipliers, such as the Dickson charge pump [20], can boost input voltage but incur a voltage drop across each stage diode. A cascaded dual-phase charge pump [21] mitigates this problem by providing a gate drive (V_{GS}) equal to the voltage swing of the clock (V_{CK}) to turn on the CTSs. This works efficiently at nominal input voltage, but at low supply, V_{CK} ($< V_{\mathrm{DD}}$) turns on the CTS only weakly. The resulting forward current in the ON phase is not much larger than the reverse leakage current in the OFF phase, thus causing inefficient charge transfer. Dynamic biasing of CTS [22] where boosted voltages are borrowed from higher stages of the charge pump to generate V_{GS} of $2 \cdot V_{\mathrm{CK}}$ for the CTS can further improve charge transfer. However, at tens of millivolts of V_{DD}, the boosted V_{GS} value still does not sufficiently improve the on-conductance of the CTS. For instance, with $V_{\mathrm{DD}} = 50$ mV, more than $6 \cdot V_{\mathrm{CK}}$ is needed to cross the threshold voltage of even low-V_{th} devices available in a 0.18-μm CMOS technology. In addition, overlapped phases of the pumping clock and the CTS gate clock in [22] result in reverse charge sharing, reducing pumping efficiency. Dynamic body biasing [23], [24] can also improve CTS on-conductance but is only effective for input voltages above 100 mV.

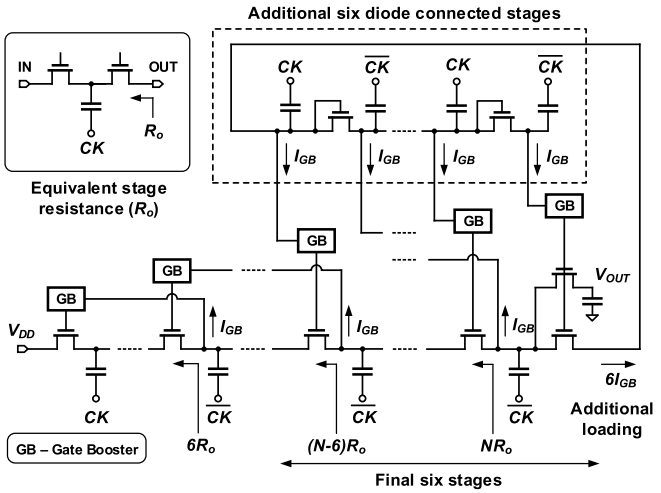


Fig. 5. Loading effect in high gate boosting by borrowing voltages from much later stages.

For ultra-low-voltage operation, high V_{GS} needed for each CTS can be generated by borrowing voltages from much later stages of the charge pump, as shown in Fig. 5. The gate boosters (GBs) represent circuit blocks such as dynamically biased inverters used to generate the gate clocks [22]. Additional diode-connected stages are needed to generate gate clocks for the final stages, which suffer from inefficient voltage boosting and will reduce CTS gate drive in the final stages. Also, the loading of these stages (six shown here) will result in a voltage drop of $6NI_{\mathrm{GB}}R_o$ at the output V_{OUT}, where N is the number of primary stages, I_{GB} is equivalent current consumption of each GB, and R_o is the equivalent resistance per stage. For 20-stage voltage multiplication, the voltage drop will be $120I_{\mathrm{GB}}R_o$. As such, the conventional gate-boosting techniques are insufficient at very low input voltage.

B. Proposed Cross-Coupled Complementary Gate Boosting

In this paper, a high-gate-boosting technique is demonstrated using cross-coupled complementary charge pumps for

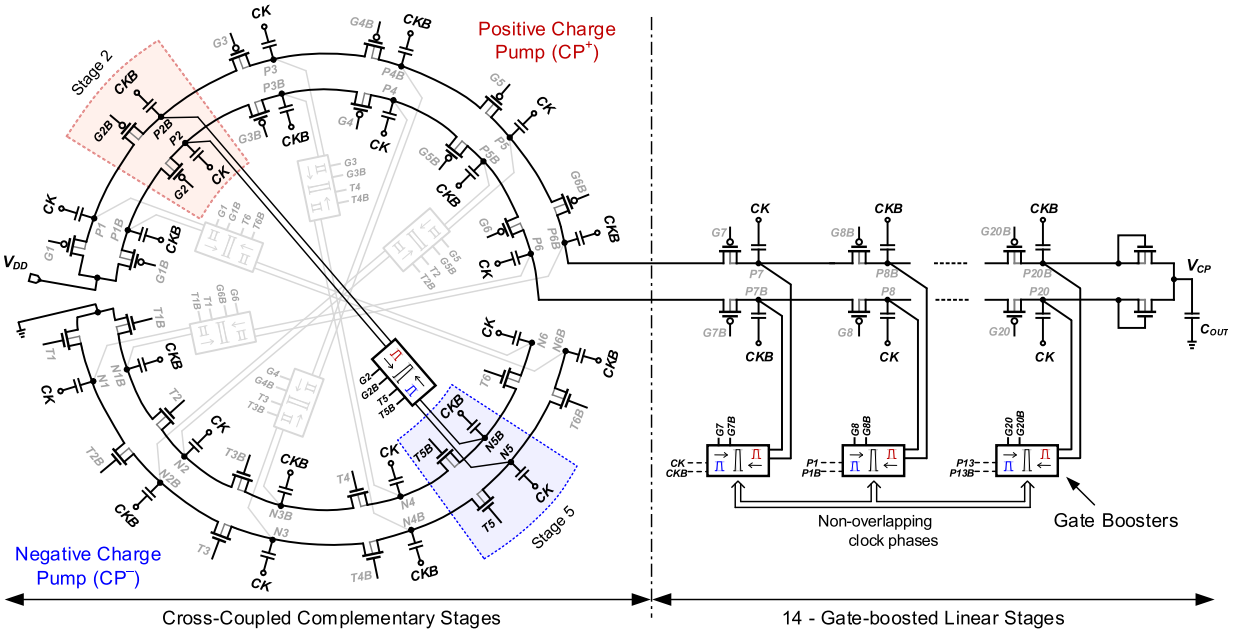


Fig. 6. Proposed start-up voltage multiplier using cross-coupled complementary charge pumps for high gate-boosting and low-voltage operation.

ultra-low-voltage operation. As shown in Fig. 6, the first section of the proposed start-up charge pump comprises of a six-stage positive charge pump (CP^+) and a six-stage negative charge pump (CP^-), each operating in dual phases. The supply voltage V_{DD} is applied to the CP^+ input, and the input of the CP^- is connected to GND. PMOS switches are used as CTSs in CP^+, whereas the isolated deep-n-well NMOS switches are used as CTSs in CP^-. The complementary charge pumps mutually boost the gate drive of their CTSs, as described in the following.

Dual-phase voltages from later stages of CP^- are borrowed to generate CTS gate clocks for earlier stages of CP^+. As shown in Fig. 7, negative dual-phase voltages $N5$ and $N5B$ from the fifth stage of CP^- and positive dual-phase voltages $P2$ and $P2B$ from the second stage of CP^+ are used to generate gate clocks $G2$ and $G2B$ that swing between a higher voltage level of $P2 - P2B$ and a lower voltage level of $N5 - N5B$ for the PMOS switches of the second stage of CP^+ using a GB circuit. The high negative-voltage swing of the gate clock will boost the gate drive, V_{SG} of the PMOS switch to $V_{DD} + 6V_{CK}$ in the charge transfer phase while ensuring $V_{SG} = 0$ in the non-conduction phase. However, as CP^- also exhibits poor CTS conductance at low voltage, negative voltage rail of the gate clocks will be affected, thereby lowering the effective V_{SG} value of the CTSs in CP^+. A fully complementary structure of the charge pumps addresses this problem, where the dual-phase voltage outputs of the complementary charge pump CP^+ are utilized to improve the CTS conductance of CP^-. With the drain and source of the NMOS switch of CP^- connected to the boosted negative voltages, the positive voltage of gate clocks $T5$ and $T5B$ utilizing a higher voltage level $P2 - P2B$ from CP^+ will increase the gate drive V_{GS} of NMOS switches of the fifth stage of CP^- to $V_{DD} + 6V_{CK}$ during the charge transfer phase,

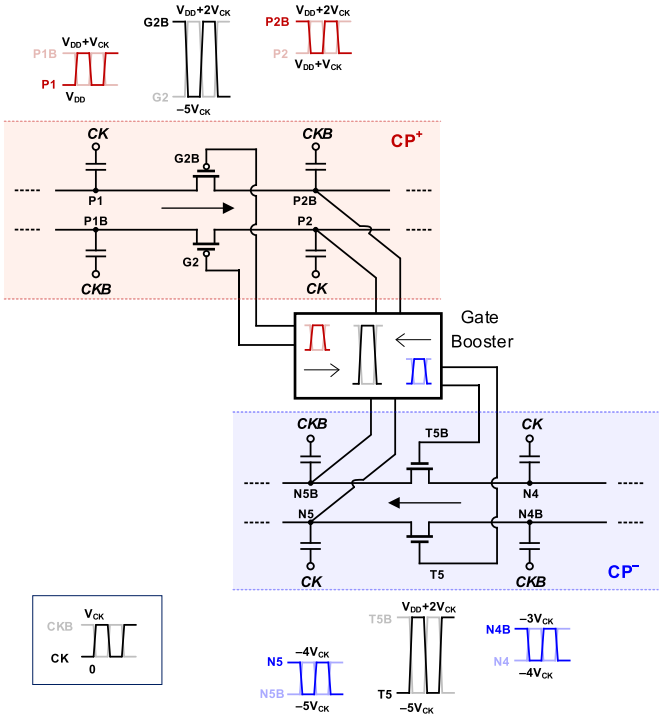


Fig. 7. Mutual voltage boosting of gate clocks borrowing dual-phased outputs of complementary charge pumps.

enhancing conduction. In a similar fashion, complementary outputs of the first CP^+ stage and sixth CP^- stage, third CP^+ stage and fourth CP^- stage, and so on generate CTS gate clocks of respective stages with the help of GBs, as shown in Fig. 6. This complementary gate boosting action improves the pumping efficiency of both charge pumps.

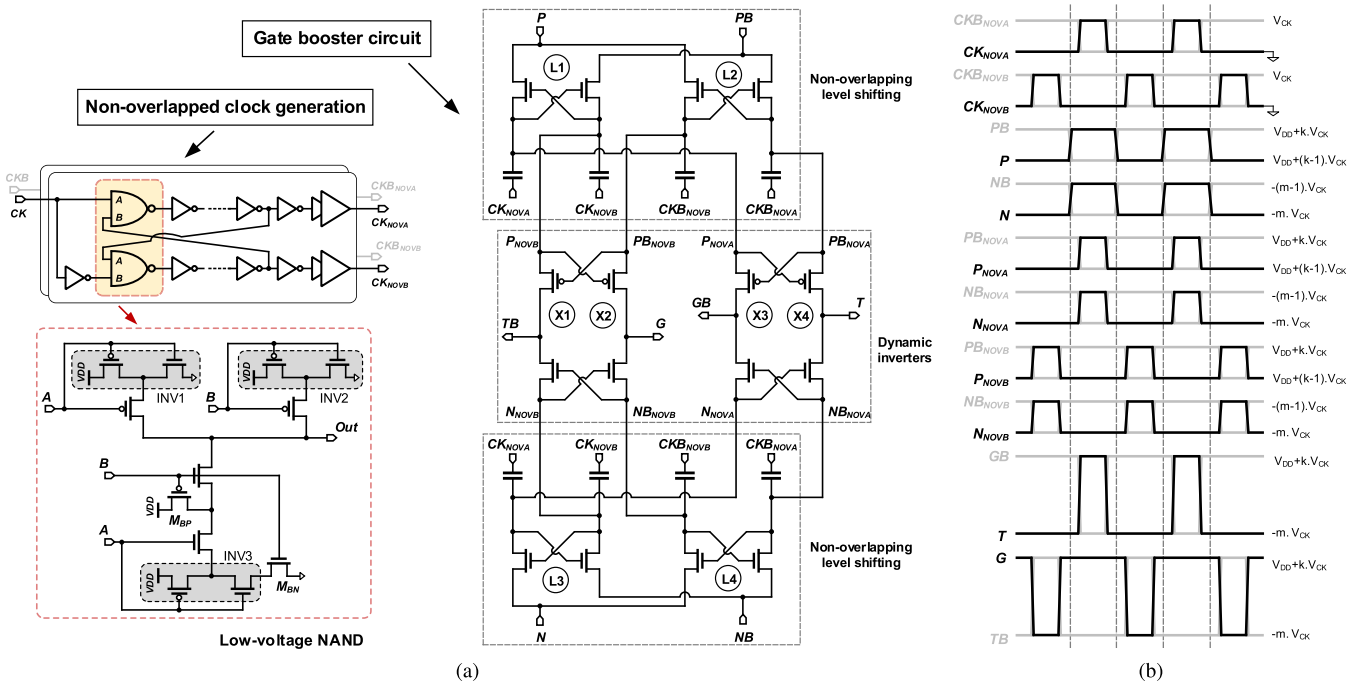


Fig. 8. (a) Generation of non-overlapping gate clocks with boosted voltage swing. (b) Timing diagram for gate clock generation.

As shown in Fig. 6, the final 14 stages of the start-up charge pump further boost the output of CP^+ using PMOS switches whose gate clocks are generated borrowing lower voltages from earlier stages. The final stage of the charge pump uses the diode-connected deep-n-well NMOS devices to prevent reverse charge flow during output voltage droop due to load transients. It is important to note that, although the gate boosting of the negative charge pump causes additional loading, the voltage drop in the load path from this effect is small ($I_{GB}.[1+2+\cdots+6]R_o = 21I_{GB}R_o$), as voltages are borrowed from the initial six stages. Compared with a conventional gate-boosting technique, which borrows voltage from later stages, the proposed technique borrows voltages from earlier stages to boost the gate clock of CTSs of CP^+. As such, no stage needs to wait for an increase in voltage at later stages for enhanced charge transfer, which makes the gate boosting action faster. Nonetheless, during initial cold-start state, the charge pump boosts the voltage using the leakage current of the CTS with the available low-voltage swing ($\sim V_{DD}$) of the intrinsic gate clocks; however, the regenerative action of the cross-coupled CP^+–CP^- assists the voltage multiplier to emerge quickly from this slow initial state.

Low-V_{th} devices are used for CTSs to improve charge transfer. While these exhibit higher leakage current compared with regular-V_{th} devices, enhanced conductivity with boosted gate drive makes reverse leakage negligible. The deep-n-well of the isolated NMOS devices in CP^- is shorted to GND, whereas the local body is shorted to the source and connected to the nearest minimum voltage terminal. This allows the NMOS switches to handle negative voltages without forward biasing the deep-n-well junction and without V_{th} degradation due to body bias. High-density MOS capacitors, each 20 pF, are used as pumping capacitors, optimizing switching resistance $1/(Cf_{CK})$ while ensuring slow switching limit operation by keeping charging time constant ($CR_{ON} \ll 1/f_{CK}$) [25]. A 120-pF decoupling capacitor C_{OUT} is added to the final output V_{CP} using MOS capacitors.

C. Non-Overlapping Boosting of Gate Clocks

Gate clocks of the CTSs are generated using the GB circuit shown in Fig. 8(a). The boosted gate clocks must be non-overlapping with the pumping clocks to avoid reverse charge flow in the non-charge-transfer phase. The level shifters L1 and L2 and L3 and L4 take dual-phase outputs of the charge pump ($P-PB$ and $N-NB$) and generate corresponding non-overlapped phases using clocks CK_{NOVA}, CK_{NOVB}, CKB_{NOVA}, and CKB_{NOVB}, as shown in the timing diagram in Fig. 8(b). These clock phases are generated using low-voltage NAND logic, implemented with a similar leakage suppression technique as discussed in Section II. As shown in Fig. 8(a), INV1 and INV2 suppress leakage currents of the pull-up transistors; INV3, M_{BN}, and M_{BP} suppress leakage currents of the pull-down transistors. MOS capacitors, each 2 pF, are used in the non-overlapping level-shifters.

Outputs of the level-shifters P_{NOVB}, PB_{NOVB}, N_{NOVB}, and NB_{NOVB} are fed to the dynamic inverter X1 to generate gate clock TB that swings between the higher positive voltage levels of $P-PB$ and the lower negative voltage levels of $N-NB$, as shown in Fig. 8(b). Similarly, gate clocks G, GB, and T are generated using X2–X4. For the final 14 stages of the voltage multiplier, the same GB circuit is used, where $N-NB$ are replaced by the positive voltage outputs of lower stages.

Poor gate drive of transistors in X1–X4 causes slow transition of the boosted gate clocks; to ensure non-overlap of the

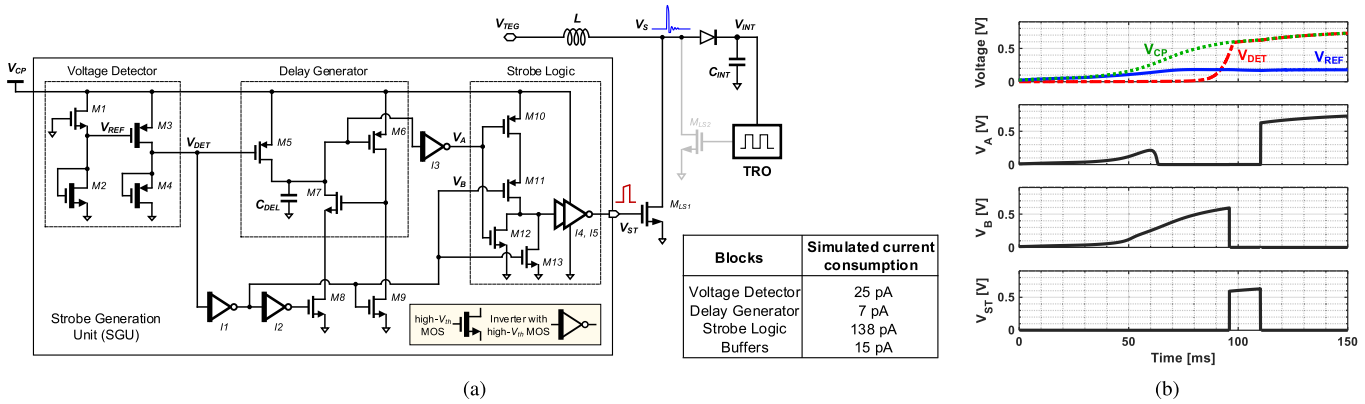


Fig. 9. (a) Circuit schematics of the SGU with simulated current consumption of each functional block. (b) Simulated waveforms showing functionality of the SGU.

final gate clocks with the pumping clocks, the delay between the falling edges of CK_{NOVA} and CK is designed to be larger than the delay between their rising edges. Timing of other phases is set accordingly. The clocks are driven by higher strength stacked-inverter cells to drive long routing paths. Routing is laid out symmetrically to ensure correct phases and minimal skew at the final destinations.

V. Strobe Generation and One-Shot Start-Up

An SGU is powered by the output of the start-up voltage multiplier V_{CP} to generate the control pulse V_{ST} required to kick-start the inductive boost converter. The SGU consists of a voltage detector, a delay generator, and a strobe logic circuit. As the output power of the charge pump is low, the SGU must operate with a very small quiescent current.

The voltage detector output V_{DET} asserts V_{ST} once V_{CP} crosses a threshold sufficiently higher than the V_{th} value of M_{LS1} to energize the inductor with required start-up current. A low-power reference generator is implemented using low-V_{th} and high-V_{th} transistors, M1 and M2, respectively [26]. Static current is minimized by using long-channel (10 μm) devices for M1 and M2; settling of V_{REF} is still fast compared with the slow rise of V_{CP}, as shown in Fig. 9(b). The detector comprises high-V_{th} PMOS transistors M3 and M4. Current through M3 is compared against leakage current through M4 (gate-source shorted); with the rise of V_{CP}, V_{SG} of M3 increases, and as current through M3 goes above the leakage current of M4, the output V_{DET} starts rising and follows V_{CP}. The width of M4 is set ten times the width of M3 for higher effective threshold, $V_{REF} + V_{SG,M3}$. M_{LS1} is sized to energize the inductor with required start-up current without substantially slowing the falling-edge transition of V_{ST} due to larger gate capacitance.

V_{DET} is delayed to generate V_A using a thyristor-based latch formed by the transistors M6 and M7 [27]. The capacitor C_{DEL} is precharged to V_{CP} by M5 before V_{DET} rises. Once M5 turns off, the latch is enabled by turning M8 on and M9 off using V_{DET}. As C_{DEL} is discharged by the leakage current while V_{CP} rises, V_{SG} of M6 increases, which charges the gate of M7; the M6 and M7 regenerative feedback quickly discharges C_{DEL}. The thyristor latch avoids crowbar current during voltage transitions and minimizes power consumption.

V_{ST} is finally generated from V_A and V_B using NOR logic (M10–M13) and buffered to the gate of M_{LS1}. All internal buffers ($I1$–$I3$) are designed with high-V_{th} transistors to reduce leakage current. Simulated current consumption of the sub-blocks of the SGU is shown in Fig. 9(a).

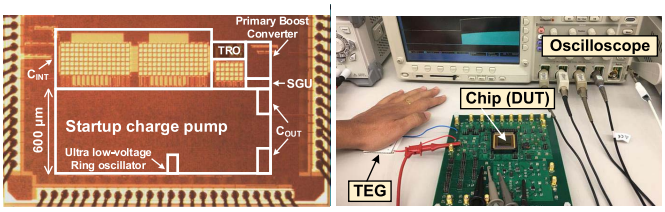
An active diode with low static current consumption [28] is used to reduce voltage drop in the current path from the inductor to the capacitor C_{INT}. An energy-efficient TRO [29] is designed to oscillate at a supply voltage as low as 400 mV. This enables the clock CK immediately following the strobe cycle, and it takes over control of the inductive boost converter. As the TRO takes the control, the inductor is energized using a wider LS switch M_{LS2}. Following a cold start, the inductive boost converter is operated in a discontinuous conduction mode (DCM), favorable for the low-power level of the application.

In order to kick-start the inductive boost converter successfully with the one-shot strobe pulse, the energy stored in the inductor during the strobe cycle must be sufficient to power the TRO, which can be expressed as follows:

$$\frac{1}{2}\cdot L\left(\frac{V_{TEG}}{R_{LS1}}\right)^2 > \frac{1}{2}\cdot C_{INT}V_{INT}^2 + \frac{V_{INT}I_{TRO}}{f_s} \tag{4}$$

where R_{LS1} is the ON-resistance of M_{LS1} during the strobe cycle, f_s is the frequency of CK, and I_{TRO} is the current drawn by the TRO. Conduction loss and leakage current through the active diode are negligible and are not included in the above-mentioned condition for simplicity. R_{LS1} is dependent on the voltage drive (V_{ST}) and the size of M_{LS1} during the strobe period, whose upper limits are bounded by the available output power of the start-up voltage multiplier at the cold-start voltage.

The inductor value L gives another degree of freedom to meet this condition, as expressed in (4). While higher f_s seems favorable to reduce the start-up energy requirement in (4), this increases I_{TRO} and the minimum value of V_{INT} to start the TRO. Based on the available output power of the voltage multiplier and on setting gate drive and size of M_{LS1} accordingly, it is calculated that an inductance value of



(a) (b)

Fig. 10. (a) Die photograph of the chip fabricated in a 0.18-μm CMOS technology. (b) Experimental set up for measurements with commercial TEG attached to the human body.

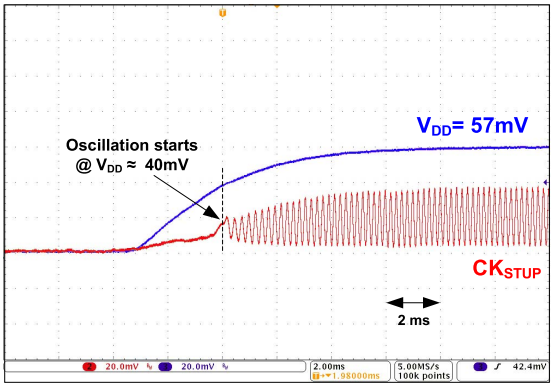


Fig. 11. Measured start-up clock generated by the ultra-low-voltage ring oscillator.

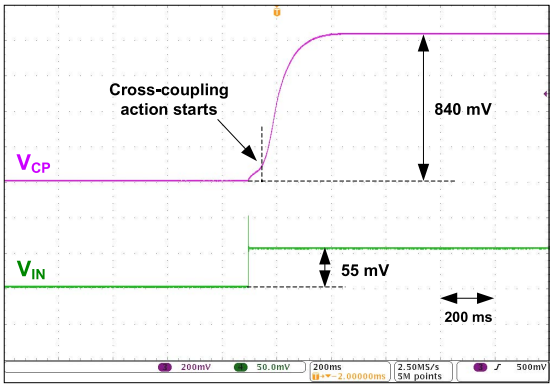


Fig. 12. Measured transient waveform of V_{CP} (buffered off-chip) with an input supply of 55 mV.

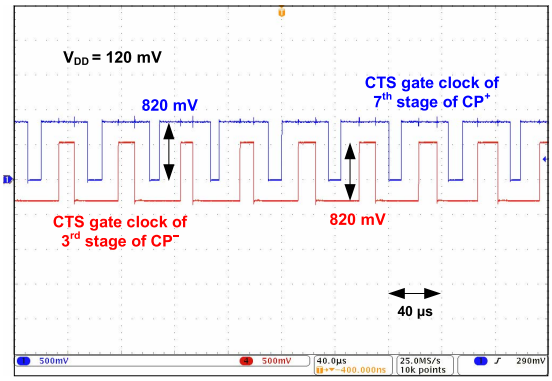


Fig. 13. Measured non-overlapping gate clocks with boosted voltage swing.

higher than 100 μH is enough to meet the condition expressed in (4).

A frequency of 25 kHz is chosen for CK to optimize the conduction and switching losses of the converter, along with meeting the requirement of starting up the TRO with a small supply of 400 mV. Although CK has a duty cycle of 66.67%, it still ensures the DCM operation of the boost converter due to the high conversion ratio ($t_{OFF} >> t_{ON}$). This creates a t_{ON} value of 26.8 μs, and the peak inductor current is kept much below the saturation current limit of the inductor for the whole input voltage range.

VI. Measurements

The proposed cold-start architecture was fabricated in a 0.18-μm CMOS process. Fig. 10(a) shows the die photograph of the implemented chip, where the cold-start block occupies 0.6 mm $\times$ 1.6 mm silicon area.

The start-up clock CK_{STUP} generated from the ultra-low-voltage ring oscillator is buffered to an output pin for measurements; buffers are powered using a separate test-only supply rail. Output transient of the start-up clock in Fig. 11 shows that oscillation starts at an input supply voltage as low as 40 mV, which demonstrates effective leakage suppression using the proposed stacked-inverter delay cells. The measured voltage swing of the clock is lower than the internal clock swing due to the loading of the low-voltage test buffers by the pad and probe parasitics.

A test output of the start-up voltage multiplier is buffered using an off-chip buffer to minimize probe loading during characterization. Measured output transient in Fig. 12 shows that an input voltage of 55 mV is boosted by the multiplier to an output of 840 mV, with an estimated load current of hundreds of picoamps due to the finite input impedance of the off-chip buffer. Boosted gate clocks cannot be measured at minimum input supply due to low drivability. As such, boosted gate clocks of the seventh stage of CP^+ and the third stage of CP^- are shown in Fig. 13 using an input supply of 120 mV.

Pumping efficiency of the charge-pump-based voltage multiplier was measured across varying input voltage using a digital multimeter with an input impedance of >1 GΩ to measure the output voltage. The output power was measured using a source meter (Keithley 2450) as a current sink. The measurement was done for an input voltage range relevant for the target application, body-heat energy harvesting, where the cold-start block will be exposed mostly to sub-100-mV TEG voltages due to the small ΔT value between the skin and the ambient environment.

As shown in Fig. 14, the proposed start-up voltage multiplier achieves a pumping efficiency higher than 78% across an input voltage range of 50–100 mV, with a peak value of 93% at an input voltage of 65 mV. Pumping efficiency of the voltage multiplier is maximized at low input voltages to reduce the minimum cold-start voltage. At higher input voltages, a large swing of the boosted gate clocks causes the GBs to

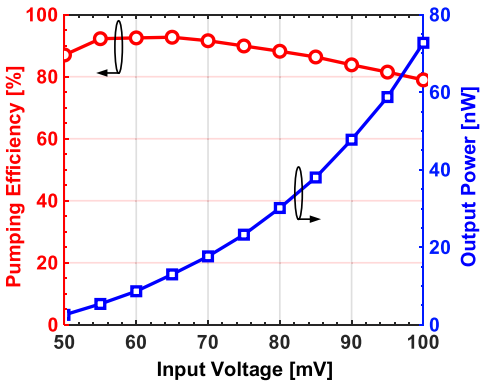


Fig. 14. Measured pumping efficiency and output power of the charge-pump-based voltage multiplier across input voltages.

TABLE I
SUMMARY OF MINIMUM OPERATIONAL VOLTAGE

Block	Min. operational voltage
Start-up ring oscillator	40 mV
Start-up voltage multiplier	50 mV
Cold-start	57 mV
Inductive boost converter	25 mV (once started)

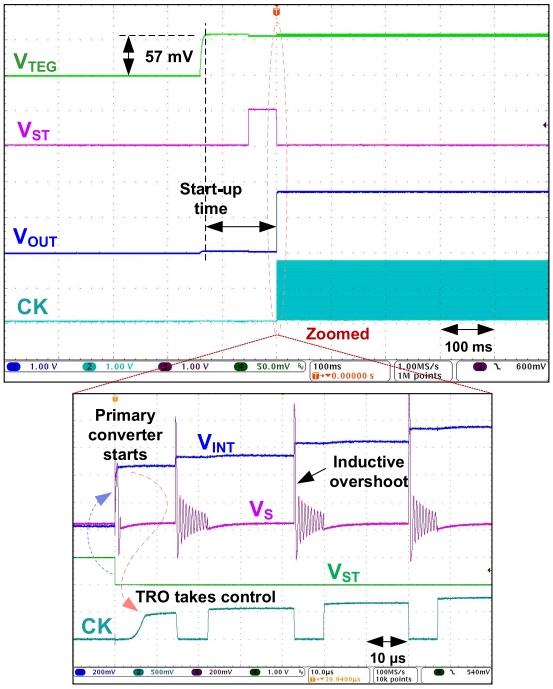


Fig. 15. Measured start-up transient of the proposed cold-start architecture. Zoomed-in view of the waveform showing triggering of the primary converter with the fast-falling edge of strobe pulse V_{ST}.

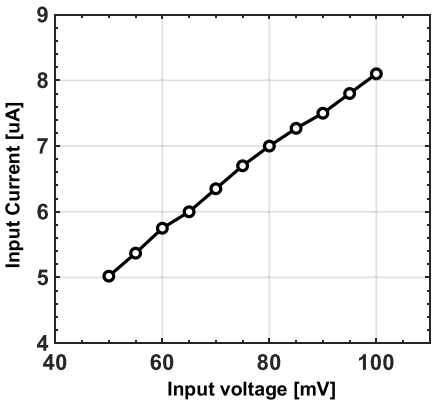


Fig. 16. Current drawn from source by the cold-start block at various input voltages.

draw more current driving CTS gates and increases internal loading. In addition, low pumping-clock frequency due to a large number of delay stages in the ring oscillator reduces the pumping efficiency of the voltage multiplier at higher input voltages. Nevertheless, the boosted output of the voltage multiplier at higher input voltages can easily power the SGU to generate the start-up strobe.

The start-up performance of the proposed architecture is characterized using a bench-top power supply with added 5-Ω series resistance to imitate a typical TEG source. A 220-μH off-chip inductor is used for the primary boost converter. The value of the inductor is chosen higher than the minimum required value derived in Section V to mitigate additional conduction losses due to inefficient routing. As shown in Fig. 15, the primary converter starts with a minimum source voltage of 57 mV. Although the stand-alone voltage multiplier operates at lower input voltage, a leakage current of the SGU loads the multiplier output and prevents start-up at a lower voltage. The minimum operational voltage of the key blocks is summarized in Table I.

Due to the fast one-shot start-up mechanism, it takes only 135 ms for cold start. The zoomed-in view of waveform in Fig. 15 shows inductive overshoot at V_S with the falling edge of V_{ST}. A rise in V_{INT} above 400 mV following the strobe-cycle starts the TRO immediately, and CK takes control of the inductive boost converter. Once started, the output voltage rises to an unregulated 1.8 V with no load.

The measured efficiency of the boost converter is 20% at the 57 mV cold-start voltage, and the efficiency increases to 47% at an input voltage of 100 mV. As observed, the efficiency of the converter is relatively low due to comparatively high conduction losses, including the ON-resistance of the LS switch M_{LS2} that charges the inductor following the cold start, as well as parasitic routing resistance that can be improved in future implementations.

While the cold-start block draws current from the source during the normal operation of the boost converter, this small input current (see Fig. 16) is drawn from the LS input voltage, and the power consumed by the cold-start block is negligible compared with the input power of the boost converter and does not affect overall efficiency. As such, the cold-start block is not functionally de-activated during normal operation. Nevertheless, disabling the cold-start block with the start of the inductive converter will increase the maximum input voltage range of the boost converter, ensuring that the devices in

TABLE II
COMPARISON WITH STATE-OF-THE-ART COLD-START VOLTAGES

Cold-start Integration	Off-chip			On-chip				
References	JSSC'11 [4]	JSSC'13 [8]	JSSC '18 [9]	JSSC'12 [11]	JSSC '15 [5]	JSSC'16 [12]	ISSCC '19 [30]	**This work**
Process	0.35 µm	65 nm	65 nm	65 nm	0.13 µm	0.13 µm	0.18 µm	**0.18 µm**
Start-up mechanism	Mechanical vibration	LC oscillator & charge pump	Colpitts oscillator & charge pump	Ring-oscillator(1) & charge pump	Ring-oscillator & charge pump	Ring-oscillator & charge pump	Ring-oscillator & charge pump	**Ring-oscillator & charge pump**
Cold-start voltage	35 mV	50 mV	40 mV	95 mV	220 mV	70 mV	129 mV	**57 mV**
Start-up time	18 ms	30 ms (2)	22 ms (2)	262 ms	3.5 s (2)	1.5 s	150 s (2)	**135 ms**
Intermediate storage capacitor(4)	470 pF (On-chip)	– (On-chip)	4.7 nF (Off-chip)	10 nF (Off-chip)	100 uF (Off-chip)	1 nF (On-chip)	– (Off-chip)	**350 pF (On-chip)**
Boost Inductor	22 µH	4.7 µH + 100 µH	3.3 µH	6.8 µH	22 µH	>200 µH	–	**220 µH**
Additional element(3)	MEMS	Inductor	Inductor	None	None	None	None	**None**

(1) Post fabrication V_{th} trimming. (2) Estimated from transient plots. (3) For cold-start purpose only. (4) Used during cold-start.

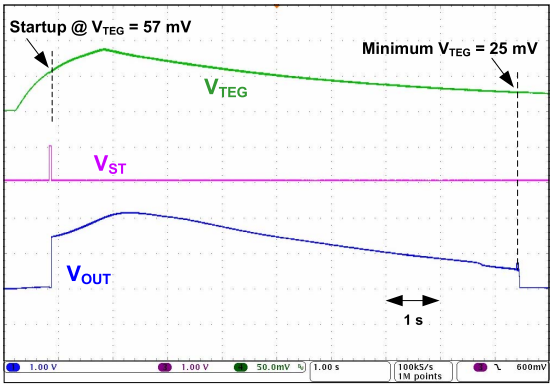


Fig. 17. Measured transient of the boost converter with a commercial TEG.

the start-up voltage multiplier remain within voltage stress tolerance at higher input voltages (>100 mV).

The cold start was also demonstrated using a commercial TEG (Marlow TG12-6-01L); the experimental setup is shown in Fig. 10(b). The measured input and output transient waveforms in Fig. 17 show that the boost converter starts at an input voltage of 57 mV, as expected, which corresponds to a temperature gradient of $\Delta T = 1.6$ °C, and sustains operation until the input voltage falls below 25 mV ($\Delta T = 0.8$ °C). The total energy used from the TEG for the cold start is 90 nJ.

Prior to the operation of the inductive converter, the cold-start block is the only active block and draws less than 6 μA of current from the source, as shown in Fig. 16. Once started, the inductive converter draws an input power of 20 μW at the cold-start voltage and sustains operation with a minimum input power of 2.5 μW. The minimum input voltage for the cold start of the converter was checked across five chips and varies from 57 to 61 mV.

The performance of the proposed cold-start architecture is compared against state of the art in Table II. While [4] achieved low-voltage cold start with the aid of mechanical vibrations, [8] and [9] used additional off-chip inductors. The cold-start time, defined as the time required from power-on to starting the primary boost converter, is determined by the ability of the low-power start-up voltage multiplier to the power start-up control circuits of the inductive boost converter. While the rise time of the final output depends on the inductor current and the output load cap, a majority of the start-up time is consumed by the slow, low-voltage cold start. The proposed fully integrated cold-start architecture achieves the cold-start of the boost converter at 18% lower input voltage and in 48% less time, even at 1.6× lower input voltage, compared with the previously demonstrated on-chip implementations [11], [12].

VII. CONCLUSION

An integrated cold-start architecture was presented to start inductive boost converters at very low input voltage toward realizing autonomous body-heat energy harvesting using TEGs. Challenges of on-chip voltage multiplication at small input voltage have been addressed by applying a unique cross-coupled gate boosting technique using complementary charge pumps. An efficient leakage suppression technique was also demonstrated using stacked inverters to generate a start-up clock using an integrated ring oscillator at a 40-mV input supply voltage. The one-shot start-up mechanism achieves the integrated cold start of the boost converter at an input voltage of as low as 57 mV, and it takes only 135 ms to start an inductive boost converter.

In general, the proposed architecture and the described design efforts were focused on the implementation and optimization of the cold-start architecture, demonstrating a fast and low-voltage one-shot cold-start technique with the aid of the proposed voltage multiplier. Once started, additional features can be added to further enhance the primary inductive boost converter efficiency, including maximum power transfer and zero-current sensing.

Cold start and handover to a primary boost converter were also demonstrated using a commercial TEG as the input with a temperature gradient <2 °C, illustrating the utility of the proposed architecture for realizing fully autonomous thermal energy harvesting from the human body heat.

ACKNOWLEDGMENT

The authors would like to thank B. Shen for valuable technical discussions and feedback. The content is solely the responsibility of the authors and does not necessarily represent the official views of the National Institutes of Health.

REFERENCES

[1] V. Leonov, T. Torfs, P. Fiorini, and C. Van Hoof, "Thermoelectric converters of human warmth for self-powered wireless sensor nodes," *IEEE Sensors J.*, vol. 7, no. 5, pp. 650–657, May 2007.

[2] G. J. Snyder and E. S. Toberer, "Complex thermoelectric materials," *Nature Mater.*, vol. 7, pp. 101–110, Feb. 2008. doi: 10.1038/nmat2090.

[3] E. J. Carlson, K. Strunz, and B. P. Otis, "A 20 mV input boost converter with efficient digital control for thermoelectric energy harvesting," *IEEE J. Solid-State Circuits*, vol. 45, no. 4, pp. 741–750, Apr. 2010.

[4] Y. K. Ramadass and A. P. Chandrakasan, "A batteryless thermoelectric energy-harvesting interface circuit with 35 mV startup voltage," *IEEE J. Solid-State Circuits*, vol. 46, no. 1, pp. 333–341, Jan. 2011.

[5] A. Shrivastava, N. E. Roberts, O. U. Khan, D. D. Wentzloff, and B. H. Calhoun, "A 10 mV-input boost converter with inductor peak current control and zero detection for thermoelectric and solar energy harvesting with 220 mV cold-start and-14.5 dBm, 915 MHz RF kick-start," *IEEE J. Solid-State Circuits*, vol. 50, no. 8, pp. 1820–1832, Aug. 2015.

[6] Y.-K. Teh and P. K. T. Mok, "Design of transformer-based boost converter for high internal resistance energy harvesting sources with 21 mV self-startup voltage and 74% power efficiency," *IEEE J. Solid-State Circuits*, vol. 49, no. 11, pp. 2694–2704, Nov. 2014.

[7] J.-P. Im, S.-W. Wang, S.-T. Ryu, and G.-H. Cho, "A 40 mV transformer-reuse self-startup boost converter with MPPT control for thermoelectric energy harvesting," *IEEE J. Solid-State Circuits*, vol. 47, no. 12, pp. 3055–3067, Dec. 2012.

[8] P.-S. Weng, H.-Y. Tang, P.-C. Ku, and L.-H. Lu, "50 mV-input batteryless boost converter for thermal energy harvesting," *IEEE J. Solid-State Circuits*, vol. 48, no. 4, pp. 1031–1041, Apr. 2013.

[9] B. Lim, J. Seo, and S. Lee, "A colpitts oscillator-based self-starting boost converter for thermoelectric energy harvesting with 40-mV startup voltage and 75% maximum efficiency," *IEEE J. Solid-State Circuits*, vol. 53, no. 11, pp. 3293–3302, Nov. 2018.

[10] K. Kadirvel *et al.*, "A 330nA energy-harvesting charger with battery management for solar and thermoelectric energy harvesting," in *Proc. IEEE Int. Solid-State Circuits Conf.*, Feb. 2012, pp. 106–108.

[11] P.-H. Chen *et al.*, "Startup techniques for 95 mV step-up converter by capacitor pass-on scheme and V_{TH}-tuned oscillator with fixed charge programming," *IEEE J. Solid-State Circuits*, vol. 47, no. 5, pp. 1252–1260, May 2012.

[12] J. Goeppert and Y. Manoli, "Fully integrated startup at 70 mV of boost converters for thermoelectric energy harvesting," *IEEE J. Solid-State Circuits*, vol. 51, no. 7, pp. 1716–1726, Jul. 2016.

[13] Z. Luo, L. Zeng, B. Lau, Y. Lian, and C.-H. Heng, "A sub-10 mV power converter with fully integrated self-start, MPPT, and ZCS control for thermoelectric energy harvesting," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 65, no. 5, pp. 1744–1757, May 2018.

[14] S. Bose, T. Anand, and M. L. Johnston, "Fully-integrated 57 mV cold start of a thermoelectric energy harvester using a cross-coupled complementary charge pump," in *Proc. IEEE Custom Integr. Circuits Conf. (CICC)*, Apr. 2018, pp. 1–4.

[15] J. D. Meindl and J. A. Davis, "The fundamental limit on binary switching energy for terascale integration (TSI)," *IEEE J. Solid-State Circuits*, vol. 35, no. 10, pp. 1515–1516, Oct. 2000.

[16] B. Zhai, D. Blaauw, D. Sylvester, and K. Flautner, "The limit of dynamic voltage scaling and insomniac dynamic voltage scaling," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 13, no. 11, pp. 1239–1252, Nov. 2005.

[17] K. Roy, S. Mukhopadhyay, and H. Mahmoodi-Meimand, "Leakage current mechanisms and leakage reduction techniques in deep-submicrometer CMOS circuits," *Proc. IEEE*, vol. 91, no. 2, pp. 305–327, Feb. 2003.

[18] S. Bose and M. L. Johnston, "A stacked-inverter ring oscillator for 50 mV fully-integrated cold-start of energy harvesters," in *Proc. IEEE Int. Symp. Circuits Syst. (ISCAS)*, May 2018, pp. 1–5.

[19] N. Lotze and Y. Manoli, "A 62 mV 0.13μm CMOS standard-cell-based design technique using schmitt-trigger logic," *IEEE J. Solid-State Circuits*, vol. 47, no. 1, pp. 47–60, Jan. 2012.

[20] J. F. Dickson, "On-chip high-voltage generation in MNOS integrated circuits using an improved voltage multiplier technique," *IEEE J. Solid-State Circuits*, vol. 11, no. 3, pp. 374–378, Jun. 1976.

[21] R. Pelliconi, D. Iezzi, A. Baroni, M. Pasotti, and P. L. Rolandi, "Power efficient charge pump in deep submicron standard CMOS technology," *IEEE J. Solid-State Circuits*, vol. 38, no. 6, pp. 1068–1071, Jun. 2003.

[22] J.-T. Wu and K.-L. Chang, "MOS charge pumps for low-voltage operation," *IEEE J. Solid-State Circuits*, vol. 33, no. 4, pp. 592–597, Apr. 1998.

[23] P.-H. Chen *et al.*, "0.18-V input charge pump with forward body biasing in startup circuit using 65 nm CMOS," in *Proc. IEEE Custom Integr. Circuits Conf.*, Sep. 2010, pp. 1–4.

[24] J. Kim, P. K. T. Mok, and C. Kim, "A 0.15 V input energy harvesting charge pump with dynamic body biasing and adaptive dead-time for efficiency improvement," *IEEE J. Solid-State Circuits*, vol. 50, no. 2, pp. 414–425, Feb. 2015.

[25] M. D. Seeman and S. R. Sanders, "Analysis and optimization of switched-capacitor DC-DC converters," *IEEE Trans. Power Electron.*, vol. 23, no. 2, pp. 841–851, Mar. 2008.

[26] M. Seok, G. Kim, D. Blaauw, and D. Sylvester, "A portable 2-transistor picowatt temperature-compensated voltage reference operating at 0.5 V," *IEEE J. Solid-State Circuits*, vol. 47, no. 10, pp. 2534–2545, Oct. 2012.

[27] G. Kim, M.-K. Kim, B.-S. Chang, and W. Kim, "A low-voltage, low-power CMOS delay element," *IEEE J. Solid-State Circuits*, vol. 31, no. 7, pp. 966–971, Jul. 1996.

[28] D. Rozgić and D. Marković, "A miniaturized 0.78-mW/cm2 autonomous thermoelectric energy-harvesting platform for biomedical sensors," *IEEE Trans. Biomed. Circuits Syst.*, vol. 11, no. 4, pp. 773–783, Aug. 2017.

[29] X. Liu and E. Sanchez-Sinencio, "A single-cycle MPPT charge-pump energy harvester using a thyristor-based VCO without storage capacitor," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Jan. 2016, pp. 364–365.

[30] P. Cao, Y. Qian, P. Xue, D. Lu, J. He, and Z. Hong, "27.1 An 84% peak efficiency bipolar-input boost/flyback hybrid converter with MPPT and on-chip cold starter for thermoelectric energy harvesting," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2019, pp. 420–422.

Soumya Bose (S'16) received the B.E. degree in electronics and communication engineering from the Indian Institute of Engineering Science and Technology, Shibpur, India, in 2009 and the M.Tech. degree from IIT Kharagpur, Kharagpur, India, in 2013. He is currently pursuing the Ph.D. degree in electrical and computer engineering with Oregon State University, Corvallis, OR, USA.

From 2013 to 2015, he was a Circuit Design Engineer with Rambus, Bengaluru, India, and worked on high-speed memory interfaces and power management integrated circuits for multi-protocol PHYs. In 2018, he was an Analog Design Intern with Texas Instruments' Kilby Labs, Dallas, TX, USA, and worked on nano-power LDOs. His research interests include energy-efficient sensor interfaces, integrated power management, and autonomous energy harvesters.

Mr. Bose serves as a Reviewer for the IEEE JOURNAL OF SOLID-STATE CIRCUITS and the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS I AND II.

Tejasvi Anand (S'12–M'15) received the M.Tech. degree (Hons.) in electronics design and technology from the Indian Institute of Science, Bengaluru, India, in 2008, and the Ph.D. degree in electrical engineering from the University of Illinois at Urbana–Champaign, Champaign, IL, USA, in 2015.

From 2008 to 2010, he was an Analog Design Engineer with Cosmic Circuits (now a part of Cadence Design Systems), Bengaluru. He is currently an Assistant Professor with the Department of Electrical Engineering and Computer Science, Oregon State University, Corvallis, OR, USA. His current research interests include wireline communication, frequency synthesizers, and energy harvesters and sensors with an emphasis on energy efficiency.

Dr. Anand serves as a Technical Committee Member of the Custom Integrated Circuits Conference (CICC). He was a recipient of the 2009 CEDT Design (gold) Medal from the Indian Institute of Science, the IEEE Solid-State Circuits Society Predoctoral Achievement Award (2014–2015), the 2015 Broadcom Foundation University Research Competition Award, and the 2015 M. E. Van Valkenburg Graduate Research Award from the University of Illinois at Urbana–Champaign.

Matthew L. Johnston (S'03–M'12) received the B.S. degree in electrical engineering from the California Institute of Technology, Pasadena, CA, USA, in 2005, and the M.S. and Ph.D. degrees in electrical engineering from Columbia University, New York, NY, USA, in 2006 and 2012, respectively.

He was the Co-Founder and the Manager of research at Helixis, Carlsbad, CA, USA, a Caltech-based spinout developing instrumentation for real-time DNA amplification, from 2007 until its acquisition by Illumina, San Diego, CA, USA, in 2010. From 2012 to 2013, he was a Postdoctoral Scholar with the Bioelectronic Systems Laboratory, Columbia University. He is currently an Assistant Professor with the School of Electrical Engineering and Computer Science, Oregon State University, Corvallis, OR, USA. His current research is focused on the integration of sensors and transducers with active CMOS substrates, lab-on-CMOS platforms for chemical and biological sensing, bio-energy harvesting, and low-power distributed sensing applications.

Dr. Johnston currently serves as an Associate Editor for the IEEE TRANSACTIONS ON BIOMEDICAL CIRCUITS AND SYSTEMS and serves on the Biomedical and Life Science Circuits and Systems Technical Committee and the Analog Signal Processing Technical Committee for the IEEE Circuits and Systems Society.