Programmable Neuron Array Based on a 2-Transistor Multiplier Using Organic Floating-Gate for Intelligent Sensors

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***Abstract*— Artificial neurons are introduced for local data processing in a large area sensor device, thereby reducing multiple sensor outputs to 1-bit digital output. To reduce the area overhead and layout complexity due to the artificial neuron array, a 2-transistor multiplier using organic floating-gate pFET is proposed. Each artificial neuron has multiple organic floating-gate pFETs embedded in it. A virtual scalable floating-gate based memory architecture is realized for selective programming of each floating-gate pFET. Threshold voltage tuning is utilized to realize both of the positive and the negative weight values for a neuron. A flexible interface pressure monitoring device with pressure-sensitive rubber sheet is developed for pressure ulcer prevention to show the feasibility of our concept. A 50 mm^2 organic sheet integrating 2×2 neuron array is fabricated with 2-V organic CMOS transistors. Selective floating-gate programming and neuron operation are successfully demonstrated.**

***Index Terms*— Organic thin film transistor, floating-gate memory, artificial neuron, local signal processing, flexible sensor sheet, pressure sensor, analog filter.**

I. Introduction

With the emergence of Internet of Things (IoT) era, more and more physical objects are being connected to the internet. These IoT devices, which in most cases include sensors, provides information of our surrounding to enable a more secure and comfortable life. In order to gather information from the physical world, various forms of devices are required including devices capable of sensing large area. Especially for health-care and bio-medical applications, flexible and large area devices that can be attached to human skin for example will provide greater options.

For flexible and large area sensor applications, thin-film transistors using semiconductor materials such as organic [1], IGZO [2] and amorphous silicon [3] have shown promise to fulfill the above needs. However, in the literature, the transistors have been primarily used as switches in a large sensor array. Sensor applications have been reported integrating on-sheet amplifiers, ring oscillators, flip-flops etc. [4]–[9]. However, the existing sensor array based applications suffer from the following limitations:

1) large number of wires for read out;
2) analog signals through long wires causing signal integrity problem; and/or
3) post-processing using computers for extracting the insights from the data.

Therefore, built-in local signal processing capability will broaden the use of sensor devices for large area monitoring. Although some functional circuits such as a microprocessor [10], transconductance amplifiers [6] or integration between flexible electronics and CMOS IC [11] have been reported, the integration with sensor array is not studied. In this paper, we propose a new sensor array architecture where local signal processing units are embedded into the sensor array to extract the essence of the sensed data and then output digital signals. Local processing reduces the number of wires significantly, thus ensures scalability of large area implementation. Digital output removes signal integrity problem.

In this paper, we show that artificial neuron can be used as a local signal processing unit. We propose a CMOS based compact 2-transistor (2T) multiplier using organic floating-gate pFET to realize an artificial neuron circuit with small transistor count. Transistor count is critical as there is limitation in metal layer resources for organic circuits. Floating-gate devices have been successfully demonstrated in [12], [13]. Researchers are developing systems that utilizes the precious floating-gate memories. One such example is an image classifier application where the floating-gate memories are used for storing weight values [13]. Floating-gate can also be used for post-fabrication tuning to encounter device variation [14]. One challenge for floating-gate memory based sensor array with local functional units is to find a way to program the floating-gate devices individually, Our proposed CMOS based multiplier scheme allows us to access the three terminal of a floating-gate device, hence implementation of a virtual memory array becomes possible.

To show the feasibility and application of the proposed system, we develop a flexible interface pressure monitoring system targeting pressure ulcer prevention. We demonstrate the application of artificial neurons for extracting real-time essence

Manuscript received May 24, 2016; revised August 19, 2016; accepted September 23, 2016. This paper was recommended by Guest Editor J. S. Chang.

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Digital Object Identifier 10.1109/JETCAS.2016.2628411

of sensor data. For example, non-uniform pressure distribution and local high pressure due to the wrinkles of clothes or bed sheet increase the rate of pressure ulcer, therefore early detection of the pressure non-uniformity is helpful. Uneven interface pressure distribution is one of the major causes for pressure ulcer development besides the high intensity pressure applied over a long period of time [15]. Constant monitoring of interface pressure can be useful in reducing the risk of pressure ulcer development. However, the conventional pressure mapping systems require external monitoring devices for image processing [16], [17]. Furthermore, as the monitored signals are analog, signal integrity is a problem to accurately capture the pressure readings. In order to overcome the above problems, we propose an intelligent pressure monitoring system that processes the analog pressure signals locally and output digital signals when an anomaly is found. The proposed intelligent system thus have the following advantages:

1) reduce the number of external wires;
2) digital output provides robust data transmission;
3) constant monitoring without human intervention by warning the anomaly; and
4) programmability for adaption based on target patient.

In this paper, the world's first artificial neuron using OFETs is proposed for local signal processing. A flexible pressure monitoring device integrating 2×2 artificial neurons is demonstrated. The key contributions of this paper are as follows:

1) propose a 2-transistor multiplier topology;
2) demonstrate artificial neuron operation that utilizes the 2T multiplier;
3) develop scalable neuron array architecture for local processing and digital output; and
4) scalable virtual floating-gate memory array with programming scheme.

The remainder of the paper is organized as follows. We describe the pressure monitoring system and its components in Section II. In Section III, an artificial neuron topology utilizing a new 2-transistor multiplier topology is proposed. In Section IV, several experimental results will be discussed to show the feasibility of the proposed system. Section V concludes the paper.

II. Intelligent Pressure Monitoring System

In this section, we develop a flexible pressure monitoring system with built-in analog filters and digital output. First, the system overview is described to show how the transistors and sensors are integrated. Then, we introduce the use of artificial neuron topology as an analog filter with small area foot print.

A. System Overview

Fig. 1 shows a photo of the developed pressure monitoring device. The device can be placed under the bed sheet to measure the pressure distribution. The system shown in Fig. 1 features local on-sheet analog signal processing for digital output. In the system, three flexible sheets are stacked and laminated together. The three sheets consist of a flexible PCB (Printed Circuit Board), a pressure-sensitive rubber sheet [12], and a plastic sheet with printed organic circuits. The rubber

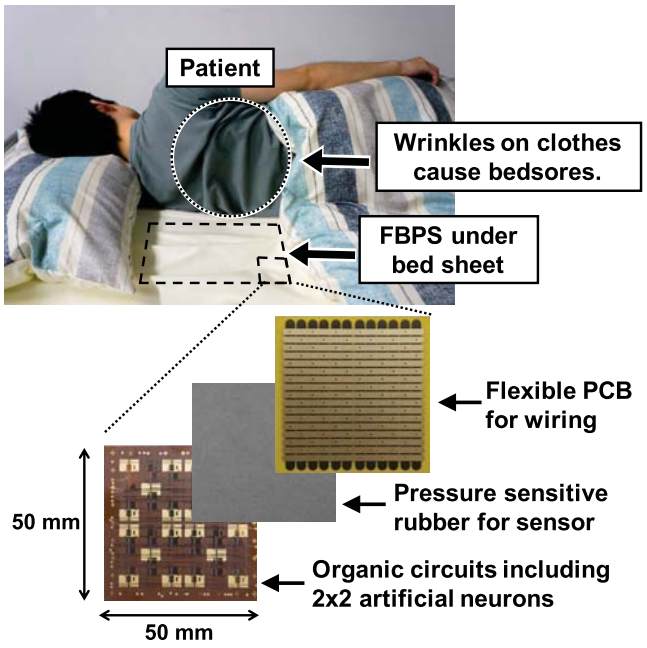


Fig. 1. Example of a flexible pressure monitoring system for pressure ulcer prevention. Three flexible sheets including a PCB, a pressure-sensitive rubber sheet and an organic circuit sheet are stacked together.

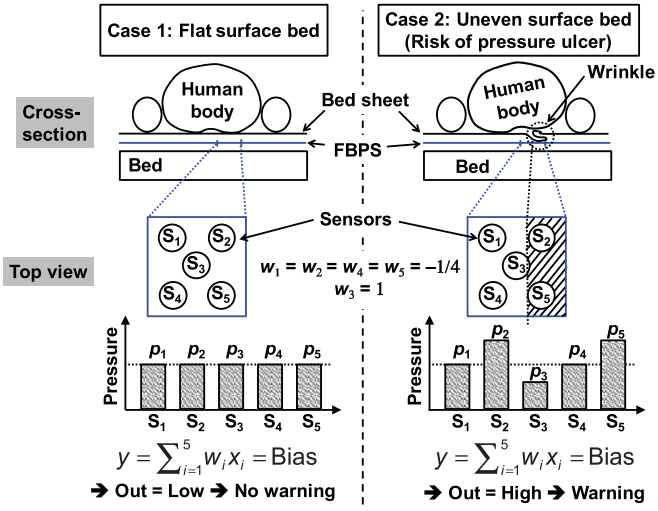


Fig. 2. An example of non-uniform pressure distribution because of uneven surface. Artificial neuron can be used to detect the non-uniform distribution.

sheet is sandwiched between the organic sheet and PCB sheet. The purpose of the PCB sheet is to supply a uniform bias voltage to one side of the rubber sheet. In fact, the PCB sheet can be replaced by any conductive sheet that is flexible. The three sheets can be sticked together with adhesive systems such as silver paste or anisotropic conductive film bonding. In [18], integration of organic sheet and rubbery sensor sheet to form flexible touch sensor device is demonstrated. We adopt the above approach to realize pressure sensor device. The PCB sheet applies a bias voltage to the rubber sheet on one surface uniformly. The organic transistors receive pressure signals from the rubber sheet through contact pads.

The operation of the proposed device is shown in Fig. 2 where two cases of pressure distributions are illustrated. In the

TABLE I
COMPARISON BETWEEN ORGANIC FET AND SILICON MOSFET

	Organic FET	Silicon MOSFET
Minimum gate length	20 μm	22 nm
Mechanical flexibility	Flexible	Very limited
Normalized ON current	50 nA /μm @ 2V	1 mA/μm @ 1V
Gate delay	10 ms @ 2V	10 ps @ 1V
Cost / area	**Low**	**High**
Cost / transistor	**High**	**Low**
Lifetime	Months	Years

first case, uniform pressures are applied to the interface, In the second case, non-uniform pressures are applied. We need a circuit to detect the non-uniformity and warn with a digital signal. As shown in the figure, this can be achieved by an analog filter. In this example, non-uniformity can occur from any direction. Weight assignment in an artificial neuron consisting of five sensors of $w_1 = w_2 = w_4 = w_5 = -1/4$ and $w_3 = 1$ will realize such a filter. On a flat surface bed, the pressures on S_1–S_5 are the same, and "Out" is low showing "No warning". In contrast, on an uneven surface bed, the pressures on S_1–S_5 are different, and "Out" is high showing "Warning".

B. Sensor Material

For any sensor application design, the choice of sensor material plays an important role. Pressure can be sensed by measuring the capacitance or the resistance between the two surfaces in between where the pressure is applied. In [17], a capacitive pressure sensor has been demonstrated. However, capacitive sensors suffer from integration complexity as dielectric materials and electrodes need to be integrated. Another example of pressure sensor is to use polymeric piezoelectric [polyvinylidene difluoride (PVDF)] sheet. In this case intermolecular polarization mechanism is used to generate small signals. However, as the signal is small, amplifiers are required that may add additional complexity to the system. Pressure-sensitive rubber has been successfully demonstrated in [12] and [18]. In this paper, we adopt a pressure-sensitive rubber approach because of high sensitivity and ease of integration. In the rubber sheet, when mechanical pressure is applied in lateral direction to the sheet, the resistance between the surfaces increases. Thus, the rubber sheet can be seen as variable resistor whose resistance varies depending on the applied pressure. The sensor resistance will then be converted to voltage levels so that the transistors can process the signals.

C. Organic Transistors and Floating-gate Devices

For biomedical and healthcare applications, large area sensing and low voltage operation is preferable. In order to understand the organic transistors and their usage, we show a comparison between organic material based FET and silicon MOSFET in Table I. Silicon MOSFETs have very high drivability and can be integrated in large number in a very small area. Thus they are suitable high performance computing. However, they are not suitable for large area as cost per area becomes high. On the other hand, cost per area is low for organic FETs. Furthermore, organic FETs provide flexibility and transparency which the silicon counterpart cannot provide. But, a key point here is that although cost per area is low for organic FETs, cost per transistor is actually very high for organic FETs. Thus, using organic FETs in small numbers is an imortant key. Another feautre of organic FET based devices is that the devices are printed on a sheet, thus there are limitations on the number of metal layers that can be used for interconnect. Based on the above limitations, circuit topologies need to be adopted to utilize the organic FETs to pave the way for new applications.

Organic transistors are also shown to be operable under 2 V [4], [12]. Self-assembled monolayer (SAM) technology is used to form very thin dielectric layer allowing low voltage operation. We use a similar technology for our demonstration in this paper. The organic semiconductors used for p-type and n-type transistors are DNTT [19] and PDI-8CN2 [20], respectively. The floating-gate in a pFET can be programmed with gate–source voltage of -6 V to -4 V and erased with gate–source voltage of +3 V. We have fabricated organic transistors and floating-gate pFETs with gate length of 50 μm. The organic sheet consists of one metal layer for transistor gate, one metal layer for source and drain, and one layer for contact pads. Through hole vias are used for connecting the three metal layers. Thanks to the small transistor count, the neuron array is designed with just two metal layers for interconnect.

D. Local Processing for Pattern Extraction

In large-scale real-time sensor application, the essence of the data is important for decision making. The proposed system locally detects the uneven pressure distributions and warn us only when the unevenness crosses a certain threshold. For such an application, the following problems need to be addressed. First, the patient weights differ largely such that the amount of pressure is different from patient to patient. Second, threshold for detecting the unevenness is not a universal value. Therefore, a system with post-fabrication capability of tuning the threshold and pressure sensitivity can be very helpful. Programming of the floating-gate memory provides the above capability.

Fig. 3 shows the block diagram of the proposed architecture. An array of artificial neurons are implemented on the organic sheet. Each neuron outputs a digital signal based on the interface pressure distribution. Word line and bit line decoders provide appropriate signals to the system for selective floating-gate programming. The bit lines are shared among the columns where each column is activated by an output decoder. During the read-out phase, the bit lines are set to the supply voltage and the output decoder selects a particular neuron column. During the programming phase, the bit line and word line voltages are tuned to program the threshold voltages. Only the neurons in the selected column drive the output lines as neurons under other columns are deactivated. The number of output wires for an $N \times N$ neuron array is only N. In this demonstration, each neuron consists of five sensor inputs. Thus, the number of output wires for each neuron is reduced from 5 to 1. In a conventional approach based on a sensor

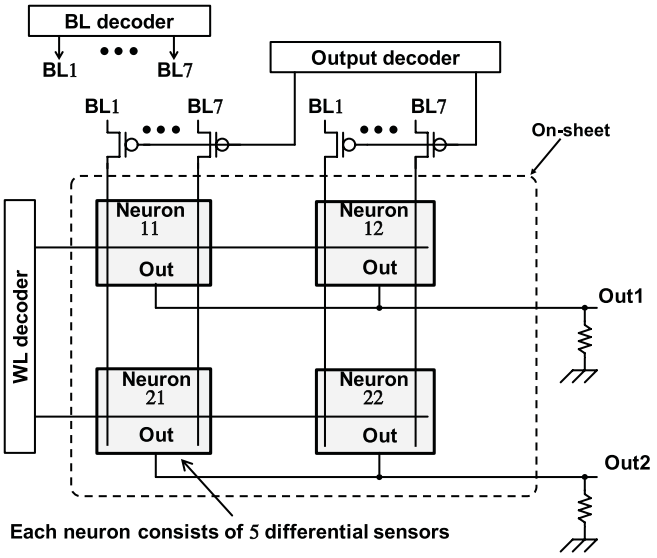


Fig. 3. Scalable neuron array for on-sheet filtering with digital output. Each neuron block corresponds to the schematic shown in Fig. 12.

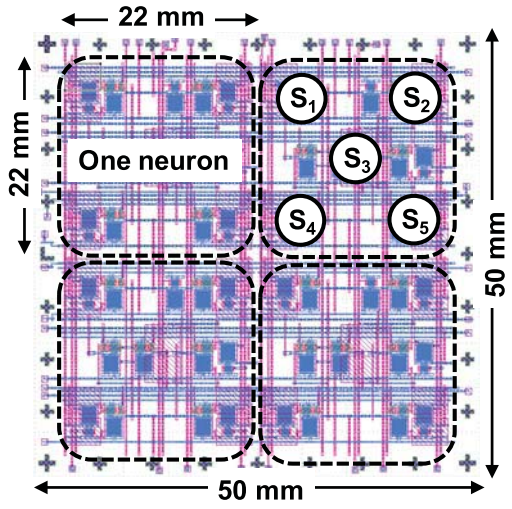


Fig. 4. Layout of an 2x2 neuron array built on an organic transistor sheet.

matrix, analog signal outputs are read through long wires. Whereas, the proposed system output digital signals.

E. Organic Sheet Layout

Fig. 4 shows the layout of a designed 2×2 neuron array on a plastic sheet. The size of each neuron is 22×22 mm^2 where five sensors are embedded. Thanks to the organic transistors and the proposed 2-transistor multiplier based neuron circuit, high spatial resolution of 1.03 sensors/cm^2 is achieved compared with 0.264 sensors/cm^2 with a capacitance sensor [17]. The operation mechanism of the neuron circuit will be discussed in the next section.

III. Artificial Neuron as Analog Filter

The heart of the proposed intelligent sensor system is the neuron circuit with small transistor counts. The small

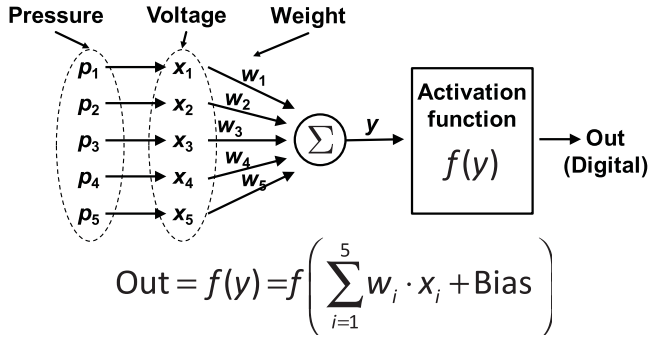


Fig. 5. Artificial neuron as analog filter for local signal processing.

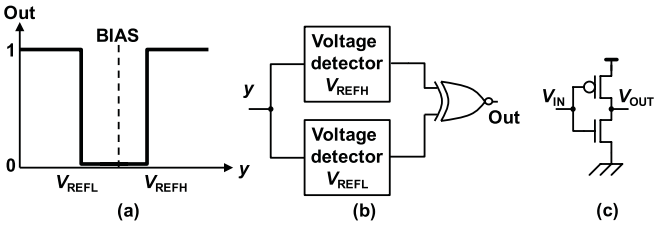


Fig. 6. Activation function for digitization.

transistor count is achieved by developing a new 2-transistor multiplier topology that utilizes threshold voltage tuning by the floating-gate. In this section, we describe the artificial neuron architecture, its usage as analog filter and the 2-transistor multiplier topology.

A. Artificial Neuron

Fig. 5 shows an artificial neuron example for five pressure inputs. Fig. 6 illustrates the activation function. Fig. 6(c) shows a CMOS inverter with floating-gate pFET as the voltage detector. By changing the threshold voltage of the floating-gate pFET, the logical threshold voltage of CMOS inverter is programmed, thereby programmable threshold voltages (V_{REFH}, V_{REFL}) are achieved.

B. 2-Transistor Multiplier

Analog multiplier based on neuron-FET or differential circuit techniques are proposed [21]–[23]. However, both of them require analog voltages as weights. Other multiplier techniques such as capacitance tuning for learning is reported [24]. [13] proposes a 4-transistor multiplier utilizing floating-gate devices for classifier implementation. Here, we propose a 2T topology.

Fig. 7 shows the proposed 2-transistor multiplier using an organic floating-gate pFET. The multiplier is a CMOS circuit with a p-type FET and a n-type FET. Compared with a previously reported 4-transistor multiplier [13], the number of transistors is reduced by half. The input voltages (Δx_{1+}, Δx_{1-}) are differential. The operation of the multiplier is explained using a square-power law model for the FET ON current. First, the ON current change of an OFET is expressed as follows:

$$\Delta I_{\mathrm{DS}} = \beta \left(\Delta V_{\mathrm{GS}} - V_{\mathrm{TH}}\right)^2, \tag{1}$$

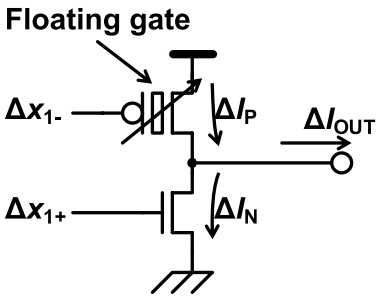


Fig. 7. A 2T multiplier cell with differential input and single-ended output.

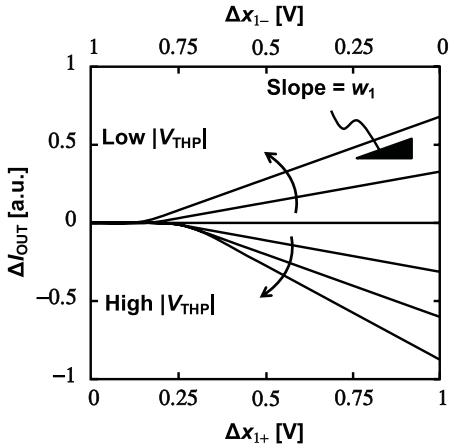


Fig. 8. Simulated ΔI_{OUT} of the 2T multiplier for different V_{THP} values. Both of the positive and the negative weights are realized by tuning the V_{THP} value.

where $\beta = \mu C_{\mathrm{OX}}(W/L)$. ΔI_{OUT} is calculated as follows:

$$\begin{aligned}\Delta I_{\mathrm{OUT}} &= \Delta I_{\mathrm{DS,P}} - \Delta I_{\mathrm{DS,N}},\\ &= 2\beta_{\mathrm{N}}(1 - m\cdot k\cdot n)V_{\mathrm{THN}}\cdot \Delta V_{\mathrm{GSN}}\\ &\quad + \beta_{\mathrm{N}}(m\cdot k^2 - 1)\cdot \Delta V_{\mathrm{GSN}}{}^2\\ &\quad + \beta_{\mathrm{N}}(m\cdot n^2 - 1)\cdot V_{\mathrm{THN}}{}^2. \end{aligned} \tag{2}$$

Here,

$$m = \frac{\beta_{\mathrm{P}}}{\beta_{\mathrm{N}}}, n = \frac{|V_{\mathrm{THP}}|}{V_{\mathrm{THN}}}, k = \frac{\Delta|V_{\mathrm{GSP}}|}{\Delta V_{\mathrm{GSN}}} \tag{3}$$

V_{THP} and V_{THN} are threshold voltages of the pFET and nFET respectively. When, $m = k = 1$, and $\Delta V_{\mathrm{GSN}} = \Delta x_{1+}$, we obtain

$$\Delta I_{\mathrm{OUT}} = 2\beta_{\mathrm{N}}\cdot(V_{\mathrm{THN}} - |V_{\mathrm{THP}}|)\cdot \Delta x_{1+} + \theta, \tag{4}$$

$$= 2\beta_{\mathrm{N}} V_{\mathrm{THN}}\cdot(1-n)\cdot \Delta x_{1+} + \theta. \tag{5}$$

Here, $\theta = \beta_{\mathrm{N}}\cdot(n^2-1)\cdot V_{\mathrm{THN}}{}^2$. In (5), ΔI_{OUT} is a product of the threshold voltage difference and the gate voltage change, hence realizes the multiplier. The term θ does not depend on the gate voltage change, thus is treated as a constant. $2\beta_{\mathrm{N}}\cdot(V_{\mathrm{THN}} - |V_{\mathrm{THP}}|)$ can be utilized as a variable weight for the artificial neuron. Both positive and negative weight are realized by tuning V_{THP} of the floating-gate pFET.

Fig. 8 shows the simulated ΔI_{OUT} for the 2T multiplier considering the ideal square-power law model for the OFET I–V characteristic. When $|V_{\mathrm{THP}}|$ is lower than V_{THN}, ΔI_{OUT} increases with the increase of nFET gate voltage increase. Whereas, when $|V_{\mathrm{THP}}|$ is higher than V_{THN}, ΔI_{OUT} decreases. The value of V_{THP} determines the gradient of ΔI_{OUT} thereby realizes different weight values.

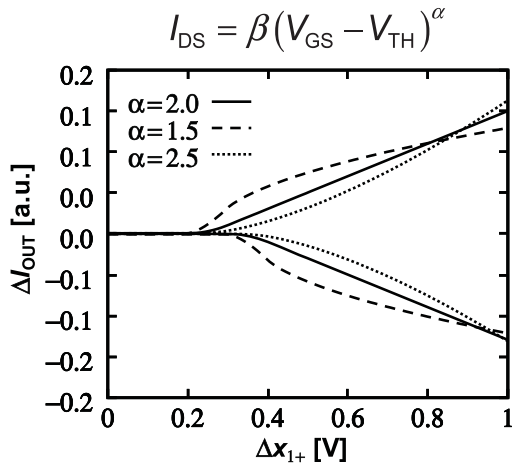


Fig. 9. Simulated ΔI_{OUT} of the 2T multiplier for different values of α in the α-power law model of transistor ON current.

In reality, the transistor ON current may not follow the ideal square-power law model. Considering velocity saturation and other mobility degradation phenomena, the α-power law model is proposed to model the ON current [25]

$$I_{\mathrm{DS}} = \beta\,(V_{\mathrm{GS}} - V_{\mathrm{TH}})^{\alpha}\,. \tag{6}$$

The detailed dc modeling of organic transistors are described in [26], [27]. From the above studies, the value of α may differ from the ideal square-power model. However, we show that even if the α value varies from the square, the multiplier operation is still achieved. Fig. 9 shows the ΔI_{OUT} change for three different values of 2.0, 1.5, and 2.5. Deviation from the ideal square-power model introduces some non-linearity, but the multiplier and variable weight characteristics exist. Thus, we conclude that the multiplier can be used as an analog filter in those cases too.

Next, we discuss on the resolution of weight tuning by V_{THP} programming. The weight, w, is represented as follows from (5)

$$w = 2\beta_{\mathrm{N}} V_{\mathrm{THN}}\cdot(1-n). \tag{7}$$

Here, n is defined as $|V_{\mathrm{THP}}|/V_{\mathrm{THN}}$. In order to realize normalized weight values of +1 and −1, the values of n need be set to 0.5 and 1.5. These values refer that V_{THP} need to tuned to the half of V_{THN} for +1 weight, and 1.5 times higher than V_{THN} for −1 weight. For example, For a V_{THN} value of 500 mV, V_{THP} need to be set at 250 mV for +1 weight, and 750 mV for −1 weight. The range of V_{THP} tuning is 500 mV. Thus, a V_{THP} tuning precision of 50 mV will give us a 10% tuning capability of the weights when V_{THN} is 500 mV. The impact of device variability and performance degradation over time need also be taken into account. As will be shown in Section IV, device variablity can be overcome by programming the devices. However, device degradation can pose a challenge. Device degradation will reduce the

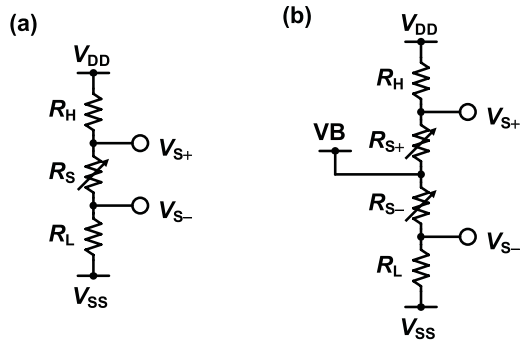


Fig. 10. Two different circuit topologies as sensor to voltage converter to generate differential voltages.

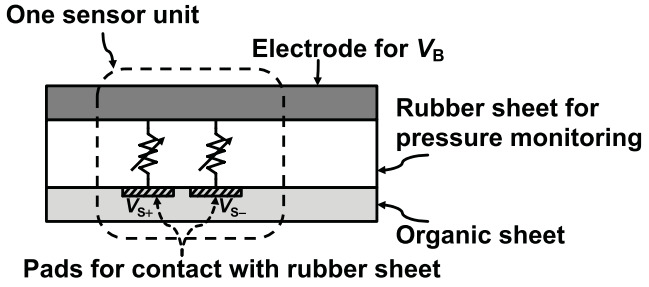


Fig. 11. Cross section of the three layers consisting of flexible PCB for bias electrode, rubber sheet for as pressure sensors and organic sheet for signal processing.

weight resolution capability. In such case, only coarse tuning of weight values might be feasible.

C. Sensor to Voltage Converter

To implement the proposed multiplier based artificial neuron, we need to generate differential input for the multiplier. Differential voltages can be generated using the two converter topologies shown in Fig. 10. For the topology in Fig. 10(a), the differential voltage, ΔV_S, is expressed as follows:

$$V_{S+} = \frac{R_S + R_L}{R_H + R_S + R_L} \cdot (V_{DD} - V_{SS}), \tag{8}$$

$$V_{S-} = \frac{R_L}{R_H + R_S + R_L} \cdot (V_{DD} - V_{SS}), \tag{9}$$

$$\Delta V_S = \frac{R_S}{R_H + R_S + R_L} \cdot (V_{DD} - V_{SS}). \tag{10}$$

ΔV_S is a function of R_S. R_H and R_L are chosen considering the required voltage sensitivity and voltage range.

The topology of Fig. 10(a) can be realized when the sensor is on the same sheet as the FETs. However, often the sensors are implemented in different sheets as is the case with our target application. We develop a converter topology shown in Fig. 10(b) to generate differential inputs. In this topology, two sensors closely placed with each other are utilized. Fig. 11 shows a cross-section view of the three stacked sheets to illustrate the feature. In this case, one sensor unit consists of two current paths in the rubber sheet. Two contact pads in the organic sheet is placed closely such that they receive similar pressure signals. The sensor output voltages then are expressed as follows:

$$V_{S+} = \frac{R_{S+}}{R_H + R_{S+}} \cdot \frac{(V_{DD} - V_{SS})}{2}, \tag{11}$$

$$V_{S-} = \frac{R_L}{R_L + R_{S-}} \cdot \frac{(V_{DD} - V_{SS})}{2}. \tag{12}$$

When, $V_B = (V_{DD} - V_{SS})/2$, $R_H = R_L = R_B$, and $R_{S+} = R_{S-}$, the differential voltage becomes as follows:

$$\Delta V_S = \left(1 - \frac{2R_B}{R_B + R_S}\right) \cdot \frac{(V_{DD} - V_{SS})}{2}. \tag{13}$$

D. Artificial Neuron With Activation Circuit

Fig. 12 shows the complete schematic of an artificial neuron with activation circuit. The neuron consists of five multipliers. Each multiplier receives differential inputs from the rubber sensor. The multiplier outputs are connected together. The currents from the multipliers are summed though the resistor R_{OUT}. A Bias voltage is applied for the bias setting. This bias voltage is global to the entire sheet. The activation circuit consists of two variable threshold inverters and a NOR gate. If the neuron output is between V_{REFH} and V_{REFL}, the circuit output is LOW. Otherwise, the output is HIGH meaning anomaly is detected.

During read operation, WL and BLs are same as V_{DD}. During programming, WL selects the target neuron and BLs select a target floating-gate pFET. By providing appropriate voltage levels to the WL and BL signals, selective programming of each floating-gate is achieved.

E. Scalable Memory Array

In order to realize a scalable memory array embedded in an array of neurons, access to all three terminals of a floating-gate device is required. Fig. 13(a) shows a 2T multiplier with sensor-to-voltage converter circuits. During writing and erasing operation, the n-type OFET is turned OFF and the sensor resistance is very high. As a result, Fig. 13(a) circuit is equivalent to the circuit in Fig. 13. The bias voltage is common for all the multipliers. Thanks to the CMOS based 2T multiplier circuit, a virtual memory array as shown in Fig. 14 can be realized. By appropriately choosing the voltage levels for the word lines and bit lines, each floating-gate device can be programmed selectively. The required voltage configurations to write a particular floating-gate is also shown in the figure. The experimental validation of the configurations will be demonstrated in Section IV.

IV. Experimental Results

In this section, we demonstrate the feasibility of our proposed system. We show the measurement results for each of the circuit components first. Then, neuron functionality for three different pressure conditions will be demonstrated.

A. Transistor I–V Characteristics

The transistor I–V characteristics are demonstrated first. The measured I_{DS}–V_{GS} of our fabricated p-type OFET is shown in Fig. 15. Square-power law model fitting is also

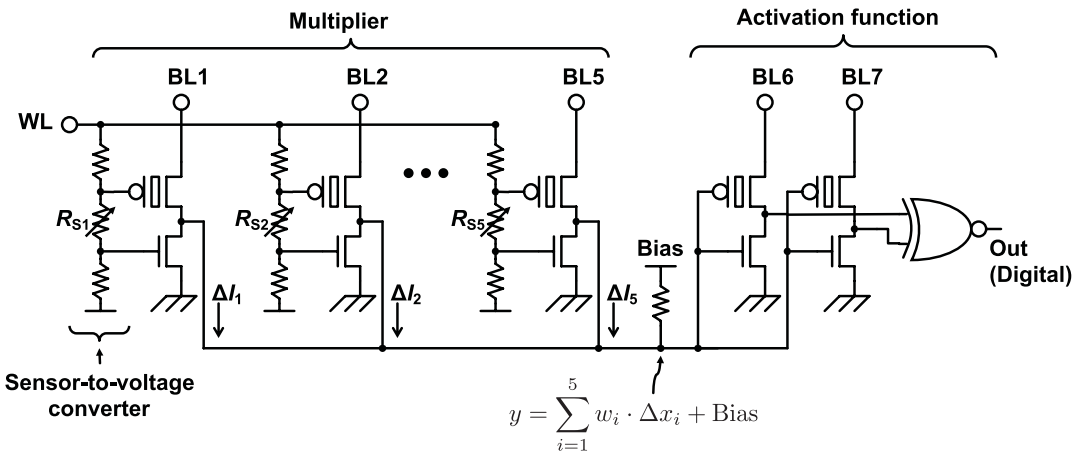


Fig. 12. Complete neuron schematic with programmable activation circuit. Output currents of the five multipliers are summed together.

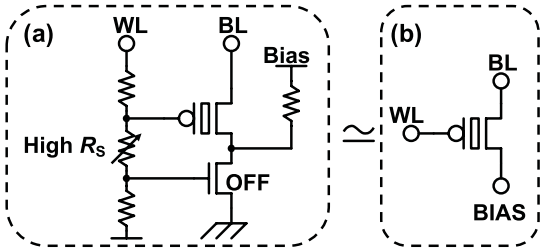


Fig. 13. Equivalent circuit to control floating-gate device terminals for selective writing and erasing.

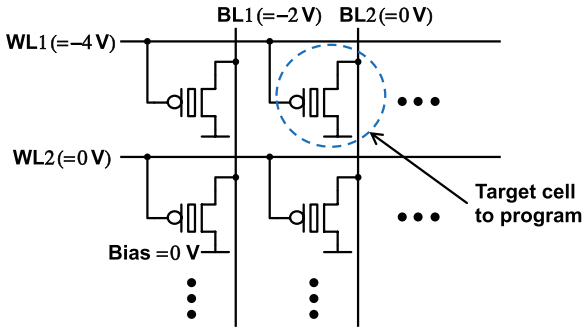


Fig. 14. Virtual floating-gate based memory array realized.

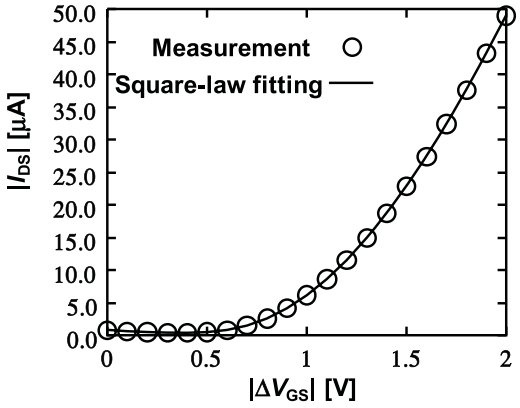


Fig. 15. Measured organic pFET ΔI_{DS}–ΔV_{GS} characteristic.

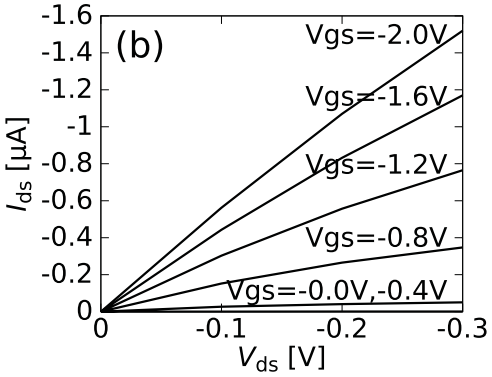


Fig. 16. Organic pFET ΔI_{DS}–V_{DS} characteristics.

shown in the figure. The square-power law model fits the I_{DS}–V_{GS} well. Next, the resistors in the system are realized by OFETs operating in small V_{DS} range. Fig. 16 shows the measured I_{DS}–V_{DS} under constant V_{GS}. I_{DS} changes linearly with V_{DS} change.

B. Multiplier Operation

Next, we demonstrate our proposed 2T multiplier which is the backbone of the whole system. Fig. 17 shows the measured ΔI_{OUT} of the multiplier cell against the differential input voltage changes. The lower X-axis shows the applied input voltage to the nFET gate and the upper X-axis shows the input voltage to the pFET gate. Y-axis shows the current difference between the pFET and the nFET. By tuning the pFET threshold voltage, V_{THP}, the output current ΔI_{OUT} either increases or decreases depending on the V_{THP} values. When $|V_{THP}|$ is low, I_{OUT} increases according the differential input increase. Whereas, when $|V_{THP}|$ is high, I_{OUT} decreases. The tangent of I_{OUT} differs which is utilized here to realize different weights. Both of the positive and negative weights are realized by V_{THP} tuning which are key characteristics for implementing analog filters.

C. Variable Threshold Inverter

Fig. 18 shows the measured voltage transfer characteristics of an inverter with a floating-gate pFET. The initial logic

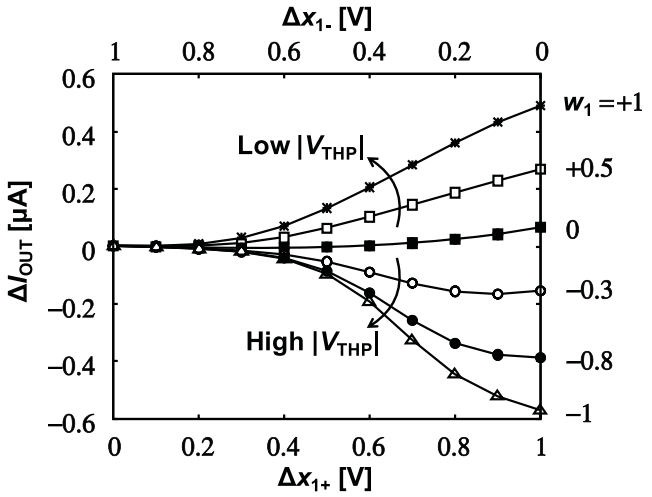


Fig. 17. ΔI_{OUT} versus gate bias change for a 2T multiplier cell.

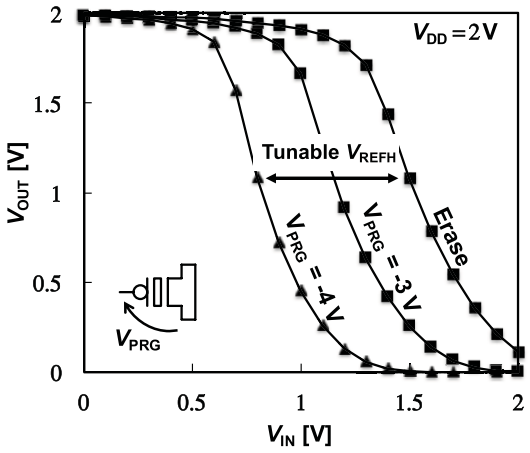


Fig. 18. Variable threshold inverter realized by floating-gate pMOS memory.

threshold before programming is around 1.6 V. Then, programming is performed by applying −3 V and −4 V between gate and source for 1 s. When programmed with −3 V, the logic threshold shifts to around 1.2 V. When programmed with −4 V after erasing the floating-gate to its initial state, the logic threshold shifts to around 0.8 V. The erase operation is performed with +3 V. The amount of threshold programming is controlled by the bias voltage and bias time [12]. Thanks to the floating-gate, a wide range of threshold values can be realized. The gain in Fig. 18 is relative low. However, it is reported that by adopting a pseudo-CMOS topology for OFETs, inverter gain can be improved significantly [4], [28].

D. Floating-Gate Programming for Scalable Array

In order to realize a scalable memory array based on organic floating-gate device, bias configurations enabling selective writing and erasing are required. As already explained in [12], gate–source voltage of −3 V or above is required to tune threshold voltage of a floating-gate pFET. Utilizing this key characteristic, we develop a scalable memory array with world lines and bit lines to selectively program floating-gate devices. For an $n \times n$ memory array, word and bit line based array

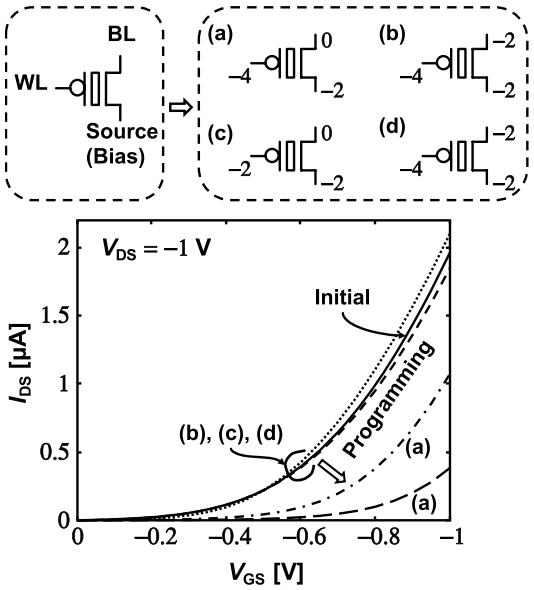


Fig. 19. Selective writing demonstration of a floating gate device in an array.

architecture reduces the number of wires from n^2 to $2 \times n$ compared with an one dimensional implementation.

Fig. 19 shows the I–V characteristics of a floating-gate pFET after four different bias configurations are applied for 1 s. The four bias configurations are shown in Fig. 19(a)–(d). With Fig. 19(a) bias conditions, gate–source voltage of −4 V is applied. As a result, the transistor V_{TH} is increased. In the plot, one curve correspond to the initial state, and two curves correspond to when −4 V is applied. Fig. 19(a) configuration is applied twice without any erase operation in between. Incremental increase in the threshold value is observed when Fig. 19(a) configuration is applied successively. Thus, as reported in [12], both the programming voltage and the programming time can use used to tune the threshold voltage. Adaptive tuning of programming voltage and programming time based on the transistor ON current reading can ensure that the target threshold voltage is achieved. Adaptive programming also has the benefit of compensating transistor to transistor variability. For the other three bias configurations, transistor I–V characteristic remains the same.

Fig. 20 shows the measured I–V characteristics of a floating-gate pFET when erasing is performed. Fig. 20(a)–(d) shows four different bias configurations. Floating-gate is erased only with the Fig. 20(a) configuration which confirms that selective erasing can be performed by tuning the bias voltages.

E. Neuron Operation

We demonstrate the feasibility of the artificial neuron operation. We apply indepenent analog voltages to each sensor pads externally instead of applying pressure on the rubber sheet. If the supply voltage and the bias voltage is set to 2 V and 1 V respectively, then the input voltage range of the sensor pads connected to pFET is $1 \sim 2$ V. The input voltage range of the sensor pads connected to nFETs is $0 \sim 1$ V. Gate voltages of pFETs and nFETs change in opposite direction according

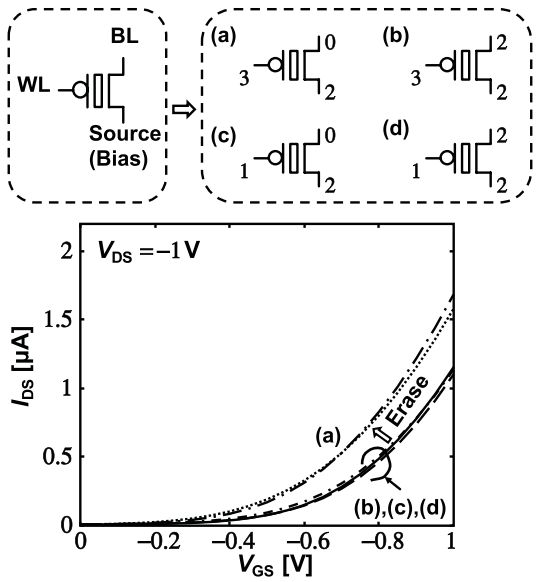


Fig. 20. Selective erasing demonstration of a floating gate device in an array.

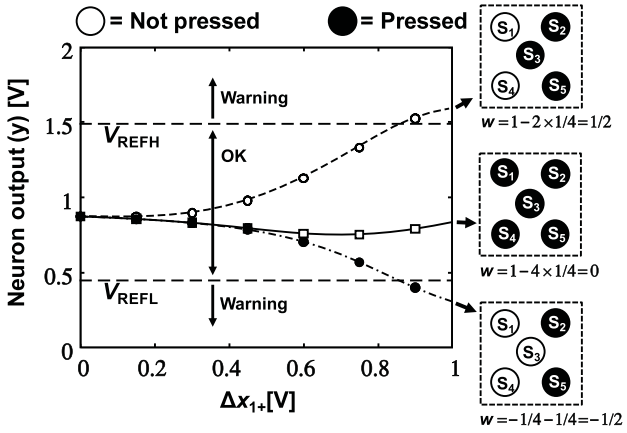


Fig. 21. System demonstration with three different pressure profiles.

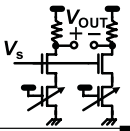
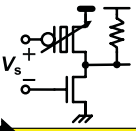
to the applied pressure. Thus, gate bias voltage relationship can be represented by

$$\Delta x_{1-} = V_{DD} - \Delta x_{1+}, \tag{14}$$

where Δx_{1+} represents nFET's gate voltage and Δx_{1-} represents pFET's gate voltage change. For simplicity, we assume that all sensors that are pressed receive the same pressure resulting in the same gate voltages.

Fig. 21 shows the neuron operation for three different scenarios. X-axis shows the change of applied gate voltage to the nFET. pFET gate voltage is applied according to (14). In the first scenario, all the sensors are assumed to have same values meaning there is no unevenness in the surface. In the second scenario, only sensors S_2 and S_5 are assumed to have pressures applied. In the third scenario, sensors S_2, S_3 and S_5 are assumed to have pressures applied. For the first case, as there is no unevenness and because of the weight assignments, the output voltage does not change much and remains within V_{REFH} and V_{REFL}. For the other two scenarios that represent uneven pressure distributions, the output voltage changes either to positive or to negative direction depending on the pressure distribution. Thus, the artificial neuron operation is confirmed.

TABLE II
COMPARISON WITH STATE-OF-THE-ART

	Conv. [8]	This work
Analog multiplier		
Transistor count	4	2 (−50%)
Non-volatile memory count	2	1 (−50%)
Scalable memory array	No	Yes
Technology	a-Si TFT nMOS	Organic TFT CMOS
Non-volatile device	Charge trap nMOS	Floating gate pMOS
Program voltage	80 V	−4 V (1/20)
Erase voltage	−80 V	+3 V

F. Comparison

Finally, we make a comparison of the proposed 2T multiplier with the one recently reported for implementing classifiers. Table II shows the comparison. The key differences are the transistor count and the number of floating-gate devices. Reducing the number of floating-gate devices and the multiplier transistor number to half is important here. The small transistor count reduces the system complexity and the number of wires required for programming. Furthermore, the CMOS based topology in our proposed multiplier enables access to the floating-gate terminals.

V. CONCLUSIONS

Embedding analog filters on top of a sensor array for local signal processing is feasible. The local processing capability makes the device intelligent and reduces the data transmission by extracting the desired pattern in the sensed signals. Transistor count is critical for organic transistor based flexible sheets as the metal layer resources are very limited. An artificial neuron is developed to detect the non-uniform interface pressure distribution that utilizes a 2-transistor multiplier topology. The multiplier topology is a CMOS circuit that multiplies the threshold voltage difference and the gate–source voltage. Organic floating-gate pFET is used as a programmable memory to realize various weights for the neuron and variable threshold inverter. A virtual floating-gate memory array is realized where word line and bit line based program architecture is developed for scalability. Thus, a programmable neuron array is realized where each neuron outputs a digital signal depending on the sensed pressure distribution. As the output is digital, signal integrity problem is avoided.

The operation of the multiplier and the neuron is demonstrated with fabricated organic transistor sheet. Measurement results show the selective programming of each floating-gate memory although the floating-gate device is embedded in a neuron circuit thanks to the CMOS multiplier. The proposed system can pave the way for versatile and smart sensor devices with large-area flexible electronics.

ACKNOWLEDGMENTS

The authors would like to thank Dr. H. Fuketa of National Institute of Advanced Industrial Science and Technology (AIST) for his advices in designing and measuring the organic transistor sheet.

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