Recent Advances in Flip-Chip Underfill: Materials, Process, and Reliability

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***Abstract*—In order to enhance the reliability of a flip-chip on organic board package, underfill is usually used to redistribute the thermomechanical stress created by the coefficient of thermal expansion (CTE) mismatch between the silicon chip and organic substrate. However, the conventional underfill relies on the capillary flow of the underfill resin and has many disadvantages. In order to overcome these disadvantages, many variations have been invented to improve the flip-chip underfill process. This paper reviews the recent advances in the material design, process development, and reliability issues of flip-chip underfill, especially in no-flow underfill, molded underfill, and wafer-level underfill. The relationship between the materials, process, and reliability in these packages is discussed.**

***Index Terms*—Flip-chip, interconnect, materials, reliability, underfill.**

I. Introduction

AS A RESULT of rapid advances in integrated circuit (IC) fabrication and the growing market for faster, lighter, smaller, yet less expensive electronic products, flip-chip has drawn tremendous attention as a first-level interconnection technique. In a flip-chip package, the active side of a silicon chip is faced down towards and mounted onto a substrate [1]. Since flip-chip was first developed about 40 years ago, many variations of the flip-chip design have been developed, among which, the Controlled Collapse Chip Connection (C4), invented by IBM in 1960s, is the most important form.[2]. The generic configuration of the C4 package is schematically shown in Fig. 1. Compared with conventional packaging using wire-bonding technology, flip-chip offers many advantages such as high I–O density, short interconnects, self-alignment, better heat dissipation through the back of the die, smaller footprint, lower profile, high throughput, etc. The outstanding merits of flip-chip have made it one of the most attractive techniques in modern electronic packaging, including multichip modules (MCM), high-frequency communications, high-performance computers, portable electronics, and fiber optical assemblies.

A major concern of flip-chip technology is the thermal mechanical fatigue life of the C4 solder joints. This thermal mechanical issue mainly arises from the coefficient of thermal expansion (CTE) mismatch between the silicon chip (2.5 ppm/°C) and the substrate (4–10 ppm/°C for ceramics and 18–24 ppm/°C for organic FR4 board). As the distance from the neutral point (DNP) increases, the shear stress at the solder joints increases accordingly. So with the increase in the chip size, the thermal mechanical reliability becomes a critical issue. Organic substrates have advantages over ceramic substrates because of their low cost and low dielectric constant, but the high CTE differences between the organic substrates and the silicon chip exert great thermal stress on the solder joint during temperature cycling. The invention of underfill was one of the most innovative developments to enable the use of low-cost organic substrate in flip-chip packages.

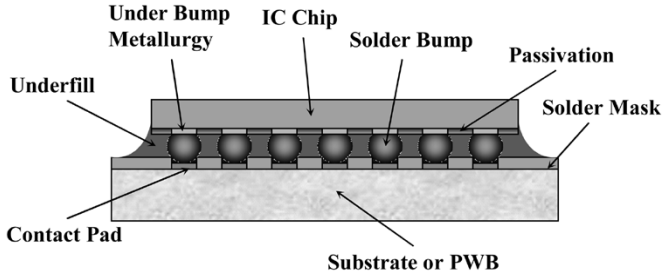

Fig. 1. Generic configuration of C4 with underfill.

Underfill is a liquid encapsulate, usually epoxy resins heavily filled with SiO_2, that is applied between the chip and the substrate after flip-chip interconnection. Upon curing, the hardened underfill exhibits high modulus, low CTE matching that of the solder joint, low moisture absorption, and good adhesion towards the chip and the substrate. Thermal stresses on the solder joints are redistributed among the chip, underfill, substrate, and all the solder joints, instead of concentrating on the peripheral joints. It has been demonstrated that the application of underfill can reduce the all-important solder strain level to 0.10–0.25 of the strain in joints, which are not encapsulated [3], [4]. Therefore, underfill can increase the solder joint fatigue life by 10 to 100 times. In addition, it provides an environmental protection to the solder joint. Underfill becomes the practical solution to extending the application of flip-chip technology from ceramics to organic substrates and from high-end to cost sensitive products. It is the main reason why flip-chip is so popular today.

II. Conventional Underfill

The advances of flip-chip technology have driven the development of both underfilling processes and underfill materials. Fig. 2 schematically shows the process steps of flip-chip with conventional underfill. Separate flux dispensing and cleaning steps are required before and after the assembling of the chip, respectively. After the chip is assembled onto the substrate, the underfill is dispensed and is dragged into the gap between the chip

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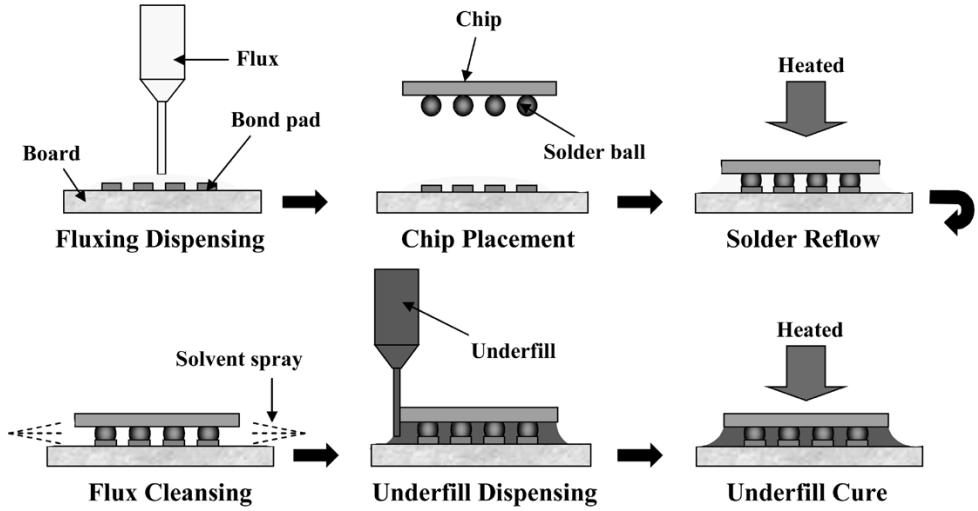

Fig. 2. Flip-chip process using conventional underfill.

and the substrate by capillary force. The capillary flow is usually slow and can be incomplete. It produces voids in the packages and also nonhomogeneity in the resin/filler system. The curing of the underfill usually takes a long time in the oven, consuming additional manufacturing time. As the gap distance gets smaller, flux cleaning becomes difficult. The incompatibility of the underfill and flux residual creates interfacial problems in the package and lowers the reliability [5]. According to the analytic study on the flow of underfill, the time required to fill a chip of length L can be calculated as [6]

$$t_{\text{fill}} = \frac{6\eta L^2}{\sigma h \cos\theta} \tag{1}$$

where η is the underfill viscosity, σ is the coefficient of the surface tension, θ is the contact angle, and h is the gap distance. Hence, the problems mentioned above aggravate further with the increase in chip dimensions and I/O counts and decrease in gap distance and pitch sizes.

In order to address the problems associated with conventional underfill, various process improvements have been invented. The pressurized underfill encapsulation utilizes a special mold to surround the flip-chip assembly [7], [8]. The underfill is injected into the mold cavity at an elevated pressure and elevated temperature, either through a mold inlet or a substrate hole. Studies showed that the pressurized underfill shortens the filling time by two or three orders of magnitude compared with the conventional dispensing process. Fig. 3 shows a schematic of the pressurized underfill encapsulation.

Fig. 4 shows the schematic of the vacuum-assisted underfill process [9]. Somewhat similar to the previous invention, a shroud device is used which defines a vacuum chamber. The dispensing device is positioned close to the gap of the chip and the board, and the flow of underfill is assisted by the vacuum applied. The application of vacuum also helps to produce a voidless underfill layer for high reliability.

In addition to pressure and vacuum, the gravity of underfill itself can be utilized to assist the underfill flow. In an invention illustrated by Fig. 5, one end of the substrate is elevated to position the flip-chip assembly on an inclined plane. The underfill is dispensed at the elevated end, and at the other end, a barrier can be used to prevent the overflow and spreading of the underfill [10].

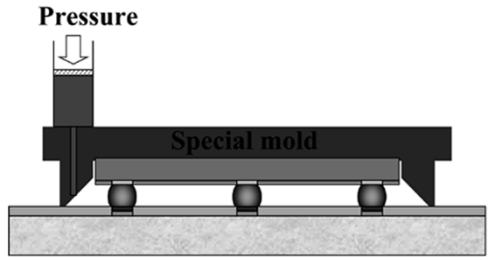

Fig. 3. Schematic of pressurized underfill encapsulation.

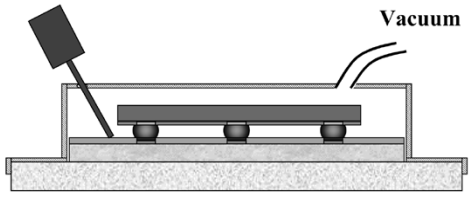

Fig. 4. Schematic of vacuum-assisted underfill process.

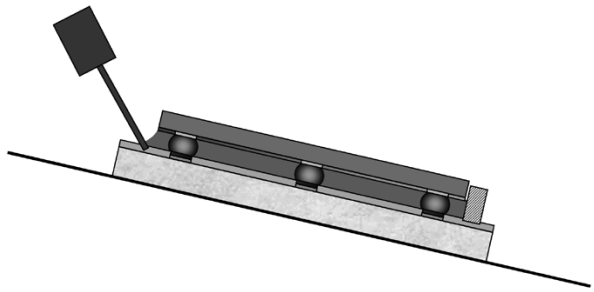

Fig. 5. Schematic of raised-die underfill.

Conventional capillary underfill is usually dispensed on one side of the chip in a line, or two sides of the chip is an L shape to prevent the entrapment of air. In a unique design showed in

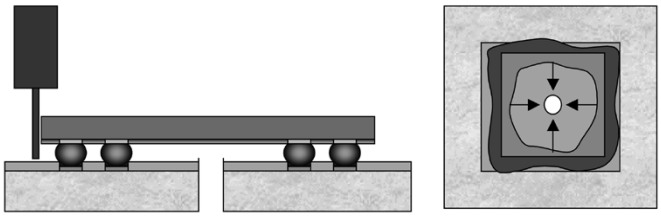

Fig. 6. Schematic of underfill with a substrate hole.

Fig. 6, a hole is drilled in the center of the substrate. The underfill is dispensed around the entire perimeter of the semiconductor die, flowing towards the center of the die and expelling any trapped air through the substrate hole [11]. Such a design not only reduces underfilling time but also helps to avoid voiding and to create a uniform fillet.

The previous approaches were invented to improve the conventional underfill process. However, they were not widely adopted by industry. Nevertheless, these ideas are creative, and they contribute to the recent advances in the flip-chip underfill process. These recent advances include no-flow underfill, molded underfill, and wafer-level underfill.

III. No-Flow Underfill

The idea of integrated flux and underfill was patented by Pennisi *et al.* at Motorola back in 1992 [12]. It triggered the research and development of the no-flow underfill process. The first no-flow underfill process was published by Wong *et al.* in 1996 [13]. The schematic process steps are illustrated in Fig. 7. Instead of underfill dispensing after the chip assembly in the conventional process, in a no-flow underfill process, the underfill is dispensed onto the substrate before the placement of the chip. Then, the chip is aligned and placed onto the substrate and the whole assembly goes through solder reflow, where the interconnection through solder balls is established while the solder melts. This novel no-flow process eliminates the separate flux dispensing and flux cleaning steps, avoids the capillary flow of underfill, and finally combines the solder bump reflow and underfill cured into a single step, hence, improving the production efficiency of underfill process. It is a step forward for the flip-chip to be compatible with surface mount technology (SMT).

The key to the success of a no-flow underfill process lies in the underfill material. The first patent on the no-flow underfill material was by Wong and Shi at the Georgia Institute of Technology [14]. The two critical properties of the no-flow underfill to enable this new process are the latent curing ability and the build-in fluxing capability. The nature of the no-flow underfill process requires that the underfill has enough reaction latency to maintain its low viscosity until the solder joints are formed. Otherwise, gelled underfill would prevent the melting solders from collapsing onto the contact pads, resulting in low yield of solder joint. On the other hand, elimination of the post cure is desired since post cure takes additional offline process time, adding to the cost of this process. Many latent catalysts for epoxy resins have been explored for the application of no-flow underfill. In the material system that Wong and Shi designed, Co(II) acetylacetonate was used as the latent catalyst [15], [16], which gave enough curing latency for no-flow underfill. The advantage of metal chelates lies not only in its latent acceleration but also in the wide curing range they offer. By exploring different metal ions and chelates, the curing behavior of different epoxy resins could be tailored to the application of no-flow underfill for lead-free solder bumped flip-chip [17]. Since lead-free solders usually have a higher melting point than eutectic SnPb solder, no-flow underfill for lead-free bumped flip-chip requires higher curing latency to ensure the wetting of the lead-free solder on the contact pad. Zhang *et al.* explored 43 different metal chelates and developed no-flow underfill compatible with lead-free solder reflow [17]. A successful lead-free bumped flip-chip onboard package using the no-flow underfill process has been demonstrated [18].

Despite the importance of the curing process of no-flow underfill, there is little study on the curing kinetics and its relation to the reflow profile. In an attempt to develop a systematic methodology to characterize the curing process of no-flow underfill, Zhang *et al.* used an autocatalytic curing kinetic model with temperature-dependent parameters to predict the evolution of degree of cure during the solder reflow process [19]. Effort was made to obtain the viscosity of the no-flow underfill curing the reflow process by Wong *et al.* using the correlation of the viscosity to the degree of cure [20]. Another approach is the *in-situ* measurement of viscosity of no-flow underfill using microdielectrometry by Morganelli *et al.* [21]. Since the viscosity is related to the ionic conductivity, the dielectric properties of the underfill can be used for the *in-situ* analysis of the no-flow underfill in the reflow process, which can be used to predict the solder wetting behavior.

The other key property for no-flow underfill is the fluxing capability. In a conventional flip-chip process, flux is used to reduce and eliminate the metal oxide on the solder and to prevent it from being reoxidized under high temperature. Instead of applying flux, no-flow underfill is dispensed before the chip placement. Hence, the self-fluxing capability is required to facilitate solder wetting. To achieve this goal, research has been done to develop reflow-curable polymer fluxes [22]. A comprehensive study on the fluxing agent of no-flow underfill material was carried out by Shi *et al.* [23]–[25], which included the relationship between the surface composite on the Cu pad and the fluxing capability of no-flow underfill, and also the effect of the addition of the fluxing agent on the curing and material properties of no-flow underfill.

The process of no-flow underfill has always attracted much attention in the assembly industry. Voids formation is often observed in many flip-chip no-flow underfill packages. The origin of the voids could be the out-gassing of the underfill, moisture in the board, trapped voids during assembly, etc. They are usually tacked to a solder bump or in between two bumps [26], [27]. Voids in the underfill, especially voids near the solder bumps, lead to early failure through a number of ways including stress concentration, underfill delaminate, and solder extrusion. Studies have shown that solder bridging might result from the solder bump extrusion through the micro voids trapped between adjacent bumps [28]. The material and process factors influencing the voiding behavior are complicated and interacting. It has been shown that the outgassing of anhydride could cause

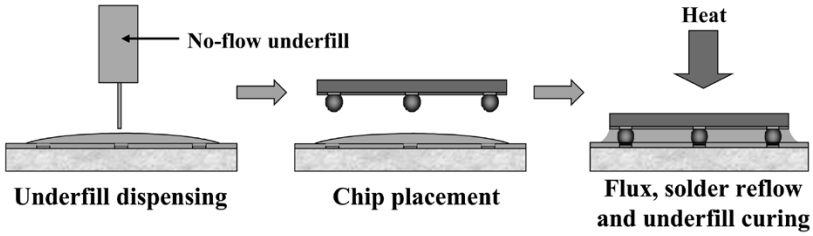

Fig. 7. Flip-chip process using no-flow underfill.

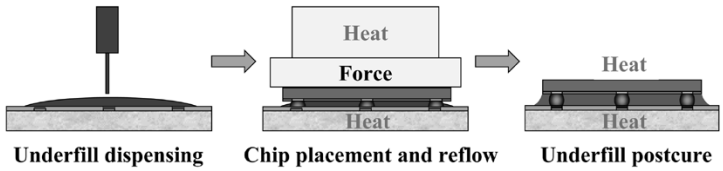

Fig. 8. Thermo-compression reflow for flip-chip.

severe voiding if the curing latency is high and also the reflow temperature is high; hence, the voiding becomes more prominent in a lead-free reflow process [29]. The important process parameters that affect underfill voiding in a no-flow process include the underfill dispensing pattern, the solder mask design, the placement force and speed, the reflow profile, etc [30], [31]. Before assembly, the printed wiring board needs to be baked to dry out any moisture to prevent voiding from the board [26]. It has been shown that in some cases, a fast gelation of underfill is desired to minimize the voiding, while in other cases, extending duration at high temperature can "push" out the voids [26], [32]. In short, with the right material and process parameters, voiding in no-flow underfill can be minimized. However, the process window is usually very narrow. An important point was raised by Zhao *et al.* [31], that for a small circuit board where the temperature distribution is more homogenous, it is relatively easy to develop a "good" reflow profile, while for complex SMT assemblies involving multiple components and significant thermal mass difference across the board, the optimization of the reflow process presents great challenge.

The reliability of flip-chip no-flow underfill package has been evaluated on many occasions. Discrepancies exist among these reports because the process and reliability of the no-flow underfill package depend largely on the package designs including the size of the chip, the pitch, the surface finish of the pad, etc. Among the earliest reporters on no-flow underfill, Gamota and Melton compared the reliability and typical failure mode of conventional underfill package and no-flow underfill package [33]. They found that in a conventional underfill assembly, the failure of the assembly mainly resulted from the interfacial delamination between the underfill and the chip passivation. However, with unfilled materials in no-flow underfill, good interfacial integrity was observed, and the assembly failed mainly due to the fracture through the solder interconnects near the printed circuit board (PCB). Since the underfill was unfilled, the CTE was high. They argued that the relative localized CTE mismatch between the chip, the underfill, and the PCB resulted in a high local stress field which initiated a fracture in the solder interconnects. No-flow underfill without silica fillers or very low filler loadings is not only high in CTE but also low in fracture toughness [34]. Combined with high CTE mismatch, the low fracture toughness leads to early underfill cracking both inside the bulk and in the underfill fillet. Fillet cracking causes delamination between the underfill and the die passivation and/or between the underfill and the board, while bulk cracking can initiate solder joint cracking and solder bridging [35]. These all become the common failure modes for flip-chip no-flow underfill package. Efforts have been made to enhance the toughness of the no-flow underfill materials through the incorporation of the toughening agents [36]. The effect of the glass transition temperature (Tg) of the no-flow underfill on the reliability of the package has been controversial. It is usually believed that the Tg of the underfill should exceed the upper limit of the temperature cycling (125 °C or 150 °C) to ensure consistent material behavior during the reliability test. However, some tests have shown that low Tg ($\sim$70 °C) underfill material performed better in liquid-to-liquid thermal shock (LLTS) [37]. The research by Zhang *et al.* on the development of non-anhydride based no-flow underfill [38] also showed that high Tg is not critical to reliability. Although the CTE of the underfill above Tg is much higher than that below Tg, the modulus of the underfill decreases dramatically; so the overall stress in the underfill does not increase when the environment temperature exceeds its Tg, but high Tg might result in a higher residue stress inside the underfill after the material cools down after curing, which leads to early cracking in the underfill.

The correlation between the material properties and package reliability in the case of flip-chip underfill is often very complicated. It is difficult to separate the effect of each factor since the material properties are often correlated with each other. The study conducted by Shi *et al.* concluded that low CTE and high modulus are favorable for high interconnect reliability [39]. Hence, the inclusion of silica fillers into the underfill is critical to enhance the reliability. However, since the underfill is predeposited on the board before the chip assembly in a no-flow process, the fillers are easily trapped in between the solder bump and contact pad and hinder the interconnection [40]. Thermo-compression reflow (TCR) has been used to exclude the silica filler from the solder joint [41]. The process step is illustrated in Fig. 8. In a TCR process, the underfill is dispensed on to a preheated substrate. The chip is then picked

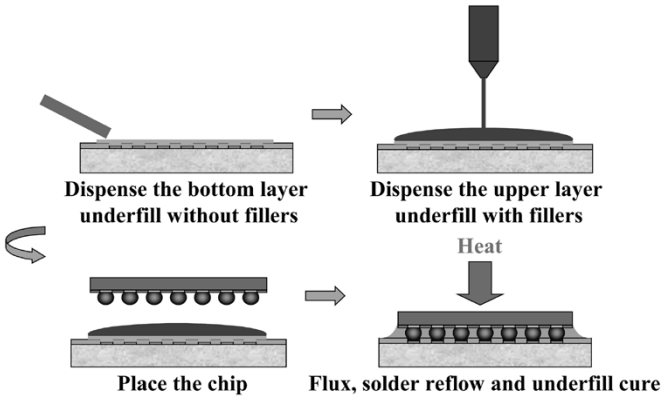

Fig. 9. Double-layer no-flow underfill process.

and bonded to the substrate and held at an elevated temperature under force for a certain period of time for solder joint formation. The assembly is post-cured afterwards. It was found that the bonding force and temperature were important factors influencing yield. In a similar process, Noro *et al.* used preset underfill sheet material in the flip-chip assembly [42]. The underfill sheet can overcome some disadvantages of the liquid underfill materials such as long dispensing time and difficult handling, etc. The high viscosity of the underfill sheet requires a bonding force and elevated temperature. It seems that with the TCR process, high silica-loaded underfill can be used to achieve good reliability. However, this process requires special bonding equipment and is not a standard SMT procedure.

Other approaches have been explored to incorporate silica fillers into no-flow underfill. In a novel patented process, Zhang *et al.* used a double-layer no-flow underfill [43], in which two layers of no-flow underfill are applied. The bottom layer underfill is relatively high in viscosity and is not filled with silica fillers. It is applied onto the substrate first; then the upper-layer underfill, which is filled with silica fillers, is dispensed. The chip is then placed onto the substrate and reflowed, during which the solder joints are formed and the underfill is cured or partially cured. The process flow chart is illustrated in Fig. 9. It was demonstrated that high yield was achieved using upper layer underfill of 65 wt% silica filled [44]. Further investigation in the process indicated that factors affecting the interconnection yield of the double-layer no-flow underfill are complicated and interacting with each other [45]. The process window is narrow and the thickness and the viscosity of the bottom layer underfill are essential to the wetting of the solder bumps, and of course, it adds another step in the flip-chip process and, in turn, disfavors the low-cost goal.

The recent advances in nanoscience and nanotechnology have enabled innovative research in materials for electronic packaging. It was found that nano-sized silica fillers with surface modifications can be mixed with thermosetting resins to provide a uniform dispersion of nonagglomerated particles. Used as no-flow underfill, the nano-composite materials allowed 50 wt% filler loading with good interconnect yield [46]. This high performance no-flow underfill developed by 3M used 123 nm silica filler. With filler loading of 50 wt%, the CTE of the material was 42 ppm/°C, and the interconnect yield using PB10 die (5×5 mm, 64 peripheral bumps) was 100%. The nanocomposite no-flow underfill material shows good potential for a highly reliability flip chip package using the no-flow underfill process.

In summary, the invention of no-flow underfill greatly simplifies the flip-chip underfill process and draws flip-chip towards SMT. A successful no-flow underfill process requires careful investigation on the materials and process parameters. A lot of research efforts have been devoted to the materials, process, and reliability of flip-chip no-flow underfill assembly. Since the underfill does not contain silica filler and, hence, behaves differently from the conventional underfill, the failure modes and reliability concerns are sometimes also different from the conventional flip-chip underfill assembly. There are several ways to enhance the reliability of a flip-chip no-flow underfill package. One way is to enhance the fracture toughness of the underfill without degrading other material properties to prevent underfill cracking in the thermal cycling. Also, low Tg and low modulus materials have been used to decrease the stress in the underfill. However, this approach diminishes the role of the underfill as a stress redistribution layer, and although it does decrease the stress in underfill, it cannot prevent solder joint fatigue failure from the thermomechanical stress, especially in the case of the large chip, high I/O count, and small pitch size applications. The other way is to add silica fillers into the underfill and march the properties of a conventional underfill. In order to overcome the difficulty of filler entrapment, different approaches have been explored. However, these approaches are less SMT-transparent and diminish the low-cost purpose of a no-flow underfill process. The great potential of no-flow underfill technology lies in the nanotechnology. The nanosilica-filled underfill with 50 wt% filler loading showed compatible CTE and allowed solder joint formation without filler interference.

IV. Molded Underfill

Epoxy molding compounds (EMCs) have been practiced in component packaging for a long time. The novel idea of combining over-molding and the underfill together results in a molded underfill [47], [48]. Molded underfill is applied to a flip-chip in package via a transfer molding process, during which the molding compound not only fills the gap between the chip and the substrate but also encapsulates the whole chip [49]. It offers the advantages of combining the underfilling and transfer molding into one step for reduced process time and improved mechanical stability [50]. It also utilizes EMCs which have long been proven to provide superior package reliability. Compared with the conventional underfill which is usually filled with silica at around 50 wt%, molded underfill can afford a much higher filler content, up to 80 wt%, which offers a low CTE close that of the solder joint and the board. Also, compared with the conventional molding compound, molded underfill requires fillers in smaller size, which also can contribute to lower the CTE of the material [51]. Molded underfill is especially suitable for flip-chip in package to improve the production efficiency. It was reported that a four-fold production rate increase can be expected using molded underfill versus a conventional underfill process [52].

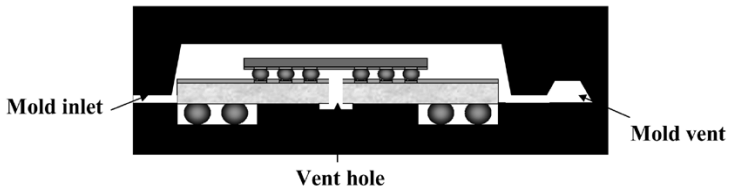

Fig. 10. Design of flip-chip BGA with molded underfill.

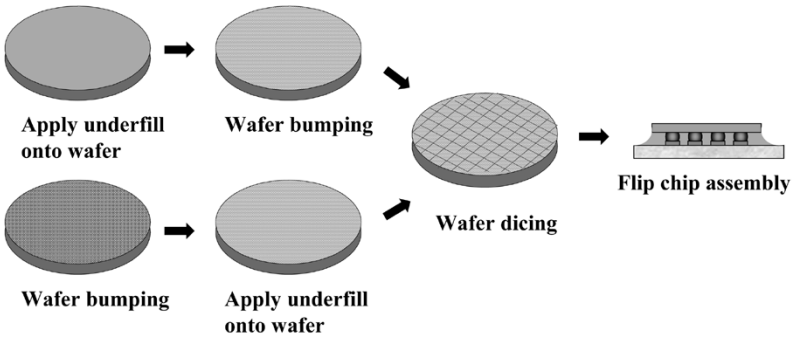

Fig. 11. Process steps of wafer-level underfill.

Molded underfill resembles the pressurized underfill encapsulation [8] in the mold design and process except that the materials in use are not liquid encapsulants that only fill up the gap between the chip and the substrate, but rather molding compounds that over-mold the entire components. Fig. 10 shows a design of the mold for flip-chip ball grid array (FCBGA) components using molded underfill.

The design of the mold faces the challenge that the flip-chip geometry has a higher resistance to the mold flow so that air might be trapped under the chip. In fact, voids have been observed in the molded underfill packages using an acoustic microscope [53]. Several molding processes can be used to minimize this geometry effect [54]. One way is to use mold vents as shown in Fig. 10, and to also use geometrical optimization to create similar flow resistance over and under the chip. One can also use vacuum assisted molding to prevent air entrapment. Another approach is to design a cavity in the substrate, as shown in Fig. 10. Though it requires a special design on the substrate, this method has proved to be a robust process and is commonly adopted.

Important process parameters in a molded underfill process include the molding temperature, clamp force, and injection pressure [53]. High-temperature molding is favored for lower viscosity of the molding compound and, hence, better flow properties and less stress on the solder joint. However, the upper limit of the molding temperature is the melting point of the solder material. Temperature near the melting temperature (Tm) combined with high injection pressure might cause the solder to melt and even the die to be "swept" away from the site. Also, the low Tg substrate is likely to be damaged at high molding temperature and high clamp force. Flash is affected by both the clamp force and the injection pressure. The overflow of the molding compound might contaminate other contact pads or testing pads on the substrate. Bump cracking and die cracking are likely to occur as a result of high injection pressure. In short, a successful molded underfill process requires a combined effort in material selection, mold design, and process optimization, but the potential cost reduction and reliability enhancement of molded underfill is attracting great efforts in the industry.

V. Wafer-Level Underfill

The invention of no-flow underfill eliminates the capillary flow and combines fluxing, solder reflow, and underfill curing into one step, which greatly simplifies the underfill process. However, as pointed out in Section III, no-flow underfill has some inherent disadvantages, including the unavailability of a heavily filled material, which is a big concern for high reliability. Also, the no-flow process still needs an individual underfill dispensing step and, therefore, is not totally transparent to standard SMT facilities. An improved concept, wafer-level underfill, was proposed as an SMT-compatible flip-chip process to achieve low cost and high reliability [55]–[58]. The schematic process steps are illustrated in Fig. 11. In this process, the underfill is applied either onto a bumped wafer or a wafer without solder bumps using a proper method, such as printing or coating. Then the underfill is B-staged and the wafer is diced into single chips. In the case of unbumped wafer, the wafer is bumped before dicing when the underfill can be used as a mask. The individual chips are then placed onto the substrate by standard SMT assembly equipment.

One clarification is needed to distinguish between the flip-chip with wafer-level underfill and wafer-level chip scale packaging (WLCSP). In recent years, a great variety of WLCSP has been developed to lower the cost of CSP. In most cases, a polymeric layer was applied on the wafer to redistribute the I/O and/or to enhance the reliability. However, this polymeric layer usually does not glue with the substrate and cannot be considered as an underfill. The wafer-level underfill discussed in the current paper is an adhesive to glue the chip and substrate together and functions as a stress-redistribution layer rather than a stress-buffering layer. Unlike WLCSP, which is mainly for low

I/O customer products, the wafer-level underfill is targeted at large wafers with high I/O counts and small bump pitch to provide a low-cost solution to highly reliability flip-chip packaging, especially for high-end products.

The attraction of the potential low cost and high reliability of the wafer-level underfill process has encouraged extensive research in this area. Since this process suggests a convergence of front-end and back-end in package manufacturing, close cooperations between chip manufacturers, packaging companies, and material suppliers are required. Several programs have been carried out by the cooperated research in this area, including the team comprising Motorola, Auburn University, and Loctite Electronic Materials sponsored by National Institute of Standards and Technology Advanced Technology Program (NIST-ATP) [59], the team comprising National Semiconductor, IBM, National Starch and Chemical Company, and the Georgia Institute of Technology, also sponsored by NIST-ATP [60], and the team comprising 3M and Delpi-Delco Electronic Systems [61].

The material and process challenges for wafer-level underfill have been identified and can be summarized by the following. First, a robust underfill deposition process is required; the resulted underfill layer must be of sufficient uniformity and consistency to enable a high yield in the assembly process, good solder joint formation, and an acceptable underfill fillet [59]. Different deposition processes have been explored including spin coating, vacuum lamination, screen printing, and stencil printing, etc. The underfill needs to be B-staged if the original form is liquid to facilitate the later handling, including dicing and storage. One method is to use solvent in the deposition process and then drive off the solvent to B-stage the underfill. However, the use of an unreactive solvent might leave residue which is likely to cause voiding during the later assembly [62]. Partial cure can be used with careful control of the curing degree that does not interfere with solder joint formation in the solder reflow. Wafer dicing presents another challenge for the underfill since the uncured material would be exposed to water that is used for cooling. If the wafer is to be diced with the underfill, the material also needs a good mechanical property to prevent cracking. Unlike liquid underfill that is usually freeze-stored, wafer-level underfill requires a long shelf-life for packing, shipping, and storage of the dies. Fortunately, B-staged material usually has the glass transition temperature above room temperature, at which the mobility of the molecules is low to prevent large-scale reactions [62].

The issues related to the wafer-level underfill in the assembly process start with the vision recognition at the placement machine. Normally, either fiducials or solder bumps on the die are located using the vision system in a pick-and-place equipment for flip-chip bonding alignment. Being covered by the underfill that is often heavily filled and, hence, translucent, these marks are difficult to recognize. Fortunately, many placement machines can adjust the illumination angle, light intensity, and image acceptance transforms, etc., to optimize imaging [63]. The coating color can also be adjusted to enhance the recognition. Some work has shown that a black color provides the best contrast to the coated bumps [64]. If no additional flux is to be dispensed on the board, the wafer-level underfill has to provide some tackiness to hold the chip in place. Several methods have been proposed including heating the board, heating the chip in a separate station, and heating the underfill through the pick-up nozzle [59]. Similar to no-flow underfill, a self-fluxing capability is required to eliminate the flux dispensing process. However, flux is known to degrade the stability of epoxy-based systems and shorten the shelf-life of the wafer-level underfill. Hence, unlike no-flow underfill, wafer-level underfill usually contains separating materials with different functions to achieve the desired result [65]. The solder wetting process with a wafer-level underfill presents challenges to high interconnect yield because the wetting is constrained by the presence of the partially cured underfill. Numerical simulation has been performed to predict the solder joint formation under constrained boundaries [66]. Similar to the no-flow underfill process, the solder joint interconnection is highly dependent on the fluxing capability and the viscosity of the underfill. However, it was found that the wetting process could be complicated by underfill outgassing and chip motion driven by forces other than surface tension of the solder [67]. The thickness of the underfill coating was critical for an optimal solder joint formation; deficiency in underfill could result in a gap between the bumps, and excess underfill would hinder the solder joint formation [59]. Other issues such as the desire for no post cure and reworkability are being addressed as well in the wafer-level underfill process.

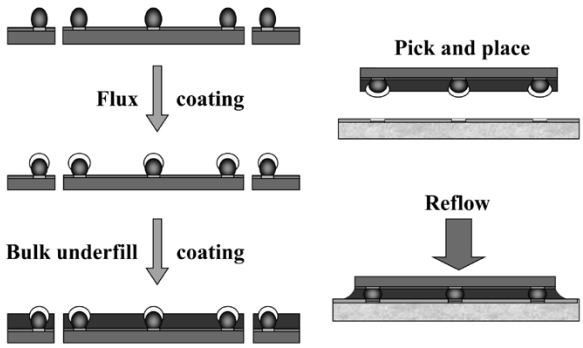

Fig. 12. Wafer-scale applied reworkable fluxing underfill process.

In order to address the previous challenges, different wafer-level underfill processes and the corresponding materials have been developed by various research teams, each providing unique solutions to the issues mentioned above. Illustrated in Fig. 12 is the wafer scale applied reworkable fluxing underfill process developed by Motorola, Loctite, and Auburn University [59], [65]. Since uncured underfill materials are likely to absorb moisture that leads to potential voiding in the assembly, in this process, the wafer is diced prior to underfill coating. Two dissimilar materials are applied: the flux layer coating by screen or stencil printing and the bulk underfill coating by a modified screen printing to keep the saw street clean. The separation of the flux from the bulk underfill material preserves the shelf life of the bulk underfill as well as prevents the deposition of fillers on top of the solder bump so as to ensure the solder joint interconnection in the flip-chip assembly. In this process, no additional flux dispensing on board is needed, and, hence, the underfill needs to be tacky in the flip-chip bonding process to ensure the attachment of the chip to the board.

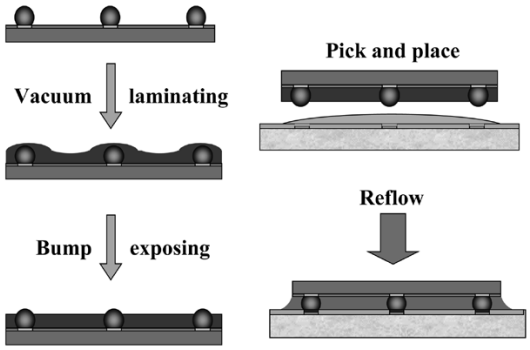

Fig. 13. Wafer-applied underfill film laminating process.

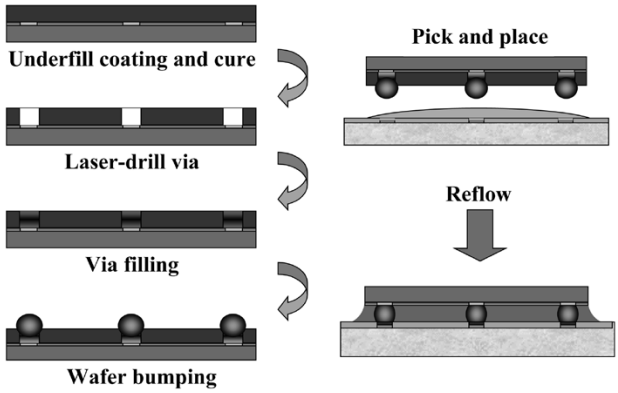

Fig. 14. Multilayer wafer-scale underfill process.

Underfill deposition on a wafer using liquid material via coating or printing requires subsequent B-staging, which is often tricky and problematic. The process developed by 3M and Delphi-Delco circumvents the B-stage step using film lamination [68]. The process steps are shown in Fig. 13, in which the solid film composed of thermoset/thermoplastic composite is laminated onto the bumped wafer in a vacuum. Heat is applied under vacuum to ensure the complete wetting of the film over the whole wafer and to exclude any voids. Then, a proprietary process is carried out to expose the solder bump without altering the original solder shape. The subsequent flip-chip assembly is carried out in a no-flow underfill-like process in which a curable flux adhesive is applied on the board and then the assembly is reflowed.

Wafer-level underfill can also be applied before the bumping process. Fig. 14 shows a multilayer wafer-scale underfill process developed by Aguila Technologies, Inc. [69]. The highly filled wafer-level underfill is screen printed onto an unbumped wafer and then cured. Then, this material is laser-ablated to form microvias that expose the bond pads. The vias are filled with solder paste and reflowed. Bumps are formed on top of the filled vias. The flip-chip assembly is similar to the no-flow underfill process, again, with a polymer flux dispensed onto the board before chip placement.

One similarity among all these three processes is the separation of flux material from the bulk underfill. The wafer-level underfill process provides the convenience of separating different functionalities by using dissimilar materials so that "the one magic material that solves everything" is not required. However, it is likely to create inhomogeneity inside the underfill layer, the impact of which on the reliability is not fully understood. Since wafer-level underfill is a relatively new concept, and most research is still in the process and material development stage, there are few reports on the reliability of a flip-chip package using wafer-level underfill. Although there is no standard process for wafer-level underfill yet, the final decision might depend on the wafer and chip size, bump pitch, and package type, etc. Like wafer-level CSP, multiple solutions can co-exist for the wafer-level underfill process.

VI. Summary

Flip-chip offers many advantages over other interconnection technologies and is practiced in many applications. Underfill is necessary for a reliable flip-chip on organic package but is process-unfriendly and becomes the bottleneck to a high production flip-chip assembly. Many variations of the conventional underfill have been invented to address the problem, among which, the newly developed no-flow underfill, molded underfill, and wafer-level underfill have attracted much attention. The no-flow underfill process simplifies the conventional flip-chip underfill process by integrating flux into the underfill, eliminating capillary flow, and combining solder reflow and underfill cure into one step. However, the predeposited underfill cannot contain high levels of silica filler due to the interference of the filler with solder joint formation. The resulting high CTE of the underfill limits the reliability of the package. Various ways have been explored to enhance the reliability through improved fracture toughness of the underfill material, low Tg and low modulus underfill, and the incorporation of fillers using other process approaches. Recent development of nanosilica-filled no-flow underfill showed great potential. Molded underfill combines underfill and over-mold together and is especially suitable for flip-chip in package to improve the capillary underfill flow and the production efficiency. Careful material selection, mold design, and process optimization are required to achieve a robust molded underfill process. Wafer-level underfill presents a convergence of front-end and back-end in packaging manufacturing and may provide a solution for a low cost and highly reliable flip-chip process. Various material and process issues including underfill deposition, wafer dicing with underfill, shelf-life, vision recognition, chip placement, and solder wetting with underfill, etc., have been addressed through novel material development and different process approaches. Although the research is still in the early stage, and there is no standard in the process yet, there have been considerable successes in demonstrating the process, which looks promising for the future packaging manufacturing. All of these three approaches require close cooperation between the material suppliers, package designers, assembly companies, and maybe chip manufacturers. A good understanding in both the materials and the processes and their inter-relationship is essential to achieve successful packages.

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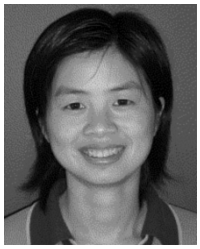

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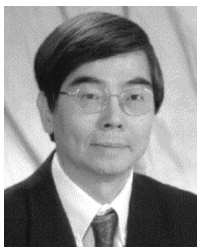

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