Design and Analysis of a High Bandwidth Rectifying Regulator With PWM and PFM Modes

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***Abstract*—We propose a novel rectifying regulator to wirelessly power a neural stimulator in 65 nm CMOS process. The regulating rectifier operates at 13.56 MHz and has two operating modes. In the high power pulse width modulation (PWM) mode, it regulates the output voltage by controlling the conduction time during every cycle of the incoming HF signal. The PWM mode is designed with a high bandwidth feedback loop to satisfy the transient time requirements of the stimulator. The rectifier also incorporates a pulse frequency modulation (PFM) mode to power the stimulator in sleep mode wherein it controls the frequency at which the rectifier conducts to efficiently deliver low output power. We present the theory and develop an analytical model for the rectifying regulator and validate the model for both PWM and PFM operating modes.**

***Index Terms*—Brain stimulation, rectifiers, regulators, wireless power transmission.**

I. Introduction

NEURAL recording and stimulation platforms have been used in recent years to reanimate limbs, enable paralyzed individual to operate prosthetic devices and effectively command electronic devices [1]. Specifically, electrocorticography (ECoG) is a class of neural signals which are recorded from and stimulated at the surface of the cerebral cortex and have been shown to be suitable for long-term usage [1]. The goal of this brief is to develop a wireless power system for a monolithic implantable neural (ECoG) recording and stimulation platform. To understand the power requirements of such systems, we first analyze the behavior of neural stimulators which dominate the power budget of neural platforms. Fig. 1 shows the time domain profile of a typical neural stimulator. A stimulation event consists of series of 100–200 μs long bi-phasic pulses spaced apart by few milliseconds in time. This stimulation event is repeated on demand every few hundreds of milliseconds [1]. The timing and the peak power requirements of the bi-phasic pulses are tailored for specific use cases. For typical applications, the peak power requirements during active stimulation can vary from 25 mW (1 mA@12 V for 50% efficient stimulator in 65 nm CMOS) to 2.5 mW (100 μA@12 V for 50% efficient stimulator in 65 nm CMOS). The key takeaway is that a typical stimulator is heavily duty cycled and quickly transitions between active and sleep mode. Hence, the wireless power system should have fast transient response and operate efficiently at both high and low output power. An efficient low power mode ensures that prolonged operation in sleep mode does not lead to tissue heating, which is highly undesirable.

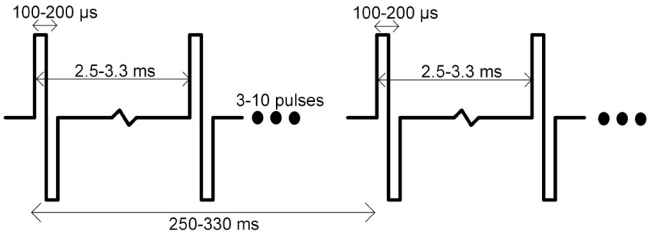

Fig. 1. Stimulation pulses corresponding to typical configuration of neural stimulators.

There are two main approaches to wirelessly power biological implants using near field. The first approach is to use an HF rectifier followed by a linear or switching dc-dc convertor. However, the cascaded system suffers from low efficiency and additional inductors required for switching convertors are prohibitive in implanted systems. Instead, a rectifier which simultaneously regulates is a popular approach to achieve high power conversion efficiency [2]–[5]. Choi *et al.* [3] introduced a 3R rectifier topology. However, this system is unsuitable for implanted systems since it requires external capacitors and diodes. Additionally, the switching frequency is low which necessitates bulky filtering capacitors and has a slow transient response. In [4], a 2 MHz active rectifier is proposed which uses a delay line as the control element in the feedback loop to regulate the output voltage. The delay line is a nonlinear block and using it in a feedback loop to control the rectifier, another nonlinear element can lead to unstable designs. Furthermore, the topology requires large decoupling capacitors, only supports high power mode and does not meet the transient requirements of stimulation platforms. Finally, recently in [5], a 1x/2x mode switching resonant rectifying regulator at 13.56 MHz has been proposed. However, this system does not support a low power mode and switches at a fraction of the operating frequency resulting in transient response on the order of 100 μs, making it unsuitable for powering neural stimulators.

In this brief, we introduce a 13.56 MHz rectifying regulator topology specifically designed to directly power a neural stimulator. The rectifying regulator operates in pulse width modulation (PWM) mode to efficiently power the stimulator in

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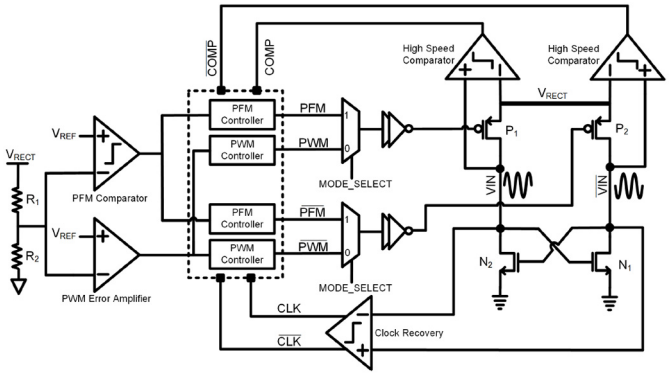

Fig. 2. Top level architecture of the rectifying regulator.

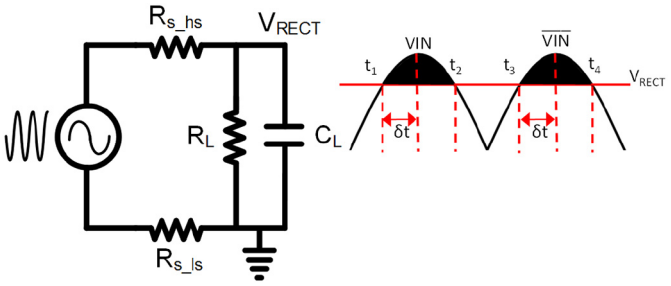

Fig. 3. Equivalent circuit for the rectifier and the associated waveform.

its active mode of operation. The PWM mode is designed with high bandwidth feedback loop to meet the transient requirements of the stimulation platform. The rectifier also has a low power pulse frequency modulation (PFM) mode to efficiently power the stimulator in sleep mode. Finally, to meet the form factor requirements of implanted neural platform, we limit the external components to one 0201 package (height similar to a silicon chip) decoupling capacitor.

An abridged version of this brief was presented in [6]. In the interest of space, in this brief we will focus on the theory, analytical modeling and architecture of the rectifying regulator. The outline of this brief is as follows. Section II provides an overview of the architecture of the rectifying regulator followed by the theory and analytical model in Section III. The design of the feedback controller and feedback loop for the PWM and PFM modes is described in Section IV. Section V presents and verifies the analytical model with simulation and Section VI concludes this brief.

II. System Overview and Architecture

The full architecture of the rectifying regulator is shown in Fig. 2. A rectifier is connected to the terminals VIN and $\overline{\text{VIN}}$ of the secondary coils (not shown) to convert the incoming HF signal into dc output power. The rectifying regulator consists of high speed comparators, clock recovery, PWM control block, PFM control block, rectifier switches, and level shifters and buffers to drive the switches. We implement a full bridge active rectifier with cross coupled nMOS transistors (N_1 and N_2) as the low side switches and pMOS based active diode as high side switches. The high frequency comparator is used for active rectification, i.e., the rectifier only conducts when the input voltage is greater than the output voltage. The details on the basic operation of an active rectifier can be found in prior works [2], [4], [5].

We design the rectifying regulator in TSMC 65 nm GP CMOS process to output a 2.5 V voltage rail. The control circuitry such as the feedback loop and clock generator are powered from a 1.0 V supply rail. The 1.0 V supply chain consumes minimal power and can derived from the 2.5 V rail using a low-dropout. Using a lower independent supply rail minimizes static power consumption and mitigates startup issues [5]. The rectifying regular has two modes of operation. In the high power PWM mode, the feedback loop controls the conduction time of the rectifier during every cycle of the input signal to regulate the output voltage. Every conduction cycle is associated with switching losses and at high output power, the switching losses are small and the power conversion efficiency is high. However, when the output power is low, the switching losses are comparable to the output power and the efficiency drops. To ensure high efficiency at low load currents, we design a PFM mode of operation where instead of conducting every cycle, the rectifier modulates the frequency at which it conducts to regulate the output voltage.

III. Theory and Modeling of Rectifiers

In this section, we develop an analytical model for the operation of the rectifying regulator. Let R_{s_hs} and R_{s_ls} be the resistance of the high side and the low side switch, respectively. For an input sinusoidal voltage of $V_0 \sin(\omega_0 t)$, the rectifier can be represented with the equivalent circuit model shown in Fig. 3. Here, R_L represents the load and C_L is the decoupling capacitor. In the steady state, the output voltage V_{RECT} is constant and the total charge delivered to the output during each time period can be written as

$$Q_{\text{out}} = \int_0^T I_L dt = \frac{V_{\text{RECT}} T}{R_L}. \tag{1}$$

Typically, the active rectifier conducts as long as the input voltage is greater than the output. This corresponds to time instance between t_1 and t_2 in the positive cycle and t_3 and t_4 in the negative cycle as shown in Fig. 3. This corresponds to the traditional operation of active rectifiers. However, the rectifier can modulate its conduction period during each switching cycle (PWM mode) or the rate at which it conducts (PFM mode) to simultaneously rectify and regulate the output voltage.

A. PWM Mode

The rectifier starts conduction at time t_1 for a period δt during the positive cycle and at time t_3 for a period of δt during the negative cycle. The total charge supplied by the input voltage source in both negative and positive conduction cycle can be written as

$$Q_{\text{in}} = 2 \int_{t_1}^{t_1+\delta t} \frac{V_0 \sin(\omega_0 t) - V_{\text{RECT}}}{R_s} dt \tag{2}$$

$$= \frac{2V_0}{R_s \omega_0} [\cos(\omega_0 t_1) - \cos(\omega_0 (t_1 + \delta t))] - \frac{2V_{\text{RECT}} \delta t}{R_s} \tag{3}$$

where $R_s = R_{s\_hs} + R_{s\_ls}$ is the switch resistance. In steady state, using the principle of conservation of charge, we can equate the charge from the input to the charge supplied to

the load in one-time period. The output voltage can be now represented as

$$V_{\text{RECT}} = \frac{2V_0R_L}{\omega_0[R_sT + 2R_L\delta t]}(\cos\omega_0 t_1 - \cos\omega_0(t_1+\delta t)) = \frac{2R_L}{\omega_0(R_sT+2R_L\delta t)}\left[\sqrt{V_0^2 - V_{\text{RECT}}^2}(1-\cos\delta t) + V_{\text{RECT}}\sin\delta t\right]. \quad (4)$$

The above equation shows that the output voltage V_{RECT} is a function of the conduction time δt and by modulating the conduction time δt, the rectifier can regulate the output voltage independent of the input voltage V_0 and the load R_L.

To design a feedback loop to modulate δt, first we need to determine the transfer function of the rectifier. The dc gain of the rectifier block with input δt and output V_{RECT} can be computed as $(\partial V_{\text{RECT}}/\partial\delta t)$ and is shown in (13), as shown at the bottom of the next page. Note that this equation is quite complex but can be numerically computed and the result for $V_0 = 3.0\ V$ is shown in Fig. 4.

In the PFM mode, the power conversion efficiency can be written as

$$\eta_{\text{PWM}} = \frac{P_{\text{out}}}{P_{\text{in}}} \quad (5)$$

$$= \frac{V_{\text{RECT}}^2/R_L}{P_{\text{cond}} + P_{\text{switch}} + P_{\text{static}}} \quad (6)$$

where $P_{\text{cond}} = 2\int_{t_1}^{t_1+\delta t} V_0\sin(\omega_0 t)((V_0\sin(\omega_0 t) - V_{\text{RECT}})/R_s)dt/T$ is the conducted power from the source and takes into account the conduction losses associated with switch resistance R_s. P_{switch} represent the switching losses associated with switching P_1 and P_2 every cycle and P_{static} is the static power of the PWM controller which was 19 μW in our implementation.

B. PFM Mode

In this mode, the feedback loop controls the frequency at which the rectifier conducts. During each switching event the rectifier conducts from t_1 to t_2 in the positive cycle and t_3 to t_4 in the negative cycle. Let us assume that the rectifier conducts for one complete cycle every T_1 seconds. The charge supplied to the load in this period can be written as

$$Q_{\text{out}} = \int_0^{T_1} I_L dt = \frac{V_{\text{RECT}}T_1}{R_L}. \quad (7)$$

Similarly, the charge supplied by the input can be written as

$$Q_{\text{in}} = \int_{t_1}^{t_2} \frac{V_0\sin(\omega_0 t) - V_{\text{RECT}}}{R_s}dt \quad (8)$$

$$= \frac{V_{\text{RECT}}(t_2' - t_1')}{R_s} \quad (9)$$

where $t_2' - t_1'$ is the effective conduction period in PFM mode and can be computed as

$$t_2' - t_1' = \frac{T}{\pi}\sqrt{\frac{V_0^2}{V_{\text{RECT}}^2} - 1} - (t_2 - t_1) \quad (10)$$

$$= \frac{T}{\pi}\sqrt{\frac{V_0^2}{V_{\text{RECT}}^2} - 1} - \frac{T}{2} + \frac{2}{\omega_0}\sin^{-1}\left(\frac{V_{\text{RECT}}}{V_{\text{OUT}}}\right). \quad (11)$$

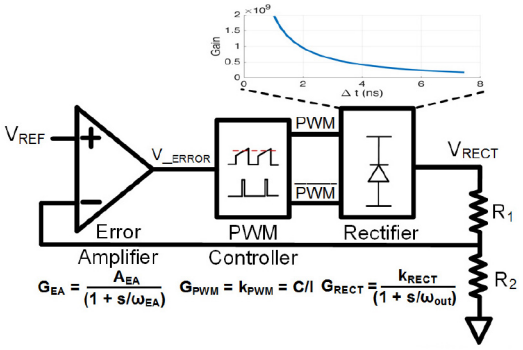

Fig. 4. Block diagram for the feedback analysis of the PWM mode.

Again using the principle of conservation of charge we can compute the switching frequency $(1/T_1)$ as

$$\frac{1}{T_1} = \frac{R_s}{R_L(t_2' - t_1')}.$$

The efficiency in the PFM mode can be written as

$$\eta_{\text{PFM}} = \frac{T_1V_{\text{RECT}}^2/R_L}{P_{\text{cond}} * (t_2 - t_1) + P_{\text{switch}} * (t_2 - t_1) + P_{\text{static}}}. \quad (12)$$

The model assumes that the rectifier conducts for only one cycle during each switching event. However, it can also be scaled for n conduction cycles for every switching event. The switching period is then nT_1 resulting in exactly the same switching frequency and efficiency, however, at the cost of higher ripple voltage. Finally, we note that the above model assumes that the comparators are perfect and have no delay. In practice there is a finite propagation delay (1–1.5 ns) and we incorporate it by adjusting the values of t_1 and t_2 while numerically computing integrals.

IV. System Architecture and Design

In this section, we describe the architecture and design of PWM and PFM mode feedback loops.

A. Pulse Width Modulation Mode

In the PWM mode, the rectifier conducts every cycle and controls the conduction period δt to regulate the output voltage V_{RECT}. The conduction period δt is set by a continuous time feedback loop consisting of a voltage divider, error amplifier and the PWM controller. The architecture of the feedback loop and the signals illustrating the PWM mode of operation are shown in Fig. 5. A voltage divider with division ratio $\beta = 5$ (for $V_{\text{ref}} = 0.5$ V) provides voltage based feedback. The feedback and reference voltage are inputs to an error amplifier. The error amplifier can be modeled with the transfer function $G_{\text{EA}} = [A_{\text{EA}}/(1 + s/\omega_{\text{EA}})]$ where ω_{EA} is the dominant pole. The secondary poles of the error amplifier are at a much higher frequency compared to the unity gain frequency of the feedback loop.

Frequency tracking is a popular technique used in near field wireless power transfer to achieve high efficiency across a range of operating distances and output power levels [7]. To ensure that the rectifier can operate across a range of input frequencies, we synchronize the control waveforms with the clock derived from the incoming HF signal. The traces and

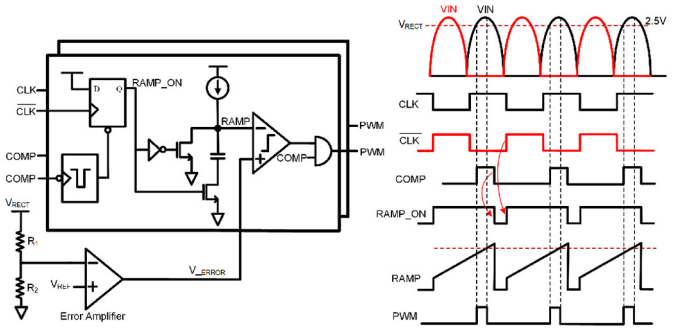

Fig. 5. Architecture of the PWM controller and the signals corresponding to the PWM mode of operation.

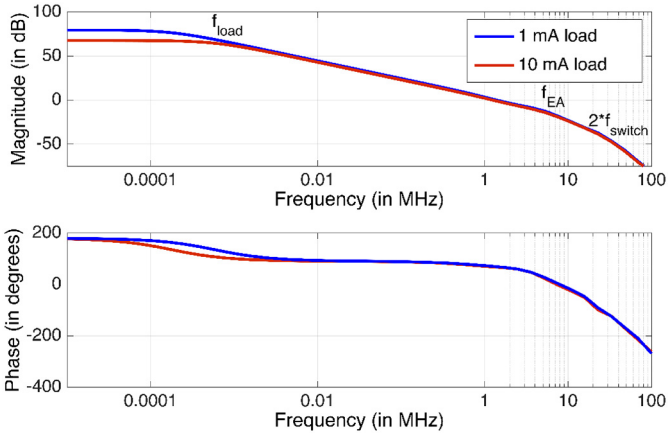

Fig. 6. Bode plots for the feedback loop of the PWM mode.

the PWM controller shown in Fig. 5 correspond to the positive cycle (VIN). To ensure that the ramp signal is at mid rail voltage levels during the conduction period, we trigger the start of the ramp signal with the positive edge of the complementary clock $\overline{\text{CLK}}$. We further improve the dynamic voltage range by using a novel ramp signal generator which kick starts the signal from a predetermined voltage instead of 0 V. During the off stage, we trap a fraction of the charge on the capacitor by disconnecting the capacitor from the ground. This charge is recycled when the ramp signal is turned on and the signal kick starts from 250 mV. Using these techniques, we can simultaneously maximize the gain and satisfy the dynamic range and timing constraints for the ramp signal. A continuous time comparator compares the ramp signal with the output of the error amplifier to generate the timing signal. This timing signal is combined with the high speed comparator output signal to generate the pulse corresponding to conduction period δt. The PWM controller can be modeled with the transfer function $G_{\text{PWM}} = k_{\text{PWM}} = C/I$ where C is the capacitor and I is the current.

The PWM mode is based on continuous mode feedback. To ensure stability across different output power levels, we develop an analytical model for the PWM control loop. The rectifier is a nonlinear element and its transfer function can be written as $G_{\text{RECT}} = [k_{\text{RECT}}/(1 + s/\omega_{\text{load}})]$ where k_{RECT} is the dc gain computed in (13) and $\omega_{\text{load}} = 1/R_L C_L$ is the pole corresponding to the output. Since we are limited to using an 0201 package decoupling cap, $C_L \leq 1\ \mu$F. Using the analytical model for the various elements, the transfer function of the PWM feedback loop can be written as

$$\frac{V_{\text{RECT}}}{V_{\text{REF}}} = \frac{G_{\text{EA}}\, G_{\text{PWM}}\, G_{\text{RECT}}}{1 + \beta\, G_{\text{EA}}\, G_{\text{PWM}}\, G_{\text{RECT}}} \tag{14}$$

$$= \frac{k_0\, \omega_{\text{out}}\, \omega_{\text{EA}}}{s^2 + s(\omega_{\text{EA}} + \omega_{\text{load}}) + (1 + \beta k_0)\omega_{\text{EA}}\, \omega_{\text{load}}} \tag{15}$$

where, $k_0 = A_{\text{EA}}\, k_{\text{PWM}}\, k_{\text{RECT}}$ is the dc gain of the feedback loop and is large enough to ensure that the error in output voltage is less than 0.1%. The model shows that the PWM feedback loop is a second order system. However, in addition to the poles shown in (14), we also have a pole corresponding to the switching frequency $2 * f_{\text{switching}} \approx 27$ MHz (positive and negative cycle). To ensure stability, first we place the gain crossover frequency a decade lower than the switching frequency. Second, we make the pole associated with the varying load the dominant pole, and move the pole of the error amplifier beyond the gain crossover point. Finally, we leverage the fact that the rectifier has high gain but lower bandwidth for low load currents whereas low gain but higher bandwidth for high load current. Using the combination of these techniques we guarantee that the gain crossover point is independent of the load current and achieve a phase margin of 70° across load currents of 1 to 10 mA with a unity gain bandwidth of 1 MHz. The phase and magnitude bode plots for the PWM feedback loop computed using periodic steady state response are shown in Fig. 6.

B. Pulse Frequency Modulation Mode

In the PFM mode, instead of controlling conduction cycle, the feedback loop modulates the rate at which conduction occurs. To maximize efficiency, during each switching action, the rectifier conducts for the entire cycle ($\delta t = t_2 - t_1$). By conducting for the entire cycle, we extract the maximum available energy for the energy consumed in each switching event. The architecture of the PFM control module and the signals illustrating the PFM mode of operation are shown in Fig. 7. A static comparator continuously monitors the output voltage and activates a switching cycle when the output drops below the 2.5 V (with a 15 mV hysteresis) threshold. When the output of the comparator PFM_OUT toggles high, a single shot pulse synchronized with the high speed comparator is generated and the rectifier conducts for a period of at least one

$$\frac{\partial V_{\text{RECT}}}{\partial \delta t} = \frac{2R_L}{\omega_s(R_s T + 2R_L \delta t)}\left[1 + \frac{2R_L}{\omega_s(R_s T + 2R_L \delta t)}\left(\frac{V_{\text{RECT}}(1 - \cos \delta t)}{\sqrt{V_0^2 - V_{\text{RECT}}^2}} - \sin \delta t\right)\right]^{-1}$$
$$\times \left[\sqrt{V_0^2 - V_{\text{RECT}}^2}(1 + \sin \delta t) + V_{\text{RECT}} \cos \delta t - \frac{2R_L}{(R_s T + 2R_L \delta t)}\left(\sqrt{V_0^2 - V_{\text{RECT}}^2}(1 - \cos \delta t) + V_{\text{RECT}} \sin \delta t\right)\right] \tag{13}$$

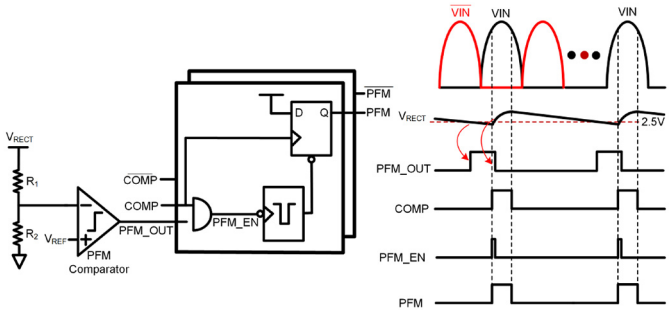

Fig. 7. Architecture of the PFM controller and the signals corresponding to the PFM mode of operation.

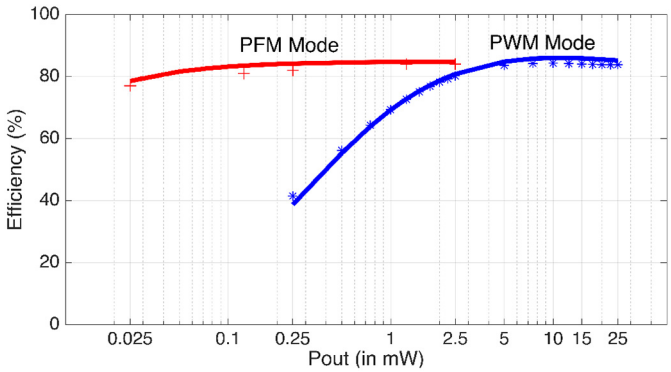

Fig. 8. Efficiency of the rectifying regulator in both PWM and PFM modes as a function of output power.

entire switching cycle. The signals corresponding to the positive cycle are shown in Fig. 7, the operations for the negative cycle are similar. The cycle repeats itself again when the voltage drops below the 2.5 V threshold. In PFM mode, the output voltage is regulated by a discontinuous, i.e., coarse comparator based feedback loop and is inherently stable. This leads to a tradeoff, although the efficiency is high, the comparator based feedback results in a higher output voltage ripple. However, since the stimulator operates in sleep mode, the higher ripple voltage in PFM mode is acceptable.

C. Sizing the Rectifier Switches

There are two key losses in a rectifier: conduction losses due to switch resistance (*Rs*) and switching losses associated with switching transistors P_1 and P_2. The key observation we make is that the conduction losses are a function of $R_{s_{ls}} + R_{s_{hs}}$, i.e., both nMOS and pMOS devices, whereas the switching losses are associated with only pMOS devices. The cross coupled nMOS devices are switched by incoming signal and do not incur any switching loss. The capacitance of the cross coupled pair can be absorbed in the parallel tuning capacitor of the receive coil. Hence, we size the cross coupled nMOS devices significantly large and size pMOS devices proportionally to tradeoff conduction and switching losses. We optimize the size of transistors N_1, N_2, P_1, and P_2 for the high power PWM mode of operation.

V. Results

The rectifying regulator was designed and implemented in TSMC 65 nm GP process. The analytical model was verified by extracting the layout of the rectifier with parasitic RC components and simulating the design using Spectre Cadence transient and periodic steady state simulations. Fig. 8 shows the efficiency of the rectifying regulator as a function of output power. The solid blue and red traces represent the analytical model for the PWM and PFM modes, respectively, whereas the simulation results are shown using markers. It can be seen that the system is efficient in the PWM mode for high output power (up to 2.5 mW) but efficiency falls at lower power levels. However, the PFM mode is efficient across a large range of output power. Since the PFM mode has high ripple voltage, it is used only during sleep mode of the stimulator at low output power levels. The analytical model and the simulation results are in good agreement which validates the proposed modeling and analysis of the rectifying regulator.

A key feature of the proposed design is its high unity gain bandwidth of 1 MHz in the PWM mode of operation. As a result, the rectifying regulator has a fast transient response. To validate this behavior, we studied two different scenarios. First, we switch the load current from 10 μA in PFM mode to 10 mA in PWM mode with a 1 ns rise time. We observed that the output of the rectifier settles very quickly, within 2 μs, with the majority of the transient dominated by the discharge of the 1 μF load capacitor from 2.515 to 2.495 V. In the second analysis, we switch the output load in the PWM mode only from 1 mA to 10 mA with a 1 ns rise time. Again the output quickly settles within 150 ns due to the high gain bandwidth product of the PWM feedback loop. We omit the transient plots due to space constraints.

VI. Conclusion

We introduced a 13.56 MHz high bandwidth rectifying regulator topology with PWM and PFM modes . We presented the theory and analytical model for the operation of the rectifying regulator and validated the model for operation in both PWM and PFM modes.

References

[1] E. C. Leuthardt, G. Schalk, J. R. Wolpaw, J. G. Ojemann, and D. W. Moran, "A brain–computer interface using electrocorticographic signals in humans," *J. Neural Eng.*, vol. 1, no. 2, pp. 63–71, 2004.

[2] K. F. E. Lee, "A timing controlled AC–DC converter for biomedical implants," in *IEEE Int. Solid State Circuits Conf. Dig. Tech. Papers (ISSCC)*, San Francisco, CA, USA, 2010, pp. 128–129.

[3] J.-H. Choi *et al.*, "A resonant regulating rectifier (3R) operating at 6.78 MHz for a 6W wireless charger with 86% efficiency," in *IEEE Int. Solid State Circuits Conf. Dig. Tech. Papers (ISSCC)*, San Francisco, CA, USA, 2013, pp. 64–65.

[4] H.-M. Lee, H. Park, and M. Ghovanloo, "A power-efficient wireless system with adaptive supply control for deep brain stimulation," *IEEE J. Solid-State Circuits*, vol. 48, no. 9, pp. 2203–2216, Sep. 2013.

[5] X. Li, C.-Y. Tsui, and W.-H. Ki, "A 13.56 MHz wireless power transfer system with reconfigurable resonant regulating rectifier and wireless power control for implantable medical devices," *IEEE J. Solid-State Circuits*, vol. 50, no. 4, pp. 978–989, Apr. 2015.

[6] V. Talla and J. R. Smith, "Design and analysis of rectifying and regulating rectifier with PWM and PFM modes," in *Proc. IEEE Int. Symp. Circuits Syst. (ISCAS)*, Montreal, QC, Canada, 2016, p. 2900.

[7] A. P. Sample, D. T. Meyer, and J. R. Smith, "Analysis, experimental results, and range adaptation of magnetically coupled resonators for wireless power transfer," *IEEE Trans. Ind. Electron.*, vol. 58, no. 2, pp. 544–554, Feb. 2011.