Analysis and Design of a Double-Quadrature CMOS VCO for Subharmonic Mixing at Ka-Band

Andrea Mazzanti, *Member, IEEE*, Enrico Sacchi, Pietro Andreani, *Member, IEEE*, and Francesco Svelto, *Member, IEEE*

***Abstract*—In this paper, we analyze the potentials of a four-phase 14-GHz CMOS voltage-controlled oscillator, tailored to a subharmonic receiver, for signal processing at Ka-band. When mild phase accuracies between in-phase and quadrature down-converted signals are required, the four-phase oscillator displays roughly the same phase noise figure-of-merit as quadrature oscillator counterparts. However, the operation at half-frequency leads to an improved performance due to a higher quality factor of the tuning varactors, and because the local oscillator circuitry and signal path run at different frequencies, relaxing coupling issues. A detailed time-variant analysis of phase noise in multiphase oscillators is introduced and validated by both simulations and experiments.**

Prototypes realized in a 65-nm technology occupy an active area of 0.5 mm^2 and show the following performances: a 26% frequency tuning range (from 12.2 to 15.9 GHz), maximum phase error from $\pi/4$ of 2°, and a phase noise of −110 dBc/Hz at 1 MHz from 14 GHz, while consuming 18 mA from 0.8-V supply.

***Index Terms*—CMOS, direct conversion, local oscillator (LO) generation, millimeter waves, multiphase, phase noise, subharmonic receivers, voltage-controlled oscillator (VCO).**

I. Introduction

An INTENSE research activity toward the realization of highly integrated solutions in silicon processes at Ka-band and millimeter-wave frequency is presently underway, after the Federal Communications Commission has granted unlicensed bands around 24, 60, and 77 GHz for several wireless applications [1], [2]. Active and passive components, building blocks, and transceiver front-ends are being intensively investigated [3]–[10]. The choice of the best suited transceiver architectures still entails several considerations. Direct conversion, usually pursued at RF frequency, facilitates a high level of integration, eliminating image-reject and IF filters. On the other hand, synthesizing a reference frequency at Ka-band and millimeter-wave bands is troublesome: variable capacitors, used as tuning elements in voltage-controlled oscillators (VCOs), present poor quality factors for a given tuning range, and dividers used in the phase-locked loop feedback path, are power hungry [4], [6], [7]. An alternative solution relies on subharmonic direct down-conversion. The local oscillator (LO) runs at a subharmonic of the received signal frequency with significant advantages in LO and dividers design. A lower frequency oscillator also mitigates other peculiar issues of direct conversion receivers, e.g., dc offsets and second-order intermodulation due to leakage of the LO into the RF path (and reverse), exacerbated at millimeter-wave frequency, due the increased difficulty in confining parasitic fields. On the contrary, at RF frequency, no clear advantage in VCO performances derives from half-frequency operation, making subharmonic receivers of minor interest.

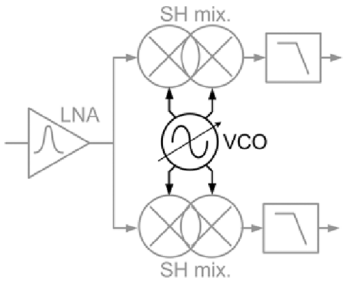

Fig. 1. Block diagram of a direct-conversion receiver based on multiphase subharmonic mixers.

There are mainly two techniques of subharmonic down-conversion, which are: 1) exploiting the nonlinear behavior of active devices to produce higher harmonics of the LO waveform [11], [12] and 2) multiplying the received signal with a number of uniformly spaced LO phases [13]–[15]. While the former determines a penalty in conversion gain and noise, the latter displays performances comparable to conventional Gilbert cells at the expense of a more complex LO generation circuit.

In this paper, we investigate a ring of four *LC* VCOs, running at half the received signal frequency, intended for in-phase (I) and quadrature (Q) demodulation in a Ka-band direct conversion receiver based on multiphase subharmonic mixers, as shown in Fig. 1. A fair comparison with a double-frequency quadrature oscillator counterpart demonstrates no penalty in phase noise figure-of-merit (FOM), while operation at half-frequency leads to an outstanding performance due to higher quality of tuning elements.

Prototypes, realized in a 65-nm CMOS process from STMicroelectronics show the following measured performances: a 26% frequency tuning range, from 12.2 to 15.9 GHz,

Manuscript received July 9, 2007; revised November 2, 2007. This work was supported in part by the Istituto Universitario di Studi Superiori (IUSS) di Pavia under the framework of Italian National Program Contract RBA06L4S5.

A. Mazzanti is with the Dipartimento di Ingegneria dell'Informazione, Università di Modena e Reggio Emilia, 41100 Modena, Italy (e-mail: amazzanti@unimore.it).

E. Sacchi was with STMicroelectronics, 27100 Pavia, Italy. He is now with Marvell, 27100 Pavia, Italy.

P. Andreani is with the Department of Electrical and Information Technology, Lund University, 22100 Lund, Sweden (e-mail: piero@eit.lth.se).

F. Svelto is with the Dipartimento di Elettronica, Università di Pavia, 27100 Pavia, Italy (e-mail: fancesco.svelto@unipv.it).

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TMTT.2007.914365

0018-9480/$25.00 © 2008 IEEE

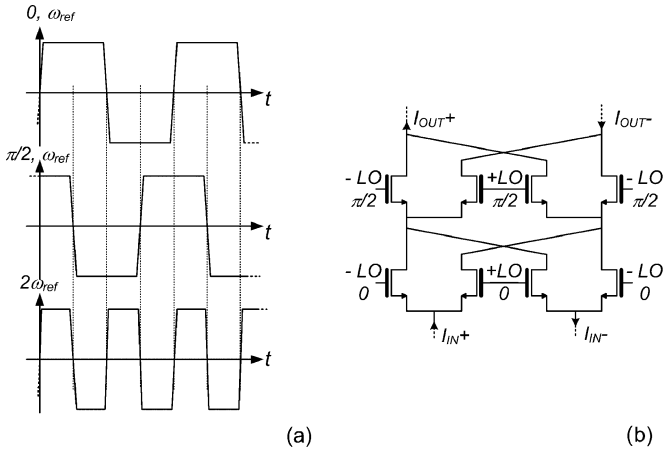

Fig. 2. Principle of subharmonic mixing. (a) Multiplication of LO waveforms $\pi/2$ shifted: equivalent effect. (b) Schematic of a CMOS subharmonic down-converter.

maximum phase error from $\pi/4$ of 2°, a phase noise of -110 dBc/Hz at 1 MHz from 14 GHz, while consuming 18 mA from 0.8-V supply.

This paper is organized as follows. Section II reviews the principle of multiphase subharmonic mixing underlying the LO requirements. Section III introduces the *LC*-tank ring VCO, while Section IV presents a time-variant phase-noise analysis. Section V describes the design of the Ka-band prototype and shows experimental results. Conclusions are drawn in Section VI.

II. Principle of Subharmonic Mixers

A conventional current commutating mixer performs frequency translation by means of multiplication, in the time domain, of an RF signal times a square-wave reference toggling between ± 1. The idea underlying subharmonic mixing is multiplying once more the frequency-translated RF signal by a phase-shifted replica of the same square-wave reference [13], [14], [15]. As shown in Fig. 2(a), multiplication by two square-waves, $\pi/2$ phase apart, corresponds to multiplication by one single square-wave reference at twice the frequency according to

$$\mathrm{sign}[\sin(\omega_{\mathrm{REF}}t)] \times \mathrm{sign}[\cos(\omega_{\mathrm{REF}}t)] = \mathrm{sign}[\sin(2\omega_{\mathrm{REF}}t)] \tag{1}$$

where $\mathrm{sign}[x] = 1$ for $x < 0$ and $\mathrm{sign}[x] = -1$ for $x < 0$.

Generalization of (1) leads to the conclusion that a reference at n times frequency is generated by multiplication of n sinusoids with π/n phase difference [14]. A differential implementation of a half-harmonic mixer is reported in Fig. 2(b), where two double-balanced differential pairs, driven by $\pi/2$ phase-shifted oscillators, are stacked. The input differential current at frequency ω_{in} is down-converted at $\omega_{\mathrm{in}} - 2\omega_{\mathrm{REF}}$ with a reference signal at ω_{REF}. A phase error from quadrature (ϕ_ε), between the two driving signals, determines a loss of gain (G), equal to $2/\pi \cos\phi_\varepsilon$. The impact is nonetheless negligible, considering that for $\phi_\varepsilon < \pi/8$, the gain loss is less than 1 dB.

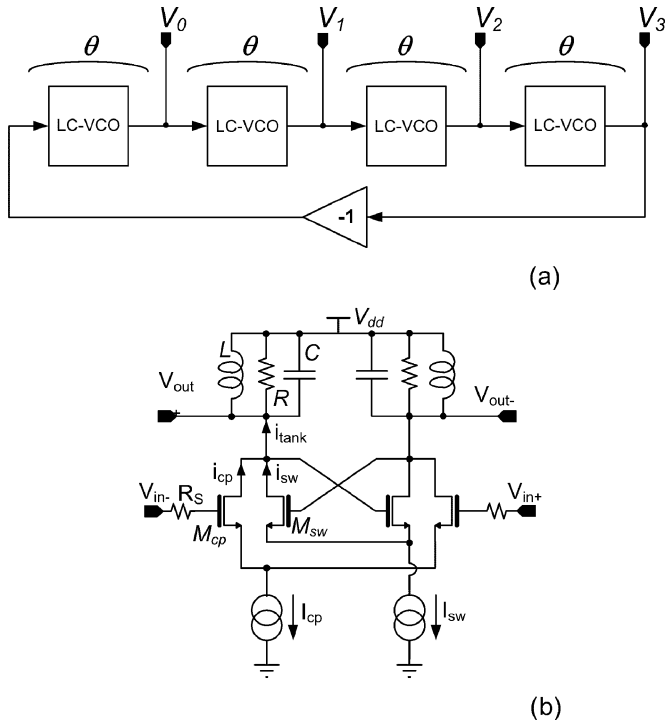

Fig. 3. (a) Block diagram of a four-phase *LC* ring oscillator. (b) Schematic of a delay cell.

From (1), we observe that if the two half frequency signals are shifted by $\pi/4$, the resulting equivalent reference oscillator is $\pi/2$ phase shifted as follows:

$$\mathrm{sign}[\sin(\omega_{\mathrm{REF}}t + \pi/4)] \times \mathrm{sign}[\cos(\omega_{\mathrm{REF}}t + \pi/4)] = \mathrm{sign}(\cos 2\omega_{\mathrm{REF}}t). \tag{2}$$

Quadrature down-conversion can thus be performed by means of two half-harmonic mixers, provided the driving signals in each switching stage follow the phase sequence reported in (1) and (2). A phase error from $\pi/4$ determines a phase error from $\pi/2$ between I and Q equivalent reference signals, reflecting the same phase error between quadrature down-converted signals.

III. LO Generation

The sequence of four differential signals, with $\pi/4$ relative phase delay, is generated by coupling four *LC* VCOs within the same ring, as shown in Fig. 3, much in the same way as two coupled oscillators are used to generate two synchronous signals $\pi/2$ apart [16], [17]. According to Barkhausen criterion, the ring assures permanent oscillation provided the loop gain is equal to 1 and the phase delay between two consecutive oscillators, θ satisfies the relation $4\theta + \pi = 2n\pi$. This equation has four different solutions in the interval $0 < \theta < 2\pi$, i.e.,

$$\theta = \pm 3/4\pi \text{ and } \theta = \pm\pi/4 \tag{3}$$

leading to four different possible oscillation modes.

The corresponding oscillation frequencies (ω_{osc}) can be derived by inspection of the single delay cell, reported in Fig. 3(b). Neglecting resistors R_s, considering large-signal operation and assuming the *LC* network filters out any current component other than the fundamental, the output voltage from

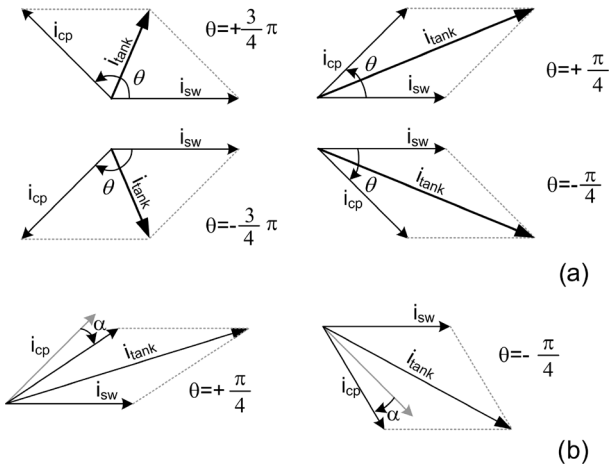

Fig. 4. (a) Vectorial diagram of the resonator currents for $\theta = \pm\pi/4, \pm 3/4\pi$. (b) Forcing a phase delay α on $i_{\rm cp}$ for $\theta = \pm\pi/4$.

each delay cell (V_0) can be expressed, with complex notation, as follows:

$$V_O = (i_{\rm sw} + i_{\rm cp} e^{j\theta}) \cdot Z(\omega_{\rm osc}) \tag{4}$$

where $i_{\rm sw} = 2/\pi I_{\rm SW}, i_{\rm cp} = 2/\pi I_{\rm CP}$. Without loss of generality, we have assumed V_o having zero phase as reference. $i_{\rm sw}$ is thus in-phase with V_0, while $i_{\rm cp}$ is in-phase with the input voltage. For a parallel *RLC* tank, the impedance $Z(\omega)$ can be approximated by

$$Z(\omega) = \frac{R}{1 + j\dfrac{2Q}{\omega_0}(\omega - \omega_0)} \tag{5}$$

with $\omega_o = 1/\sqrt{LC}$ and Q are the resonance frequency and quality factor, respectively, while the parallel resistance (R) captures the effect of losses near resonance frequency.

Separation of (4) into real and imaginary parts, and use of the results reported in (3), leads to the following expressions for $\omega_{\rm osc}$:

$$\begin{aligned}\omega_{\rm osc} &\approx \omega_0 + \frac{\omega_0}{2Q}\frac{m \cdot \sin(\theta)}{1 + m \cdot \cos(\theta)} \\ &= \begin{cases} \omega_0 - \dfrac{\omega_0}{2Q}\dfrac{m}{\sqrt{2} - m}, & \theta = -3/4\pi \\ \omega_0 - \dfrac{\omega_0}{2Q}\dfrac{m}{\sqrt{2} + m}, & \theta = -\pi/4 \\ \omega_0 + \dfrac{\omega_0}{2Q}\dfrac{m}{\sqrt{2} + m}, & \theta = +\pi/4 \\ \omega_0 + \dfrac{\omega_0}{2Q}\dfrac{m}{\sqrt{2} - m}, & \theta = +3/4\pi \end{cases}\end{aligned} \tag{6}$$

where m, defined as $i_{\rm cp}/i_{\rm sw} (= I_{\rm CP}/I_{\rm SW})$, represents the coupling strength between the oscillators.

The four possible oscillation frequencies are symmetric with respect to the tank resonance. Actually, the two modes, corresponding to $\pm 3\pi/4$ phase difference, are overwhelmed. To gain insight, Fig. 4(a) reports the vector diagram of the cell currents, assuming $m = 1$ for the four possible cases. The total tank current is larger for $\theta = \pm\pi/4$ than for $\theta = \pm 3\pi/4$, leading to a larger loop gain, and a consequent selection of the former. There is, however, still ambiguity between $\theta = +\pi/4$ and $\theta = -\pi/4$. Notice from (6) that, for $\theta = +\pi/4$, the oscillation frequency is higher than tank resonance, while the opposite is true for $\theta = -\pi/4$. Real life *LC* resonators typically present an asymmetric impedance magnitude in the proximity of resonance [18]. In particular, if the inductor's series resistance is determining the tank losses (as is at relatively low working frequencies), the impedance magnitude is larger for positive frequency offsets from resonance giving a larger loop gain for $\theta = +\pi/4$. The opposite is true at very high frequencies where the varactor dominates tank losses. While many quadrature oscillators operating below 10 GHz rely on this mechanism for proper mode startup [16], [19]–[21], between 10–20-GHz inductors and varactors feature comparable quality factors making the described mechanism not reliable enough.

Resistors Rs, in series with the coupling pair of Fig. 3(b), are added to solve the ambiguity, ensuring startup of mode with $\theta = +\pi/4$ even with a symmetric *LC* resonator. In fact, Rs introduces, together with the gate capacitance of transistors $M_{\rm CP}$, a phase delay (α) in the coupling currents $i_{\rm cp}$. The vectorial sum of the tank currents taking into account α is sketched in Fig. 4(b) (only for $\theta \pm \pi/4$). With respect to Fig. 4(a), the currents $i_{\rm cp}$ are rotated clockwise by α and, as a consequence, the magnitude of $i_{\rm tank}$ becomes larger for $\theta = +\pi/4$ than for $\theta = -\pi/4$.

IV. Phase-Noise Analysis

From the theory of quadrature oscillators, it is well known that, for a fixed current consumption, increasing oscillators coupling deteriorates the phase-noise performance [22]–[25]. The recent work by Romano *et al.* [17] extends the theory developed by the same authors for the quadrature case [23] to an arbitrary number of phases. While [17] is a very significant step forward, it still employs a linear time invariant (LTI) approach in the study of phase noise, which is known to be wanting in general (see e.g., [26]–[28]). Here, we make use of a linear time variant (LTV) approach based on Hajimiri and Lee's impulse sensitivity function (ISF) [29], [30], which accurately captures the contributions of both active and passive components to phase noise. The ultimate goal is a comparison between a quadrature and a four-phase oscillator in terms of phase noise and phase accuracy in the framework of direct conversion receivers built around conventional and subharmonic mixers, respectively.

A. Phase-Noise Analysis in the $1/f^2$ Region

The phase noise of a generic oscillator can be expressed as

$$L(\Delta\omega) = 10 \cdot \mathrm{Log}\left(\frac{\sum_i N_{Li}}{A_0^2/2}\right) \tag{7}$$

where A_0 is the oscillation amplitude and N_{Li} (referred to simply as *effective noise* hereafter) is the power spectral density

of the noise generating phase noise for a given noise source inside the oscillator. N_{Li} is given by [26], [29]

$$N_{Li} = \frac{1}{4C^2\Delta\omega^2}\frac{1}{T}\int_0^T \Gamma_{\rm tank}^2(t)\cdot\overline{i_{n-i}^2(t)}dt \qquad (8)$$

where C is the tank capacitance, $\Delta\omega$ is the frequency offset from the oscillation frequency, $\overline{i_{n-i}^2(t)}$ is the power spectral density of the current injected into the tank by the ith noise source, and the weighting function $\Gamma_{\rm tank}$ is the tank ISF, representing the time-dependent sensitivity of the phase of the oscillation to the current noise injected into the tank.

In single-ended and differential harmonic oscillators, the ISF is a sinusoid in quadrature with the voltage across the tank, but this assumption is no longer valid when many oscillators are coupled to each other. Applying the analytical technique proposed in [25], the following expression of the tank ISF for the case of N coupled oscillators can be derived:[1]

$$\Gamma_{\rm tank}(\phi) = \frac{1}{N\cdot\cos(\psi)}\cos(\phi+\psi) \qquad (9)$$

with

$$\psi = \text{arctg}\left(\frac{m\cdot\sin(\theta)}{1+m\cdot\cos(\theta)}\right), \qquad \theta = 2\pi/N$$

where the angle $\phi(0\leqslant\phi<2\pi)$ is used instead of $\omega_{\rm osc}t$ for simplicity, N is the number of phases (including differential ones), and θ is the angle between the two oscillator phases driving the same tank. Notice that, through ψ, magnitude and phase of $\Gamma_{\rm tank}$ depend on θ and m. In particular, the dependence of the phase of $\Gamma_{\rm tank}$ on ψ encodes the time-variant nature of the conversion of noise into phase noise.

Looking now at the circuit schematic of Fig. 3(b), three main noise current sources are identified: the tank resistance R, and the two differential pairs made of transistors $M_{\rm SW}$ and $M_{\rm CP}$. Fig. 5 sketches the noise currents, together with $\Gamma_{\rm tank}$, for both weak and strong coupling, providing an intuitive understanding of the expected phase-noise deterioration with increasing m. In fact, we notice that the magnitude of $\Gamma_{\rm tank}$, plotted in Fig. 5 from (9) (with $\theta=\pi/4$), increases with m, while at the same time, its maxima tends to align with the zero-crossings of $V_{\rm in}$ (i.e., the time instants when $M_{\rm CP}$ injects noise into the tank). Therefore, we expect that, when m is large, the phase noise increases and becomes dominated by R and $M_{\rm CP}$. It is worth remarking that the phase noise generated by R, being stationary, can also be found via an alternative LTI analysis, as shown in [17], while the correct evaluation of the phase noise contributed by all transistors necessitates a truly LTV approach since there the phase of the ISF plays a key role.

[1]The actual calculations follow the procedure found in [25, Appendix]. They are omitted here for space consideration.

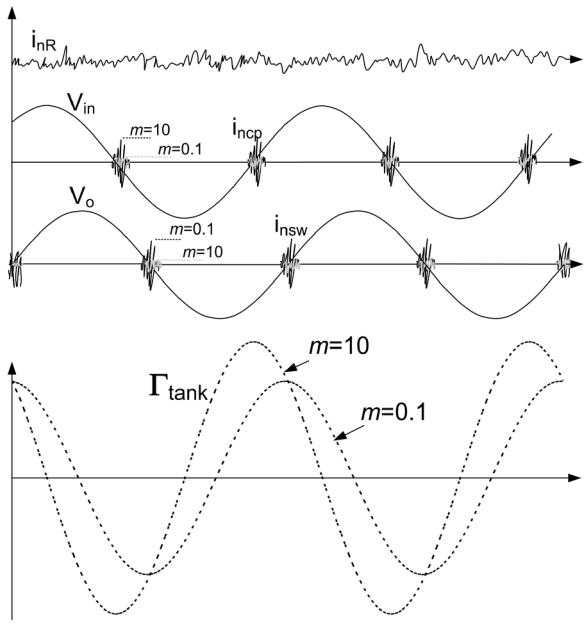

Fig. 5. Noise currents injected in the resonator and ISF for weak and strong oscillators coupling.

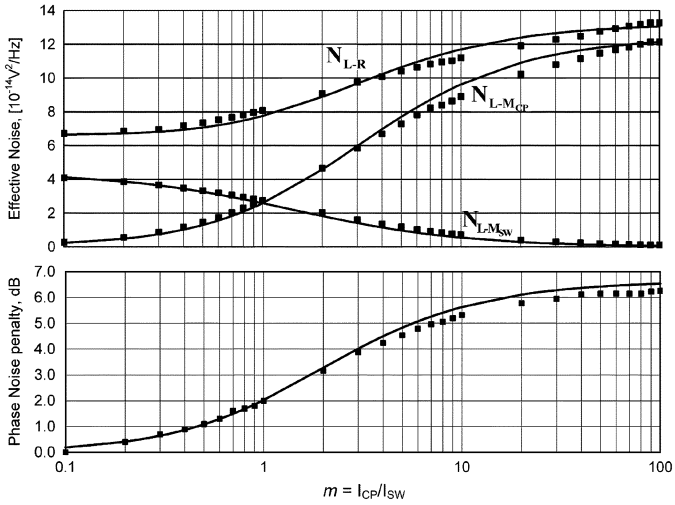

Fig. 6. Calculated (lines) and simulated (dots) effective noise (top curves) at 1-MHz offset from the carrier and phase noise penalty (bottom curve) versus oscillators coupling ($fo = 14$GHz, $Q = 9$, $I_{\rm bias} = 18$ mA).

Starting with R, whose noise power spectral density is $\overline{i_{n-R}^2} = 4k_BT/R$, we obtain that the effective noise of all N tank resistors is

$$N_{L-R} = N\cdot\frac{1}{4C^2\Delta\omega^2}\frac{1}{2\pi}\int_0^{2\pi}\Gamma_{\rm tank}^2(\phi)\cdot\frac{4k_BT}{R}d\phi = \frac{k_BT}{2NC^2\Delta\omega^2R}\left(1+\left(\frac{m\sin(\theta)}{1+m\cos(\theta)}\right)^2\right) \qquad (10)$$

where we have used the fact that all tank resistors contribute equally to the effective noise [24]. Following the derivation

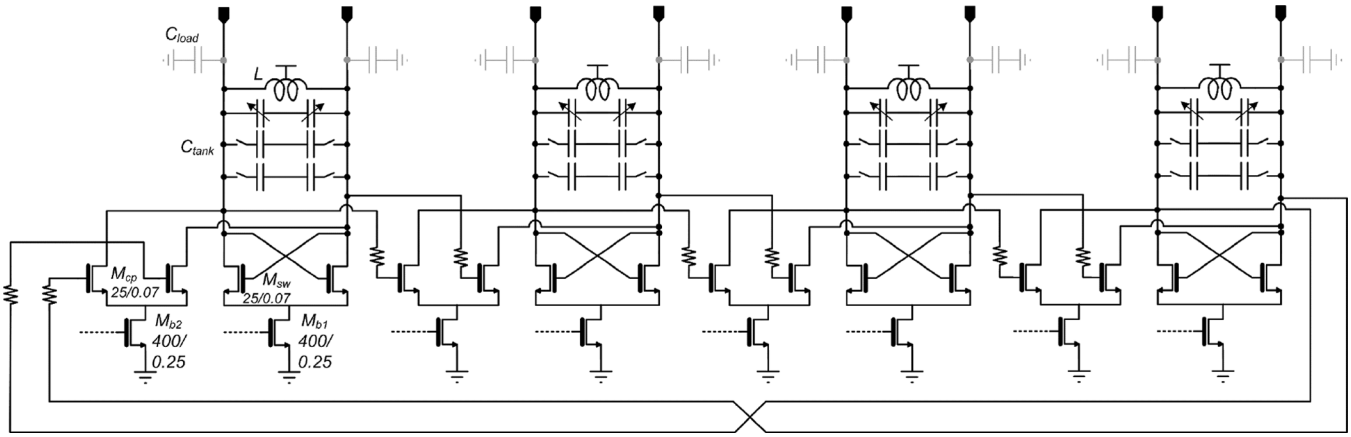

Fig. 7. Schematic of the four (differential) phases VCO.

found in the Appendix, the contributions of transistors $M_{\rm SW}$ and $M_{\rm CP}$, called $N_{L-M_{\rm SW}}$ and $N_{L-M_{\rm CP}}$, respectively, are

$$N_{L-M_{\rm sw}} = N \cdot \frac{4kT\gamma}{\Delta\omega^2 4C^2} \cdot \frac{1}{2\pi}\int_0^{2\pi} \Gamma_{\rm tank}^2(\phi)\cdot i_{n-sw1}^2(\phi)d\phi = \frac{\gamma k_B T}{2NC^2\Delta\omega^2 R}\cdot\frac{1}{1+m\cos(\theta)} \tag{11}$$

$$N_{L-M_{\rm CP}} = \frac{\gamma k_B T}{2NC^2\Delta\omega^2 R}\cdot\frac{m}{1+m\cos(\theta)}\frac{\cos^2(\theta-\psi)}{\cos^2(\psi)}. \tag{12}$$

Equations (10)–(12) are plotted in Fig. 6 (top) as functions of m for $N = 8$, and compared to numerical spectreRF simulations. A very good matching is obtained for the effective noise data, where it should also be appreciated that all plots are on a linear scale. As expected from the previous qualitative analysis, $N_{L-M_{\rm CP}}$ and N_{L-R} increase with m, while $N_{L-M_{\rm SW}}$ decreases. The overall phase noise is found from (7) and (10)–(12) once the expression for A_0 has been calculated from (4) and (5) as

$$A_0 \approx \frac{2}{\pi} R I_{\rm sw}(1+m\cos(\theta)). \tag{13}$$

Fig. 6 (bottom) plots the white phase noise penalty of the four-phase oscillator with increasing m. Theory and simulations yield almost identical results. A maximum of ~6.5 dB is paid for extremely large m values. The advantage of a large coupling strength is higher accuracy of generated phases, as will be discussed in Section V. Interestingly, with small m values, when only mild phase accuracies are to be assured as in the application of interest in this study [6], the phase-noise penalty is minimum. Looked at in another way, minimum power consumption is achieved for given phase noise with small m.

V. Design and Experiments

A prototype of the ring oscillator has been realized in a 65-nm CMOS technology from STMicroelectronics. The complete schematic is shown in Fig. 7. The resonators are made of a center-tapped single-turn inductor of 400 pH, an array of two binary weighted switched capacitors and thick oxide MOS varactors with $Lg = 0.25$ μm. The tuning voltage ranges from 0 to 2 V. The parasitic load capacitance, due to all the circuit blocks driven by the oscillator in the test chip, is estimated to be 180 fF. The tank quality factor is 8, equally determined by inductors and capacitors. The center frequency is set to 14 GHz. Polysilicon resistors of 50 Ω in series with the coupling transistors introduce $10^\circ \sim 12^\circ$ phase shift in the coupling current. Based on simulations, this is enough to solve the ambiguity in oscillator startup under process, voltage, and temperature (PVT) variations while determining a negligible phase-noise degradation (less than 0.5 dB). The two differential pairs in each oscillators are biased independently and bias currents can be regulated off-chip.

In a conventional receiver with direct quadrature generation, two (differential) coupled oscillators running at the carrier frequency are employed to generate I and Q phases. The phase-noise expressions for a quadrature oscillator with differential phases is again given by (7)–(13) with $N = 4$ instead of $N = 8$. For the sake of comparison, the phase-noise $L(\Delta\omega)$ of both quadrature and four-phase oscillators can be normalized with respect to power consumption P, carrier frequency ω_0, and offset frequency $\Delta\omega$ by means of the FOM [31]

$$\text{FOM} = 10\text{Log}\left(\left(\frac{\omega_0}{\Delta\omega}\right)^2\frac{1}{P_{\rm diss}}\right) - L(\Delta\omega). \tag{14}$$

Fig. 8 plots FOMs degradation versus m of the four-phase oscillator and a double-frequency quadrature oscillator, respectively. We have assumed the same tank quality factor, constant current consumption (equal in the two cases), and the same supply. Changing m, the same total current is redistributed between the crossed and coupling differential pairs. As expected, for very small coupling, the two FOMs are equal. However, as m increases, the four-phase oscillator shows a superior performance.[2] Interestingly, not only a subharmonic receiver allows the adoption of a half-frequency oscillator, beneficial by itself, but also the associated four-phase oscillator proves to be superior to a quadrature oscillator for the same m.

In reality, a quantification of the benefit coming from the four-phase oscillator requires also determining m to achieve the desired quadrature accuracy in down-converted signals. As

[2]For simplicity, we do not take into account the possibility of introducing phase shifters between oscillator phases [22], [32], [33], which, while attractive, does increase the complexity of the design, as well as power consumption.

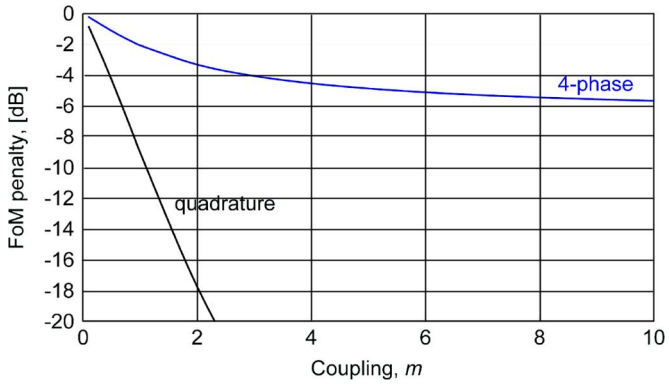

Fig. 8. Comparison of phase-noise FOM for quadrature and four-phase VCOs versus m.

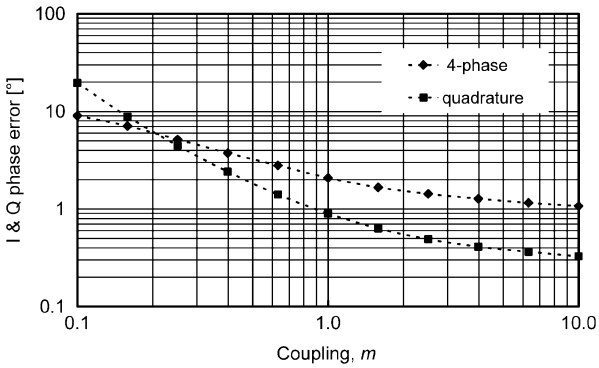

Fig. 9. Simulated phase deviation from quadrature of the I and Q baseband signals due to 0.5% tank mismatches for a downconverter driven by a quadrature oscillator (squares–dots) and for a subharmonic mixer driven by the four-phase oscillator (diamonds–dots).

in quadrature oscillators, component mismatches and parasitic coupling between resonators cause deviation from nominal LO phase shifts [21]. A larger oscillators coupling (m) reduces the phase deviation. To gain quantitative insight, we assumed a 0.5% mismatch[3] randomly distributed among the tank capacitors. The average phase deviation from $\pi/4$ has been estimated through simulations, while the induced departure from quadrature of I and Q down-converted signals has been derived according to (1) and (2). Fig. 9 (diamonds–dots) shows the simulated results. Targeting an I and Q phase error of 2°, tolerable in this framework [6], simulations indicate a required m larger than unity (i.e., $I_{\rm CP} = I_{\rm SW}$).

For comparison, Fig. 9 (squares–dots) also reports simulated phase error of a quadrature oscillator working at double frequency (28-GHz center frequency). The same target phase error is achieved with $m \approx 0.5$. Fig. 8 points out a penalty in FOM of roughly 1 dB if compared with the four-phase oscillator.

As a result, a four-phase oscillator proves performances very close to coupled oscillator counterpart for a direct conversion solution, when both target phase accuracy and phase noise are taken into account. A subharmonic direct conversion solution thus leaves with the advantage of an oscillator running at half-frequency, not compromised by the need for generation of twice reference signals, with more closely spaced phases.

[3]This is very likely an overestimate for the solely capacitors mismatch, but it is assumed also representative of other effects like mismatches between active devices and bias currents and finite isolation between resonators.

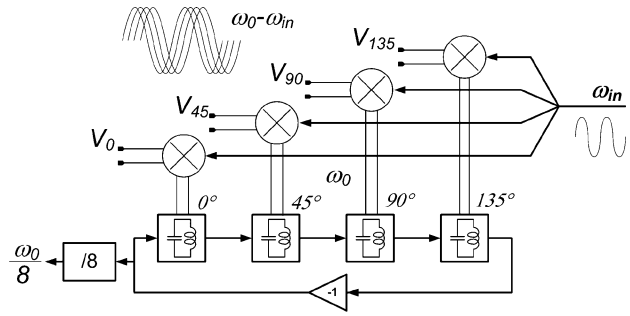

Fig. 10. Block diagram of the realized test chip.

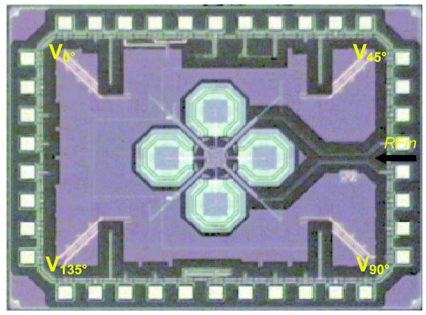

Fig. 11. Photomicrograph of the test chip.

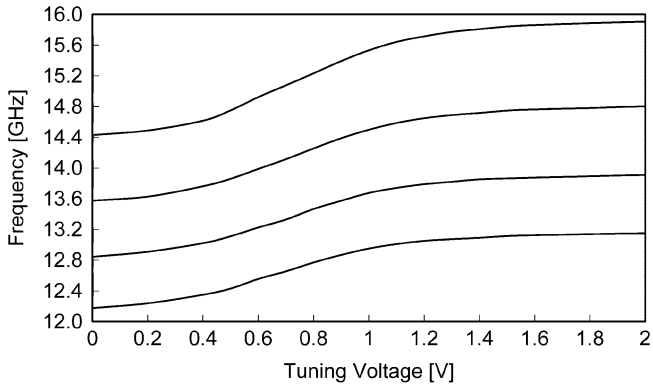

Fig. 12. Measured tuning curves.

The block diagram of the test chip is shown in Fig. 10, while the chip photomicrograph is shown in Fig. 11. The active area is 700 μm $\times$ 700 μm, while total die area is 1800 μm $\times$ 1400 μm. The VCO, drawing 18 mA from 0.8-V supply, directly drives four passive down-conversion mixers (with a common input signal provided off chip) in order to measure the accuracy of the generated phases at a lower frequency where mismatches in the measurement setup are negligible. For characterization, one of the VCO cells drives a frequency divider by 8 to implement an off-chip PLL, while three other dummy dividers are included to balance the VCO loading. The frequency divider is made of standard current–mode–logic (CML) latches and draws 7 mA.

The oscillation frequency is tunable from 12.2 to 15.9 GHz, as shown in Fig. 12. Fig. 13 shows the scope output when the four signals are down-converted at 45 MHz. Measurements are carried out with $I_{\rm CP} = I_{\rm SW}$, i.e., with unit oscillators coupling $(m = 1)$. In particular, the measured phase difference between signals, nominally $\pi/4$ apart, and between signals, nominally

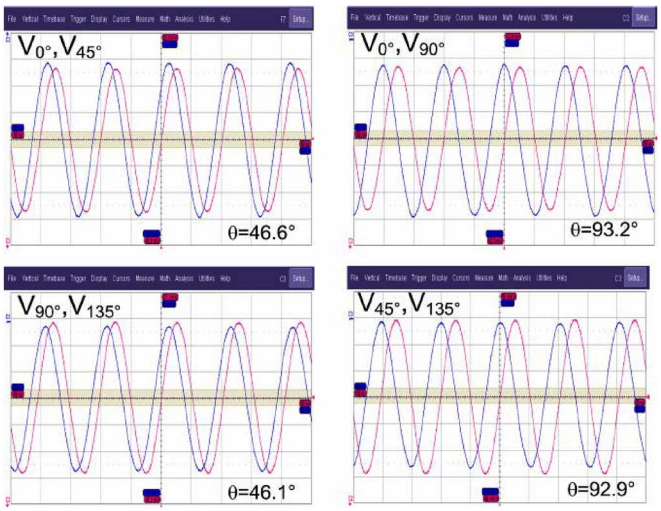

Fig. 13. VCO waveforms down-converted at IF (horizontal and vertical scales are 10 ns/div and 5 mV/div, respectively).

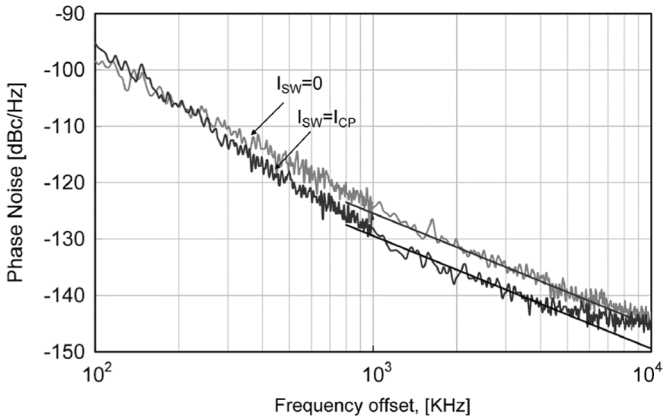

Fig. 14. Phase noise measured at the output of the divider by 8 for $m = 1 (I_{\rm CP} = I_{\rm SW})$ and $m = \infty (I_{\rm SW} = 0)$.

$\pi/2$ apart, is shown. Measurements have been repeated on available samples. Maximum deviation from $\pi/4$ is 2° while maximum from $\pi/2$ is 3.5°. Measured phase noise for $I_{\rm SW} = I_{\rm CP}$ (i.e., $m = 1$) and $I_{\rm SW} = 0$ (i.e., $m = \infty$) is shown in Fig. 14. The frequency of the signal at divider output is 1.75 GHz, corresponding to 14 GHz at VCO core. Due to the frequency division, the measured phase noise is lower than the VCO phase noise. Assuming a negligible phase-noise deterioration from the dividers, the phase noise is expected to improve by 6 dB for each division by two. The conservative estimate of the VCO phase noise is, therefore, 18 dB higher than what is measured at the output of the cascaded dividers. As predicted, white phase noise worsens at large coupling. In the $1/f^2$ region, the phase noise penalty from $m = 1$ to $m = \infty$ is 4 dB, which is in good agreement with theory (see Fig. 6). Fig. 15 plots VCO phase noise versus the output frequency at 1-MHz offset for $m = 1$. The average phase noise level is -109.5 dBc/Hz, which is very close to the simulated value of -111.5 dBc/Hz.

Finally, Table I compares state-of-the-art VCOs, providing the reference signal to transceivers operating in the same band.

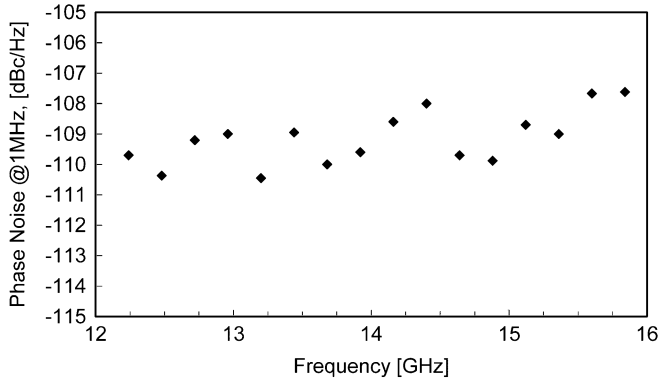

Fig. 15. Measured phase noise at 1-MHz offset versus oscillation frequency.

TABLE I
COMPARISON OF THE FOUR-PHASE OSCILLATOR WITH STATE-OF-THE-ART VCO

Ref.	f_o [GHz]	T.R. [%]	P.N.@ 1MHz [dBc/Hz]	Power [mW]	FoM [dBc/Hz]	Notes
[34]	24.2	6	-99.3	14.5* (14.5mA, 1V)	175.3	Differential
[35]	16.9	8.6	-108	10.5 (7.5mA , 1.4V)	182.3	Differential
[36]	19.9	2.7	-108	32 (17.8mA , 1.8V)	179.0	Differential
[37]	23.7	10.5	-94.0	22 (6.7mA , 3.3V)	168.0	Quadrature
[38]	32	6.3	-97	140 (43mA, 5V)	165.5	Quadrature
[39]	26.8	15.2	-84.2	129 (25.8mA, 5V)	151.6	Quadrature
This Work	**14**	**26.3**	**-110**	**15 (18mA, 0.8V)**	**181.2**	**Half-Frequency (4-phase)**

* VCO and divider by 2

The proposed four-phase oscillator outperforms quadrature oscillators, and proves power and phase-noise performances comparable or better than single *LC* oscillators. Due to the lower frequency of operation, the frequency tuning range is the largest reported to date.

VI. CONCLUSION

The choice of the transceiver integrated circuit architecture for communication applications is key to enable a low-cost mass-production solution. Millimeter-wave applications present several peculiarities with respect to RF, motivating a careful re-visitation of alternative processing circuits. In this framework, a careful analysis of multiphase oscillators, coupled with subharmonic direct conversion receivers, show significant advantages with respect to a conventional direct conversion solution. In fact, the synthesizer works at half-frequency with significant power saving. At this time, as this paper has demonstrated, the need for double references closely spaced in phase does not compromise performances.

APPENDIX

The phase-noise expressions (11) and (12), stated in Section IV-A, will be derived here. We first have to identify the noise injected by each transistor into the tank. Making use of earlier results obtained for a standalone *LC*-tank oscillator [26],

the noise power of the current injected by one differential-pair device into the corresponding resonator is

$$i^2_{n-M_{\rm SW1}}(\phi) = 4k_BT\gamma \cdot g_{m-{\rm SW1}}(\phi) \cdot \left(\frac{2g_{m-{\rm SW2}}(\phi)}{g_{m-{\rm SW1}}(\phi)+g_{m-{\rm SW2}}(\phi)}\right)^2 \quad \text{(A1)}$$

where, with reference to Fig. 3(b), we called $M_{\rm SW1}$ the device facing node $Vo+$ and $M_{\rm SW2}$ the other. $g_{m-{\rm SW1}}(\phi)$ and $g_{m-{\rm SW2}}(\phi)$ are the respective time-dependent transconductances given by [26]

$$g_{m-{\rm SW1}}(\phi) = \beta_{\rm sw}A_0\left(\sin(\phi)+\sqrt{2\sin^2(\Phi_{\rm sw})-\sin^2(\phi)}\right)$$
$$g_{m-{\rm SW2}}(\phi) = \beta_{\rm sw}A_0\left(-\sin(\phi)+\sqrt{2\sin^2(\Phi_{\rm sw})-\sin^2(\phi)}\right) \quad \text{(A2)}$$

with $\beta_{\rm sw} = \mu_n C_{\rm ox}W_{\rm SW}/L_{\rm SW}$($\mu_n$ being the electron mobility, $C_{\rm ox}$ being the gate–oxide capacitance per unit area, and $W_{\rm SW}$ and $L_{\rm SW}$ being the transistors width and length, respectively), and where $\Phi_{\rm SW} = \arcsin\sqrt{I_{\rm SW}/(\beta_{\rm SW}A_0^2)}$. The expressions in (A2) are only defined for $-\Phi_{\rm SW} < \phi < \Phi_{\rm SW}$ and $\pi - \Phi_{\rm SW} < \phi < \pi + \Phi_{\rm SW}$, i.e., when both transistors are on. By means of (A1) and (A2) in (8) and abundant trigonometric manipulations, the contribution to phase noise of $M_{\rm SW}$, given by (10), is obtained.

The contribution of the coupling pair devices is found in much the same way. Looking at the schematic in Fig. 3(b) and the waveforms in Fig. 5, we can reuse all the equations introduced for $M_{\rm SW}$, provided that $g_{m-{\rm SW1,2}}$ in (A1) are replaced by $g_{m-{\rm CP1,2}}$, $\beta_{\rm sw}$ and $I_{\rm SW}$ in (A2) are replaced by $\beta_{\rm cp}$ and $I_{\rm CP}(=mI_{\rm SW})$, and all equations are phase shifted by $2\pi/N$ (except $\Gamma_{\rm tank}(\phi)$, which is, of course, the same for all noise sources). In this way, (12) is eventually retrieved.

ACKNOWLEDGMENT

This study was carried out within the Studio di Microelecttronica, a joint research laboratory of the Università di Pavia, Pavia, Italy, and STMicroelectronics, Pavia, Italy.

REFERENCES

[1] P. Smulders, "Exploiting the 60 GHz band for local wireless multimedia access: Prospects and future directions," *IEEE Commun. Mag.*, vol. 40, pp. 140–147, 2002.

[2] I. Gresham, A. Jenkins, R. Egri, C. Eswarappa, N. Kinayman, N. Jain, R. Anderson, F. Kolak, R. Wohlert, S. P. Bawell, J. Bennett, and J. P. Lanteri, "Ultra-wideband radar sensors for short-range vehicular applications," *IEEE Trans. Microw. Theory Tech.*, vol. 52, no. 9, pp. 2105–2122, Sep. 2004.

[3] S. Emami, C. H. Doan, A. M. Niknejad, and R. W. Brodersen, "A highly integrated 60 GHz CMOS front-end receiver," in *IEEE Int. Solid-State Circuits Conf. Tech. Dig.*, Feb. 2007, pp. 190–192.

[4] C. Changhua and K. K. O. , "Millimeter-wave voltage-controlled oscillators in 0.13 μm CMOS Technology," *IEEE J. Solid-State Circuits*, vol. 41, no. 6, pp. 1297–1304, Jun. 2006.

[5] C. H. Doan, S. Emami, A. M. Niknejad, and R. W. Brodersen, "Millimeter-wave CMOS design," *IEEE J. Solid-State Circuits*, vol. 40, no. 1, pp. 144–155, Jan. 2006.

[6] B. A. Floyd, S. K. Reynolds, U. R. Pfeiffer, T. Zwick, T. Beukema, and B. Gaucher, "SiGe bipolar transceiver circuits operating at 60 GHz," *IEEE J. Solid-State Circuits*, vol. 40, no. 1, pp. 156–167, Jan. 2005.

[7] S. K. Reynolds, B. A. Floyd, U. R. Pfeiffer, T. Beukema, J. Grzyb, C. Haymes, B. Gaucher, and M. Soyuer, "A silicon 60 GHz receiver and transmitter chipset for broadband communications," *IEEE J. Solid-State Circuits*, vol. 41, no. 12, pp. 2820–2831, Dec. 2006.

[8] A. Natarajan, A. Komijani, X. Guan, A. Babakhani, and A. Hajimiri, "A 77-GHz phased-array transceiver with on-chip antennas in silicon: Transmitter and local lo-path phase shifting," *IEEE J. Solid-State Circuits*, vol. 41, no. 12, pp. 2807–2819, Dec. 2006.

[9] A. Babakhani, X. Guan, A. Komijani, A. Natarajan, and A. Hajimiri, "A 77-GHz phased-array transceiver with on-chip antennas in silicon: Receiver and antennas," *IEEE J. Solid-State Circuits*, vol. 41, no. 12, pp. 2795–2806, Dec. 2006.

[10] A. Hajimiri, H. Hashemi, A. Natarajan, G. Xiang, and A. Komijani, "Integrated phased array systems in silicon," *Proc. IEEE*, vol. 93, no. 9, pp. 1637–1655, Sep. 2005.

[11] H. Juo-Jung, T. M. Hancock, G. M. Rebeiz, H. Juo-Jung, T. M. Hancock, and G. M. Rebeiz, "A 77 GHz SiGe sub-harmonic balanced mixer," *IEEE J. Solid-State Circuits*, vol. 40, no. 11, pp. 2167–2173, Nov. 2005.

[12] M. Bao, H. Jacobsson, L. Aspemyr, G. Carchon, and X. Sun, "A 9–31-GHz subharmonic passive mixer in 90-nm CMOS technology," *IEEE J. Solid-State Circuits*, vol. 41, no. 10, pp. 2257–2264, Oct. 2006.

[13] S. Liwei, J. C. Jensen, and L. E. Larson, "A wide-bandwidth Si/SiGe HBT direct conversion sub-harmonic mixer/downconverter," *IEEE J. Solid-State Circuits*, vol. 35, no. 9, pp. 1329–1337, Sep. 2000.

[14] L. Kyeongho, P. Joonbae, L. Jeong-Woo, L. Seung-Wook, H. Hyung Ki, J. Deog-Kyoon, and K. Wonchan, "A single-chip 2.4-GHz direct-conversion CMOS receiver for wireless local loop using multiphase reduced frequency conversion technique," *IEEE J. Solid-State Circuits*, vol. 36, no. 5, pp. 800–809, May 2001.

[15] R. M. Kodkani and L. E. Larson, "A 24 GHz CMOS direct-conversion sub-harmonic downconverter," in *RFIC Symp. Dig.*, 2007, pp. 485–488.

[16] A. Rofougaran, J. Rael, M. Rofougaran, and A. Abidi, "A 900 MHz CMOS *LC*-oscillator with quadrature outputs," in *IEEE Int. Solid-State Circuits Conf. Tech. Dig.*, Feb. 1996, pp. 392–393.

[17] L. Romano, S. Levantino, C. Samori, and A. L. Lacaita, "Multiphase *LC* oscillators," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 53, no. 7, pp. 1579–1588, Jul. 2006.

[18] A. Rofougaran, G. Chang, J. J. Rael, J. Y. C. Chang, M. Rofougaran, P. J. Chang, M. Djafari, M. K. Ku, E. W. Roth, A. A. Abidi, and H. Samueli, "A single-chip 900-MHz spread-spectrum wireless transceiver in 1 μm CMOS—Part I: Architecture and transmitter design," *IEEE J. Solid-State Circuits*, vol. 33, no. 4, pp. 515–534, Apr. 1998.

[19] P. Andreani, A. Bonfanti, L. Romano, and C. Samori, "Analysis and design of a 1.8-GHz CMOS *LC* quadrature VCO," *IEEE J. Solid-State Circuits*, vol. 37, no. 12, pp. 1737–1747, Dec. 2002.

[20] M. Tiebout, "Low-power low-phase-noise differentially tuned quadrature VCO design in standard CMOS," *IEEE J. Solid-State Circuits*, vol. 36, no. 7, pp. 1018–1024, Jul. 2001.

[21] A. Mazzanti, F. Svelto, and P. Andreani, "On the amplitude and phase errors of quadrature *LC*-tank CMOS oscillators," *IEEE J. Solid-State Circuits*, vol. 41, no. 6, pp. 1305–1313, Jun. 2002.

[22] J. van der Tang, P. van de Ven, D. Kasperkovitz, and A. van Roermund, "Analysis and design of an optimally coupled 5-GHz quadrature *LC* oscillator," *IEEE J. Solid-State Circuits*, vol. 37, no. 5, pp. 657–661, May 2002.

[23] L. Romano, S. Levantino, A. Bonfanti, C. Samori, and A. L. Lacaita, "Phase noise and accuracy in quadrature oscillators," in *Int. Circuits Syst. Symp.*, 2004, vol. 1, pp. 161–164.

[24] P. Andreani and X. Wang, "On the phase-noise and phase-error performances of multiphase *LC* CMOS VCOs," *IEEE J. Solid-State Circuits*, vol. 39, no. 11, pp. 1883–1893, Nov. 2004.

[25] P. Andreani, "A time-variant analysis of the $1/f^2$ phase noise in CMOS parallel *LC*-tank quadrature oscillators," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 53, no. 8, pp. 1749–1770, Aug. 2006.

[26] P. Andreani, X. Wang, L. Vandi, and A. Fard, "A study of phase noise in Colpitts and *LC*-tank CMOS oscillators," *IEEE J. Solid-State Circuits*, vol. 40, no. 5, pp. 1107–1118, May 2005.

[27] P. Andreani and A. Fard, "More on the $1/f^2$ phase noise performance of CMOS differential-pair *LC*-tank oscillators," *IEEE J. Solid-State Circuits*, vol. 41, no. 12, pp. 2703–2712, Dec. 2006.

[28] A. Fard and P. Andreani, "An analysis of $1/f^2$ phase noise in bipolar Colpitts oscillators (with a digression on bipolar differential-pair *LC* oscillators)," *IEEE J. Solid-State Circuits*, vol. 42, no. 2, pp. 374–387, Feb. 2007.
[29] A. Hajimiri and T. H. Lee, "A general theory of phase noise in electrical oscillators," *IEEE J. Solid-State Circuits*, vol. 33, no. 2, pp. 179–194, Feb. 1998.
[30] A. Hajimiri and T. H. Lee, "Corrections to 'A general theory of phase noise in electrical oscillators'," *IEEE J. Solid-State Circuits*, vol. 33, no. 6, p. 928, Jun. 1998.
[31] P. Kinget, "Integrated gigahertz voltage controlled oscillators," in *Analog Circuit Design*. Norwell, MA: Kluwer, 1999, pp. 353–381.
[32] P. Vancorenland and M. S. J. Steyaert, "A 1.57-GHz fully integrated very low-phase-noise quadrature VCO," *IEEE J. Solid-State Circuits*, vol. 37, no. 5, pp. 653–656, May 2002.
[33] A. Mirzaei, M. E. Heidari, and A. A. Abidi, "Analysis of oscillators locked by large injection signals: Generalized Adler's equation and geometrical interpretation," in *IEEE Custom Integrated Circuit Conf.*, San Jose, 2006, pp. 737–740.
[34] A. W. L. Ng, G. C. T. Leung, K. Ka-Chun, L. L. K. Leung, and H. C. Luong, "A 1-V 24-GHz 17.5-mW phase-locked loop in a 0.18-μm CMOS process," *IEEE J. Solid-State Circuits*, vol. 41, no. 6, pp. 1236–1243, Jun. 2006.
[35] C. R. C. De Ranter and M. S. J. Steyaert, "A 0.25 μm CMOS 17 GHz VCO," in *IEEE Int. Solid-State Circuits Conf. Tech. Dig.*, Feb. 2001, pp. 370–371.
[36] H. Hsieh-Hung and L. Liang-Hung, "A low-phase-noise K-band CMOS VCO," *IEEE Microw. Wireless Compon. Lett.*, vol. 16, no. 10, pp. 552–554, Oct. 2006.
[37] M. A. T. Sanduleanu and E. Stikvoort, "Highly linear, varactor less, 24 GHz IQ oscillator," in *Proc. RFIC Symp.*, 2005, pp. 577–580.
[38] W. L. Chan, H. Veenstra, and J. R. Long, "A 32 GHz quadrature *LC*-VCO in 0.25 μm SiGe BiCMOS technology," in *IEEE Int. Solid-State Circuits Conf. Tech. Dig.*, Feb. 2005, pp. 538–539.
[39] S. Hackl, J. Bock, G. Ritzberger, M. Wurzer, and A. L. Scholtz, "A 28-GHz monolithic integrated quadrature oscillator in SiGe bipolar technology," *IEEE J. Solid-State Circuits*, vol. 38, no. 1, pp. 135–137, Jan. 2001.

Andrea Mazzanti (S'01–M'06) was born in Modena, Italy, in 1976. He received the Laurea and Ph.D. degrees in electrical engineering from the Università di Modenae Reggio Emilia, Modena, Italy, in 2001 and 2005, respectively.

During the summer of 2003, he was an Student Intern with Agere Systems, Allentown, PA. In 2005, he accepted a post-doctoral position with the Dipartimento di Elettronica, Università di Pavia, Pavia, Italy, where he was involved with CMOS power amplifiers. He is currently an Assistant Professor with the Università di Modenae Reggio Emilia. His main research interests concern device modeling and integrated circuit design for RF and millimeter-wave communications.

Enrico Sacchi was born in Pavia, Italy, in 1971. He received the Laurea degree in electrical engineering and Ph.D. degree in electrical engineering and computer science from the Università di Pavia, Pavia, Italy, in 1995 and 1999, respectively. His doctoral research concerned optimization of CMOS spiral inductors.

In 1999, he joined the Studio di Microelectronica, a joint research laboratory of STMicroelectronics, Pavia, Italy, and Università di Pavia, where he was an RFIC CMOS Designer, mainly involved in research and development activities concerning both TX and RX analog parts of RF CMOS transceivers. From September 2000 to August 2001, he was a Visiting Industrial Fellow of STMicroelectronics with the Electrical Engineering and Computer Science Department, University of California at Berkeley. In September 2007, he joined Marvell, Pavia, Italy, where he is currently a Senior Design Engineer.

Pietro Andreani (S'98–A'99–M'03) received the M.S.E.E. degree from the University of Pisa, Pisa, Italy, in 1988, and the Ph.D. degree from Lund University, Lund, Sweden, in 1999.

From 1990 to 1993 and 1995 to 2001, he was with the Department of Applied Electronics (now Electrical and Information Technology), Lund University, during which time he was an Associate Professor in charge of the analog integrated circuits courses. From 2001 to 2007, he was a Professor with the Center for Physical Electronics, Technical University of Denmark, Lyngby, Denmark. Since May 2007, he has been with the Department of Electrical and Information Technology, Lund University, where his research mainly concerns analog/RF integrated circuit design.

Francesco Svelto (S'93–M'98) received the Laurea and Ph.D. degrees in electrical engineering from the Università di Pavia, Pavia, Italy, in 1991 and 1995, respectively.

From 1995 to 1997, he held an industry grant for research in RF CMOS. In 1997, he became an Assistant Professor with the Università di Bergamo. In 2000, he joined the Università di Pavia, where he is currently a Professor. Since January 2006, he has been the Director of the joint scientific laboratory Studio di Microelecttronica, of the Università di Pavia and STMicrolectronics, which is dedicated to research in microelectronics. His current interests are RF and millimeter-wave integrated circuits for telecommunications.

Dr. Svelto is currently a member of the Technical Program Committee of the International Solid State Circuits Conference and Custom Integrated Circuits Conference. He has been member of the Bipolar/BiCMOS Circuits Technology Meeting and the European Solid State Circuits Conference. He was an associate editor for the IEEE JOURNAL OF SOLID-STATE CIRCUITS (2003–2007) and was a guest editor for that publication in March 2003. He was a corecipient of the IEEE JOURNAL OF SOLID-STATE CIRCUITS 2003 Best Paper Award.