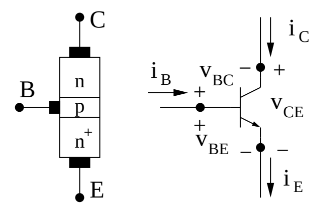
III. Transistors (Introduction & Large Signal Model)

3.1 III. Bipolar-Junction (BJT) Transistors

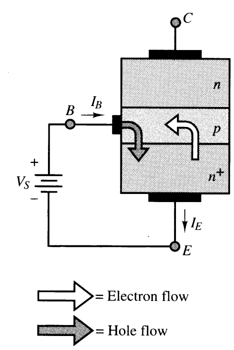
A bipolar junction transistor is formed by joining three sections of semiconductors with alternative different dopings. The middle section (base) is narrow and one of the other two regions (emitter) is heavily doped. The other region is called the collector. Two variants of BJT are possible: NPN (base is made of p-type material) and PNP (base is made of n-type material). Let's first consider a NPN transistor.



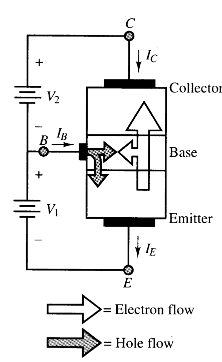
A BJT has three terminals. Six parameters; i_C, i_B, i_E, v_{CE}, v_{BE}, and v_{BC}; define the state of the transistor. However, because BJT has three terminals, KVL and KCL should hold for these terminals:

$$i_E = i_C + i_B \qquad\qquad v_{BC} = v_{BE} - v_{CE}$$

Thus, only four of these 6 parameters are independent. The relationships among these four parameters (i_B, v_{BE}, i_C and v_{CE}) represent the "iv" characteristics of the BJT.



At the first glance, a BJT looks like 2 diodes placed back to back. Indeed this is the case if we apply a voltage to only two of the three terminals, letting the third terminal float. This is also the way that we check if a transistor is working: use an am-meter to ensure both diodes are in working conditions. (One should also check the resistance between CE terminals and read a vary high resistance as one may have a burn through the base connecting collector and emitter.)



BJT behavior is quite different, however, when voltages are applied to both BE and CE terminals. The BE junction acts like a diode. When this junction is forward biased ($v_{BE} = V_{D0}$), electrons flow from the emitter to the base to combine with holes there. But as the emitter region is heavily doped, there is a large number of electrons crossing into the base compared to available holes. As the base region is narrow, most of these electrons diffuse into the collector region. Then, if a positive voltage is applied between collector and base ($v_{CB} > 0$ but can be small), these electrons are "collected" by the collector electrode. Note that the BC junction is reverse biased ($v_{BC} < 0$) but a large current flows.

Because the BE junction acts as a diode: 1) The number of electrons that cross from the emitter into the base and diffuse into collector region depends exponentially on the voltage applied to the BE junction, v_{BE} (similar to the diode equation). 2) For a given v_{BE}, the number of holes traveling from base to emitter (proportional to i_B) is a constant fraction of the number of electrons traveling from emitter to base (proportional to i_c). This ratio depends on doping level, temperature, and other manufacturing parameters. In a BJT, because emitter is heavily doped, there are a lot more electrons (from emitter) than holes (from the base), *e.g.,* on the average, out of every 200 electrons traveling from emitter to base only one combines with a hole and the other 199 travel to the collector. As such, the ratio of $i_C/i_B = \beta$ is a large and a constant (depending on doping, temperature, etc.). Parameter β is called the BJT common-emitter current gain or current gain for short.

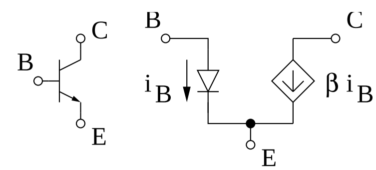
The above discussion, identifies two modes of operation for a NPN BJT.

1) BE junction is reverse biased ($i_B = 0$): No electrons would flow from emitter into the base and into the collector, leading to $i_C = 0$. This mode is called the cut-off.

2) BE is forward biased and BC is reverse biased. This is called the active-linear mode (or active mode for short). In this case, a large $i_C = \beta i_B$ flows. Using diode iv equation for BE junction:

$$i_B = I_{S,B}\left(e^{v_{BE}/nV_T} - 1\right) \equiv \frac{I_S}{\beta}\left(e^{v_{BE}/nV_T} - 1\right) \approx \frac{I_S}{\beta}\,e^{v_{BE}/nV_T}$$

$$i_C = I_S\left(e^{v_{BE}/nV_T} - 1\right) \approx I_S\,e^{v_{BE}/nV_T}$$



We can also construct a circuit model for a BJT which is valid for cut-off and active modes.

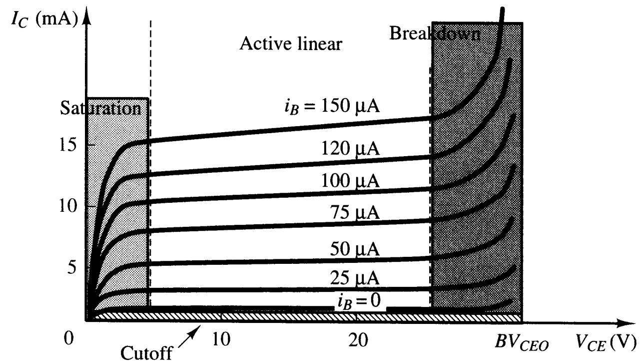
In the active mode, BE is forward biased ($v_{BE} = V_{D0}$) while BC is reverse biased ($v_{BC} < 0$). Thus $v_{CE} = -v_{BC} + v_{BE} \geq V_{D0}$. Now, let's consider the case when v_{CE} is reduced below V_{D0} and BC junction becomes forward biased. In this case, extra holes will be injected into the base region. These extra holes will combine with the electrons traveling from emitter to collector, reducing the collector current. This mode of operation is called the saturation mode and for a given v_{BE} has a smaller collector current than the active mode, or $i_C/i_B < \beta$.

We saw in the diode section that when the junction is forward biased, a negligible current flows until the forward bias voltage is large enough, typically ~ 0.3 V for a Si diode. Thus, as v_{CE} is decreased below V_{D0}, for the first ~ 0.3 V ($v_{CE} \geq 0.4$ V) i_C changes little as a negligible number of extra holes are injected in the base. This mode is called "soft saturation" and transistor acts nearly as if it is in active mode, *i..e.,* $i_C \approx \beta i_B$. For this reason, some text books define the boundary of the active mode to be $v_{CE} \geq 0.4$ V instead of $v_{CE} \geq V_{D0} = 0.7$ V for Si BJTs, thereby including the soft saturation operation in the active mode).

When v_{BC} is increased above ~ 0.3 V, an appreciable number of holes are injected in the base and the collector current drops substantially. For a Si BJT, this part of saturation translates into $v_{CE} = 0.1 - 0.3$ V and i_C is substantially smaller than βi_B.

BJT iv characteristics are shown as plots of i_C vs v_{CE} for different values of i_B as is shown. The three main modes (or states) of BJT can be clearly seen: cut-off, active-linear, and saturation.

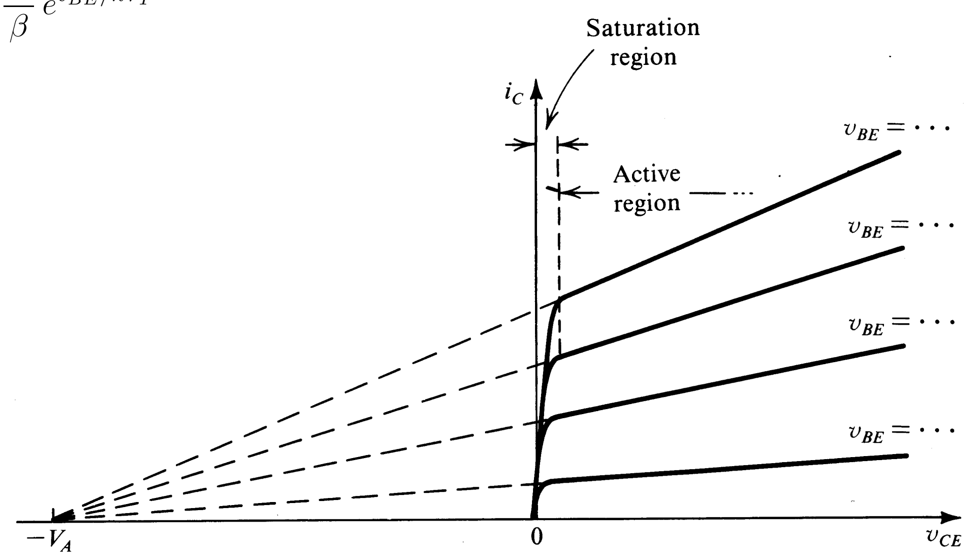
Note that a transistor can be damaged if (1) a large positive voltage is applied across the CE junction (breakdown region), or (2) product of $i_C v_{CE}$ exceed power handling of the transistor, or (3) a large reverse voltage is applied between any two terminals.



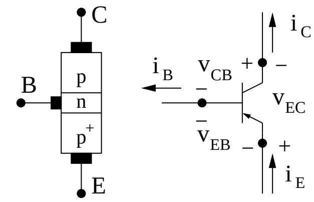
Looking at $i_C V_{CE}$ characteristics above (which is for a real BJT) for the active mode, one notes that for a given i_B, i_C increases slightly as v_{CE} is increased (as opposed to $i_C \beta i_B$). The reason for this increase in i_C is that as v_{CE} is increased, the "effective" width of the base region is reduced and more electrons can reach the collector. This is called the "Early" effect. In fact, we extrapolate all characteristics lines, they would meet at a negative voltage $v_{CE} = -V_A$ as is shown below. The voltage V_A is particular to each BJT (depends on its manufacturing) and has a typical value of 50 to 100 V. It is called the "Early" voltage. The Early effect can be accounted for by the following addition to the i_C equation (Note i_B equation does NOT change):

$$i_C = I_S e^{v_{BE}/nV_T} \left(1 + \frac{v_{CE}}{V_A}\right)$$

$$i_B = \frac{I_S}{\beta}\, e^{v_{BE}/nV_T}$$



PNP transistor

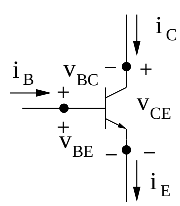


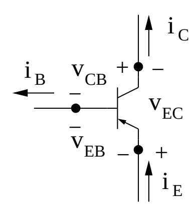
A PNP transistor operates in a similar manner to a NPN BJT, expect that the majority carriers are now holes. Emitter region is doped heavily with a p-type material, holes from emitter travel through the base and reach the collector region.

As can be seen, currents and voltages will have to reverse sign compared to a NPN transistor, *e.g.,* $v_{EB} = V_{D0}$ for EB junction to be forward biased. As holes move slower than electrons in a semiconductor, PNP transistors have a slower response time. They are mainly used in pairs with NPN transistors, *e.g.,* push-pull amplifiers.

Summary of BJT Large-Signal Models:

	NPN	**PNP**
Cut-off:		
BE reverse biased	$i_B = 0,$	$i_B = 0$
	$i_C = 0$	$i_C = 0$
Active Linear:		
BE forward biased	$i_B = \dfrac{I_S}{\beta}\, e^{v_{BE}/nV_T}$	$i_B = \dfrac{I_S}{\beta}\, e^{v_{EB}/nV_T}$
CE reverse biased	$i_C = I_S\, e^{v_{BE}/nV_T}\left(1 + \dfrac{v_{CE}}{V_A}\right)$	$i_C = I_S\, e^{v_{EB}/nV_T}\left(1 + \dfrac{v_{EC}}{V_A}\right)$
Saturation:		
BE forward biased	$i_B = \dfrac{I_S}{\beta}\, e^{v_{BE}/nV_T}$	$i_B = \dfrac{I_S}{\beta}\, e^{v_{EB}/nV_T}$
CE forward biased	$i_C < \beta i_B$, $v_{CE} = 0.1 - 0.3$ V	$i_C < \beta i_B$, $v_{EC} = 0.1 - 0.3$ V





The above model is called a "large signal" model as it applies to any size currents/voltages applied to the BJT (as opposed to a "small-signal" model discussed later). In addition, this is a "low-frequency" model as the junction capacitances are NOT taken into account (you will see high-frequency transistor models in ECE102). PSpice uses the Ebers-Moll model which includes a better treatment of transistor operation in the saturation mode.

Similar to diodes, BJT *iv* equations above are non-linear. For analytical calculations, we will develop a simple piecewise linear model for BJT below.

3.2 Piecewise Linear, Large Signal Model for BJT

First let's consider a NPN transistor. In the cut-off and active modes, BE junction acts like a diode and $i_C = \beta i_B(1 + v_{CE}/VA)$. As such, we can use our piecewise linear model for the diode to arrive at a piecewise linear model for the BJT.

$$\begin{aligned}
\textbf{Cut-Off:}\quad & i_B = 0, \qquad v_{BE} < V_{D0} \\
& i_C = i_E = 0 \\
\textbf{Active:}\quad & v_{BE} = V_{D0}, \qquad i_B \geq 0 \\
& i_C = \beta i_B, \qquad v_{CE} \geq V_{D0}
\end{aligned}$$

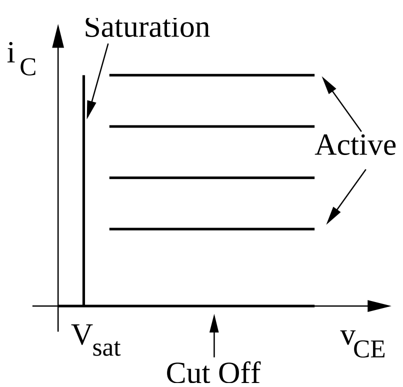
Early Effect is ignored in this simple model as additional accuracy ($< 5\%$) does not justify additional work. Early Effect can be included by setting $i_C = \beta i_B(1 + v_C E)/V_A)$.

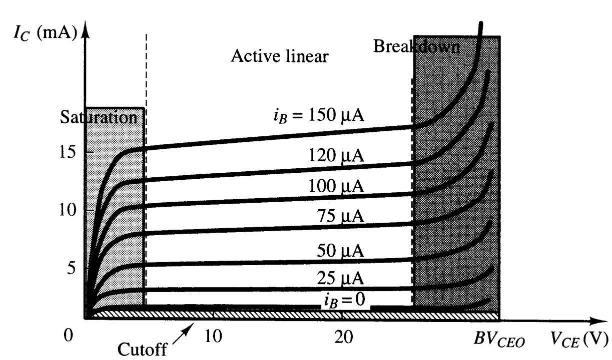
Also, in the soft saturation mode , ($v_{CE} \geq 0.4$ V for Si BJTs), $i_C \approx \beta i_B$ and thus, we can replace $v_{CE} \geq V_{D0}$ in the model for the active mode with $v_{CE} \geq 0.4$ V. However, care should be taken in designing circuit in which a BJT is in soft saturation. As such, in this course, we will use $v_{CE} \geq V_{D0}$ as the boundary between active and saturation modes.

For a Si BJT in saturation, $0.1 \leq v_{CE} \leq 0.3$ V. Given that an exact model for saturation mode is complicated, it is sufficient for a piecewise linear model to assume $v_{CE} = V_{sat}$ (with $V_{sat} \approx 0.2$ V for Si transistors). Thus:

$$\begin{aligned}
\textbf{Saturation:}\quad & v_{BE} = V_{D0}, \qquad i_B > 0 \\
& v_{CE} \approx V_{sat}, \qquad i_C < \beta i_B
\end{aligned}$$

The above simple, large-signal model is shown below. A comparison of this simple model with the real BJT characteristics demonstrates the degree of approximation used.

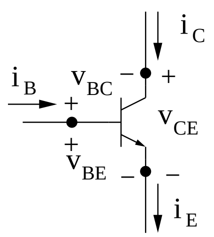


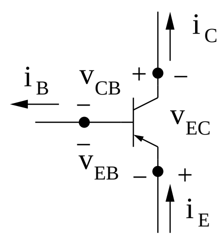


A similar piecewise linear model for PNP transistor can also constructed:

Summary of BJT piecewise linear large-signal Model

	NPN	**PNP**
Cut-off:	$i_B = 0$, $v_{BE} < V_{D0}$ $i_C = 0$	$i_B = 0$, $v_{EB} < V_{D0}$ $i_C = 0$
Active Linear:	$v_{BE} = V_{D0}$, $i_B > 0$ $i_C = \beta i_B > 0$, $v_{CE} > V_{D0}$	$v_{EB} = V_{D0}$, $i_B > 0$ $i_C = \beta i_B > 0$, $v_{EC} > V_{D0}$
Saturation:	$v_{BE} = V_{D0}$, $i_B > 0$ $v_{CE} = V_{sat}$, $i_C < \beta i_B$	$v_{EB} = V_{D0}$, $i_B > 0$ $v_{EC} = V_{sat}$, $i_C < \beta i_B$





How to solve BJT circuits:

Similar to diode circuits, we need assume that BJT is in a particular state, use BJT model for that state to solve the circuit and check the validity of our assumption.

Recipe for solving NPN BJT circuits:

1) Write down a KVL including the BE terminals.

2) Write down a KVL including CE terminal.

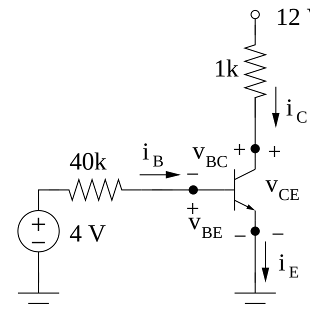
3) Assume BJT is in cut-off (this is the simplest). Set $i_B = 0$. Calculate v_{BE} from BE-KVL.
3a) If $v_{BE} < V_{D0}$, then BJT is in cut-off, $i_B = 0$ and v_{BE} is what you just calculated. Set $i_C = i_E = 0$, and calculate v_{CE} from CE-KVL. You are done.
3b) If $v_{BE} > V_{D0}$, then BJT is not in cut-off. Set $v_{BE} = V_{D0}$. Solve above KVL to find i_B. You should get $i_B > 0$.

4) Assume that BJT is in linear mode. Let $i_E \approx i_C = \beta i_B$. Calculate v_{CE} from CE-KVL.
4a) If $v_{CE} > V_{D0}$, then BJT is in active mode. You are done.
4b) If $v_{CE} < V_{D0}$, then BJT is not in active mode. It is in saturation. Let $v_{CE} = V_{sat}$ and compute i_C from CE-KVL. You should find that $i_C < \beta i_B$. You are done.

For PNP transistors, substitute, v_{BE} with v_{EB} and v_{CE} with v_{EC} in the above recipe.

Note: While in BJT circuits, value of v_{BC} is not calculated (and is not important, value i_E can appear in our equations. In the active mode, $i_E = i_C + i_B = (\beta+1)i_B$ and $i_E = [(\beta+1)/beta]i_C$. Since $\beta \gg 1$, it is convenient to use $i_E \approx i_C$ for simplicity. Note that for a practical BJT circuit even in saturation mode $i_C \gg i_B$ and $i_E \approx i_C$.

Example 1: Compute the parameters of this circuit ($\beta = 100$).



Following the procedure above (for NPN transistor):

$$\text{BE-KVL:} \quad 4 = 40\times 10^3 i_B + v_{BE}$$
$$\text{CE-KVL:} \quad 12 = 10^3 i_C + v_{CE},$$

Assume BJT is in cut-off. Set $i_B = 0$ in BE-KVL:

$$\text{BE-KVL:} \quad 4 = 40\times 10^3 i_B + v_{BE} \quad \rightarrow \quad v_{BE} = 4 > V_{D0} = 0.7 \text{ V}$$

So BJT is not in cut off and BJT is ON. Set $v_{BE} = 0.7\ V$ and use BE-KVL to find i_B.

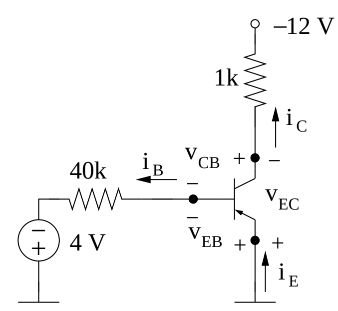
$$\text{BE-KVL:} \quad 4 = 40\times 10^3 i_B + v_{BE} \quad \rightarrow \quad i_B = \frac{4-0.7}{40,000} = 82.5\ \mu\text{A}$$

Assume BJT is in active linear, Find $i_C = \beta i_B$ and use CE-KVL to find v_{CE}:

$$i_C = \beta i_B = 100 i_B = 8.25 \text{ mA}$$
$$\text{CE-KVL:} \quad 12 = 1,000 i_C + v_{CE}, \quad \rightarrow \quad v_{CE} = 12 - 8.25 = 3.75 \text{ V}$$

As $v_{CE} = 3.75 > V_{D0}$, the BJT is indeed in active-linear and we have: $v_{BE} = 0.7$ V, $i_B = 82.5\ \mu$A, $i_E = (\beta+1)i_C = 8.33$ mA, and $v_{CE} = 3.75$ V.

Example 2: Compute the parameters of this circuit ($\beta = 100$).



Following the procedure above (for PNP transistor):

$$\text{BE-KVL:} \quad -4 = -40\times 10^3 i_B - v_{EB}$$
$$\text{CE-KVL:} \quad -12 = -10^3 i_C - v_{EC},$$

Assume BJT is in cut-off. Set $i_B = 0$ in BE-KVL:

$$\text{BE-KVL:} \quad -4 = -40\times 10^3 i_B - v_{EB} \quad \rightarrow \quad v_{EB} = 4 \quad \rightarrow \quad v_{EB} = 4 > V_{D0} = 0.7 \text{ V}$$

So BJT is not in cut off and BJT is ON. Set $v_{EB} = 0.7\ V$ and use BE-KVL to find i_B.

$$\text{BE-KVL:} \qquad -4 = -40 \times 10^3 i_B - v_{EB} \quad \rightarrow \quad i_B = \frac{4 - 0.7}{40,000} = 82.5\ \mu\text{A}$$

Assume BJT is in active mode. Find $i_C = \beta i_B$ and use CE-KVL to find v_{EC}:

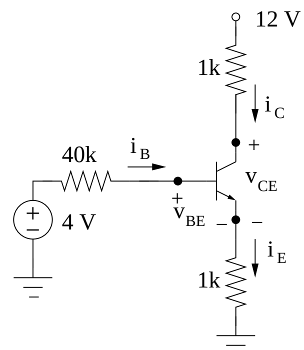
$$i_C = \beta i_B = 100 i_B = 8.25 \text{ mA}$$

$$\text{CE-KVL:} \qquad -12 = -10^3 i_C - v_{EC}, \quad \rightarrow \quad v_{EC} = 12 - 8.25 = 3.75 \text{ V}$$

As $v_{EC} = 3.75 > V_{D0}$, the BJT is indeed in active mode and we have: $v_{EB} = 0.7$ V, $i_B = 82.5\ \mu$A, $i_E = (\beta + 1) i_C = 8.33$ mA, and $v_{EC} = 3.75$ V.

Note: Comparing Examples 1 and 2, they are identical circuits (expect voltages and currents changed sign) one with a NPN transistor and one with a PNP transistor (similar βs). As can be seen all currents and voltages are the same (expect signs).

Example 3: Compute the parameters of this circuit ($\beta = 100$).



$$\text{BE-KVL:} \qquad 4 = 40 \times 10^3 i_B + v_{BE} + 10^3 i_E$$

$$\text{CE-KVL:} \qquad 12 = 1,000 i_C + v_{CE} + 1,000 i_E$$

Assume BJT is in cut-off. Set $i_B = 0$ and $i_E = i_C = 0$ in BE-KVL:

$$\text{BE-KVL:} \qquad 4 = 40 \times 10^3 i_B + v_{BE} + 10^3 i_E \quad \rightarrow \quad v_{BE} = 4 > 0.7 \text{ V}$$

So BJT is not in cut off and $v_{BE} = 0.7$ V and $i_B > 0$. Here, we cannot find i_B right away from BE-KVL as it also contains i_E. Assume BJT is in active linear, $i_E = (\beta + 1) i_B$:

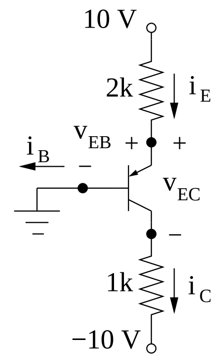
$$\text{BE-KVL:} \qquad 4 = 40 \times 10^3 i_B + v_{BE} + 10^3 (\beta + 1) i_B = 0.7 + (40 \times 10^3 + 10^3 \times 101) i_B$$

$$i_B = 24\ \mu\text{A} \quad \rightarrow \quad i_C = \beta i_B = 2.4 \text{ mA}, \qquad i_E = (\beta + 1) i_B = 2.4 \text{ mA}$$

$$\text{CE-KVL:} \qquad 12 = 1,000 i_C + v_{CE} + 1,000 i_E, \quad \rightarrow \quad v_{CE} = 12 - 4.8 = 7.2 \text{ V}$$

As $v_{CE} = 7.2 > V_{D0}$, the BJT is indeed in active-linear and we have: $v_{BE} = 0.7$ V, $i_B = 24\ \mu$A, $i_E \approx i_C = 2.4$ mA, and $v_{CE} = 7.2$ V.

Example 4: Compute the parameters of the Si transistor ($\beta = 100$) in the circuit below.



Since there is a 10 V supply in the BE-loop, it is a good starting assumption that BJT is ON (PNP: $v_{EB} = V_{D0} = 0.7$ V and $i_B > 0$)

BE-KVL: $\quad 10 = 2 \times 10^3 i_E + v_{EB}$

$$i_E = \frac{10 - 0.7}{2 \times 10^3} = 4.65 \text{ mA}$$

Since $i_E > 0$, the assumption of BE ON is justified (since $i_E > 0$ requires both i_B and $i_C > 0$). Assuming BJT in active:

$$i_E = i_C + i_B = (\beta + 1) i_B \quad \rightarrow \quad i_B = 4.65/101 \simeq 50\ \mu\text{A}$$

$$i_C = i_E - i_B \simeq 4.6 \text{ mA}$$

CE-KVL: $\quad 10 = 2 \times 10^3 i_E + v_{EC} + 10^3 i_C - 10$

$$10 = 9.3 + v_{EC} + 10^3 \times 4.6 \times 10^{-3} - 10 = v_{EC} + 3.9$$

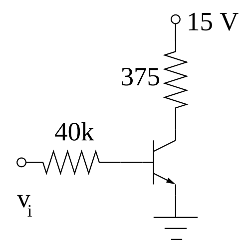
$$v_{EC} = 6.1 \text{ V}$$

Since $v_{EC} = 6.1 > 0.7 = V_{D0}$), the assumption of BJT in active is justified and $v_{EB} = 0.7$ V, $i_B = 50\ \mu$A, $v_{EC} = 6.1$ V, and $i_C = 4.6$ mA,

Load line

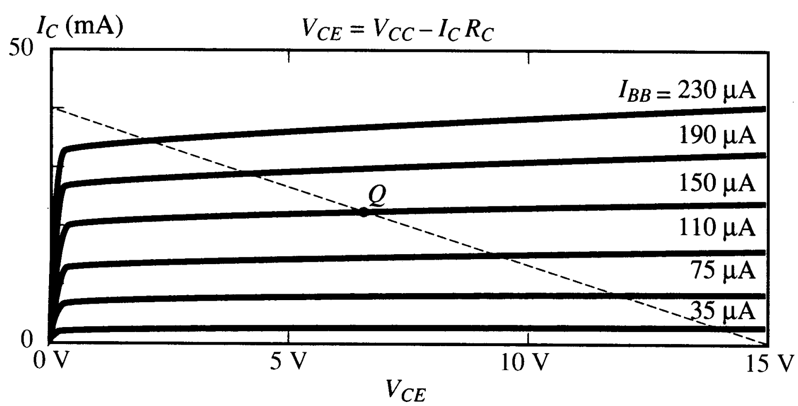
The operating point of a BJT can be found graphically using the concept of a load line (similar to diode load line). For BJTs, the load line is the relationship between i_C and v_{CE} that is imposed on BJT by the external circuit. For a given value of i_B, the $i_C v_{CE}$ characteristics curve of a BJT is the relationship between i_C and v_{CE} as is set by BJT internals. The intersection of the load line with the BJT characteristics represent a pair of i_C and v_{CE} values which satisfy both conditions and, therefore, is the operating point of the BJT (often called the Q point for Quiescent point).

The equation of a load line for a BJT should include only i_C and v_{CE} (no other unknowns). This equation is usually found by writing a KVL around a loop containing v_{CE}. For the circuit shown, we have:



KVL: $\quad 15 = 375 i_C + v_{CE}$

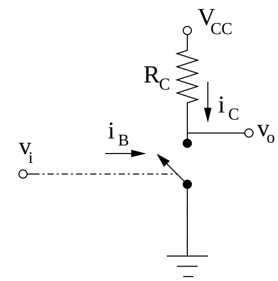
which is the equation of a line in the $i_C v_{CE}$ space. This "load line" and the $i_C v_{CE}$ characteristics lines of the BJT are shown below. The operating point of the BJT (Q-point) is also shown for $i_B = 150$ μA (or $v_i = 6.7$ V in the example above).



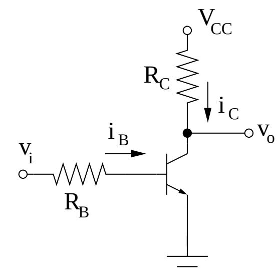
Note that if an emitter resistor is present (*e.g.*, Example 3 in page 3-8), the load line can still be constructed noting that $i_E = [(\beta + 1)/\beta] i_C =\approx i_C$:

KVL: $\quad 12 = 1,000 i_C + v_{CE} + 1,000 i_E \quad \rightarrow \quad 12 \approx 2,000 i_C + v_{CE}$

3.3 BJT Switches and Logic Gates



The basic element of logic circuits is the transistor switch. A schematic of such a switch is shown. When the switch is open, $i_C = 0$ and $v_o = V_{CC}$. When the switch is closed, $v_o = 0$ and $i_C = V_{CC}/R_C$.



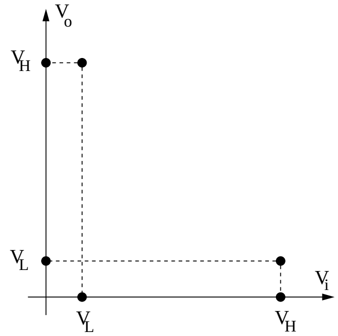
In electronic circuits, mechanical switches are not used. The switching action is performed by a transistor, as is shown. When $v_i = 0$, BJT will be in cut-off, $i_C = 0$, and $v_o = V_{CC}$ (open switch). When v_i is in "high" state, BJT can be in saturation with $v_o = v_{CE} = V_{sat} \approx 0.2$ V and $i_C = (V_{CC} - V_{sat})/R_C$ (closed switch). When R_c is replaced with a load, this circuit can switch a load ON or OFF (see *e.g.,* Problems 12 & 13).

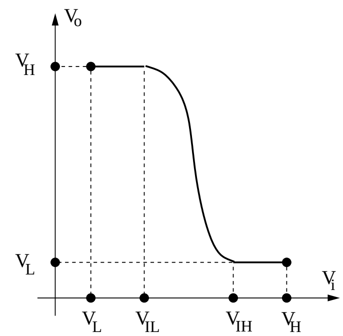
3.3.1 Logic Gates

You have seen binary mathematics and logic gates in ECE25. We will explore some electronic logic gates in this course. Binary mathematics is built upon two states: 0, and 1. We need to relate the binary states to currents or voltages as these are the parameters that we can manipulate in electronic circuits. Similar to our discussion of analog circuits, it is advantageous (from power point of view) to relate these the binary states to voltages. As such, we "choose" two voltages to represent the binary states: v_L for state 0 or Low state and v_H for state 1 or High state (for example, 0 V to represent state 0 and 5 V to represent state 1). These voltages are quite arbitrary and can be chosen to have any value.

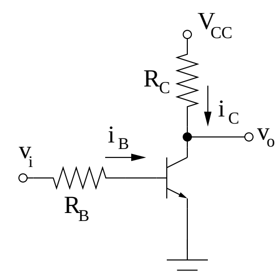
Similar to analog circuits, we plot the voltage transfer function of a gate. For example, the transfer function of an "ideal" inverter is shown in the figure: when the input is low, the output is high and the when the input is high, the output is low. We can see a difficulty right away. In a practical circuit, there would be an output voltage for any input voltage, so the output voltage makes a "smooth" transition for the high voltage to the low voltage as the input voltage is varied. We have to be also careful as it is extremely difficult, if not impossible, to design an electronic circuit to give exactly a voltage value like 5 V (what if the input voltage was 4.99 V?). So, we need to define a range of voltages (instead of one value) to represent high and low states. We will try very hard to make sure that the output of our gates to be as close as possible to V_H and V_L, But, we need to design our gates such that they respond to a range of voltages, *i.e.,* the gate would think that the input is low if the input voltage is smaller than v_{IL} and would think that the input is high if the input voltage is larger than v_{IH} (see figure).

With these definitions, the transfer function of a practical inverter (plot of v_o as a function of v_i) is shown. The range of voltages, v_L to v_{IL} and $_{IH}$ to v_H are called the noise margins. The range of voltages between v_{IL} to v_{IH} is the forbidden region as in this range, the output of the gate does not correspond to any binary state. The maximum speed that a logic gate can operate is set by the time it takes to traverse this region as the input voltage is varied from one state to another state.





3.3.2 Resistor-Transistor Logic (RTL)



The BJT switch circuit discussed above is also an "inverter" or a "NOT" logic gate. This circuit is a member of RTL family of logic gates. Let's assume that the "low" state is at $v_L = 0.2$ V (V_{sat}) and the "high" state is $v_H = V_{CC}$.

To find the transfer function of this gate, we need to find v_o for a range of v_i values. This plot will also help identify the values of v_{IL} and v_{IH}.

From BE-KVL, $v_i = R_B i_B + v_{BE}$, we find that for $v_i < V_{D0}$, BJT will be in cut-off, $i_C = 0$ and $v_o = V_{CC}$ (high state). Therefore, when $v_i = v_L = V_{sat}$, $v_o = V_{CC} = v_H$. Moreover, The output will be high as long as $v_i < V_{D0}$, or $v_{IL} = V_{D0}$. Note that v_{IL} corresponds to the case where $v_{BE} = V_{D0}$ and $i_B > 0$ but small such that the term $i_B R_B$ can be ignored compared to v_{BE}.

When v_i exceeds V_{D0}, BE junction will be forward biased and a current i_B flows into BJT:

$$i_B = \frac{v_i - V_{D0}}{R_B}$$

As BE junction is forward biased, BJT can be either in saturation or active-linear. Let's assume BJT is is in saturation. In that case, $v_o = v_{CE} = V_{sat}$ and $i_C/i_B < \beta$. Then:

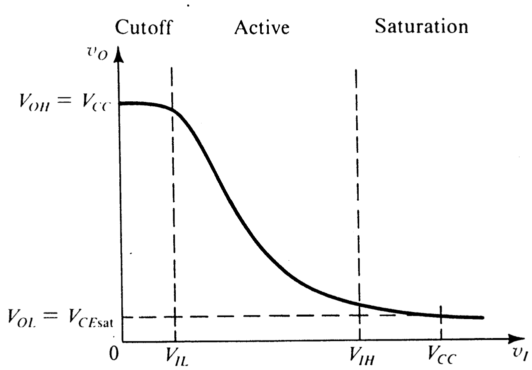
$$i_C = \frac{V_{CC} - V_{sat}}{R_C} \qquad \rightarrow \qquad i_B > \frac{i_C}{\beta} = \frac{V_{CC} - V_{sat}}{\beta R_C}$$

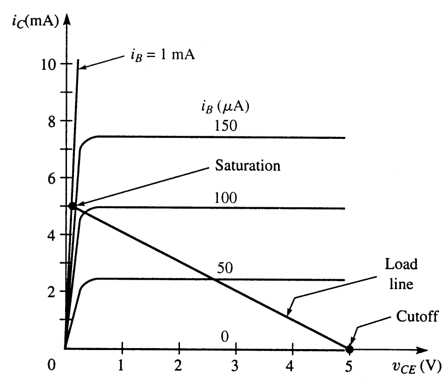
Therefore, BJT will be in saturation only if i_B exceeds the value given by the formula above. This occurs when v_i become large enough:

$$v_i = V_{D0} + R_B i_B > V_{D0} + R_B \times \frac{V_{CC} - V_{sat}}{\beta R_C} = v_{IH}$$

If we choose R_B and R_C such that $v_{IH} < V_{CC}$, then for $vi = V_{CC}$, BJT will be in saturation, and $v_{CE} = V_{sat}$. Overall, for $v_i = v_L = V_{sat}$, $v_o = V_{CC} = v_H$ and for $v_i = v_H = V_{CC}$, $v_o = V_{sat} = v_L$. Thus, this is a NOT gate.

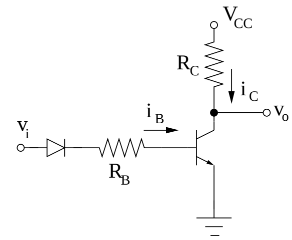
For v_i values between v_{IL} and v_{IH}, the BE junction is forward biased but the BJT is NOT in saturation, and thus, it is in active linear. In this case, the output voltage smoothly changes for its high value to its low value as is shown in the plot of transfer function. This range of v_i is the "forbidden" region and the gate would not work properly in this region. This behavior can also seen in the plot of the BJT load line. For small values of v_i ($i_B = 0$) BJT is in cut-off. As v_i is increased, i_B is increased and the operating point moves to the left and up on the load line and enters the active-linear region. When i_B is raised above certain limit, the operating point enters the saturation region.





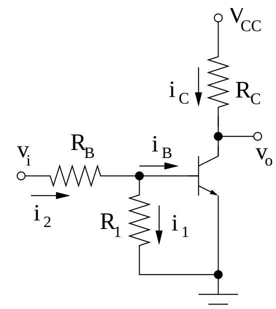
A major drawback of the this RTL inverter gate is the limited input range for the "low" signal (v_{IL}). For "high" state, the noise margin for "high" state can be controlled by adjusting values of R_C and R_B. However, our analysis indicated that $v_{IL} = V_{D0}$, that is the gate input is low for voltages between 0.2 V and $V_{D0} \approx 0.7$ V which is quite a small noise margin. For the above analysis, we have been using a constant-voltage piecewise linear model for the BE junction diode. In reality, the BJT will come out of cut-off (BE junction will conduct) at smaller voltages (~ 0.5 V), making the noise margin for "low" state even smaller.

In order to build a gate with a larger noise margin for "low" voltage, we examine the BE-KVL: $v_i = R_B i_B + v_{BE}$. Note that $v_i = v_{IL}$ corresponds to $v_{BE} = V_{D0}$ and $i_B > 0$ but small. Two approaches are possible: 1) Add an element in series with R_B which would have a large voltage drop for a small current, *e.g.,* a diode, 2) Allow the current in R_B to be larger than i_B. We explore both options below:



For this circuit, BE-KVL gives: $v_i = v_D + R_B i_B + v_{BE}$. Then to find v_{IL}, we substitute for $v_{BE} = V_{D0}$ and $i_B > 0$ but small to get: $v_{IL} \approx v_D + V_{D0}$. Since $i_D = i_B > 0$ but small, the diode should also be forward biased and $v_D = V_{D0}$. Thus, $v_{IL} \approx 2V_{D0} = 1.4$ V. Note that v_{IL} can be increased further in increments of V_{D0} by adding more diodes in the input.

This approach works reasonably well in ICs as the diode and BE junction can be constructed with similar reverse saturation currents. However, for a circuit built with discrete components (*e.g.,* a BJT switch) this approach may not work well as the reverse saturation current for discrete diodes, I_{sD}, is typically 2 to 3 orders of magnitude larger than reverse saturation current for the BE junction. As such, the small current needed to make $v_{BE} \simeq V_{D0}$ only leads to $v_D = 0.2 - 0.3$ V. (see Lab 4 for a solution to this problem).



The second method to increase the noise margin is to add a resistor between the base and ground as is shown. To see the impact of this resistor, note that V_{IL} is the input voltage when BJT is just leaving the cut-off region. At this point, $v_{BE} = V_{D0}$, and i_B is positive but very small (effectively zero). Since a voltage v_{BE} has appeared across R_1, we have:

$$i_1 = \frac{v_{BE}}{R_1} \qquad\qquad i_2 = i_B + i_1 \approx i_1 = \frac{v_{BE}}{R_1}$$

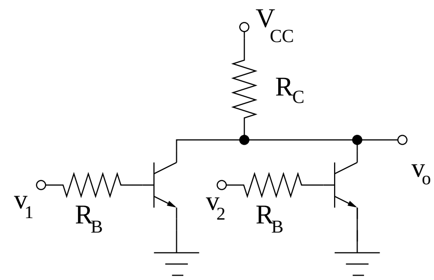
$$v_{IL} = v_i = R_B i_2 + v_{BE} = v_{BE}\frac{R_B}{R_1} + v_{BE} = V_{D0}\left(1 + \frac{R_B}{R_1}\right)$$

This value should be compared with $v_{IL} = V_{D0}$ in the absence of resistor R_1. It can be seen that for $R_B = R_1$, v_{IL} can be raised from 0.7 to 1.4 V. Moreover, arbitrary values of v_{IL} can be achieved by proper choice of R_B and R_1. Typically, R_1 does not affect v_{IH} as i_B needed to put the BJT in saturation is typically several times larger than i_1.

RTL NOR Gate

Logic circuits are typically constructed from "basic" logic gates like NOR or NAND. You have seen in ECE25 that all higher level logic gates, *e.g.,* flip-flops, can be made by a combination of NOR gates or NAND gates. So, for each logic gate that we will work on, we have to remember that the output of the logic gate is attached to the input of another logic gate.

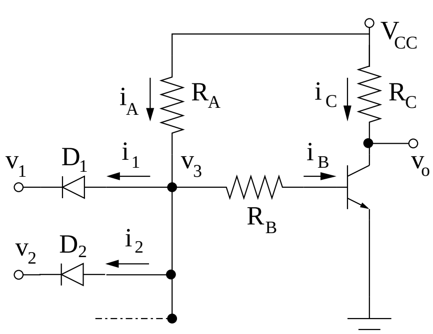
By combining two or more RTL inverters, one obtains the basic logic gate circuit of RTL family, a "NOR" gate, as is shown (see Problem 15). More BJTs can be added for additional input signals.

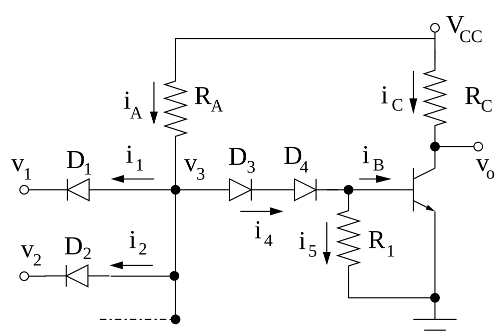


RTLs were the first digital logic circuits using transistors. They require at least one resistor and one BJT per input. They were replaced with diode-transistor logic, DTL (reduced number of resistors and BJTs) and transistor-transistor logic, TTL (which "packs" all of the didoes in a special transistor). Most popular BJT gates today are TTL or emitter coupled logic, ECL. With the advent of CMOS technology, BJT-based gates are now only used for special purpose circuits (for example, high speed gates utilizing ECL).

3.3.3 Diode-Transistor Logic (DTL)

The basic gate of DTL logic circuits is a NAND gate which is constructed by a combination of a diode AND gate (analyzed in pages 2-12) and a BJT inverter gate as is shown below (left figure). Because R_B is large, on ICs, this resistor is usually replaced with two diodes. The combination of the two diodes and the BE junction diode leads to a voltage of 2.1 V for the inverter to switch and a $v_{IL} = 1.4$ V for the NAND gate (Why?). Resistor R_1 is necessary because without this resistor, current i_B will be too small and the voltage across D_3 and D_4 will not reach 0.7 V although they are both forward biased.





Example: Verify that the DTL circuit above (with $R_A = 5$ kΩ, $R_C = 1$ kΩ, $R_1 = 5$ kΩ, and $V_{CC} = 5$ V) is a NAND gate. Assume that "low"state is 0.2 V, "high" state is 5 V, and BJT $\beta_{min} = 40$.

Case 1: $v_1 = v_2 = 0.2$ V   It appears that the 5-V supply will forward bias D_1 and D_2. Assume D_1 and D_2 are forward biased: $v_{D1} = v_{D2} = V_{D0} = 0.7$ V and $i_1 > 0$, $i_2 > 0$. In this case:

$$v_3 = v_1 + v_{D1} = v_2 + v_{D2} = 0.2 + 0.7 = 0.9 \text{ V}$$

Voltage $v_3 = 0.9$ V is not sufficient to froward bias D_3 and D_4 as $v_3 = v_{D3} + v_{D4} + v_{BE}$ and we need at least 1.4 V to forward bias the two diodes. So both D_3 and D_4 are OFF and $i_4 = 0$. (Note that D_3 and D_4 can be forward biased without BE junction being forward biased as long as the current i_4 is small enough such that voltage drop across the 5 kΩ resistor parallel to BE junction is smaller than 0.7 V. In this case, $i_5 = i_4$ and $i_B = 0$.) Then:

$$i_1 + i_2 = i_A = \frac{5 - v_3}{5,000} = \frac{5 - 0.9}{5,000} = 0.82 \text{ mA}$$

And by symmetry, $i_1 = i_2 = 0.5 i_A = 0.41$ mA. Since both i_1 and i_2 are positive, our assumption of D_1 and D_2 being ON are justified. Since $i_4 = 0$, $i_B = 0$ and BJT will be in cut-off with $i_C = 0$ and $v_o = 5$ V.

So, in this case, D_1 and D_2 are ON, D_3 and D_4 are OFF, BJT is in cut-off, and $v_o = 5$ V.

Case 2: $v_1 = 0.2$ V, $v_2 = 5$ V   Following arguments of case 1, assume D_1 is ON. Again, $v_3 = 0.7 + 0.2 = 0.9$ V, and D_3 and D_4 will be OFF with $i_4 = 0$. We find that voltage across D_2 is $v_{D2} = v_3 - v_2 = 0.9 - 5 = -4.1$ V and, thus, D_2 will be OFF and $i_2 = 0$. Then:

$$i_1 = i_A = \frac{5 - v_3}{5,000} = \frac{5 - 0.9}{5,000} = 0.82 \text{ mA}$$

and since $i_1 > 0$, our assumption of D_1 ON is justified. Since $i_4 = 0$, $i_B = 0$ and BJT will be in cut-off with $i_C = 0$ and $v_o = 5$ V.

So, in this case, D_1 is ON, D_2 is OFF, D_3 and D_4 are OFF, BJT is in cut-off, and $v_o = 5$ V.

Case 3: $v_1 = 5$ V, $v_2 = 0.2$ V   Because of the symmetry in the circuit, this is exactly the same as case 2 with roles of D_1 and D_2 reversed.

So, in this case, D_1 is OFF, D_2 is ON, D_3 and D_4 are OFF, BJT is in cut-off, and $v_o = 5$ V.

Case 4: $v_1 = v_2 = 5$ V   Examining the circuit, it appears that the 5-V supply will NOT be able to forward bias D_1 and D_2. Assume D_1 and D_2 are OFF: $i_1 = i_2 = 0$, $v_{D1} < V_{D0}$ and

$v_{D2} < V_{D0}$. On the other hand, it appears that D_3 and D_4 will be forward biased. Assume D_3 and D_4 are forward biased: $v_{D3} = v_{D4} = V_{D0} = 0.7$ V and $i_4 > 0$. Further, assume the BJT is not in cut-off $v_{BE} = V_{D0} = 0.7$ V and $i_B > 0$. In this case:

$$v_3 = v_{D3} + v_{D4} + v_{BE} = 0.7 + 0.7 + 0.7 = 2.1 \text{ V}$$
$$v_{D1} = v_3 - v_1 = 2.1 - 5 = -2.9 \text{ V} < V_{D0} \qquad v_{D2} = v_3 - v_2 = 2.1 - 5 = -2.9 \text{ V} < V_{D0}$$

Thus, our assumption of D_1 and D_2 being OFF are justified. Furthermore:

$$i_4 = i_A = \frac{5 - v_3}{5,000} = \frac{5 - 2.1}{5,000} = 0.58 \text{ mA}$$
$$i_5 = \frac{v_{BE}}{5,000} = \frac{0.7}{5,000} = 0.14 \text{ mA}$$
$$i_B = i_4 - i_5 = 0.58 - 0.14 = 0.44 \text{ mA}$$

and since $i_4 > 0$ our assumption of D_3 and D_4 being ON are justified and since $i_B > 0$ our assumption of BJT not in cut-off is justified.

We still do not know if BJT is in active-linear or saturation. Assume BJT is in saturation: $v_o = v_{CE} = V_{sat} = 0.2$ V and $i_C/i_B < \beta$. Then, assuming no gate is attached to the circuit, we have

$$i_C = \frac{5 - V_{sat}}{1,000} = \frac{5 - 0.2}{1,000} = 4.8 \text{ mA}$$

and since $i_C/i_B = 4.8/0.44 = 11 < \beta = 40$, our assumption of BJT in saturation is justified.

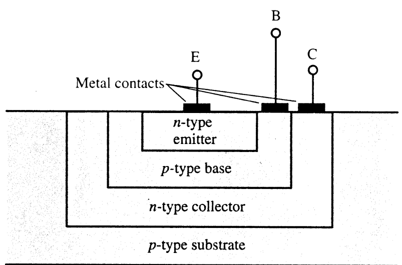
So, in this case, D_1 and D_2 are OFF, D_3 and D_4 are ON, BJT is in saturation and $v_o = 0.2$ V.

Overall, the output in "low" only if both inputs are "high", thus, this is a NAND gate.

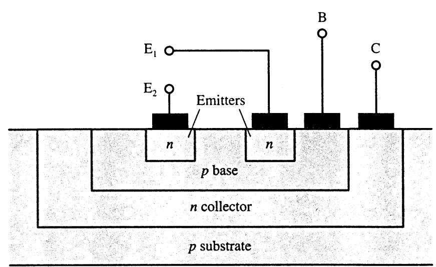
Note: It is interesting to note that at the input of this gate, the current actually flows out of the gate. In the example above, when both inputs were high $i_1 = i_2 = 0$, when both were low $i_1 = i_2 = 0.4$ mA, and when one input was low, *e.g.,* v_1 was low, $i_1 = 0.8$mA. The input current flowing in (or out of the gate in this case) has an important implication as this current should be supplied by the previous logic gate. As such, an important parameter for a logic gate is its "fan-out" (defined as the maximum number of similar gates that can be attached to it).

3.3.4 Transistor-Transistor Logic (TTL)

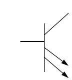
A simplified version of an IC-chip NPN transistor is shown. The device is fabricated on a p-type substrate (or body) in a vertical manner by embedding alternating layers of N and P-type semiconductors. By embedding more than one N-type emitter region, one can obtain a multiple-emitter NPN transistor as shown. The multiple-emitter NPN transistors can be used to replace the input diodes of a DTL NAND gate and arrive at a NAND gate entirely made of transistors, hence Transistor-Transistor Logic (TTL) gates.



(a) IC *npn* transistor



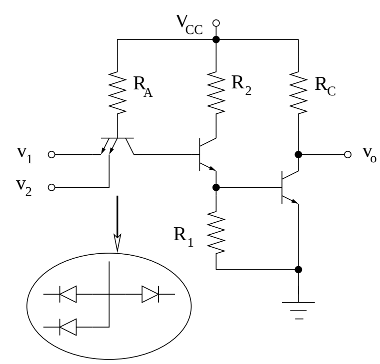
(a) two-emitter IC *npn* transistor



Circuit Symbol

A simple TTL gate is shown with the multiple-emitter BJT replacing the input diodes. This transistor operates in "reverse-active" mode, *i.e.,* like a NPN transistor in active-linear mode but with collector and emitter switched. Operationally, this BJT acts as two diodes back to back as shown in the circle at the bottom of the figure. As such the operation of this gate is essentially similar to the DTL NAND gate described above (note position of driver transistor and D_4 diode is switched).

Similar to DTL NAND gates, a typical TTL NAND gate has three stages: 1) Input stage (multi-emitter transistor), 2) driver stage, and 3) output stage. Modern TTL gates basically have the same configuration as is shown with the exception that the output stage is replaced with the "Totem-Pole" output stage to increase switching speed and gate fan-out. For a detailed description of TTL gate with "Totem-Pole" output stage, consult Sedra and Smith, 6th Ed (page 1191).

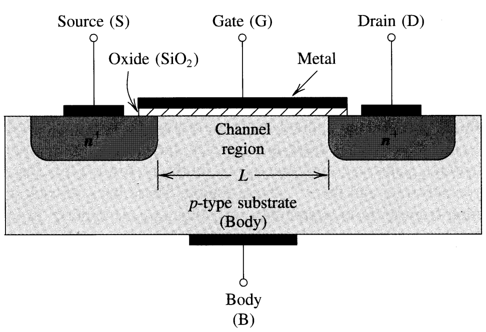


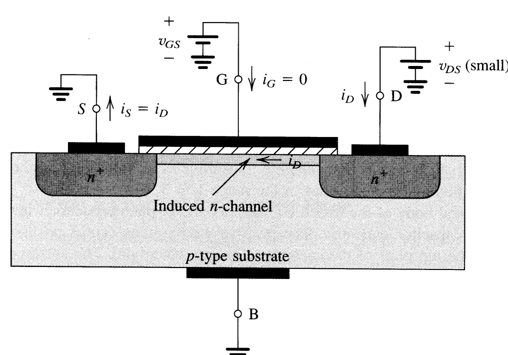
3.4 Field-Effect (FET) Transistors

In a field-effect transistor (FET), the width of a conducting channel in a semiconductor and, therefore, its current-carrying capability, is varied by the application of an electric field (thus, the name field-effect transistor). The most widely used FETs are Metal-Oxide-Semiconductor FETs (MOSFET or MOS for short). MOSFETs can be manufactured as enhancement-type or depletion-type and each can be fabricated either as a n-channel device or a p-channel device. We will focus below on the operation of enhancement MOSFETs that are the most popular (depletion-type) MOS operation is similar to enhancement type. There exists another type of FET, the Junction Field-Effect Transistors (JFET) which is not based on metal-oxide fabrication technique.

n-Channel Enhancement-Type MOSFET (NMOS)

The physical structure of a n-Channel Enhancement-Type MOSFET (NMOS) is shown. The device is fabricated on a p-type substrate (or Body). Two heavily doped n-type regions (Source and Drain) are created in the substrate. A thin (fraction of micron) layer of SiO_2, which is an excellent electrical insulator, is deposited between source and drain region. Metal is deposited on the insulator to form the Gate of the device (thus, metal-oxide semiconductor). Metal contacts are also made to the source, drain, and body region.

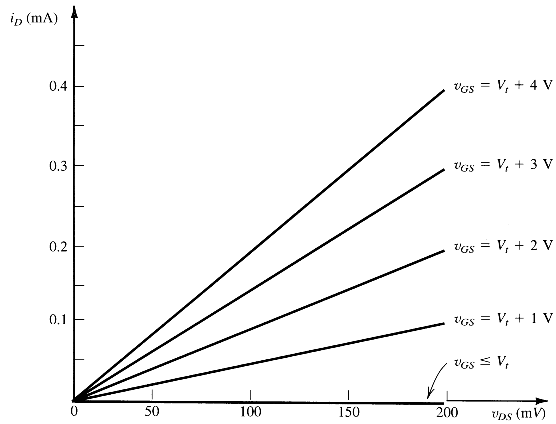




To see the operation of a NMOS, let's ground the source and the body and apply a voltage v_{GS} between the gate and the source, as is shown above. This voltage repels the holes in the p-type substrate near the gate region, lowering the concentration of the holes. As v_{GS} increases, hole concentration decreases, and the region near gate behaves progressively more like intrinsic semiconductor material (when excess hole concentration is zero) and then, finally, like a n-type material as electrons from n^+ electrodes (source and drain) enter this region. As a result, when v_{GS} become larger than a threshold voltage, V_t, a narrow layer between source and drain regions is created that is populated with n-type charges (see figure). The thickness of this channel is controlled by the applied v_{GS} (it is proportional to $v_{GS} - V_t$).

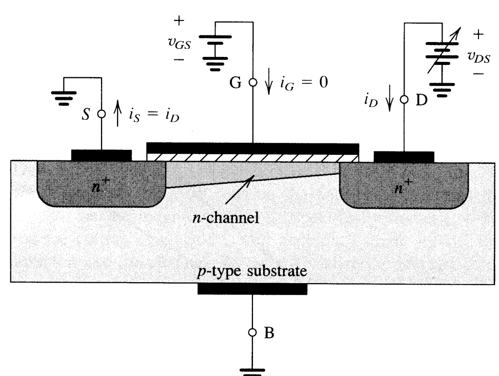
As can be seen, this device works as a channel is induced in the semiconductor and this channel contains n-type charges (thus, n-channel MOSFET). In addition, increasing v_{GS} increases channel width (enhances it). Therefore, this is an n-channel Enhancement-type MOSFET or Enhancement-type NMOS.

Now for a given values of $v_{GS} > V_t$ (so that the channel is formed), let's apply a small and positive voltage v_{DS} between drain and source. Then, electrons from n^+ source region enter the channel and reach the drain. If v_{DS} is increased, current i_D flowing through the channel increases. Effectively, the device acts like a resistor; its resistance is set by the dimension of the channel and its n-type charge concentration. In this mode, plot of i_D versus v_{DS} is a straight line (for a given values of $v_{GS} > V_t$) as is shown.

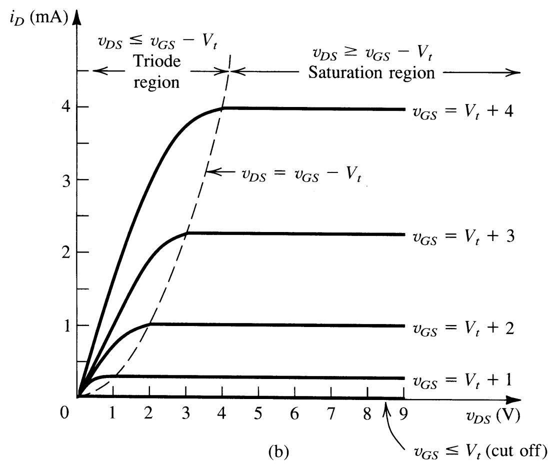


The slope of i_D versus v_{DS} line is the conductance of the channel. For $v_{GS} \leq V_t$ no channel exists (zero conductance). As value of $v_{GS} - V_t$ increases, channel becomes wider and its conductivity increases (because its n-type charge concentration increases). Therefore, the channel conductance (slope of i_D versus v_{DS} line) increases with any increase in $v_{GS} - V_t$ as is shown above.

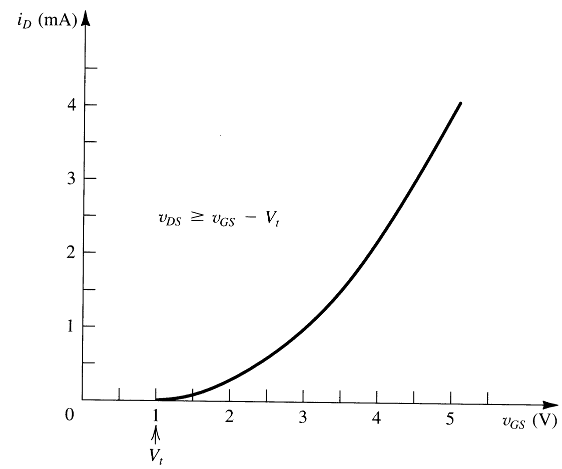
The above description is correct for small values of v_{DS} as in that case, $v_{GD} = v_{GS} - v_{DS} \approx v_{GS}$ and the induced channel is fairly uniform (*i.e.,* has the same width near the drain as it has near the source). For a given $v_{GS} > V_t$, if we now increase v_{DS}, $v_{GD} = v_{GS} - v_{DS}$ becomes smaller than v_{GS}. As such the size of channel near drain becomes smaller compared to its size near the source, as is shown. As the size of channel become smaller, its resistance increases and the curve of i_D versus v_{DS} starts to roll over, as is shown below.



For values of $v_{GD} = V_t$ (or $v_{DS} = v_{GS} - V_t$), width of the channel approaches zero near the drain (channel is "pinched" off). Increasing v_{DS} beyond this value has only a small effect on the channel length, and the current through the channel remains "relatively" constant at the value reached when $v_{DS} = v_{GS} - V_t$. So when the channel is pinched off. i_D only depends on v_{GS} (approximately). In reality, i_D increases slightly when v_{DS} is increased. This effect is called "channel-width modulation" and is similar to Early effect in BJTs



NMOS Characteristic Curves



i_D versus v_{GS} in the saturation (or active) mode

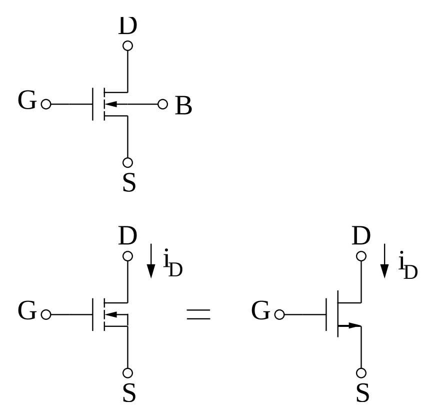
In sum, a MOSFET can operate in three modes:

1) Cut-off mode in which no channel exists ($v_{GS} < V_t$ for NMOS) and $i_D = 0$ for any v_{DS}.

2) Triode or Ohmic mode in which the channel is formed and not pinched off ($v_{GS} > V_t$ and $v_{DS} \le v_{GS} - V_t$ for NMOS).

3) Saturation or Active mode in which the channel is pinched off ($v_{GS} \ge V_t$ and $v_{DS} > v_{GS} - V_t$ for NMOS) and i_D changes little with v_{DS}.

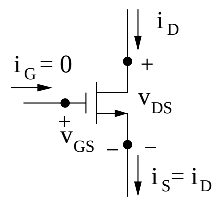
As can be seen from NMOS physical structure, the device is symmetric, that is position of drain and source can be replaced without any change in device properties. The circuit symbol for a NMOS is shown on the right. For most applications, however, the body is connected to the source, leading to a 3-terminal element. In that case, source and drain are not interchangeable. A simplified circuit symbol for this configuration is usually used. By convention, current i_D flows into the drain for a NMOS (see figure). As $i_G = 0$, the same current will flow out of the source.



Direction of "arrows" used to identify semiconductor types in a transistor may appear confusing. The arrows do NOT represent the direction of current flow in the device. Rather, they denote the type of the underlying *pn* junction: arrow pointing inward for *p*-type, arrow pointing outward for *n*-type. For a NMOS, the arrow is placed on the body and pointing inward as the body is made of *p*-type material. (Arrow is not on source or drain as they are interchangeable.) In the simplified symbol for the case when body and source is connected, arrow is on the source (device is not symmetric now) and is pointing outward as the source is made of *n*-type materials. .

3.5 NMOS Large Signal Model

Like BJT, a NMOS (with the source connected to the body) has six circuit parameters (three voltages and three currents), two of which (i_S and v_{GD}) can be found in terms of the other four by KVL and KCL. MOS is simpler than BJT because $i_G = 0$ (and $i_S = i_D$). Therefore, NMOS has one characteristics equation relating i_D to v_{GS} and v_{DS}.



Cut-off:	$v_{GS} < V_{tn},$	$i_D = 0$
Triode:	$v_{GS} > V_{tn}, v_{DS} \leq v_{GS} - V_{tn}$	$i_D = \frac{1}{2}\, k_n' \, \frac{W}{L} \, [2v_{DS}(v_{GS} - V_{tn}) - v_{DS}^2]$
Saturation:	$v_{GS} > V_{tn}, v_{DS} \geq v_{GS} - V_{tn}$	$i_D = \frac{1}{2}\, k_n' \, \frac{W}{L} \, (v_{GS} - V_{tn})^2(1 + \lambda v_{DS})$

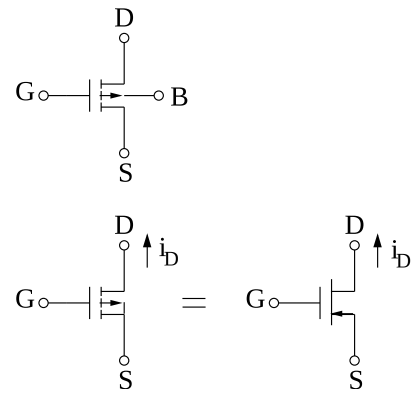
Where V_{tn} is the threshold voltage (subscript n is introduced to differentiate this from that of a PMOS). $k_n' = \mu_n C_{ox}$ where μ_n is the mobility of electrons in the n-type material and C_{ox} is the gate capacitance per unit area (typically in F/m^2). W and L are width and length of the channel, respectively. Parameter λ is the channel-length modulation coefficient. Manufacturers sometime quote the parameter $V_A = 1/\lambda$ (using V_A notation, the channel-length modulation correction formula, $1+v_{DS}/V_A$, becomes similar to that of the Early effect in BJTs). Note that V_A is much larger than the threshold voltage.

As the factor $(1/2)\mu_n C_{ox}(W/L)$ occurs in both formulas, in some text books this quantity is denoted by $K_n = (1/2)\mu_n C_{ox}(W/L)$. Unfortunately, in some text book, $k_n = \mu_n C_{ox}(W/L)$ is introduced (Note $K_n = 0.5k_n$!). To avoid confusion while minimizing notation, we follow Sedra and Smith notation here and have defined $k_n' = \mu_n C_{ox}$

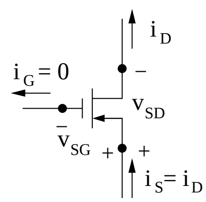
As mentioned above, for small values of v_{DS} ($v_{DS} \ll v_{GS} - V_{tn}$), NMOS behaves as resistor, r_{DS}, and the value of r_{DS} is controlled by $v_{GS} - V_{tn}$. This can be seen by dropping v_{DS}^2 in i_D equation of triode mode:

$$r_{DS} = \frac{v_{DS}}{i_D} \approx \frac{1}{k_n'(W/L)(v_{GS} - V_{tn})}$$

p-Channel Enhancement-Type MOSFET (PMOS)



The physical structure of a PMOS is identical to a NMOS except that the semiconductor types are interchanged, *i.e.,* body and gate are made of n-type material and source and drain are made of p-type material and a p-type channel is formed. As the sign of the charge carriers are reversed, all voltages and currents in a PMOS are reversed. By convention, the drain current is flowing out of the drain as is shown. With this, all of the NMOS discussion above applies to PMOS as long as we multiply all voltages by a minus sign:



Cut-off:	$v_{SG} < \lvert V_{tp}\rvert,$	$i_D = 0$
Triode:	$v_{SG} > \lvert V_{tp}\rvert, v_{SD} \leq v_{SG} - \lvert V_{tp}\rvert$	$i_D = \dfrac{1}{2}\, k_p' \, \dfrac{W}{L}\, [2v_{SD}(v_{SG} - \lvert V_{tp}\rvert) - v_{SD}^2]$
Saturation:	$v_{SG} > \lvert V_{tp}\rvert, v_{SD} \geq v_{SG} - \lvert V_{tp}\rvert$	$i_D = \dfrac{1}{2}\, k_p' \, \dfrac{W}{L}\, (v_{SG} - \lvert V_{tp}\rvert)^2 (1 + \lambda v_{SD})$

Note that V_{tp} is negative for a PMOS and $k_p' = \mu_p C_{ox}$ where μ_p is the mobility of holes.

Several important point should be noted:

1) No current flows into the gate, $i_G = 0$ (note the insulator between gate and the body).

2) When MOSFET is in cut-off, $i_D = 0$. However, $i_D = 0$, does not mean that MOSFET is in cut-off. MOSFET is in cut-off only when no channel exists ($v_{GS} < V_t$) and $i_D = 0$ for any applied v_{DS}. However, MOSFET can be in triode mode, *i.e.,* a channel is formed, but $i_D = 0$ because $v_{DS} = 0$.

3) The MOSFET saturation mode is called "saturation" because i_D is "saturated" (does not change with v_{DS} if we ignore channel length modulation effect). This mode is equivalent to the BJT active mode and not to the BJT saturation mode. As such, some of the modern books call this mode, active.

4) The $i_D v_{DS}$ characteristic curves of a MOSFET look similar to $i_C v_{CE}$ curves of a BJT. Both devices are in cut-off when the "input" voltage is below a threshold value: $v_{BE} < V_{D0}$ for NPN BJT and $v_{GS} < V_{tn}$ for NMOS. They exhibit an active mode in which the "output" current (i_C or i_D) is proportional to the input voltage. There are, however, major differences. Most importantly, a BJT requires i_B to operate but in a MOSFET $i_G = 0$ (actually very small). These differences become clearer as we explore MOSFETs.

Recipe for solving NMOS & PMOS Circuits:

Solution method is very similar to BJT circuit. For a NMOS circuit :

1) Write down a KVL including GS terminals (call it GS-KVL) and a KVL including DS terminals (call it DS-KVL).

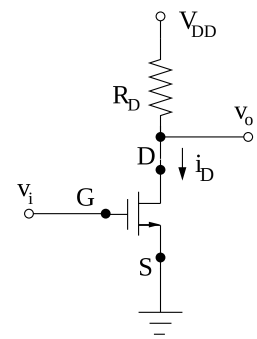
3) From GS-KVL, compute v_{GS} (using $i_G = 0$)
3a) If $v_{GS} < V_{tn}$, NMOS is in cut-off. Let $i_D = 0$, solve for v_{DS} from DS-KVL. We are done.
3b) If $v_{GS} > V_{tn}$, NMOS is not in cut-off. Go to step 4.

4) Assume NMOS is in saturation mode. Compute i_D for NMOS equation Then, use DS-KVL to compute v_{DS}. If $v_{DS} > v_{GS} - V_{tn}$, we are done. Otherwise go to step 5.

5) NMOS has to be in triode mode. Substitute for i_D from NMOS equation in DS-KVL to get a quadratic equation in v_{DS}. Find v_{DS} (one of the two roots would be unphysical). Check that $v_{DS} < v_{GS} - V_{tn}$. Substitute v_{DS} in DS-KVL to find i_D.

(For PMOS, replace v_{GS}, v_{DS}, and V_{tn} with v_{SG}, v_{SD}, and $|V_{tp}|$ in the NMOS recipe.)

Example: Consider NMOS circuit below with $k'_n(W/L) = 0.5$ mA/V^2, $V_{tn} = 2$ V, and $\lambda = 0$. Find v_o when $v_i = 0$, 6, and 12 V for $R_D = 1$ KΩ and $V_{DD} = 12$ V.



GS-KVL: $\quad v_{GS} = v_i$

DS-KVL: $\quad V_{DD} = R_D i_D + v_{DS}$

A) $v_i = 0$ V. From GS-KVL, we get $v_{GS} = v_i = 0$. As $v_{GS} < V_{tn} = 2$ V, NMOS is in cut-off, $i_D = 0$, and v_{DS} is found from DS-KVL:

DS-KVL: $\quad v_o = v_{DS} = V_{DD} - R_D i_D = 12$ V

B) $v_i = 6$ V. From GS-KVL, we get $v_{GS} = v_i = 6$ V. Since $v_{GS} = 6 > V_{tn} = 2$, NMOS is not in cut-off. Assume NMOS in saturation mode. Then:

$$i_D = 0.5k'_n(W/L)(v_{GS} - V_{tn})^2 = 0.25 \times 10^{-3}(6-2)^2 = 4 \text{ mA}$$

DS-KVL: $\quad v_{DS} = V_{DD} - R_D i_D = 12 - 4 \times 10^3 \times 10^{-3} = 8$ V

Since $v_{DS} = 8 > v_{GS} - V_{tn} = 4$, NMOS is indeed in saturation mode and $i_D = 4$ mA and $v_o = v_{DS} = 8$ V.

C) $v_i = 12$ V. From GS-KVL, we get $v_{GS} = 12$ V. Since $v_{GS} > V_{tn}$, NMOS is not in cut-off. Assume NMOS in saturation mode. Then:

$$i_D = 0.5k'_n(W/L)(v_{GS} - V_{tn})^2 = 0.25 \times 10^{-3}(12-2)^2 = 25 \text{ mA}$$

DS-KVL: $\quad v_{DS} = V_{DD} - R_D i_D = 12 - 25 \times 10^3 \times 10^{-3} = -13$ V

Since $v_{DS} = -13 < v_{GS} - V_{tn} = 12 - 2 = 10$, NMOS is NOT in saturation mode.

Assume NMOS in triode mode. Then:

$$i_D = 0.5k'_n(W/L)[2v_{DS}(v_{GS} - V_{tn}) - v_{DS}^2] = 0.25 \times 10^{-3}[2v_{DS}(12-2) - v_{DS}^2]$$
$$i_D = 0.25 \times 10^{-3}[20v_{DS} - v_{DS}^2]$$

Substituting for i_D in DS-KVL, we get:

DS-KVL: $\quad V_{DD} = R_D i_D + v_{DS} \quad \rightarrow \quad 12 = 10^3 \times 0.25 \times 10^{-3}[20v_{DS} - v_{DS}^2] + v_{DS}$

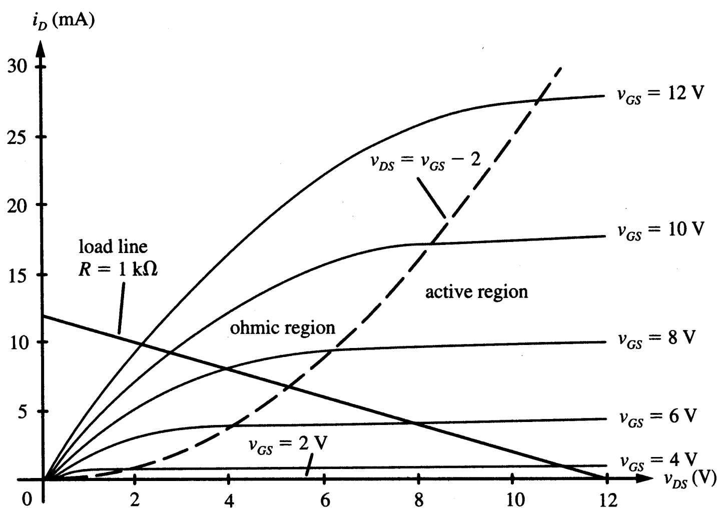
$$v_{DS}^2 - 24v_{DS} + 48 = 0$$

This is a quadratic equation in v_{DS}. The two roots are: $v_{DS} = 2.2$ V and $v_{DS} = 21.8$ V. The second root is not physical as the circuit is powered by a 12 V supply. Therefore, $v_{DS} = 2.2$ V. As $v_{DS} = 2.2 < v_{GS} - V_{tn} = 10$, NMOS is indeed in triode mode with $v_o = v_{DS} = 2.2$ V and

$$\text{DS-KVL:} \qquad v_{DS} = V_{DD} - R_D i_D \quad \rightarrow \quad i_D = \frac{12 - 2.2}{1,000} = 9.8 \text{ mA}$$

Load Line: Operation of NMOS circuits can be better understood using the concept of load line. Similar to BJT, load line is basically the line representing DS-KVL in i_D versus v_{DS} space. Load line of the example circuit is shown here.

Exercise: Mark the Q-points of the previous example for $v_i = 0$, 6, and 12 V on the load line figure below.



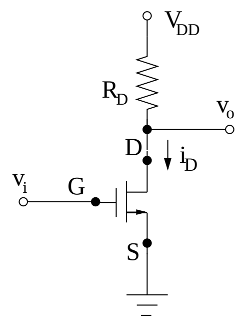
(b)

Body Effect

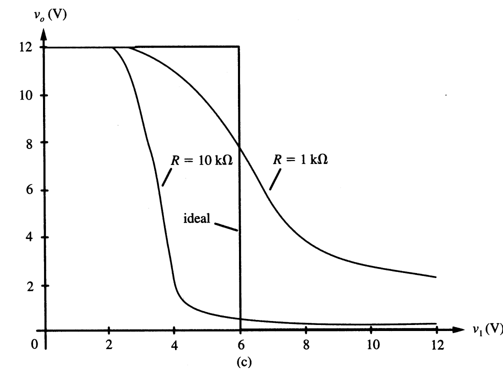
In deriving NMOS (and other MOS) i_D versus v_{DS} characteristics, we had assumed that the body and source are connected. This is not possible in an integrated chip which has a common body and a large number of MOS devices (connection of body to source for all devices means that all sources are connected). The common practice is to attach the body of the chip to the smallest voltage available from the power supply (zero or negative). In this case, the pn junction between the body and source of all devices will be reverse biased. The impact of this to lower threshold voltage for the MOS devices slightly and its called the body effect. Body effect can degrade device performance. For analysis here, we will assume that body effect is negligible.

3.6 MOSFET Inverters and Switches

NMOS Inverters and Switches



The basic NMOS inverter circuit is shown; the circuit is very similar to a BJT inverter. This circuit was solved in page 3-24 for $V_{DD} = 12$ and $R_D = 1$ kΩ. We found that if $v_i = 0$ (in fact $v_i < V_{tn}$), NMOS will be in cut-off with $i_D = 0$ and $v_o = V_{DD}$. When $v_i = 12$ V, NMOS will be in triode mode with $i_D = 10$ mA and $v_{DS} = 2.2$ V. Therefore, the circuit is an inverter gate. It can also be used as switch.

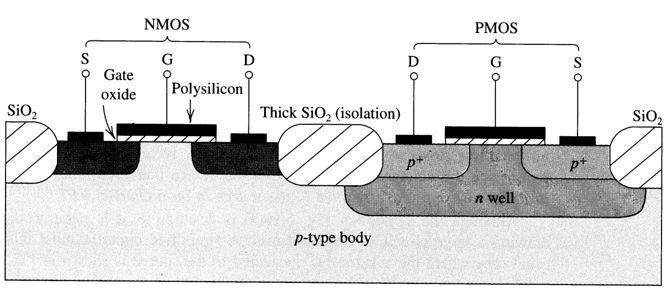


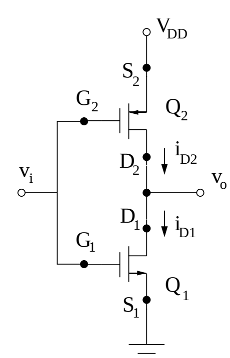
There are some important difference between NMOS and BJT inverter gates. First, BJT needs a resistor R_B. This resistor "converts" the input voltage into an i_B and keep $v_{BE} \approx V_{D0}$. NMOS does not need a resistor between the source and the input voltage as $i_G = 0$ and $v_i = v_{GS}$ can be directly applied to the gate. Second, if the input voltage is "high," the BJT will go into saturation with $v_o = v_{CE} = V_{sat} = 0.2$ V. In the NMOS gate, if the input voltage is "high," NMOS is in the triode mode. In this case, v_{DS} can have any value between 0 and $v_{GS} - V_t$; the value of $v_o = v_{DS}$ is set by the value of the resistor R_D. This effect is shown in the figure.

Exercise: Compute v_o for the above circuit with $V_{DD} = 12$ and $R_D = 10$ kΩ when $v_i = 12$ V.

Complementary MOS (CMOS)

Complementary MOS technology employs MOS transistors of both polarities as is shown below. CMOS devices are more difficult to fabricate than NMOS, but many more powerful circuits are possible with CMOS configuration. As such, most of MOS circuits today employ CMOS configuration and CMOS technology is rapidly taking over many applications that were possible only with bipolar devices a few years ago.





CMOS Inverter

The CMOS inverter, the building block of CMOS logic gates, is shown below. The "low" and "high"states for this circuit correspond to 0 and V_{DD}, respectively. CMOS gates are built on the same chip such that both NMOS and PMOS have the same threshold voltage $V_{tn} = \bar{V}_t$, $V_{tp} = -\bar{V}_t$ ($|V_{tp}| = \bar{V}_t$). This circuit works only if $V_{DD} > 2V_t$ by a comfortable margin.

1) by KVL $v_{GS1} = v_i$, $v_{SG2} = V_{DD} - v_i$, $v_o = v_{DS1} = V_{DD} - v_{SD2}$,

2) by KCL $i_{D1} = i_{D2}$

$\underline{v_i = 0}$ Since $v_{GS1} = v_i = 0 < \bar{V}_t$, NMOS will be in cut-off. Therefore, $i_{D1} = 0$. Since $v_{SG2} = V_{DD} - v_i = V_{DD} > \bar{V}_t$, PMOS will be ON while $i_{D2} = i_{D1} = 0$.

$$\begin{array}{llll} v_{GS1} = v_1 = 0 < \bar{V}_t & \rightarrow \text{ Q1 is OFF} & \rightarrow & i_{D1} = 0 \\ v_{GS2} = V_{DD} - v_i = V_{DD} > \bar{V}_t & \rightarrow \text{ Q2 is ON} & & \end{array}$$

Since PMOS is ON, a channel is formed between its source and drain. In this case, $i_{D2} = 0$ only if $v_{SD2} = 0$ and PMOS is in triode mode and acts as resistor. (Recall i_D versus v_{DS} characteristic curves of a MOSFET, each labeled with a values of $V_{GS} > \bar{V}_t$. This lines cross $i_D = 0$, $v_{DS} = 0$ point when MOSFET is in triode region.)

$$\begin{array}{lllll} v_{GS1} = v_1 = 0 < \bar{V}_t & \rightarrow \text{ Q1 is OFF} & \rightarrow & i_{D1} = 0 & \\ v_{GS2} = V_{DD} - v_i = V_{DD} > \bar{V}_t & \rightarrow \text{ Q2 is ON} & & i_{D2} = 0 & \rightarrow \quad v_{SD2} = 0 \end{array}$$

Output voltage can now be found by KVL: $v_o = V_{DD} - v_{SD2} = V_{DD}$. So, when $v_i = 0$, $v_o = V_{DD}$.

$\underline{v_i = V_{DD}}$ Since $v_{GS1} = v_i = V_{DD} > \bar{V}_t$, NMOS will be ON. Since $v_{SG2} = V_{DD} - v_i = 0 < \bar{V}_t$, PMOS will be in cut-off and $i_{D2} = 0$.

$$\begin{array}{llll} v_{GS1} = v_1 = V_{DD} > \bar{V}_t & \rightarrow \text{ Q1 is ON} & & \\ v_{GS2} = v_i - V_{DD} = 0 < \bar{V}_t & \rightarrow \text{ Q2 is ON} & \rightarrow & i_{D2} = 0 \end{array}$$

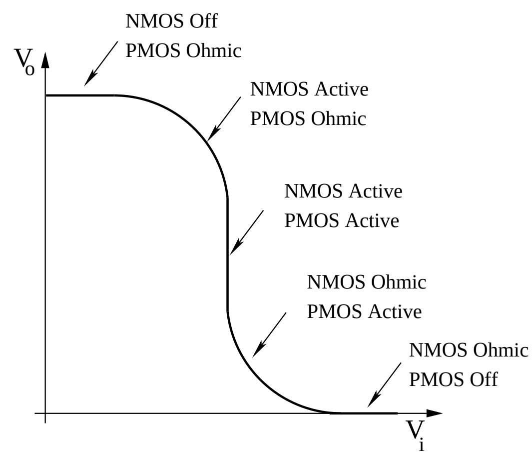
Since $i_{D1} = i_{D2} = 0$ and NMOS is ON, NMOS should be in triode mode with $v_{DS1} = 0$.

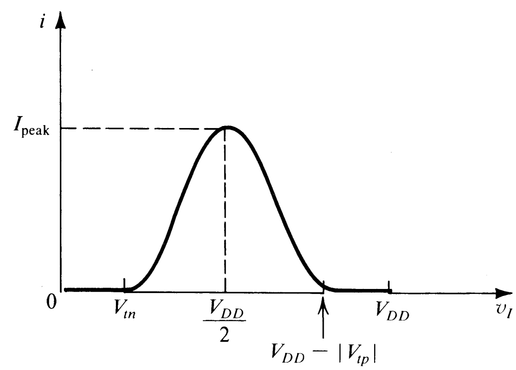
$$\begin{array}{lllll} v_{GS1} = v_1 = V_{DD} > \bar{V}_t & \rightarrow \text{ Q1 is ON} & & i_{D1} = 0 & \rightarrow \quad v_{SD1} = 0 \\ v_{GS2} = v_i - V_{DD} = 0 < \bar{V}_t & \rightarrow \text{ Q2 is ON} & \rightarrow & i_{D2} = 0 & \end{array}$$

Then $v_o = v_{DS1} = 0$. So, when $v_i = V_{DD}$, $v_o = 0$

In sum, when $v_i = 0$, $v_o = V_{DD}$ and when $v_i = V_{DD}$, $v_o = 0$. Therefore, this is an inverter (or a NOT gate). The transfer function of the CMOS inverter is shown below.

CMOS inverter has many advantages compared to the NMOS (or BJT) inverter. The "low" and high" states are clearly defined (low state of NMOS depended on the value of R_D). It does not include any resistors and thus takes less area on the chip. Lastly, $i_{D1} = i_{D2} = 0$ for both cases of output being low or high. This means that the gate consumes very little power (theoretically zero) in either state. A non-zero $i_{D1} = i_{D2}$, however, flows in the circuit when the gate is transitioning from one state to another as is seen in the figure.



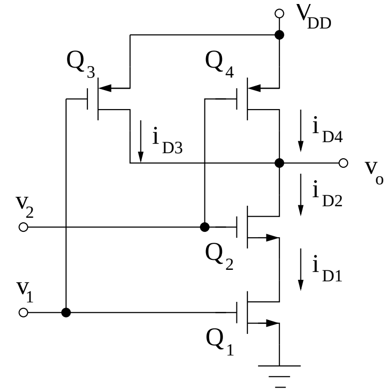


If the transistors have the same $k'_n(W/L)_n = k'_p(W/L)_p$, the CMOS will have a "symmetric" transfer function, *i.e.,* $v_o = 0.5V_{DD}$ when $v_i = 0.5V_{DD}$ as is shown below. For $v_i = 0.5V_{DD}$, $v_{GS1} = v_i = 0.5V_{DD}$ and $v_{SG2} = V_{DD} - v_i = 0.5V_{DD}$. Since, $v_{GS1} = v_{SG2} > \bar{V}_t$, both transistors will be ON. Furthermore, as transistors have same threshold voltage, same $k'(W/L)$, $i_{D1} = i_{D2}$, and $v_{GS1} = v_{SG2}$, both transistor will be in the same state (either triode or saturation) and will have identical v_{DS}: $v_{DS1} = v_{SD2}$. Since $v_{DS1} - v_{SD2} = V_{DD}$, then $v_{DS1} = 0.5V_{DD}$, $v_{SD2} = -0.5V_{DD}$, and $v_o = 0.5V_{DD}$. Note that since $V_{DD} > 2V_t$, both transistors are in the saturation mode. In this case, the maximum value of i_D that flows through the gate occurs when $v_i = 0.5V_{DD}$ and $v_o = 0.5V_{DD}$.

For example, consider the CMOS inverter with $V_{DD} = 12$ V, $\bar{V}_t = 2$ V, and $k'_n(W/L)_n = k'_p(W/L)_p = 0.5$ mA/V^2. Maximum i_D flows when $v_i = v_{GS1} = 0.5V_{DD} = 6$ V. At this point, $v_{DS1} = v_o = 0.5V_{DD} = 6$ V. As, $v_{DS1} = 6 > v_{GS1} - V_t = 4$ V, NMOS is in saturation mode. Then:

$$i_{D1} = 0.5k'_n(W/L)_n(v_{GS1} - V_{tn})^2 = 0.25 \times 10^{-3}(6 - 2)^2 = 4 \text{ mA}$$

CMOS NAND Gate



As mentioned before CMOS logic gates have "low" and "high" states of 0 and V_{DD}, respectively. We need to consider all possible cases to show that this a NAND gate. To start, we can several general observations:

1) by KVL $v_{GS1} = v_1$, $v_{GS2} = v_2 - v_{DS1}$, $v_{SG3} = V_{DD} - v_1$, and $v_{SG4} = V_{DD} - v_2$,

2) by KCL $i_{D1} = i_{D2} = i_{D3} + i_{D4}$

3) by KVL $v_o = v_{DS1} + v_{DS2} = V_{DD} - v_{SD3}$ and $v_{SD3} = v_{SD4}$.

The procedure to solve/analyze CMOS gates are as follows:
A) For a given set of input voltages, use KVLs (1 above) to find v_{GS} of all transistors and find which ones are ON or OFF.
B) Set $i_D = 0$ for all transistors that are OFF. Use KCLs to find i_D for other transistors.
C) Look for transistors that are ON and have $i_D = 0$. These transistors have to be in triode mode with $v_{DS} = 0$.
D) Use KVLs (3 above) to find v_o based on v_{DS}.

$\underline{v_1 = 0,\ v_2 = 0}$ We first find v_{GS} and state of all transistors by using KVLS in no. 1 above.

$$\begin{array}{lll}
v_{GS1} = v_1 = 0 < \bar{V}_t & \rightarrow & \text{Q1 is OFF} \rightarrow i_{D1} = 0 \\
v_{GS2} = v_2 - v_{DS1} = -v_{DS1} & \rightarrow & \text{Q2 is ?} \\
v_{SG3} = V_{DD} - v_1 = V_{DD} > \bar{V}_t & \rightarrow & \text{Q3 is ON} \\
v_{SG4} = V_{DD} - v_2 = -V_{DD} > \bar{V}_t & \rightarrow & \text{Q4 is ON}
\end{array}$$

Since $i_{D1} = 0$, by KCLs in no. 2 above , $i_{D2} = i_{D1} = 0$ and $i_{D3} + i_{D4} = i_{D1} = 0$. Since $i_D \geq 0$ for both PMOS and NMOS, the last equation can be only satisfied if $i_{D3} = i_{D4} = 0$. We add the value of i_D to the table above and look for transistors that are ON and have $i_D = 0$. These transistors (Q3 and Q4) have to be in triode mode with $v_{SD3} = v_{SD4} = 0$.

$$\begin{array}{lllll}
v_{GS1} = v_1 = 0 < \bar{V}_t & \rightarrow & \text{Q1 is OFF} \rightarrow & i_{D1} = 0 & \\
v_{GS2} = v_2 - v_{DS1} = -v_{DS1} & \rightarrow & \text{Q2 is ?} & i_{D2} = 0 & \\
v_{SG3} = V_{DD} - v_1 = V_{DD} > \bar{V}_t & \rightarrow & \text{Q3 is ON} & i_{D3} = 0 & \rightarrow v_{SD3} = 0 \\
v_{SG4} = V_{DD} - v_2 = -V_{DD} > \bar{V}_t & \rightarrow & \text{Q4 is ON} & i_{D4} = 0 & \rightarrow v_{SD4} = 0
\end{array}$$

Finally, from KVLs in no. 3. above, we have $v_o = V_{DD} - v_{SD3} = V_{DD}$. So, when both inputs are low, the output is HIGH.

If needed, we can go back and find the state of Q2. Assume Q2 is ON. This requires $v_{GS2} > \bar{V}_t$. Since $i_{D2} = 0$ and Q2 is ON, $v_{DS2} = 0$ (Q2 in triode). From KVLs in no. 3.

above, we have $v_o = v_{DS1} + v_{DS2} = V_{DD}$. This gives $v_{DS1} = V_{DD}$ and $v_{GS2} = v_2 - v_{DS1} = 0 - V_{DD} = -V_{DD} < \bar{V}_t$, a contradiction of of Q2 being ON. Therefore, Q2 should be OFF.

<u>$v_1 = 0$, $v_2 = V_{DD}$</u>

$$
\begin{array}{lclcl}
v_{GS1} = v_1 = 0 < \bar{V}_t & \rightarrow & \text{Q1 is OFF} & \rightarrow & i_{D1} = 0 \\
v_{GS2} = v_2 - v_{DS1} = V_{DD} - v_{DS1} & \rightarrow & \text{Q2 is ?} & & \\
v_{SG3} = V_{DD} - v_1 = V_{DD} > \bar{V}_t & \rightarrow & \text{Q3 is ON} & & \\
v_{SG4} = V_{DD} - v_2 = 0 < \bar{V}_t & \rightarrow & \text{Q4 is OFF} & \rightarrow & i_{D4} = 0
\end{array}
$$

Since $i_{D1} = 0$, by KCLs in no. 2 above , $i_{D2} = i_{D1} = 0$. Also, $i_{D3} + i_{D4} = i_{D1} = 0$ leading to $i_{D3} = 0$. We add the value of i_D to the table above and look for transistors that are ON and have $i_D = 0$. This transistor (Q3) have to be in triode mode with $v_{SD3} = 0$.

$$
\begin{array}{lclclcl}
v_{GS1} = v_1 = 0 < \bar{V}_t & \rightarrow & \text{Q1 is OFF} & \rightarrow & i_{D1} = 0 & & \\
v_{GS2} = v_2 - v_{DS1} = V_{DD} - v_{DS1} & \rightarrow & \text{Q2 is ?} & & i_{D2} = 0 & & \\
v_{SG3} = V_{DD} - v_1 = V_{DD} > \bar{V}_t & \rightarrow & \text{Q3 is ON} & & i_{D3} = 0 & \rightarrow & v_{SD3} = 0 \\
v_{SG4} = V_{DD} - v_2 = 0 < \bar{V}_t & \rightarrow & \text{Q4 is OFF} & \rightarrow & i_{D4} = 0 & &
\end{array}
$$

Finally, $v_o = V_{DD} - v_{SD3} = V_{DD}$. So, when v_1 is LOW and v_2 is HIGH, the output is HIGH.

We can go back and find the state of Q2. We will find Q2 to be OFF (left as an exercise).

<u>$v_1 = V_{DD}$, $v_2 = 0$</u>

$$
\begin{array}{lclcl}
v_{GS1} = v_1 = V_{DD} > \bar{V}_t & \rightarrow & \text{Q1 is ON} & & \\
v_{GS2} = v_2 - v_{DS1} = -v_{DS1} < \bar{V}_t & \rightarrow & \text{Q2 is OFF} & \rightarrow & i_{D2} = 0 \\
v_{SG3} = V_{DD} - v_1 = 0 < \bar{V}_t & \rightarrow & \text{Q3 is OFF} & \rightarrow & i_{D3} = 0 \\
v_{SG4} = V_{DD} - v_2 = V_{DD} > \bar{V}_t & \rightarrow & \text{Q4 is ON} & &
\end{array}
$$

In the above, we used the fact that $v_{DS1} \geq 0$. Since $i_{D2} = 0$, by KCLs, $i_{D1} = i_{D2} = 0$. Also, $i_{D3} + i_{D4} = i_{D2} = 0$ leading to $i_{D4} = 0$. We add the value of i_D to the table above and look for transistors that are ON and have $i_D = 0$. These transistors (Q1 and Q4) have to be in triode mode with $v_{DS1} = v_{SD4} = 0$.

$$
\begin{array}{lclclcl}
v_{GS1} = v_1 = V_{DD} > \bar{V}_t & \rightarrow & \text{Q1 is ON} & & i_{D1} = 0 & \rightarrow & v_{DS1} = 0 \\
v_{GS2} = v_2 - v_{DS1} = -v_{DS1} < \bar{V}_t & \rightarrow & \text{Q2 is OFF} & \rightarrow & i_{D2} = 0 & & \\
v_{SG3} = V_{DD} - v_1 = 0 < \bar{V}_t & \rightarrow & \text{Q3 is OFF} & \rightarrow & i_{D3} = 0 & & \\
v_{SG4} = V_{DD} - v_2 = V_{DD} > \bar{V}_t & \rightarrow & \text{Q4 is ON} & & i_{D4} = 0 & \rightarrow & v_{SD4} = 0
\end{array}
$$

Finally, $v_o = V_{DD} - v_{SD4} = V_{DD}$. So, when v_1 is HIGH and v_2 is LOW, the output is HIGH.

$\underline{v_1 = V_{DD},\, v_2 = V_{DD}}$

$$
\begin{array}{llll}
v_{GS1} = v_1 = V_{DD} > \bar{V}_t & \rightarrow \quad \text{Q1 is ON} & & \\
v_{GS2} = v_2 - v_{DS1} = V_{DD} - v_{DS1} & \rightarrow \quad \text{Q2 is ?} & & \\
v_{SG3} = V_{DD} - v_1 = 0 < \bar{V}_t & \rightarrow \quad \text{Q3 is OFF} & \rightarrow & i_{D3} = 0 \\
v_{SG4} = V_{DD} - v_2 = 0 < \bar{V}_t & \rightarrow \quad \text{Q4 is OFF} & \rightarrow & i_{D4} = 0
\end{array}
$$

From KCLs in no. 2 above , $i_{D2} = i_{D1} = i_{D3} + i_{D4} = 0$. We add the value of i_D to the table above and look for transistors that are ON and have $i_D = 0$. These transistors (Q1 and Q2) have to be in triode mode with $v_{DS1} = v_{DS2} = 0$.

$$
\begin{array}{llllll}
v_{GS1} = v_1 = V_{DD} > \bar{V}_t & \rightarrow \quad \text{Q1 is ON} & & i_{D1} = 0 & \rightarrow & v_{DS1} = 0 \\
v_{GS2} = v_2 - v_{DS1} = V_{DD} - v_{DS1} = V_{DD} > \bar{V}_t & \rightarrow \quad \text{Q2 is ON} & & i_{D2} = 0 & \rightarrow & v_{DS2} = 0 \\
v_{SG3} = V_{DD} - v_1 = 0 < \bar{V}_t & \rightarrow \quad \text{Q3 is OFF} & \rightarrow & i_{D3} = 0 & & \\
v_{SG4} = V_{DD} - v_2 = 0 < \bar{V}_t & \rightarrow \quad \text{Q4 is OFF} & \rightarrow & i_{D4} = 0 & &
\end{array}
$$

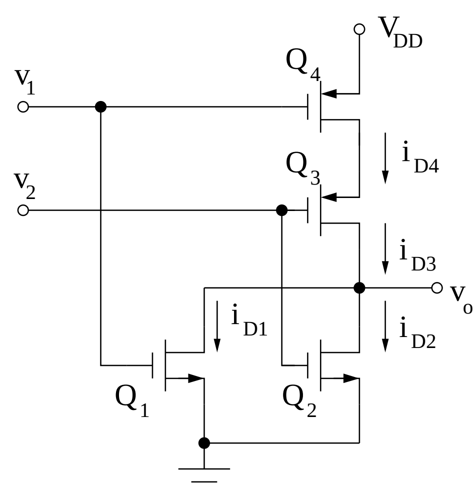
In the above, we used $v_{DS1} = 0$ to find the state of Q2 leading to $v_{DS2} = 0$.

Finally, $v_o = v_{DS1} + v_{DS1} = 0$. So, when v_1 is HIGH and v_2 is HIGH, the output is LOW.

From the "truth table," the output of this gate is LOW only if both input states are HIGH. Therefore, this is a NAND gate.

CMOS NOR Gate

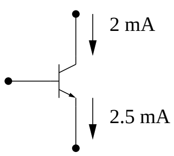
Exercise: Show that this is a NOR gate.



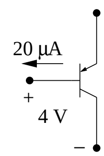
3.7 Exercise Problems

Problems 1 to 6. In circuits below find v_{BE}, i_C, v_{CE}, and state of the transistor (Si BJTs with $\beta = 100$).

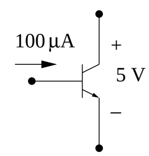
Problem 7. Find I (Si BJTs with $\beta = 100$).



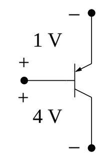
Problem 1



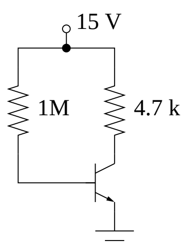
Problem 2



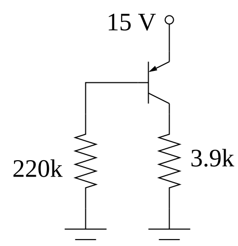
Problem 3



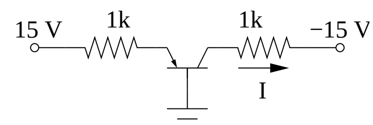
Problem 4



Problem 5



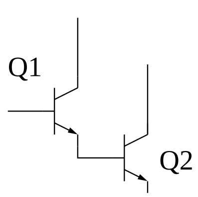
Problem 6



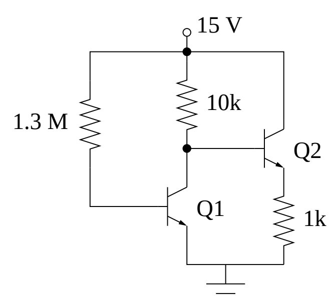
Problem 7

Problem 8. This configuration is called a Darlington Pair. Show that A) If Q1 is OFF, Q2 will be OFF, if Q1 is ON Q2 will ON, B) Show that if both BJTs are in active mode, the transistor pair act like one BJT in saturation with $\beta = i_{C2}/i_{B1} = \beta_1\beta_2$.

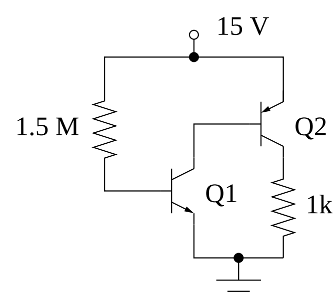
Problems 9 and 10. Find i_B, v_{BE}, i_C, v_{CE}, and state of both transistors (Si BJTs with $\beta = 100$).



Problem 8



Problem 9



Problem 10

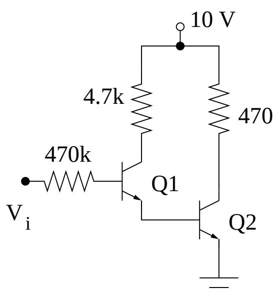
Problem 11. Find i_B, v_{BE}, i_C, v_{CE}, and state of both transistors for A) $v_i = 1$ V, B) $v_i = 3$ V, C) $v_i = 5$ V. Si BJTs with $\beta_1 = 100$ and $\beta_2 = 50$.

Problem 12. The diode in the circuit is a light-emitting diode (LED). It is made of GaAs and has a $V_{D0} = 1.7$ V. This is a switching circuit. v_i is the output of a logic gate which turns the diode on or off depending on the state of the logic gate. A) Show that for $v_i = 0$, LED will be OFF, B) Show that for $v_i = 5$ V, LED will be ON, and C) Starting from $v_i = 0$, we slowly increase v_i. At what voltage LED starts to light up? (Si BJTs with $\beta = 100$.)

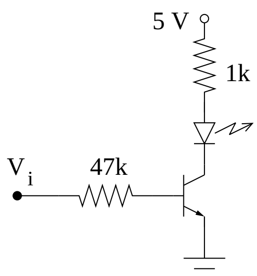
Problem 13. Design a switch circuit similar to problem 12 which turns an LED OFF and ON such that the LED is OFF for $v_i < 2.5$ V and is ON for $v_i > 2.5$ V. (Hint: See page 3-14 of lecture notes).

Problem 14. The circuit shown is a Resistor-Transistor Logic (RTL) NOR gate configured with two identical BJTs. Show that this is NOR gate with the LOW state of 0.2 V and the HIGH state of 5 V.

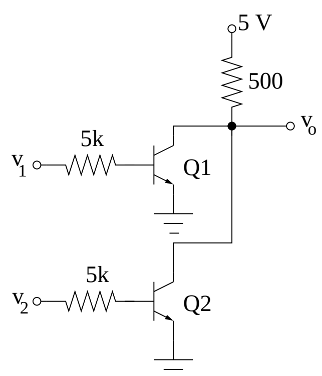
Problem 15. Prove that the circuit below is a NAND Gate. Assume that low state is 0.4 V and high state is 1.2 V. Use $\beta = 200$.



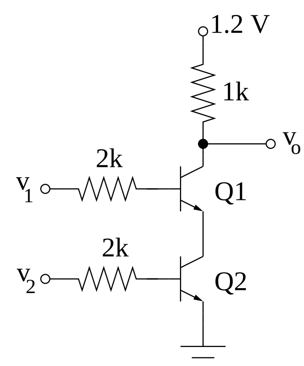
Problem 11



Problem 12

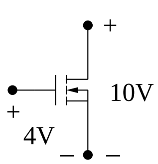


Problem 14

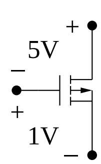


Problem 15

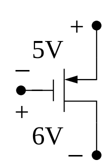
Problems 16 to 22. In circuits below find v_{GS}, i_D, v_{DS}, and state of the transistor (Use $k'_n(W/L)_n = k'_p(W/L)_p = 0.4$ mA/V^2, $\lambda = 0$, $V_{tn} = 3$ V and $V_{tp} = -3$ V).



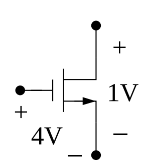
Problem 16



Problem 17

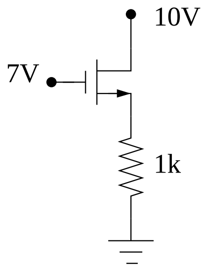


Problem 18

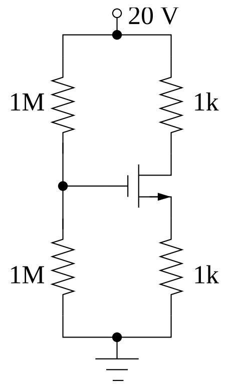


Problem 19

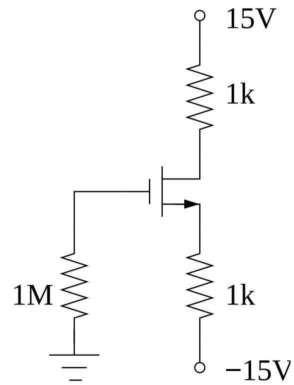
Problem 23. Find v_o when $v_i = 0$ and $12\ V$ (Use $k'_n(W/L)_n = 0.5$ mA/V^2,$\lambda = 0$, $V_{tn} = 2$ V).



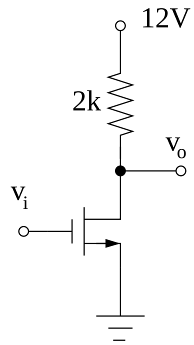
Problem 20



Problem 21



Problem 22

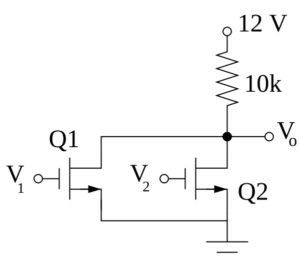


Problem 23

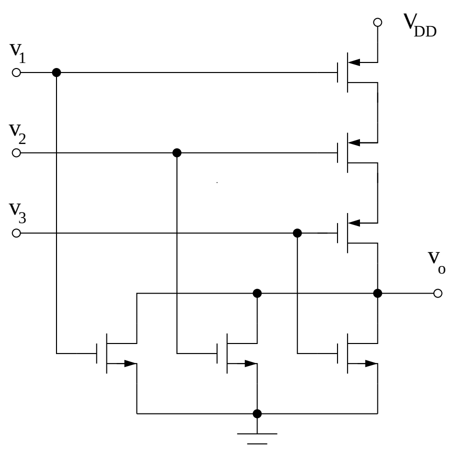
Problem 24. Show that this circuit is a NOR gate with a LOW state of 0.2 V and a HIGH state of 12 V (Use $k'_n(W/L)_n = 0.5$ mA/V^2, $V_{tn} = 1$ V).

Problem 25. Show that this is a three-input NOR gate.

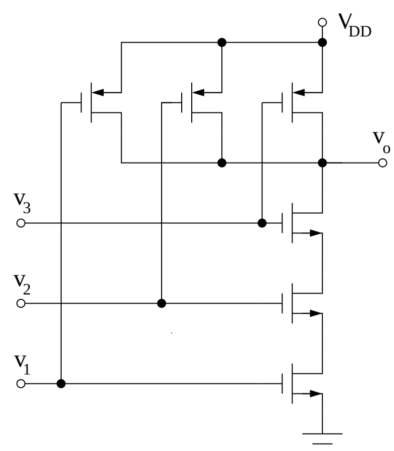
Problem 26. Show that this is a three-input NAND gate.



Problem 24



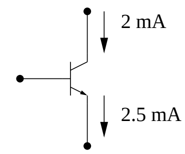
Problem 25



Problem 26

3.8 Solution to Selected Exercise Problems

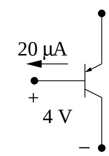
Problem 1. In circuit below find v_{BE}, i_C, v_{CE}, and state of the transistor (Si BJTs with $\beta = 100$).



This is a NPN transistor with $i_C = 2$ mA and $i_E = 2.5$ mA.

$$i_B = i_E - i_C = 0.5 \text{ mA} > 0 \quad \rightarrow \quad \text{BJT is ON} \quad \rightarrow \quad v_{BE} = 0.7 \text{ V}$$
$$\frac{i_C}{i_B} = \frac{2}{0.5} = 4 < 100 = \beta \quad \rightarrow \quad \text{BJT is in saturation} \quad \rightarrow \quad v_{CE} = 0.2 \text{ V}$$

Problem 2. In circuit below find v_{EB}, i_C, v_{EC}, and state of the transistor (Si BJTs with $\beta = 100$).



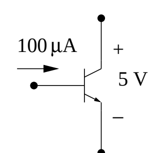
This is a PNP transistor with $i_B = 20$ μA and $v_{CB} = -4$ V.

Since $i_B > 0$, EB is ON and $v_{EB} = 0.7$ V.

Since $v_{CB} = -4 < V_{D0} = 0.7$ V, CB is reverse biased and this transistor is in active mode:

$$v_{EC} = v_{EB} + v_{BC} = 0.7 + 4 = 4.7 \text{ V}$$
$$i_C = \beta i_B = 2 \text{ mA}$$

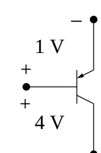
Problem 3. In circuit below find v_{BE}, i_C, v_{CE}, and state of the transistor (Si BJTs with $\beta = 100$).



This is a NPN transistor with $i_B = 100$ μA and $v_{CE} = 5$ V.

$$i_B = 100 \ \mu \text{ A} > 0 \quad \rightarrow \quad \text{BJT is ON} \quad \rightarrow \quad v_{BE} = 0.7 \text{ V}$$
$$v_{CE} = 5 \text{ V} > V_{D0} = 0.7 \text{ V} \quad \rightarrow \quad \text{BJT is in active} \quad \rightarrow \quad i_C = \beta i_B = 10 \text{ mA}$$

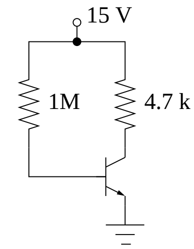
Problem 4. In circuit below find v_{EB}, i_C, v_{EC}, and state of the transistor (Si BJTs with $\beta = 100$).



This is a PNP transistor with $v_{EB} = -1$ V and $v_{CB} = -4$ V.

$$v_{EB} = -1 \text{ V} < 0.7 = V_{D0} \quad \rightarrow \quad \text{BJT is in cut-off} \quad \rightarrow \quad i_B = 0 \quad \& \quad i_C = 0$$
$$v_{EC} = v_{EB} + v_{BC} = -1 + 4 = 3 \text{ V}$$

Problem 5. In circuit below find v_{BE}, i_C, v_{CE}, and state of the transistor (Si BJTs with $\beta = 100$).



BE-KVL: $\quad 15 = 10^6 i_B + v_{BE}$

CE-KVL: $\quad 15 = 4.7 \times 10^3 i_C + v_{CE}$

Assume BJT is ON, $v_{BE} = 0.7$ V, $i_B > 0$. BE-KVL gives:

BE-KVL: $\quad 15 = 10^6 i_B + 0.7 \quad \rightarrow \quad i_B = 14.3\ \mu$A

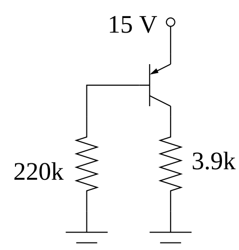
Since $i_B > 0$, our assumption of BJT is ON is justified.

Assume BJT is in active: $i_C = \beta i_B = 100 i_B = 1.43$ mA and $v_{CE} > 0.7$ V. CE-KVL gives:

CE-KVL: $\quad 15 = 4.7 \times 10^3 \times 1.43 \times 10^{-3} + v_{CE} \quad \rightarrow \quad v_{CE} = 8.28$ V

Since $v_{CE} = 8.28 > 0.7$ V our assumption of BJT in active is justified with $i_B = 14.3\ \mu$A, $i_C = 1.43$ mA, and $v_{CE} = 8.28$ V.

Problem 6. In circuit below find v_{EB}, i_C, v_{EC}, and state of the transistor (Si BJTs with $\beta = 100$).



BE-KVL: $\quad 15 = v_{EB} + 220 \times 10^3 i_B$

CE-KVL: $\quad 15 = v_{EC} + 3.9 \times 10^3 i_C$

Assume BJT (PNP) is ON, $v_{EB} = 0.7$ V, $i_B > 0$. BE-KVL gives:

BE-KVL: $\quad 15 = 0.7 + 220 \times 10^3 i_B \quad \rightarrow \quad i_B = 65\ \mu$A

Since $i_B > 0$, our assumption of BJT ON is justified.

Assume BJT is in active: $i_C = \beta i_B = 100 i_B = 6.5$ mA and $v_{EC} > 0.7$ V. CE-KVL gives:

CE-KVL: $\quad 15 = v_{EC} + 3.9 \times 10^3 \times 6.5 \times 10^{-3} \quad \rightarrow \quad v_{EC} = -10.4$ V

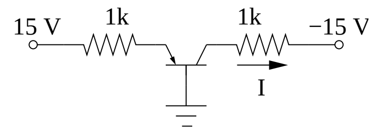
Since $v_{EC} = -10.4 < 0.7$ V our assumption of BJT in active is NOT justified.

Assume BJT in saturation, $v_{EC} = 0.2$ V, and $i_C < \beta i_B$. CE-KVL gives:

$$15 = 0.2 + 3.9 \times 10^3 i_C \quad \rightarrow \quad i_C = 3.79 \text{ mA}$$

Since $i_C/i_B = 3.79/0.065 = 58 < 100 = \beta$, our assumption of BJT in saturation is justified with $i_B = 65\ \mu$A, $i_C = 3.79$ mA, and $v_{EC} = 0.2$ V.

Problem 7. Find I (Si BJTs with $\beta = 100$).



BE-KVL: $\quad 15 = 10^3 i_E - v_{BE}$

CE-KVL: $\quad 15 = 10^3 i_E - v_{CE} + 10^3 i_C - 15$

Assume BJT (NPN) is OFF, $i_B = i_C = i_E = 0$ and $-v_{BE} < 0.7$ V. BE-KVL gives:

BE-KVL: $\quad 15 = -v_{BE}$

Since $-v_{BE} = 15 > 0.7$ V, BJT is NOT in cut-off.

Assume BJT is ON, $v_{BE} = -0.7$ V, $i_B > 0$. BE-KVL gives:

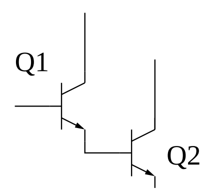
BE-KVL: $\quad 15 = 10^3 i_E - (-0.7) \quad \rightarrow \quad i_E = 14.3$ mA

Assume BJT is in active: $i_E \approx i_C = \beta i_B$ and $-v_{CE} > 0.7$ V. Therefore $i_C \approx i_E = 14.3$ mA and $i_B = i_C/100 = 143$ μA. CE-KVL gives

CE-KVL: $\quad 15 = 10^3 \times 14.3 \times 10^{-3} - v_{CE} + 10^3 \times 14.3 \times 10^{-3} - 15 \quad \rightarrow \quad v_{CE} = -1.4$ V

Since $-v_{CE} = 1.4 > 0.7$ V, BJT is in active with $i_B = 143$ μA, $i_C = 14.3$ mA, and $v_{CE} = -1.4$V.

Problem 8. This configuration is called a Darlington Pair. Show that A) If Q1 is OFF, Q2 will be OFF, if Q1 is ON Q2 will ON, B) Show that if both BJTs are in active, the transistor pair act like one BJT in active with $\beta = i_{C2}/i_{B1} = \beta_1\beta_2$.



Darlington pair are arranged such that $i_{E1} = i_{B2}$.

Part A:

If Q1 is OFF, $i_{B1} = i_{C1} = i_{E1} = 0$. Because of Darlington pair arrangement, $i_{B2} = i_{E1} = 0$ and Q2 would also be OFF. If Q1 is ON, $i_{E1} > 0$. Because of Darlington pair arrangement, $i_{B2} = i_{E1} > 0$ and Q2 would also be ON.

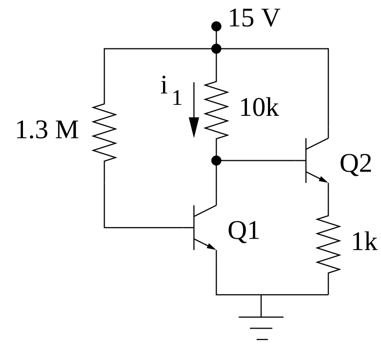
Part B:

If Q1 & Q2 are both in active:

$$i_{C2} = \beta_2 i_{B2} = \beta_2 i_{E1} \approx \beta_2 i_{C1} = \beta_1\beta_2 i_{B1} \quad \rightarrow \quad \frac{i_{C2}}{i_{B1}} = \beta_1\beta_2$$

So, the Darlington pair act as a super high β BJT.

Problem 9. Find i_B, v_{BE}, i_C, v_{CE}, and state of both transistors (Si BJTs with $\beta = 100$).



BE1-KVL:	$15 = 1.3 \times 10^6 i_{B1} + v_{BE1}$
CE1-KVL:	$15 = 10 \times 10^3 i_1 + v_{CE1}$
BE2-KVL:	$v_{CE1} = v_{BE2} + 10^3 i_{E2}$
CE2-KVL:	$15 = v_{CE2} + 10^3 i_{E2}$
KCL:	$i_1 = i_{C1} + i_{B2}$

Assume Q1 is ON, $V_{BE1} = 0.7$ V and $i_{B1} > 0$. BE1-KVL gives:

BE1-KVL: $\quad 15 = 1.3 \times 10^6 i_{B1} + 0.7 \quad \rightarrow \quad i_{B1} = 11\ \mu$A

Since $i_{B1} > 0$, our assumption of Q1 ON is justified.

Assume Q1 is active, $i_{C1} = 100 i_{B1} = 1.1$ mA and $v_{CE1} > 0.7$ V. In principle, we should move forward and assume state of Q2 and solve the remaining three equations together. However, solution can be simplified if we assume $i_{B2} \ll i_{C1}$ and check this assumption after solution.

If $i_{B2} \ll i_{C1}$, then $i_1 \approx i_{C1}$. CE1-KVL gives:

CE1-KVL: $\quad 15 = 10 \times 10^3 i_{C1} + v_{CE1} = 10 \times 10^3 \times 1.1 \times 10^{-3} + v_{CE1} \rightarrow v_{CE1} = 3.9$ V

Since $v_{CE1} > 0.7$ V, our assumption of Q1 in active is correct. State of Q2 can be found from BE2-KVL and CE2-KVL. Assume Q2 active: $V_{BE2} = 0.7$ V, $i_{B2} > 0$, $i_{C2} = 100 i_{B2}$, and $v_{CE2} > 0.7$ V. Then $i_{E2} \approx i_{C2}$ and:

BE2-KVL: $\quad v_{CE1} = v_{BE2} + 10^3 i_{E2}$

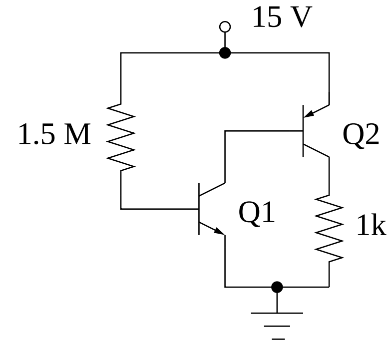
$\quad 3.9 = 0.7 + 10^3 i_{C2} \quad \rightarrow \quad i_{C2} = 3.2$ mA

CE2-KVL: $\quad 15 \approx v_{CE2} + 10^3 i_{C2} = v_{CE2} + 10^3 \times 3.2 \times 10^{-3} \quad \rightarrow \quad v_{CE2} = 11.8$ V

Since $v_{CE2} > 0.7$ V, our assumption of Q2 in active is correct. Then $i_{B2} = i_{C2}/100 = 32\ \mu$A. We note that $i_{B2} = 32\ \mu\text{A} \ll i_{C1} = 1.1$ mA. Therefore that assumption was also correct.

In sum, bot BJTs are in active and $v_{BE1} = 0.7$ V, $i_{B1} = 11\ \mu$A, $i_{C1} = 1.1$ mA, $v_{CE1} = 3.9$ V, $v_{BE2} = 0.7$ V, $i_{B2} = 32\ \mu$A, $i_{C2} = 3.2$ mA, $v_{CE2} = 11.8$ V.

Problem 10. Find i_B, v_{BE}, i_C, v_{CE}, and state of both transistors (Si BJTs with $\beta = 100$).



Note that Q2 is a PNP transistor

$$
\begin{aligned}
\text{BE1-KVL:} \quad & 15 = 1.5 \times 10^6 i_{B1} + v_{BE1} \\
\text{CE1-KVL \& BE2-KVL:} \quad & 15 = v_{EB2} + v_{CE1} \\
\text{CE2-KVL:} \quad & 15 = v_{EC2} + 10^3 i_{C2} \\
\text{KCL:} \quad & i_{C1} = i_{B2}
\end{aligned}
$$

Assume Q1 is ON, $v_{BE1} = 0.7$ V and $i_{B1} > 0$. BE1-KVL gives:

$$\text{BE1-KVL:} \qquad 15 = 1.5 \times 10^6 i_{B1} + 0.7 \quad \rightarrow \quad i_{B1} = 9.5\ \mu\text{A}$$

Since $i_{B1} > 0$, our assumption of Q1 ON is correct. Also, since $i_{B2} = i_{C1} > 0$, Q2 is ON and $v_{EB2} = 0.7$ V. Then CE1-KVL gives $v_{CE1} = 14.3$ V. Since $v_{CE1} > 0.7$ V, Q1 is in active and $i_{C1} = 100 i_{B1} = 0.95$ mA.

KCL gives $i_{B2} = i_{C1} = 0.95$ mA. Assume Q2 is in active: $i_{C2} = 100 i_{B2} = 95$ mA and $v_{EC2} > 0.7$ V. CE2-KVL gives

$$\text{CE2-KVL:} \qquad 15 = v_{EC2} + 10^3 i_{C2} = v_{EC2} + 10^3 \times 95 \times 10^{-3} \quad \rightarrow \quad v_{EC2} = -80 \text{ V}$$

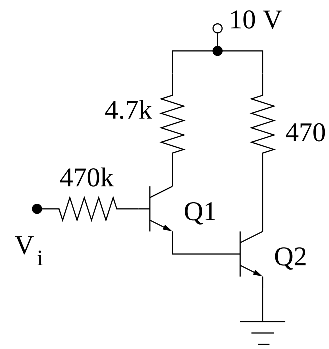
Since $v_{EC2} = -80 < 0.7$ V, our assumption of Q2 in active is incorrect. Assume Q2 is in saturation: $v_{EC2} = 0.2$ V and $i_{C2}/i_{B2} < 100$. CE2-KVL gives:

$$\text{CE2-KVL:} \qquad 15 = v_{EC2} + 10^3 i_{C2} = 0.2 + 10^3 i_{C2} \quad \rightarrow \quad i_{C2} = 14.8 \text{ mA}$$

Since $i_{C2}/i_{B2} = 14.8/0.95 = 15.6 < 100$, our assumption of Q2 in saturation is correct.

In sum, Q1 is in active, Q2 is in saturation, and $v_{BE1} = 0.7$ V, $i_{B1} = 9.5\ \mu$A, $i_{C1} = 0.95$ mA, $v_{CE1} = 14.3$ V, $v_{EB2} = 0.7$ V, $i_{B2} = 0.95$ mA, $i_{C2} = 14.8.2$ mA, $v_{EC2} = 0.2$ V.

Problem 11. Find i_B, v_{BE}, i_C, v_{CE}, and state of both transistors for A) $v_i = 1$ V, B) $v_i = 3$ V, C) $v_i = 5$ V. Si BJTs with $\beta_1 = 100$ and $\beta_2 = 50$.



Note that BJTs are arranged as a Darlington pair with $i_{E1} = i_{B2}$. So they will be either both ON or both OFF.

$$\begin{aligned}
\text{BE1-KVL:}\quad & V_i = 470 \times 10^3 i_{B1} + v_{BE1} + v_{BE2} \\
\text{CE1-KVL \& BE2-KVL:}\quad & 10 = 4.7 \times 10^3 i_{C1} + v_{CE1} + v_{BE2} \\
\text{CE2-KVL:}\quad & 10 = 470 i_{C2} + v_{CE2} \\
\text{KCL:}\quad & i_{C1} = i_{B2}
\end{aligned}$$

Part A: $v_i = 1$ V.

Assume both BJTs are ON: $v_{BE1} = v_{BE2} = 0.7$ V, $i_{B1} > 0$, and $i_{B2} > 0$. BE1-KVL gives:

$$\text{BE1-KVL:}\quad 1 = 470 \times 10^3 i_{B1} + 0.7 + 0.7 \quad \rightarrow \quad i_{B1} = -0.8\ \mu\text{A}$$

Since $i_{B1} < 0$, our assumption is incorrect and both BJTs are in cut-off with $i_{B1} = i_{C1} = i_{B2} = i_{C2} = 0$. CE2-KVL gives $v_{CE2} = 10$ V. CE1-KVL gives $v_{CE1} + v_{BE2} = 10$ V. Our simple large-signal model for the BJT cannot resolve the values of v_{CE1} and v_{BE2} because any values of $v_{BE2} < 0.7$V and the corresponding value of $v_{CE1} = 10 - v_{BE2}$ will be acceptable.

The problem of not finding unique values for v_{CE1} and v_{BE2} is due to our simple diode model of the BE junction. In reality both BE junctions will be forward biased with voltages smaller than 0.7 V (so both i_B's will be very small) and BJTS will have small values of i_C's.

Part B: $v_i = 3$ V.

Assume both BJTs are ON: $v_{BE1} = v_{BE2} = 0.7$ V, $i_{B1} > 0$, and $i_{B2} > 0$. BE1-KVL gives:

$$\text{BE1-KVL:}\quad 3 = 470 \times 10^3 i_{B1} + 0.7 + 0.7 \quad \rightarrow \quad i_{B1} = 3.4\ \mu\text{A}$$

Since $i_{B1} > 0$, our assumption is correct and both BJTs are ON.

Assume Q1 in active: $i_{C1} = 100 i_{B1} = 0.34$ mA and $v_{CE1} > 0.7$ V. Then CE1-KVL gives:

$$\begin{aligned}
\text{CE1-KVL \& BE2-KVL:}\quad & 10 = 4.7 \times 10^3 i_{C1} + v_{CE1} + v_{BE2} \\
& 10 = 4.7 \times 10^3 \times 0.34 \times 10^{-3} + v_{CE1} + 0.7 \quad \rightarrow \quad v_{CE1} = 7.7\ \text{V}
\end{aligned}$$

Since $v_{CE1} = 7.7 > 0.7$ V, our assumption of Q1 in active is correct. Then, $i_{B2} = i_{E1} \approx i_{C1} = 0.34$ mA.

Assume Q2 is in active: $i_{C2} = 50 i_{B2} = 17$ mA and $v_{CE2} > 0.7$ V. Then CE2-KVL gives:

$$\text{CE2-KVL:} \qquad 10 = 470 i_{C2} + v_{CE2} = 470 \times 17 \times 10^{-3} + v_{CE2} \quad \rightarrow \quad v_{CE2} = 2.01 \text{ V}$$

Since $v_{CE2} = 2.01 > 0.7$ V, our assumption of Q2 in active is correct.

Therefore, Q1 & Q2 are in active, and $v_{BE1} = v_{BE2} = 0.7$ V, $i_{B1} = 3.4$ μA, $i_{C1} = 0.34$ mA, $v_{CE1} = 7.7$ V, $i_{B2} = 0.34$ mA, $i_{C2} = 17$ mA, and $v_{CE2} = 2.01$ V.

Part C: $v_i = 5$ V.

Assume both BJTs are ON: $v_{BE1} = v_{BE2} = 0.7$ V, $i_{B1} > 0$, and $i_{B2} > 0$. BE1-KVL gives:

$$\text{BE1-KVL:} \qquad 5 = 470 \times 10^3 i_{B1} + 0.7 + 0.7 \quad \rightarrow \quad i_{B1} = 7.66 \ \mu\text{A}$$

Since $i_{B1} > 0$, our assumption is correct and both BJTs are ON.

Assume Q1 is in active: $i_{C1} = 100 i_{B1} = 0.77$ mA and $v_{CE1} > 0.7$ V. Then CE1-KVL gives:

$$\text{CE1-KVL \& BE2-KVL:} \qquad 10 = 4.7 \times 10^3 i_{C1} + v_{CE1} + v_{BE2}$$
$$10 = 4.7 \times 10^3 \times 0.77 \times 10^{-3} + v_{CE1} + 0.7 \ \rightarrow \ v_{CE1} = 5.70 \text{ V}$$

Since $v_{CE1} = 5.70 > 0.7$ V, our assumption of Q1 in active is correct. Then, $i_{B2} = i_{E1} \approx_{C1} = 0.77$ mA.

Assume Q2 is in active: $i_{C2} = 50 i_{B2} = 38.3$ mA and $v_{CE2} > 0.7$ V. Then CE2-KVL gives:

$$\text{CE2-KVL:} \qquad 10 = 470 i_{C2} + v_{CE2} = 470 \times 38.3 \times 10^{-3} + v_{CE2} \quad \rightarrow \quad v_{CE2} = -8.0 \text{ V}$$

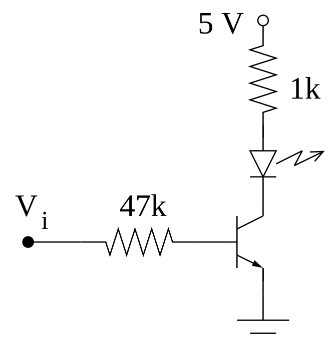
Since $v_{CE2} = -8.0 < 0.7$ V, our assumption is incorrect and Q2 is in saturation: $v_{CE2} = 0.2$ V and $i_{C2}/i_{B2} < 50$. Then CE2-KVL gives:

$$\text{CE2-KVL:} \qquad 10 = 470 i_{C2} + v_{CE2} = 470 i_{C2} + 0.2 \quad \rightarrow \quad i_{C2} = 20.9 \text{ mA}$$

Since $i_{C2}/i_{B2} = 20.9/0.77 = 27 < 50$, our assumption is correct.

Therefore, Q1 is in active, Q2 is in saturation, and $v_{BE1} = v_{BE2} = 0.7$ V, $i_{B1} = 7.66$ μA, $i_{C1} = 0.77$ mA, $v_{CE1} = 5.7$ V, $i_{B2} = 0.77$ mA, $i_{C1} = 20.9$ mA, and $v_{CE2} = 0.2$ V.

Problem 12. The diode in the circuit is a light-emitting diode (LED). It is made of GaAs and has a $V_{D0} = 1.7$ V. This is a switching circuit. v_i is the output of a logic gate which turns the diode on or off depending on the state of the logic gate. A) Show that for $v_i = 0$, LED will be OFF, B) Show that for $v_i = 5$ V, LED will be ON, and C) Starting from $v_i = 0$, we slowly increase v_i. At what voltage LED starts to light up? (Si BJTs with $\beta = 100$.)



BE-KVL: $\quad v_i = 47 \times 10^5 i_B + v_{BE}$

CE-KVL: $\quad 5 = 10^3 i_C + v_D + v_{CE}$

$$i_C = i_D$$

Part A: $v_i = 0$:

Assume BJT is OFF, $i_B = 0$ and $v_{BE} < 0.7$ V. BE-KVL gives:

BE-KVL: $\quad 0 = 47 \times 10^3 i_B + v_{BE} = 0 + v_{BE} \quad \rightarrow \quad v_{BE} = 0$

Since $v_{BE} = 0 < 0.7$ V, our assumption of BJT in cut-off is correct and $i_C = 0$. Since $i_D = i_C = 0$, the diode will be OFF.

Part B: $v_i = 5$ V:

Assume BJT is ON, $v_{BE} = 0.7$ V, $i_B > 0$. BE-KVL gives:

BE-KVL: $\quad 5 = 47 \times 10^3 i_B + 0.7 \quad \rightarrow \quad i_B = 91.5\ \mu$A

Since $i_B > 0$ our assumption of BJT is ON is justified. When BJT is ON, $i_C > 0$ and since $i_D = i_C > 0$, the LED will be on with $v_D = 1.7$ V.

Assume BJT is in active: $i_C = \beta i_B = 100 i_B = 9.15$ mA and $v_{CE} > 0.7$ V. CE-KVL gives:

CE-KVL: $\quad 5 = 10^3 i_C + v_D + v_{CE}$

$$5 = 10^3 \times 9.15 \times 10^{-3} + 1.7 + v_{CE} \quad \rightarrow \quad v_{CE} = -5.85 \text{ V}$$

Since $v_{CE} = -5.85 < 0.7$ V our assumption of BJT in active is NOT justified.

Assume BJT in saturation, $v_{CE} = 0.2$ V, and $i_C < \beta i_B$. CE-KVL gives:

CE-KVL: $\quad 5 = 10^3 i_C + v_D + v_{CE} = 10^3 i_C + 1.7 + 0.2 \quad \rightarrow \quad i_C = 3.1$ mA

Since $i_C / i_B = 3.1/0.0915 = 34 < 100 = \beta$, our assumption of BJT in saturation is justified.

Therefore, for $v_i = 5$ V, LED is ON, BJT is in saturation, and $v_{BE} = 0.7$ V, $v_D = 1.7$ V, $i_B = 91.5\ \mu$A, $i_C = 3.1$ mA, and $v_{CE} = 0.2$ V.

Part C:

LED is ON when $i_D > 0$. Since $i_C = i_D > 0$, the BJT should be ON.

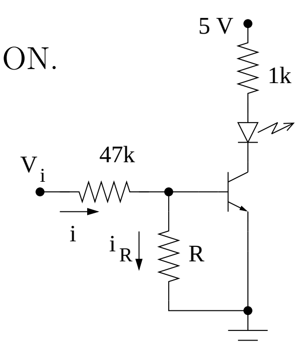
We found that for $v_i = 0$, BJT is in cut-off and LED is OFF. As we increase v_i and while BJT is still in cut-off, BE-KVL gives $v_{BE} = v_i$ since $i_B = 0$. So as we increase v_i, v_{BE} increases while i_B remains zero.

When v_i reaches 0.7 V, v_{BE} also reaches 0.7 V while i_B is still zero.

If we increase v_i beyond this point, v_{BE} cannot increase, rather i_B becomes positive and BJT will be turned ON leading to $i_C > 0$ and LED turning ON.

So, LED will light up when $v_i \geq 0.7$ V.

Problem 13. Design a switch circuit similar to problem 12 which turns an LED OFF and ON such that the LED is OFF for $v_i < 2.5$ V and is ON for $v_i > 2.5$ V. (Hint: See page 3-14 of lecture notes).



Addition of a resistor R (see circuit) will raise v_i that turns the LED ON.

In problem 12, we saw that LED will just turn ON when $v_{BE} = 0.7$ V and $i_B \approx 0$. BE-KVL gives:

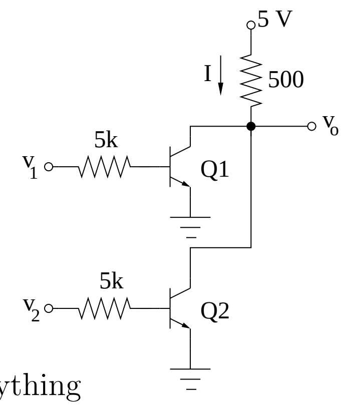
$$\text{BE-KVL:} \qquad v_i = 47 \times 10^3 i + v_{BE}$$

$$2.5 = 47 \times 10^5 i + 0.7 \quad \rightarrow \quad i = 38.3\ \mu\text{A}$$

Since $i_B = 0$, $i_R = i = 38.3\ \mu$A. Ohm's law for the resistor R gives:

$$v_{BE} = Ri_R \quad \rightarrow \quad 0.7 = 38.3 \times 10^{-6} R \quad \rightarrow \quad R = 18.3\ \text{k}\Omega$$

Problem 14. The circuit shown is a Resistor-Transistor Logic (RTL) NOR gate configured with two identical BJTs. Show that this is NOR gate with a LOW state of 0.2 V and a HIGH state of 5 V (Si BJTs with $\beta = 100$).



We first find the state of Q1 for the two cases of $V_1 = 0.2$ and 5 V.

BE1-KVL: $\quad v_1 = 500 i_{B1} + v_{BE1}$

For $v_1 = 0.2$ V, assume that Q1 is in cut-off ($i_{B1} = 0$ and $v_{BE1} < V_{D0} = 0.7$ V). Then, BE1-KVL gives $V_{BE1} = 0.2 < 0.7$ V and, thus, Q1 is indeed in cut-off. So:

$$v_1 = 0.2 \text{ V} \quad \rightarrow \quad i_{B1} = i_{C1} = 0, \quad v_{BE1} = 0.2 \text{ V}, \quad v_{CE1} \text{ can be anything}$$

For $v_1 = 5$ V, assume that Q1 is NOT in cut-off ($i_{B1} > 0$ and $v_{BE1} = V_{D0} = 0.7$ V). Substituting for $v_{BE1} = 0.7$ in BE1-KVL, we get $I_{B1} = 4.3/5,000 = 0.86$ mA. Since $i_{B1} > 0$, Q1 is indeed NOT in cut-off. Therefore,

$$v_1 = 5 \text{ V} \quad \rightarrow \quad \text{BJT is ON (not in cut-off)} \qquad i_{B1} = 0.86 \text{ mA} \quad v_{BE1} = 0.7 \text{ V} \quad i_{C1} > 0$$

Note that because the circuit is symmetric (*i.e.,* there is no difference between Q1 circuit and Q2 circuit), the above results also applies to Q2.

<u>Case a: $v_1 = v_2 = 0.2$ V</u> From above, both BJTs will be in cut-off and $i_{C1} = i_{C2} = 0$. By KCL, $I = i_{C1} + i_{C2} = 0$, and v_o can be found from Ohm's Law:

$$5 - v_o = 500I = 0 \quad \rightarrow \quad v_o = 5 \text{ V}$$

<u>Case b: $v_1 = 0.2$ V, $v_2 = 5$ V</u> Since $v_1 = 0.2$ V, Q1 will be in cut-off with $i_{C1} = 0$. Since $v_2 = 5$ V, Q2 will not be in cut-off with $i_{B2} = 0.86$ mA. Assume Q2 is in saturation ($v_{CE2} = 0.2$ V and $i_{C2}/i_{B2} < \beta$). In this case, $v_o = v_{CE2} = 0.2$ V and $I = i_{C1} + i_{C2} = i_{C2}$. By Ohm's Law:

$$500I = 500 i_{C2} = 5 - V_o = 5 - v_{CE2} = 4.8 \quad \rightarrow \quad i_{C2} = 4.8/500 = 9.6 \text{ mA}$$

Since $i_{C2}/i_{B2} = 11 < \beta = 100$, Q2 is indeed in saturation. So, in this case, $v_o = 0.2$ V.

<u>Case c: $v_1 = 5$, $v_2 = 0.2$ V</u> Because the circuit is symmetric (*i.e.,* there is no difference between Q1 circuit and Q2 circuit), results from Case b can be applied here. Thus, Q2 will be in cut-off with $i_{C2} = 0$ and Q1 will be in saturation with $i_{C1} = 9.6$ mA and $v_o = v_{CE2} = 0.2$ V.

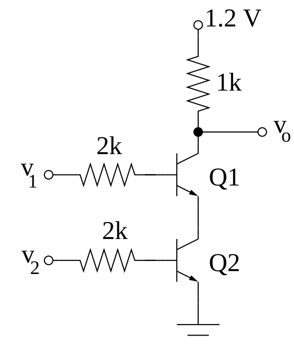
Case d: $v_1 = v_2 = 5$ V Both BJTs will be ON with $i_{B1} = i_{B2} = 0.86$ mA and $v_{BE1} = v_{BE2} = 0.7$ V. Since from the circuit, $v_{CE1} = v_{CE2}$, both BJTs will be in saturation or both in active-linear. Assume that both are in saturation. Then, $v_o = v_{CE1} = v_{CE2} = 0.2$ V and we should have $i_{C1}/i_{B1} < \beta$ and $i_{C2}/i_{B2} < \beta$. By Ohm's Law:

$$500I = 5 - v_o = 5 - 0.2 = 4.8 \quad \rightarrow \quad I = 4.8/500 = 9.6 \text{ mA}$$

Since BJTs are identical and have same i_B, we should have $i_{C1} = i_{C2}$ and current I should be equally divided between two BJTs. Thus, $i_{C1} = i_{C2} = 0.5I = 4.8$ mA. To check if BJTs are in saturation: $i_{C1}/i_{B1} = 4.8/0.86 = 5 < \beta = 100$ and $i_{C2}/i_{B2} = 4.8/0.86 = 5 < \beta = 100$ so both BJTs are indeed in saturation and $v_o = 0.2$ V.

In summary, the output is high when both inputs are low and the output is low otherwise. Therefore, this is a NOR gate.

Problem 15. Show that this is NAND gate with a LOW state of 0.4 V and a HIGH state of 1.2 V (Si BJTs with $\beta = 200$).



$$i_{E1} = i_{c2}$$

CE-KVL: $1.2 = 10^3 i_{C1} + v_{CE1} + v_{CE2}$

$$v_o = v_{CE1} + v_{CE2} = 1.2 - 10^3 i_{C1}$$

BE1-KVL: $v_1 = 2 \times 10^3 i_{B1} + v_{BE1} + v_{CE2}$

BE2-KVL: $v_2 = 2 \times 10^3 i_{B2} + v_{BE2}$

Case 1: $v_1 = 0.4$, $v_2 = 0.4$: Assume Q2 is off ($i_{B2} = 0$, $v_{BE2} < V_{D0}$). Substituting for $i_{B2} = 0$ in the BE2-KVL above, we get: $v_{BE2} = v_2 = 0.4 < 0.7 = V_{D0}$. Thus, Q2 is off and $i_{C2} = 0$. Since $i_{E1} = i_{C2} = 0$ and $i_{E1} = i_{C1} + i_{B1} = 0$, we should have $i_{C1} = 0$ (because $i_{C1} \geq 0$ and $i_{B1} \geq 0$) . Then, from CE-KVL above:

$$v_o = 1.2 - 10^3 i_{C1} = 1.2 \text{ V}$$

Case 2: $v_1 = 1.2$, $v_2 = 0.4$: Similar to Case 1, assume Q2 is off to find $i_{c1} = 0$ and $v_o = 1.2$ V.

Case 3: $v_1 = 0.4$, $v_2 = 1.2$: Assume Q1 is off ($i_{B1} = 0$, $v_{BE1} < V_{D0}$). Substituting for $i_{B1} = 0$ in the BE1-KVL above, we get: $v_{BE1} = 0.4 - v_{CE2}$. Since v_{CE2} cannot be negative (powered by 1.2 V),$v_{BE1} = 0.4 - v_{CE2} < 0.7 = V_{D0}$ and Q1 is off ($i_{C1} = 0$). Then:

$$v_o = 1.2 - 10^3 i_{C1} = 1.2 \text{ V}$$

Case 4: $v_1 = 1.2$, $v_2 = 1.2$: Since both inputs are high, we start by assuming that both BJTs are ON (we still need to prove it): $i_{B2} > 0$, $v_{BE2} = V_{D0} = 0.7$ V and $i_{B1} > 0$, $v_{BE1} = V_{D0} = 0.7$ V. Four possible combinations exist with Q1 and Q2 being respectively in active & active, active & saturation, saturation & active, and saturation & active. Since problem states that this is NAND gate and the low voltage is 0.4 V, a good guess is that both BJTs are in saturation $v_{CE1} = V_{sat} = 0.2$ V, $i_{C1}/i_{B1} < \beta$ and $v_{CE2} = V_{sat} = 0.2$ V, $i_{C2}/i_{B2} < \beta$.

Starting with BE1-KVL and BE2-KVL above, we get:

$$1.2 = 2 \times 10^3 i_{B2} + 0.7 \qquad \rightarrow \qquad i_{B2} = 0.25 \text{ mA}$$
$$1.2 = 2 \times 10^3 i_{B1} + 0.7 + 0.2 \qquad \rightarrow \qquad i_{B1} = 0.15 \text{ mA}$$

Since $i_{B2} > 0$, and $i_{B1} > 0$, assumption of both BJTs ON is correct. Then, CE-KVL gives:

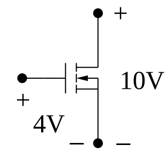
$$1.2 = 10^3 i_{C1} + 0.2 + 0.2 \qquad \rightarrow \qquad i_{C1} = 0.8 \text{ mA}$$

Since $i_{C1}/i_{B1} = 0.8/0.15 = 5.3 < \beta = 200$, our assumption of Q1 being in saturation is justified. To find i_{C2}, we note $i_{C2} = i_{E1} = i_{C1} + i_{B1} = 0.8 + 0.15 = 0.95$ mA. Then $i_{C2}/i_{B1} = 0.95/0.25 = 3.8 < \beta = 200$, so our assumption of Tr2 being in saturation is also justified. Lastly,

$$v_o = v_{CE1} + v_{CE2} = 0.2 + 0.2 = 0.4 \text{ V}$$

Overall, $v_o = 1.2$ V or HIGH State (cases 1, 2, and 3) unless both inputs are HIGH (case 4). Therefore, this is a NAND gate.

Problem 16. In circuit below find v_{GS}, i_D, v_{DS}, and state of the transistor (Use $k'_n(W/L)_n = k'_p(W/L)_p = 0.4$ mA/V^2, $\lambda = 0$, $V_{tn} = 3$ V and $V_{tp} = -3$ V).



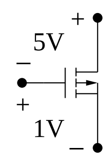
This is a NMOS transistor with $v_{GS} = 4$ V and $v_{DS} = 10$ V.

Since $V_{GS} = 4 > 3 = V_{tn}$, NMOS is ON

Since $v_{DS} = 10 > v_{GS} - V_{tn} = 1$ V, NMOS is in Saturation:

$$i_D = 0.5k'_n(W/L)_n(v_{GS} - V_{tn})^2 = 0.2 \times 10^{-3}(1)^2 = 0.2 \text{ mA}$$

Problem 17. In circuit below find v_{SG}, i_D, v_{SD}, and state of the transistor (Use $k'_n(W/L)_n = k'_p(W/L)_p = 0.4$ mA/V^2,$\lambda = 0$, $V_{tn} = 3$ V and $V_{tp} = -3$ V).

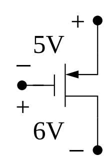


This is a PMOS transistor with $v_{SG} = -1$ V and $v_{DG} = 5$ V.

Since $v_{SG} = -1 < 3 = |V_{tp}|$, PMOS is OFF and $i_D = 0$.

Also, $v_{SD} = v_{SG} + v_{GD} = -1 - 5 = -6$ V.

Problem 18. In circuit below find v_{SG}, i_D, v_{SD}, and state of the transistor (Use $k'_n(W/L)_n = k'_p(W/L)_p = 0.4$ mA/V^2,$\lambda = 0$, $V_{tn} = 3$ V and $V_{tp} = -3$ V).



This is a PMOS transistor with $v_{SG} = 5$ V and $v_{DG} = -6$ V.

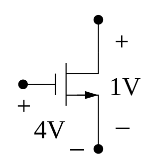
Since $v_{SG} = 5 > 3 = |V_{tp}|$, PMOS is ON.

$v_{SD} = v_{SG} + v_{GD} = 5 + 6 = 11$ V.

Since $v_{SD} = 11 > v_{SG} - |V_{tp}| = 5 - 3 = 2$ V, PMOS is in saturation:

$$i_D = 0.5k'_p(W/L)_p(v_{GS} - |V_{tp}|)^2 = 0.2 \times 10^{-3}(-5 + 3)^2 = 0.8 \times 10^{-3} = 0.8 \text{ mA}$$

Problem 19. In circuit below find v_{GS}, i_D, v_{DS}, and state of the transistor (Use $k'_n(W/L)_n = k'_p(W/L)_p = 0.4$ mA/V^2,$\lambda = 0$, $V_{tn} = 3$ V and $V_{tp} = -3$ V).



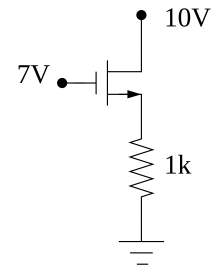
This is a NMOS transistor with $v_{GS} = 4$ V and $v_{DS} = 1$ V.

Since $V_{GS} = 4 > 3 = V_{tn}$, NMOS is ON

Since $v_{DS} = 1 = v_{GS} - V_{tn} = 1$ V, NMOS is at the boundary of saturation and triode modes. We can use either formulas for i_D.

$$i_D = 0.5k'_n(W/L)_n(v_{GS} - V_{tn})^2 = 0.2 \times 10^{-3}(1)^2 = 0.2 \text{ mA}$$

Problem 20. In circuit below find v_{GS}, i_D, v_{DS}, and state of the transistor (Use $k_n'(W/L)_n = k_p'(W/L)_p = 0.4$ mA/V^2,$\lambda = 0$, $V_{tn} = 3$ V and $V_{tp} = -3$ V).



GS-KVL: $\quad 7 = v_{GS} + 10^3 i_D$

DS-KVL: $\quad 10 = v_{DS} + 10^3 i_D$

Assume NMOS is in cut-off: $i_D = 0$, $v_{GS} < V_{tn} = 3$ V.

GS-KVL gives $v_{GS} = 7 > V_{tn} = 3$ V. Therefore, NMOS is NOT in cut-off.

Assume NMOS in saturation: $i_D = 0.5k_n'(W/L)_n(v_{GS} - V_{tn})^2$ and $v_{DS} > v_{GS} - V_{tn}$. Substituting for i_D in GS-KVL, we get:

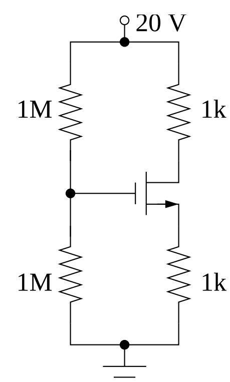
$$\text{GS-KVL:} \quad 7 = v_{GS} + 10^3 \times 0.2 \times 10^{-3}(v_{GS} - 3)^2 = v_{GS} + 0.2v_{GS}^2 - 1.2v_{GS} + 1.8$$

$$v_{GS}^2 - v_{GS} - 26 = 0 \quad \rightarrow \quad v_{GS} = -4.62 \text{ V} \quad \text{and} \quad v_{GS} = 5.62 \text{ V}$$

Negative root is unphysical so $v_{GS} = 5.62$ V. GS-KVL give $i_D = 1.35$ mA. DS-KVL gives $v_{DS} = 10 - 1.35 = 8.65$ V Since $v_{DS} = 8.65 > v_{GS} - V_{tn} = 5.62 - 3 = 2.62$ V, our assumption of NMOS in saturation is justified.

In sum, NMOS is in saturation with $v_{GS} = 5.62$ V, $v_{DS} = 8.65$ V, and $i_D = 1.35$ mA

Problem 21. In circuit below find v_{GS}, i_D, v_{DS}, and state of the transistor (Use $k_n'(W/L)_n = k_p'(W/L)_p = 0.4$ mA/V^2,$\lambda = 0$, $V_{tn} = 3$ V and $V_{tp} = -3$ V).



Since $i_G = 0$, the two 1 MΩ resistors form a voltage divider and $v_G = 20 \times (10^6)/(10^6 + 10^6) = 10$ V.

GS-KVL: $\quad v_G = v_{GS} + 10^3 i_D$

DS-KVL: $\quad 20 = v_{DS} + 2 \times 0^3 i_D$

Assume NMOS is in cut-off: $i_D = 0$, $v_{GS} < V_{tn} = 3$ V.

GS-KVL gives $v_{GS} = 10 > V_{tn} = 3$ V. Therefore, NMOS is NOT in cut-off.

Assume NMOS in saturation: $i_D = 0.5k_n'(W/L)_n(v_{GS} - V_{tn})^2$ and $v_{DS} > v_{GS} - V_{tn}$. Substituting for i_D in GS-KVL, we get:

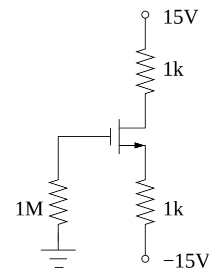
$$\text{GS-KVL:} \quad 10 = v_{GS} + 10^3 \times 0.2 \times 10^{-3}(v_{GS} - 3)^2 = v_{GS} + 0.2v_{GS}^2 - 1.2v_{GS} + 1.8$$

$$v_{GS}^2 - v_{GS} - 41 = 0 \quad \rightarrow \quad v_{GS} = -5.92 \text{ V} \quad \text{and} \quad v_{GS} = 6.92 \text{ V}$$

Negative root is unphysical so $v_{GS} = 6.92$ V. GS-KVL give $i_D = 3.08$ mA. DS-KVL gives $v_{DS} = 20 - 6.16 = 13.8$ V Since $v_{DS} = 13.8 > v_{GS} - V_{tn} = 6.92 - 3 = 3.92$ V, our assumption of NMOS in saturation is justified.

In sum, NMOS is in saturation with $v_{GS} = 6.92$ V, $v_{DS} = 13.8$ V, and $i_D = 3.08$ mA

Problem 22. In circuit below find v_{GS}, i_D, v_{DS}, and state of the transistor (Use $k'_n(W/L)_n = k'_p(W/L)_p = 0.4$ mA/V^2,$\lambda = 0$, $V_{tn} = 3$ V and $V_{tp} = -3$ V).



$$\begin{aligned}
\text{GS-KVL:} \quad & 0 = v_{GS} + 10^3 i_D - 15 \\
\text{DS-KVL:} \quad & 15 = 10^3 i_D + v_{DS} + 10^3 i_D - 15 \\
& 30 = 2 \times 10^3 i_D + v_{DS}
\end{aligned}$$

Assume NMOS is in cut-off: $i_D = 0$, $v_{GS} < V_{tn} = 3$ V.

GS-KVL gives $v_{GS} = 15 > V_{tn} = 3$ V. Therefore, NMOS is NOT in cut-off.

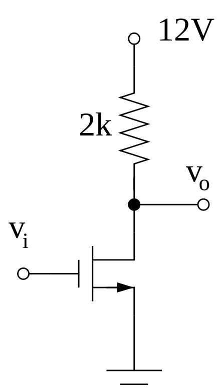
Assume NMOS in saturation: $i_D = 0.5k'_n(W/L)_n(v_{GS} - V_{tn})^2$ and $v_{DS} > v_{GS} - V_{tn}$. Substituting for i_D in GS-KVL, we get:

$$\begin{aligned}
\text{GS-KVL:} \quad & 0 = v_{GS} + 10^3 \times 0.2 \times 10^{-3}(v_{GS} - 3)^2 - 15 \quad \rightarrow \quad 0 = 5v_{GS} + (v_{GS} - 3)^2 - 75 \\
& v_{GS}^2 - v_{GS} - 66 = 0 \quad \rightarrow \quad v_{GS} = -7.64 \text{ V} \quad \text{and} \quad v_{GS} = 8.64 \text{ V}
\end{aligned}$$

Negative root is unphysical so $v_{GS} = 8.64$ V. i_D relationship gives $i_D = 6.3$ mA. DS-KVL gives $v_{DS} = 17.5$ V. Since $v_{DS} = 17.5 > v_{GS} - V_{tn} = 8.64 - 3 = 5.64$ V, our assumption of NMOS in saturation is justified.

In sum, NMOS is in saturation with $v_{GS} = 8.64$ V, $v_{DS} = 17.5$ V, and $i_D = 6.3$ mA

Problem 23. Find v_o when $v_i = 0$ and $12\ V$ (Use $k'_n(W/L)_n = 0.5$ mA/V^2,$\lambda = 0$, $V_{tn} = 2$ V).



$$\begin{aligned}
\text{GS-KVL:} \quad & v_{GS} = v_i \\
\text{DS-KVL:} \quad & 12 = 2 \times 10^3 i_D + v_{DS}
\end{aligned}$$

A) $v_i = 0$ V. From GS-KVL, we get $v_{GS} = v_i = 0$. As $v_{GS} < V_{tn} = 2$ V, NMOS is in cut-off, $i_D = 0$, and v_{DS} is found from DS-KVL:

$$\text{DS-KVL:} \quad v_o = v_{DS} = 12 - 2 \times 10^3 i_D = 12 \text{ V}$$

B) $v_i = 12$ V. From GS-KVL, we get $v_{GS} = 12$ V. Since $v_{GS} > V_{tn}$, NMOS is not in cut-off. Assume NMOS in saturation mode. Then:

$$i_D = 0.5k'_n(W/L)_n(v_{GS} - V_{tn})^2 = 0.25 \times 10^{-3}(12 - 2)^2 = 25 \text{ mA}$$

$$\text{DS-KVL:} \quad v_{DS} = 12 - 2 \times 10^3 i_D = 12 - 25 \times 2 \times 10^3 \times 10^{-3} = -38 \text{ V}$$

Since $v_{DS} = -38 < v_{GS} - V_{tn} = 12 - 2 = 10$, NMOS is NOT in saturation mode.

Assume NMOS in triode mode. Then:

$$i_D = 0.5k'_n(W/L)_n[2v_{DS}(v_{GS} - V_{tn}) - v_{DS}^2] = 0.25 \times 10^{-3}[2v_{DS}(12 - 2) - v_{DS}^2]$$

$$i_D = 0.25 \times 10^{-3}[20v_{DS} - v_{DS}^2]$$

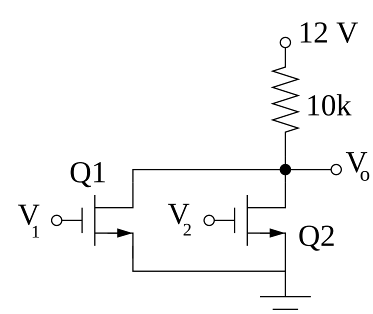
Substituting for i_D in DS-KVL, we get:

$$\text{DS-KVL:} \quad 12 = 2 \times 10^3 i_D + v_{DS} \quad \rightarrow \quad 12 = 2 \times 10^3 \times 0.25 \times 10^{-3}[20v_{DS} - v_{DS}^2] + v_{DS}$$

$$v_{DS}^2 - 22v_{DS} + 24 = 0$$

This is a quadratic equation in v_{DS}. The two roots are: $v_{DS} = 1.15$ V and $v_{DS} = 20.8$ V. The second root is not physical as the circuit is powered by a 12 V supply. Therefore, $v_{DS} = 1.15$ V. As $v_{DS} = 1.15 < v_{GS} - V_{tn} = 10$, NMOS is indeed in triode mode with $v_o = v_{DS} = 1.15$ V and

Problem 24. Show that this circuit is a NOR gate with a LOW state of 0.2 V and a HIGH state of 12 V (Use $k'_n(W/L)_n = 0.5$ mA/V^2, $V_{tn} = 1$ V).



By KVL and KCL:

$$v_{GS1} = v_1, \qquad v_{GS2} = v_2, \qquad v_o = v_{DS1} = v_{DS2}$$

$$i_1 = i_{D1} + i_{D2}$$

$$12 = 10,000 i_1 + v_o$$

Case 1: $v_1 = v_2 = 0.2$. Since $v_{GS1} = 0.2 < V_{tn} = 1$ and $v_{GS2} = 0.2 < V_{tn} = 1$, both transistors will be in cut-off: $i_{D1} = i_{D2} = 0$. Then, $i_1 = i_{D1} + i_{D2} = 0$ and from KVL,

$v_o = 12$ V.
So, When $v_1 = 0.2$ (LOW) and $v_2 = 0.2$ (LOW), $v_o = 12$ V (HIGH).

Case 2: $v_1 = 0.2, v_2 = 12$ V. Since $v_{GS1} = 0.2 < V_{tn} = 1$, Q_1 will be in cut-off and $i_{D1} = 0$. Since $V_{GS2} = 12 > V_{tn} = 1$, M_2 will not be in cut-off. Assume M_2 is in saturation mode. Then:

$$i_{D2} = 0.5k_n'(W/L)_n(v_{GS2} - V_{tn})^2 = 0.25 \times 10^{-3}(12-1)^2 = 30 \text{ mA}$$
$$v_{DS2} = v_o = 12 - 10,000(i_{D2} + i_{D1}) = -288 \text{ V}$$

Since $V_{DS2} < v_{GS2} - V_{tn} = 12 - 1 = 11$ V, M_2 is not in saturation mode. Assume M_2 is in triode:

$$i_{D2} = K[2v_{DS2}(v_{GS2} - V_{tn}) - v_{DS2}^2] = 0.25 \times 10^{-3}[22v_{DS2} - v_{DS2}^2]$$
$$12 = 10,000 i_{D2} + v_{DS2} \quad \rightarrow \quad 12 = 2.5[22v_{DS2} - v_{DS2}^2] + v_{DS2}$$
$$v_{DS2}^2 - 22.4v_{DS2} + 4.8 = 0$$

The two roots are: $v_{DS2} = 22.2$ V and $v_{DS2} = 0.22$ V. First root is not physical as the circuit is powered by a 12 V supply. So, $v_{DS2} = 0.2$ V. Since $v_{DS2} = 0.2 < v_{GS2} - V_{tn} = 12 - 1 = 11$, our assumption of M_2 in triode mode is justified.
So, When $v_1 = 0.2$ (LOW) and $v_2 = 12$ V (HIGH), $v_o = 0.2$ V (LOW).

Case 3: $v_1 = 12, v_2 = 0.2$ V. This is similar to case 2. By symmetry:
When $v_1 = 12$ V (HIGH) and $v_2 = 0.2$ (LOW), $v_o = 0.2$ V (LOW).

Case 4: $v_1 = 12, v_2 = 12$ V. Since $v_{GS1} = 12 > V_{tn} = 1$, and $v_{GS2} = 12 > V_{tn} = 1$, both transistors will be ON. Since the two transistors are identical, $i_{D1} = i_{D2} = 0.5i_1$ and $v_{DS1} = v_{DS2}$ and both transistors will be in the same state (we only need to analyze one of them). Assume both transistors are in triode mode:

$$i_{D2} = K[2v_{DS2}(v_{GS2} - V_{tn}) - v_{DS2}^2] = 0.25 \times 10^{-3}[22v_{DS2} - v_{DS2}^2]$$
$$12 = 2 \times 10,000 i_{D2} + v_{DS2} \quad \rightarrow \quad 12 = 5[22v_{DS2} - v_{DS2}^2] + v_{DS2}$$
$$v_{DS2}^2 - 22.2v_{DS2} + 2.4 = 0$$

The two roots are: $v_{DS2} = 22.1$ V and $v_{DS2} = 0.11$ V. First root is not physical as the circuit is powered by a 12 V supply. So, $v_{DS2} = 0.11$ V. Since $v_{DS2} = 0.11 < v_{GS2} - V_{tn} = 12 - 1 = 11$, our assumption of M_2 in triode mode is justified. Similarly, we find $v_{DS1} = 0.11$ V.
So, When $v_1 = 12$ V (HIGH) and $v_2 = 12$ V (HIGH), $v_o = 0.1$ V (LOW).

Since the output is HIGH only when both inputs are LOW, this is NOR gate.