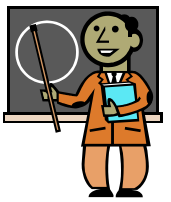
Implementation of Components and Circuits

- Fundamental concepts
- Examples

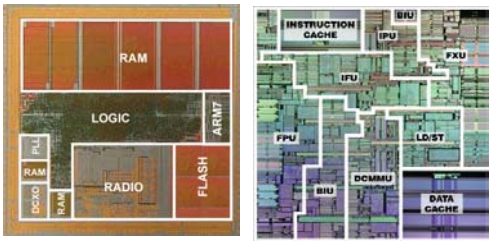
Outline

- Layout basic concepts and examples
- Layout vs. Schematic: origin of differences
  - Fabrication
  - Design
- Design rules
- Layout of large area components
- Layout for matching
- Effects of Layout on IC reliability
- Layout for reliability



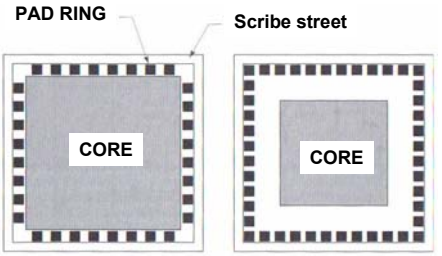
Floorplan

- Sketch of the layout
- Estimation of the IC area
- Technology dependent
  - List of components – subcircuits
    - View
    - Library - models
  - Physical layers available



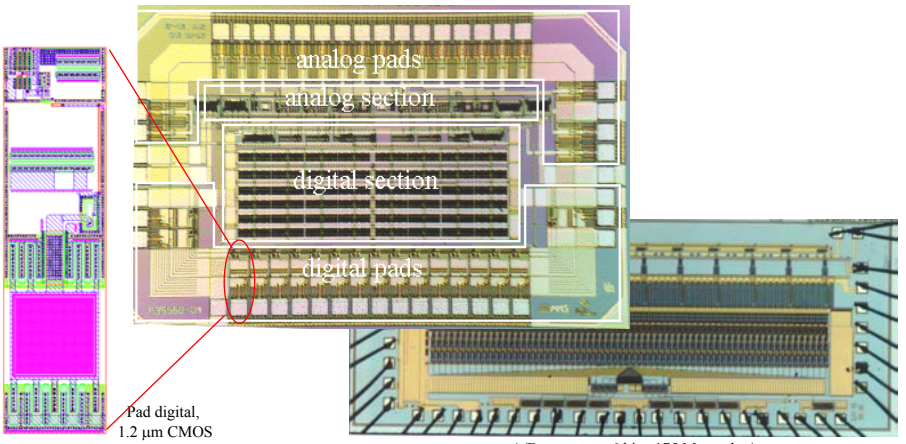
Floorplan of a communications SoC (left) and microprocessor (right)

- Pad limited vs. Core limited designs



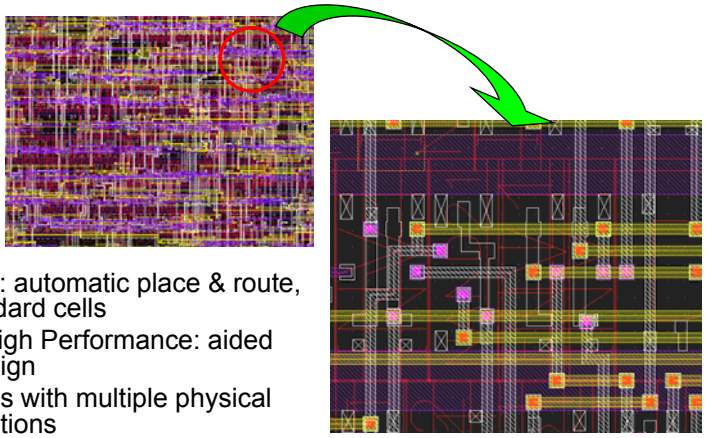
Pads

- Provide surface for bond-wire soldering
- Include I/O protection circuitry



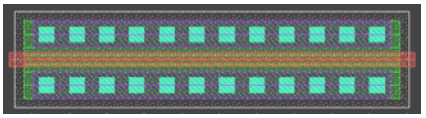
A/D converter, 6 bits, 175 Msamples/s

Layouts

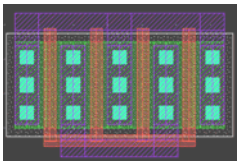


- Digital logic: automatic place & route, use of standard cells
- Analog & High Performance: aided manual design
- Components with multiple physical implementations
  - Resistors
  - Capacitors
  - Bipolar transistors
  - Power components

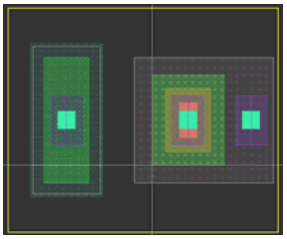
Example of components: transistors



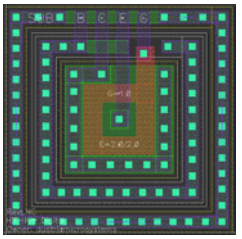
Single-gate NMOS, 0.35 μm



Multiple-gate NMOS, 0.35 μm



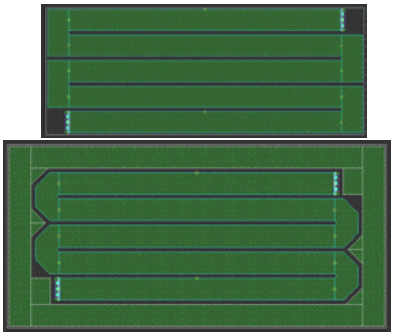
Vertical NPN BJT, 0.35 μm



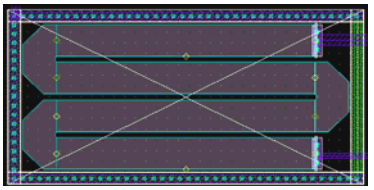
Lateral BJT, 0.35 μm

Example of components: passives

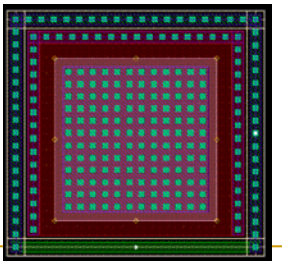
- N Diffusion resistor



- Polysilicon resistor

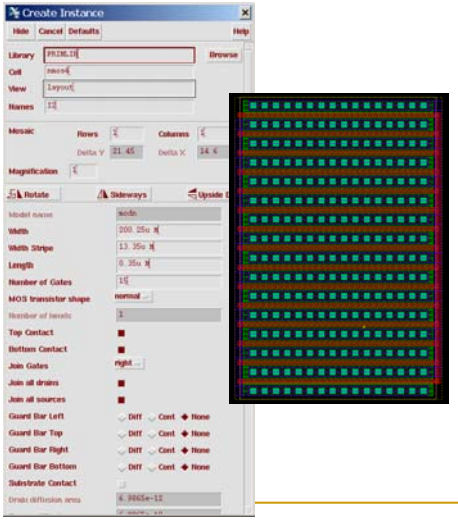


- Polysilicon capacitor

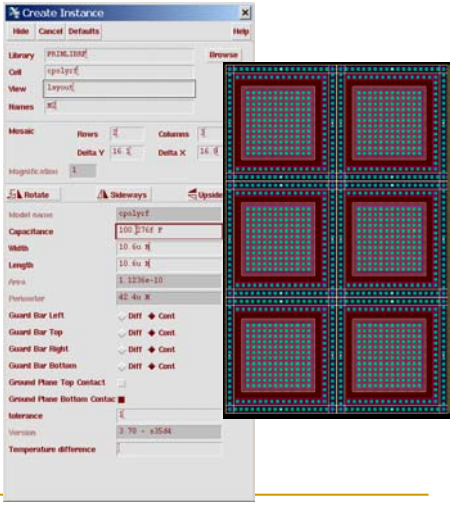


P-cells

- NMOS transistor



- Polysilicon capacitor



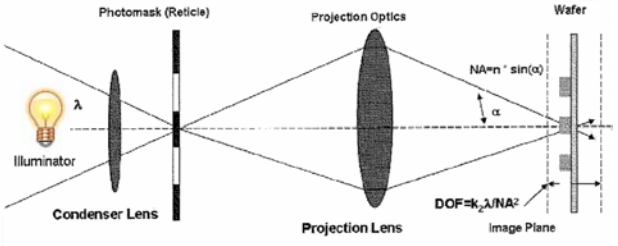
Designing a layout: CAD Tools

- Layout design aids in nowadays CAD Tools:
  - Library of components' layouts (Design Kit)
  - Parameterized layouts
  - Automatic layout generation (Place & route)
  - Layout vs. Schematic
  - Rules checking
  - Extractor and layout simulation
- Is the proposed layout a good layout?

Designing a layout: CAD Tools

- A good layout must be:
  - Ease manufacturability (increase yield)
  - Robust to variations
  - Robust to gradients (matching)
  - Robust against perturbations
  - Robust against other undesired phenomena

Lithography



from Chiang, Kawa: "Design and Manufacturability and Yield for Nano-Scale CMOS", Springer 2007

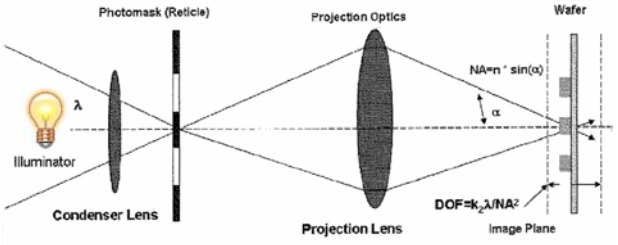
Illuminator: can be Krypton Floride (KrF, λ=248 nm), Argon Floride (ArF, λ=193 nm), Fluorine (F2, λ=157 nm).

Condenser Lens: focuses light on 4x (or 5x) mask

Photomask: made of fused quartz (aka. fused silica)

Projection lens: focuses light on wafer
characterized by its **numerical aperture NA**

Lithography



from Chiang, Kawa: "Design and Manufacturability and Yield for Nano-Scale CMOS", Springer 2007

Definition of numerical aperture NA

$$NA = n \cdot \sin\alpha$$

where *n* is a diffraction index:
1 for air
~1.5 for water, oils

Rayleigh's equations:

$$resolution = k_1 \frac{\lambda}{NA} \qquad depth\ of\ \ focus\ (DOF) = k_2 \frac{\lambda}{NA^2}$$

where k_1, k_2 depend on the quality of the photolithography system (typ. $k_1 \sim 0{,}25 - 0{,}7$, $k_2 \sim 0{,}5$)

Lithography

• Example: which is the critical dimension that can be achieved with λ=248 nm?
Reasonable NA for air is 0,8
Guess k_1=0,4

$$resolution = 0,4\frac{248nm}{0,8} = 124nm$$

• Example: which is the critical dimension that can be achieved with λ=193 nm?
Reasonable NA for air is 0,8
Guess k_1=0,3

$$resolution = 0,3\frac{193nm}{0,8} = 72nm$$

Lithography

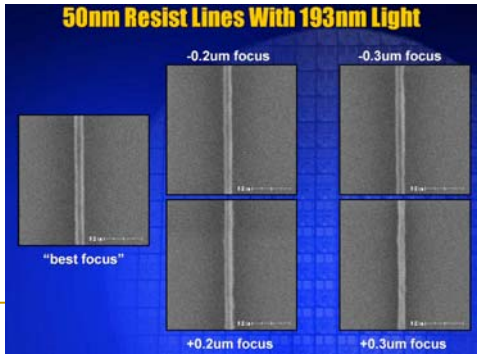
• 436 nm: used down to 3 μm technologies

• 365 nm: used down to 0,6 μm technologies

• 248 nm: used down to 130 nm technologies

• 193 nm in air (dry lithography)

Used in technologies down to 90 nm
(still in use for some layers in 65 nm, 45 nm...)



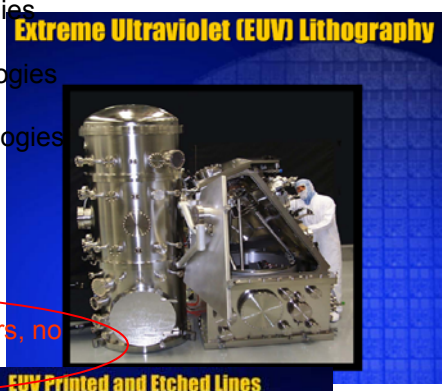
Lithography

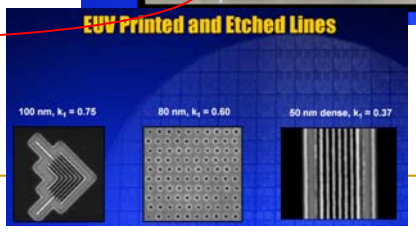
- 436 nm: used down to 3 μm technologies
- 365 nm: used down to 0,6 μm technologies
- 248 nm: used down to 130 nm technologies
- 193 nm in air (dry lithography)
- 157 nm: needs special lens materials

Abandoned definitively in 2005 (due to technical difficulties associated with the mask and photoresist materials for this wavelength; also for the economical cost)

Lithography

- 436 nm: used down to 3 μm technologies
- 365 nm: used down to 0,6 μm technologies
- 248 nm: used down to 130 nm technologies
- 193 nm in air (dry lithography)
- ~~157 nm: needs special lens materials~~
- EUV (λ=13 nm). New approach: mirrors, no lenses



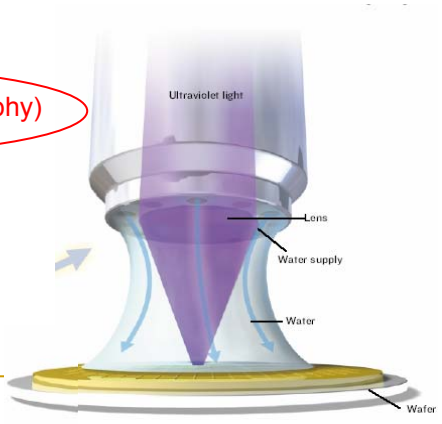


Optimistic forecast: ready for 22 nm technology node (~2011)

Lithography

- 436 nm: used down to 3 μm technologies
- 365 nm: used down to 0,6 μm technologies
- 248 nm: used down to 130 nm technologies
- 193 nm in air (dry lithography)
- 193 nm in liquid (immersion lithography)

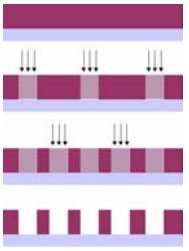
Used in 65 nm, 45 nm, (32 nm) technology nodes (NA 1.1 → 1.3)

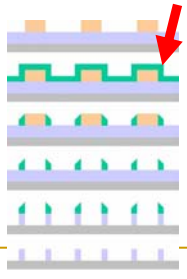


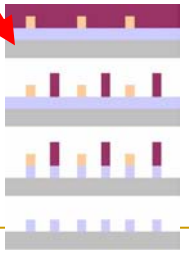
Lithography

- 193 nm in air (dry lithography)
- 193 nm in liquid (immersion lithography)

Double patterning: generate a single layer by using two masks

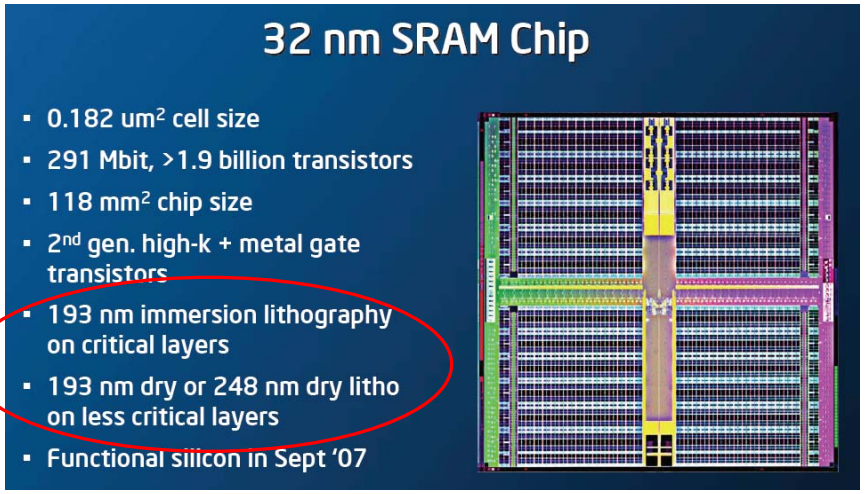

Double exposure


Spacer mask

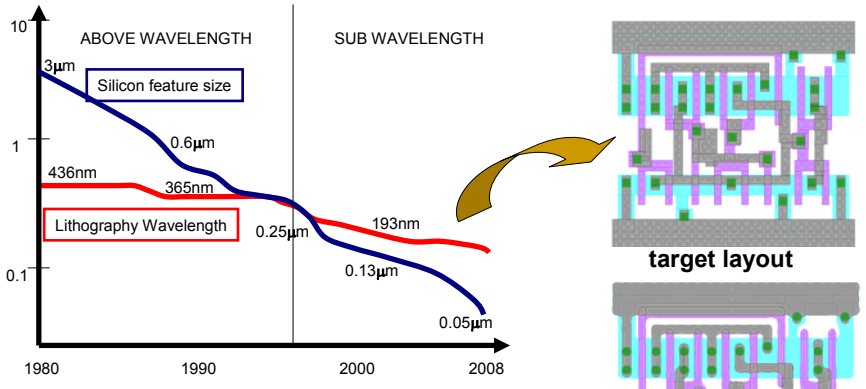

Heterogeneous mask

Used in 65 nm, 45 nm, technology nodes

Lithography



Manufacturing: subwavelength gap

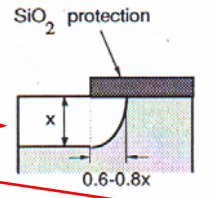


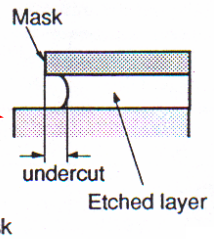
⇒ Increased difraction effects!

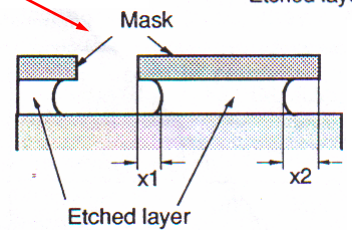
from Massimo Conti, BCN 2006

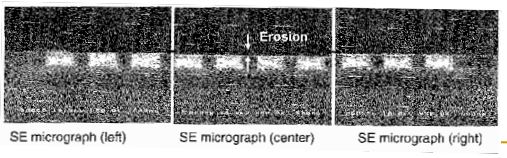
Differences between layout and Circuit (I)

- Fabrication process limitations
  - Lateral diffusion
  - Etching under protection
  - Boundary dependent etching
  - Three-dimensional effects
    - Chemical Mechanical Polishing (CMP)
    - Surface topography



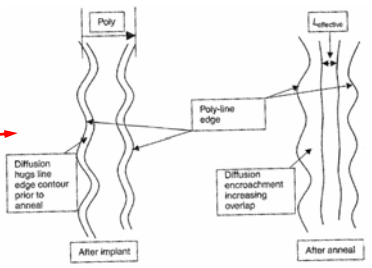


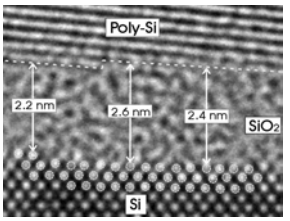




Differences between layout and Circuit (II)

- Fabrication process limitations
  - Narrowing after annealing
  - Inherent grain variability
  - Proximity effects
  - Errors and limitations
    - Mask productions
    - Mask alignment





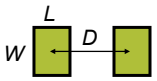
Oxide variations over a 20 Å nominal oxide thickness

Differences between layout and Circuit (III)

- Absolute accuracy of physical parameters
  - Controlled at technological level
  - Simulation: Process variation

$$\frac{\sigma^2(\beta)}{\beta^2} = \frac{A_\beta^2}{WL} + S_\beta^2 D^2$$

$$\sigma^2(V_T) = \frac{A_{V_T}^2}{WL} + S_{V_T}^2 D^2$$

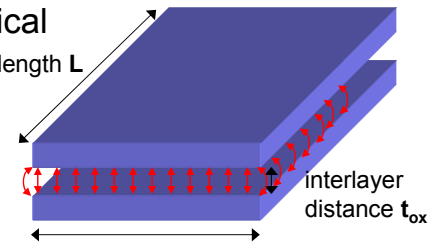


from Massimo Conti, BCN 2006

Differences between layout and Circuit (III)

- Absolute accuracy of physical parameters

$$C = \varepsilon_{dielectric} \frac{L \cdot W}{t_{ox}}$$



$$\left(\frac{C}{\Delta C}\right)^2 = \left(\frac{\varepsilon_{dielectric}}{\Delta\varepsilon_{dielectric}}\right)^2 + \left(\frac{t_{ox}}{\Delta t_{ox}}\right)^2 + \left(\frac{L}{\Delta L}\right)^2 + \left(\frac{W}{\Delta W}\right)^2$$

- oxide damage
- impurities
- temperature
- stress
- bias conditions

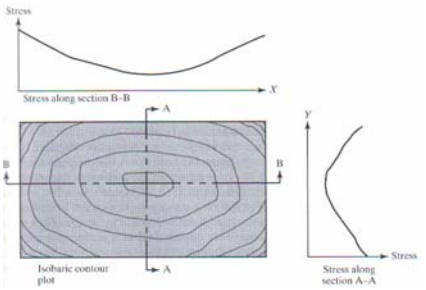
- growth rate
- grain size

- etching inaccuracy
- mask alignment

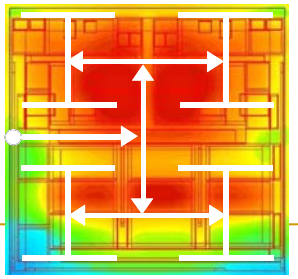
from Franco Maloberti, "Layout of Analog CMOS ICs"

Differences between layout and Circuit (IV)

- Relative inaccuracies of physical parameters
  - Gradients, local variations
    - Compensated with suitable layout techniques
  - Crystal orientation variations
    - Components required to be laid in a determined orientation



Pressure gradients



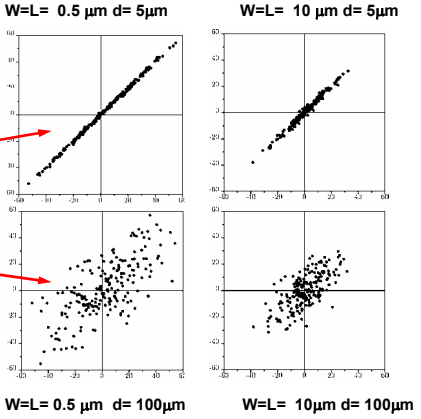
Thermal gradients

Differences between layout and Circuit (IV)

- Example: normalized drain current dispersions of 2 MOSFETs for different geometries and distances

Inaccuracy in absolute value, but matched devices

Inaccuracy in absolute value, and mismatched devices



from Massimo Conti, BCN 2006

Differences between layout and Circuit (V)

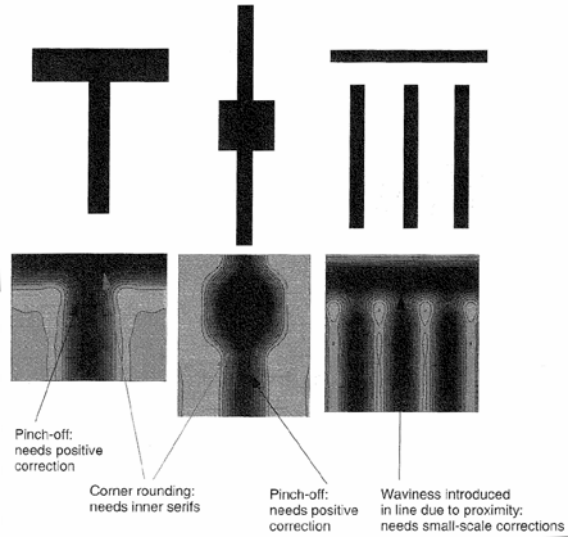
- Parasitic coupling
  - Capacitive coupling
  - Couplings through the power supply
  - Couplings through the substrate
- Parasitic resistances
  - Contacts
  - Interconnect

What you get is not what you draw!

- Many of the systematic inaccuracies can be avoided through good layout style.
- But designers must understand the limitations and apply design techniques to mitigate these effects.

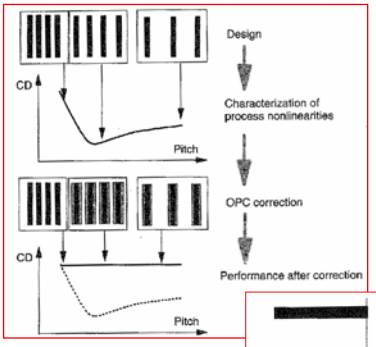
Corrections performed by the foundry

- Some manufacturing distortions can be predicted and fixed by introducing modifications to the mask
  - OPC: Optical Proximity Correction

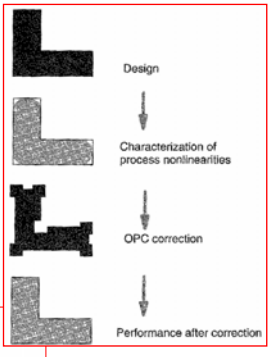


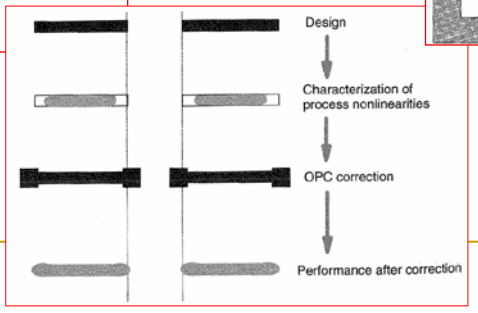
From "Nano-CMOS Circuit and Physical Design", Wong et al, IEEE Press

Corrections performed by the foundry



Examples of corrections automatically introduced by a OPC algorithm to the shapes in the mask





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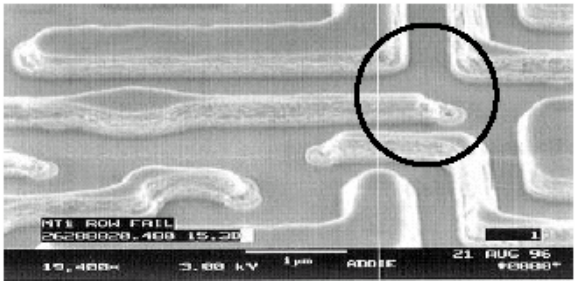
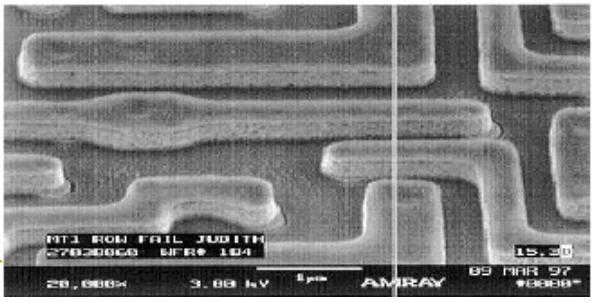


This top down SEM image was taken without any OPC. The pullback over the contact is clearly seen

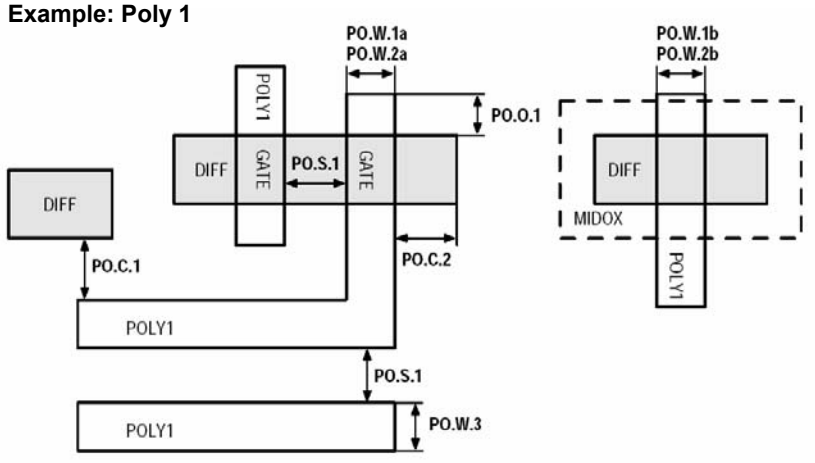
This image of the same structure was taken with OPC implemented on the mask. Good contact coverage can be seen.



From Intel Ireland

Design for manufacturability: design rules:

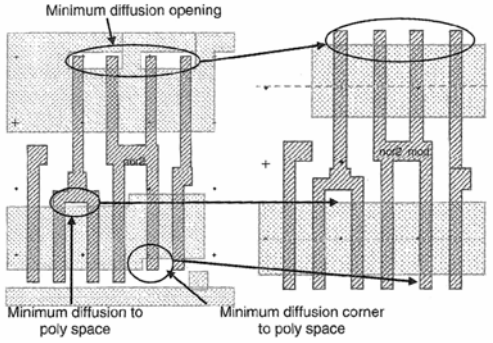
Example: Poly 1



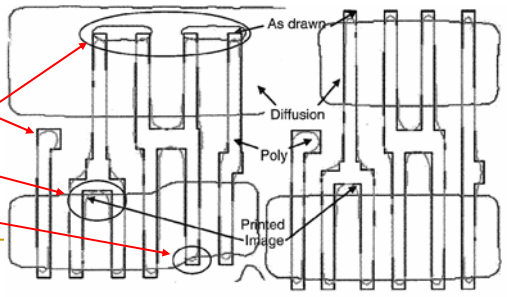
Example of design rules for POLY 1

- PO.W.1a
  - Minimum gate length of PMOS
- PO.W-2a
  - Minimum gate length of NMOS
- PO.W.3
  - Minimum POLY1 width for interconnect
- PO.S.1
  - Minimum POLY1 spacing
- PO.C.1
  - Minimum POLY 1 to DIFF spacing
- PO.C.2
  - Minimum DIFF extension of GATE
- PO.O.1
  - Minimum POLY1 extension of GATE

Optimized layouts:



Bad layout **Optimized layout**

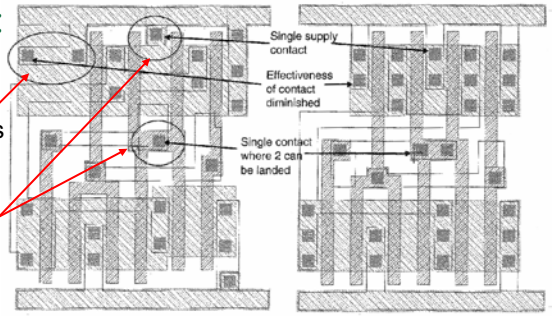


From "Nano-CMOS Circuit and Physical Design", Wong et al, IEEE Press

Optimized layouts:

Optimize efficiency of vias/contacts

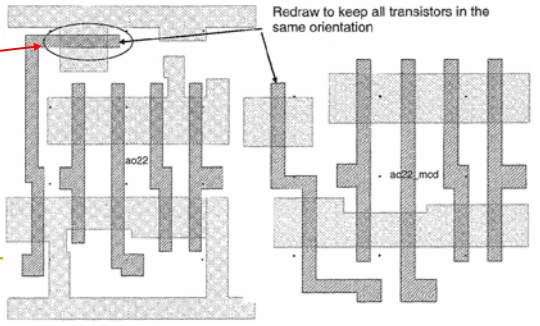
Maximize number of vias/contacts



Optimized layout

All transistors in the same orientation

- Better control of manufacturing
- Easier lithography (mask) corrections



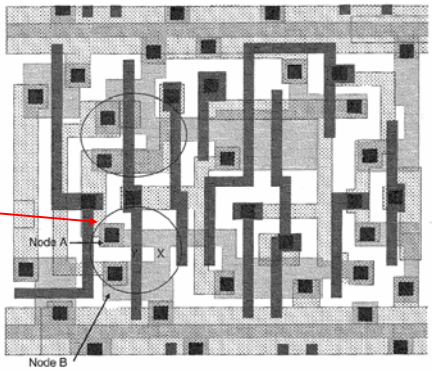
From "Nano-CMOS Circuit and Physical Design", Wong et al, IEEE Press

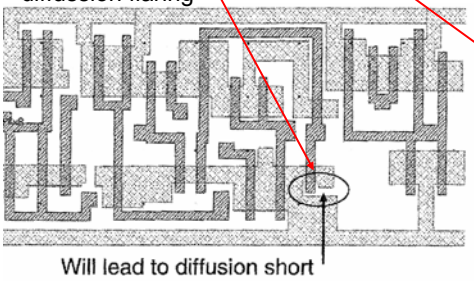
Optimized layouts:

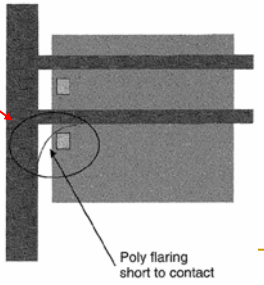
Possible shortcircuit of nodes A and B due to diffussion flaring and mask misalingment

Possible shortcircuit due to poly flaring

Possible shortcircuit due to diffussion flaring



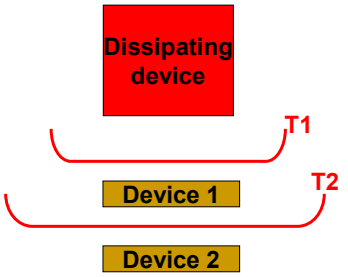


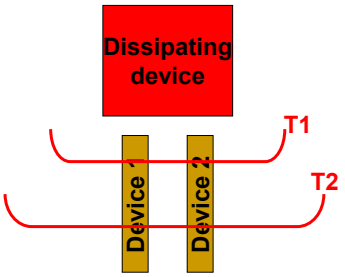


From "Nano-CMOS Circuit and Physical Design", Wong et al, IEEE Press

Layout for matching

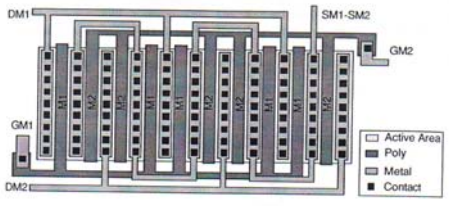
- Devices with the same orientation
  - Current in the same direction
- Gradients increase with distance
- Same orientation towards physical gradients



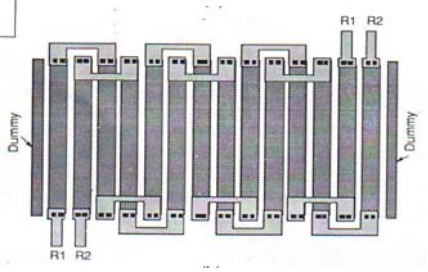


Layout for matching

- Interdigitated structures



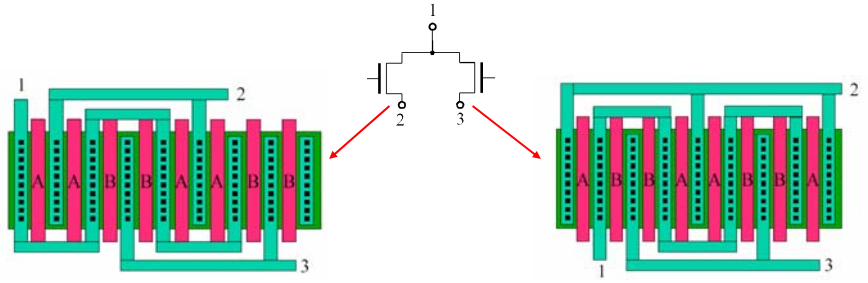
MOS transistors M1 and M2



Resistors R1 and R2

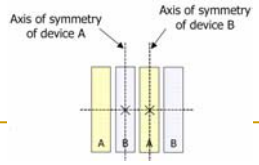
Layout for matching

- Interdigitated structures

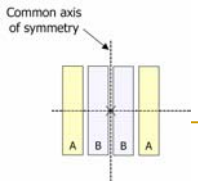


Different symmetry axes for transistors A and B

Same symmetry axis for transistors A and B



from Franco Maloberti, "Layout of Analog CMOS ICs"



Layout for matching

- Common centroid:

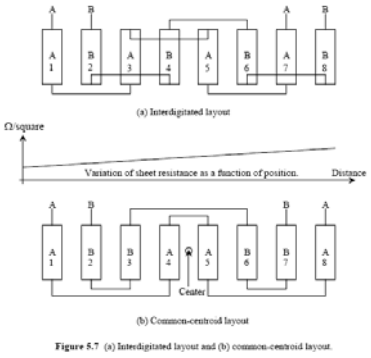
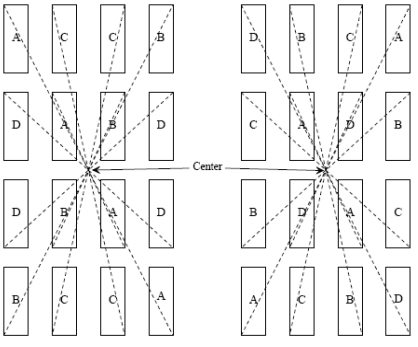


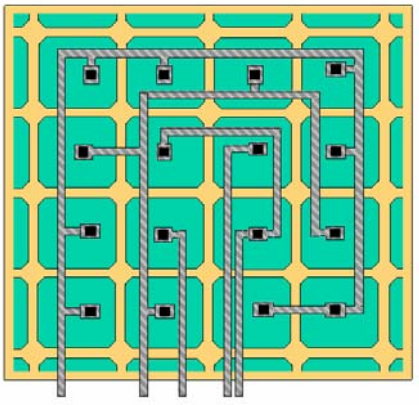
Figure 5.7 (a) Interdigitated layout and (b) common-centroid layout.

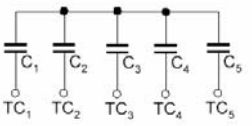


Layout for matching: Common centroid

- Coincidence
  - Centroids of matched devices should coincide
- Symmetry
  - Array symmetric around both X and Y axis
- Dispersion
  - Segment of each device distributed throughout the array as uniformly as possible
- Compactness
  - Ideally: array should be square

Layout for matching: Common centroid



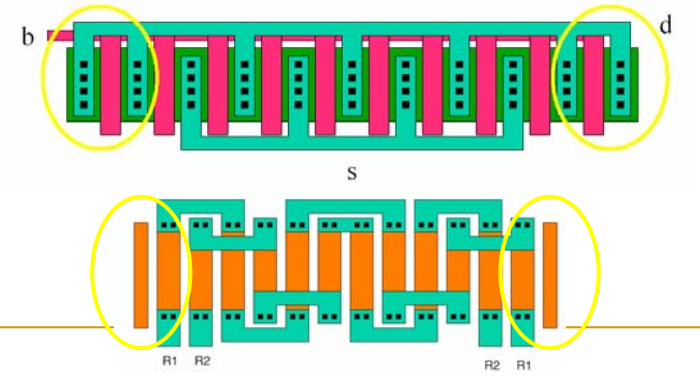


$C_2 = C_1$
$C_3 = 2C_1$
$C_4 = 4C_1$
$C_5 = 8C_1$

from Franco Maloberti, "Layout of Analog CMOS ICs"

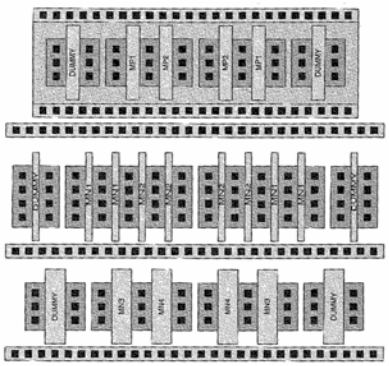
Layout for matching: Use of dummies

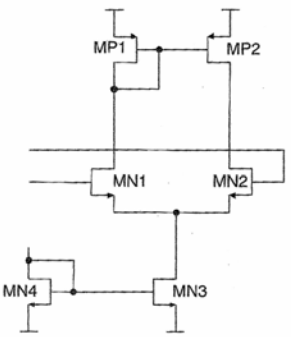
- Dummies
  - Use dummy devices to provide the same contour conditions.
    - Ground dummies (do not let them float)
    - Dummies can be full (shorted) devices, or part of them
    - Beware of their parasitics!



Layout for matching: Use of dummies

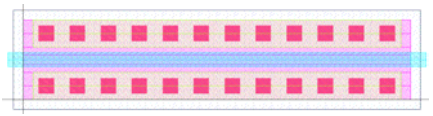
- Reference cell
  - Use multiple basic transistors instead of different sizes
    - Same W, same orientation,

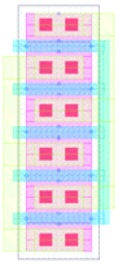




Design of large area components

- MOS Transistors
  - Multiple gates to minimize serial resistance
  - Multiple contacts to minimize serial resistance
    - No big contacts!!!
  - “stacked” structures
    - Lower parasitic capacitances
    - Lower area
  - Analogue applications
    - Avoid minimum size

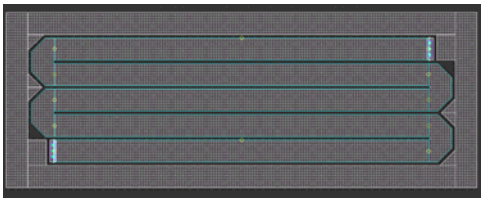




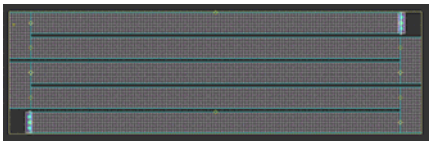
Automatically generated layouts
AMS, 0.35 microns, 10/0.35

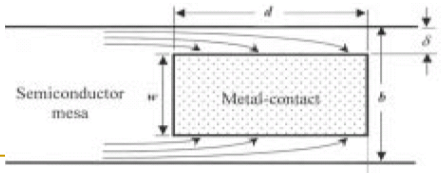
Design of large area components

- Resistances
  - Bended structures
  - Dummy structures
  - 45 degrees (avoid non laminar current flow)
  - Contacts
    - Current in the same direction
    - Multiple contacts
  - Piezoresistive effect



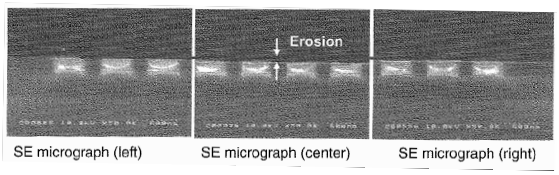
Resistor: 5K, 275x3 sq microns.
Example of “good” and “bad” layout

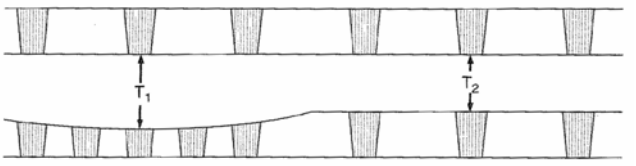




Layout for matching: interconnects

- CMP:
  - Erosion effect: denser interconnects will have higher R





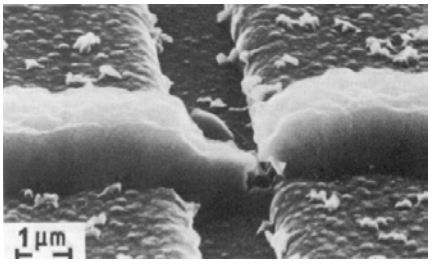
From "Nano-CMOS Circuit and Physical Design", Wong et al, IEEE Press

Rules for matching

- Same W and L: Vary M
- Capacitors
  - Multiple M of a capacitance reference C_R
- Ms: Even (factors of 4!!)
- Clean and balanced routing
  - IR drops
  - Parasitic capacitance and couplings
  - Kelvin connections
- Avoid minimum sizing and overlapping
- Use dummy structures
- Same spacing in interconnects

Layout Strategies for circuit reliability (I)

- Electromigration
  - **Electromigration** is the transport of material caused by the gradual movement of the ions in a conductor due to the momentum transfer between conducting electrons and diffusing metal atoms
  - Dependent on:
    - Temperature
    - Current density
    - Conductor Shape
    - Material

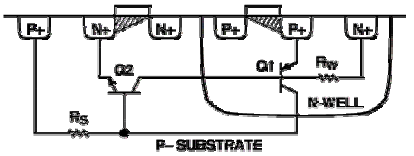


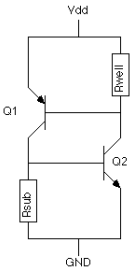
Layout for reliability: Electromigration

- Exist technological preventive measures
  - Type of metal layer (Cu better than Al)
  - Oxidation (better over field oxide)
  - Use of protective overcoats
- Width of interconnections: M µm/mA
  - Typical M: between 1 and 0.5
- Maximum current per contact and vias

Layout Strategies for circuit reliability (II)

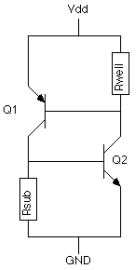
- Latch-up
  - A **latchup** is the inadvertent creation of a low-impedance path between the power supply rails of an electronic component, triggering a parasitic device, which then acts as a short circuit, leading to malfunctioning of the part and perhaps even its destruction with the overcurrent





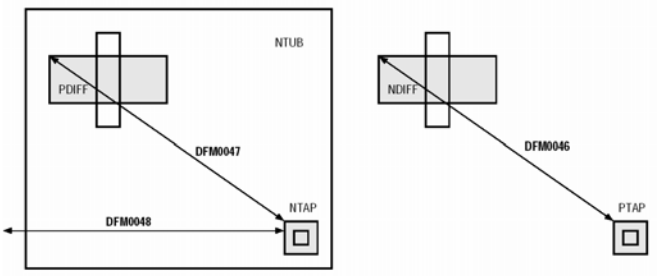
Layout for reliability: Latch-up

- Activation:
  - If voltages higher than VDD
  - If voltages lower than GND
  - If currents through the well/substrate
  - I/O Circuitry more sensitive
- Elimination of minority carriers
  - Guard rings
  - Biased with low resistances
- Reduce beta parasitic transistors. Reduce forward bias resistance



Layout for reliability: Latch-up

- Reduce forward bias resistance:



Rules:

Description
Maximum distance from any point inside NSD to the nearest PTAP
Maximum distance from any point inside PSD to the nearest NTAP
NTUB must be covered with NTAP sized by

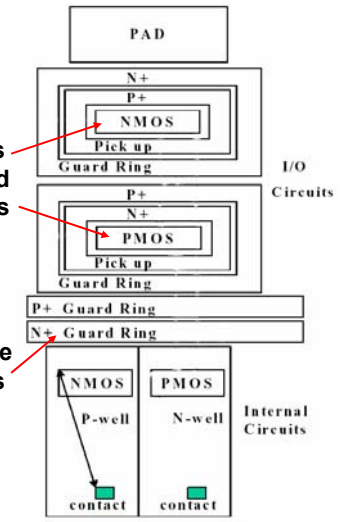
Layout for reliability: Latch-up

- I/O Circuitry more sensitive

Guideline	Description	Value [um]
LAT.1a	A double guard ring structure should be inserted in between NMOS and PMOS of I / O buffers	
LAT.1b	Minimum PTAP and NTAP guard ring width for I / O buffers	X
LAT.1c	Maximum distance from PTAP or NTAP guard ring to source DIFF for I / O buffers	X
LAT.2	Minimum NMOS to PMOS spacing for I / O buffers and ESD devices Active DIFF area in this spacing is not allowed.	X
LAT.3	Maximum distance from any point inside source / drain DIFF to the nearest TAP DIFF of the same NTUB or PSUB.	
LAT.4	A guard ring structure with NTUB pseudo-collector and PTAP should be inserted between I / O buffers and internal circuit area	
LAT.5	Minimum I / O buffer to internal circuit spacing	X
LAT.6	Any HOT_NDIFF area connecting to I / O pads should be surrounded by double guard ring.	
LAT.7	Any NTUB without direct connection to VDD and with HOT_NDIFF inside it should be surrounded by double guard ring.	
LAT.8	For special devices such as bipolar transistor, diode, resistor, or special circuits such as charge pump, power regulator, high noise or high power circuitry, a double guard ring should be inserted surrounding and between them.	
LAT.9	All the guard rings and pickups should be connected to VDD / VSS with very low series resistance. That is, NTUB should be tied together with NTAP, and DIFF should be tied together with contacts and metal to VDD / VSS. As many as possible CONT should be used.	

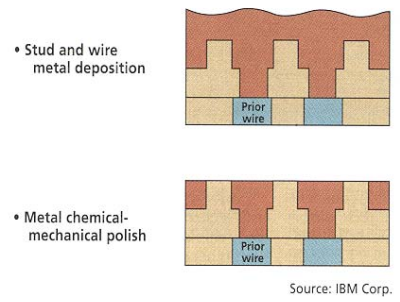
I/O transistors surrounded by pick-ups and guard rings

I/O and core transistors separated by guard rings



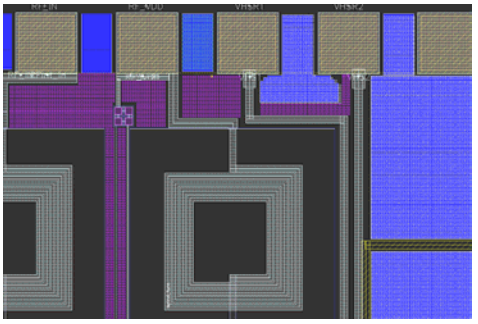
Layout Strategies for circuit reliability (III)

- CMP
  - Chemical Mechanical Polishing or Chemical Mechanical Planarization
  - Removal any irregular topography
  - Surface within the depth of field of a photolithography system.

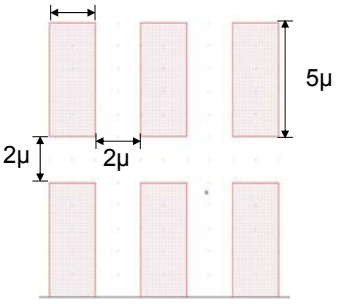


Layout for reliability: CMP

- Example: MOSIS 0.25
  - (TSMC)
- Design rules:
  - Minimum % coverage of
  - Metal layers
  - Polysilicon layers
  - Capacitor Layers



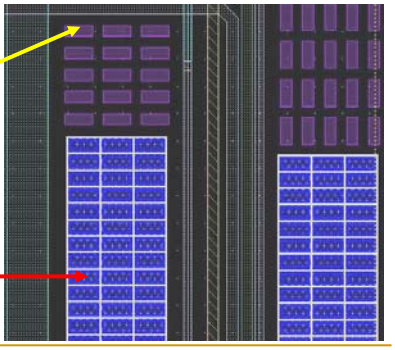
Layout for reliability: CMP



Dummy patterns are distributed over the chip as uniformly as possible in order to reach the required coverage for each material (Metal 1, 2, 3, 4, 5, Poly 1 and CTM (capacitor top metal))

All Metal Fill pattern
(staked M1, M2, M3, M4)

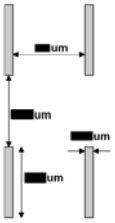
Poly 1 Fill pattern as metal



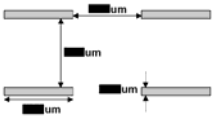
Layout for reliability: CMP

1. Orientation of dummy pattern should be perpendicular to previous layer
2. Top layer should have larger dummy pattern

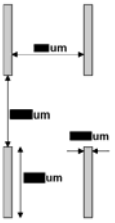
Example: 4-metal technology



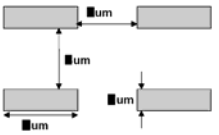
Pattern for M1



Pattern for M2



Pattern for M3

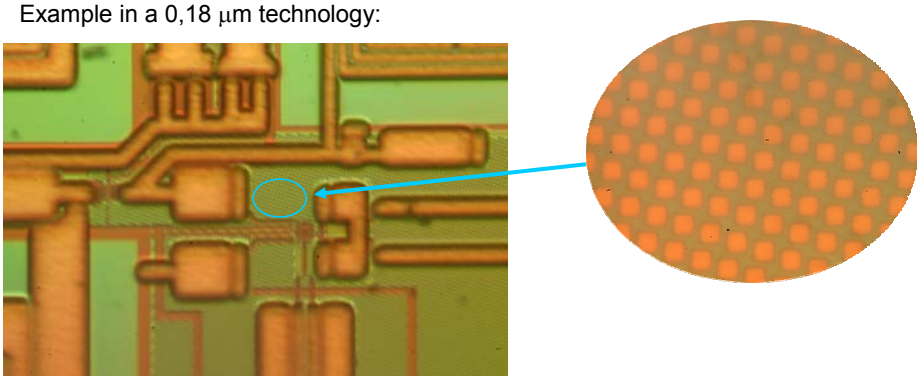


Pattern for M4 (top)

Layout for reliability: CMP

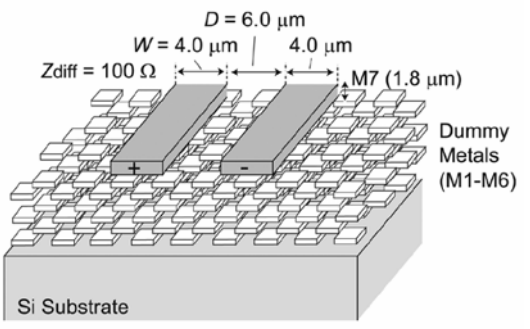
- Patterns generated automatically by the foundry
- User has masks to define areas that will NOT be filled with patterns (Ex: inductors, capacitors, test strcutures, etc)

Example in a 0,18 μm technology:



Layout for reliability: CMP

Example of Transmission line in M7 with dummy metals below :



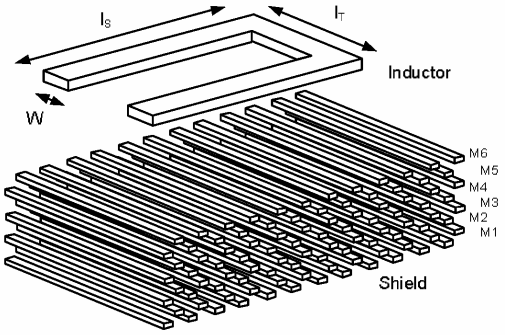
"A Bidirectional and Multi-Drop Transmission-Line Interconnect...", IEEE JSSC April 2008

Open question: How do dummy metal fills affect transmission lines and passives ?

Layout for reliability: CMP

Proposal: slow-wave transmission lines

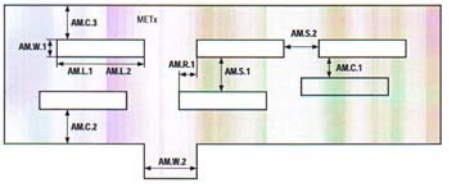
- Low Q
- Small area
- Necessary grid fulfills metal coverage



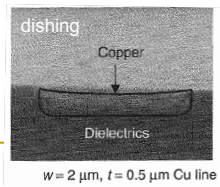
Boermans et al. "VCO design for 60 GHz applications using differential shielded inductors in 0.13 µm CMOS". RFIC08

Layout for reliability: CMP

- Slots
  - Act both as stress releasers and to minimize dishing
  - Slots in metals W> Value (tech. dependent)
  - Possible library of components
    - Corners
    - Pads



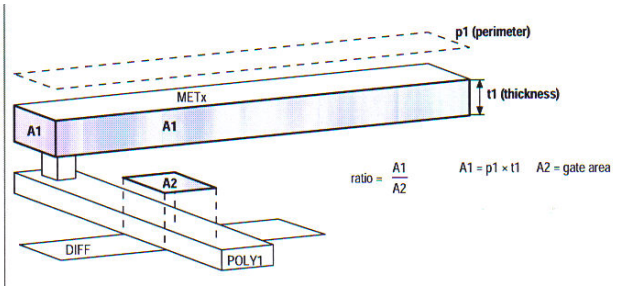
AM.C.1	Minimum slots spacing between neighbor layers (i.e.: MET1 / MET2, MET2 / MET3, MET3 / MET4)
AM.C.2	Minimum slot to inner metal edge spacing
AM.C.3	Minimum slot to outer metal edge spacing
AM.W.2	Minimum width of METx connected to wide METx with slots No slot is allowed opposite this metal
AM.R.1	Starting position of parallel slots should be staggered.
AM.R.2	Slot must be parallel to the current direction.



$w = 2\ \mu m$, $t = 0.5\ \mu m$ Cu line

Layout Strategies for circuit reliability (IV)

- Antenna Effects or Plasma-Induced damage
  - The "Antenna Rules" deal with process induced gate oxide damage. Reactive ion-etching may induce charges to exposed polysilicon and metal structures. If these structures are connected to gates (and not to diffusion), they may develop potentials sufficiently large to cause Fowler Nordheim current to flow through the thin oxide



Layout for reliability: Antenna

- Vulnerability depends on ratio between periphery/area of trapping material to gate area
- Fab. 1: Rules Poly and metal layers (including contacts)
  - Max perimeter ratio of field poly to active poly
  - Max perimeter ratio of floating metals to active poly
  - Max drawn area of CO vs. Active Poly

Poly and Metal ratio definition

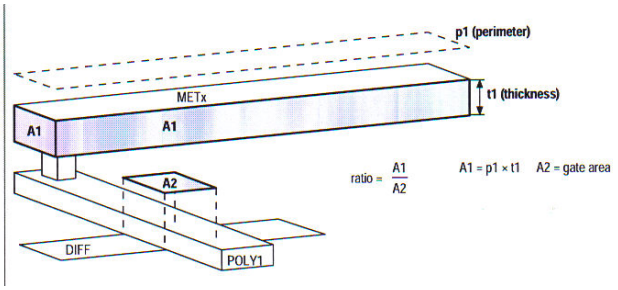
$$ratio = \frac{2[(L1+W1)\cdot Z1]}{W2\cdot L2}$$

Contact and via ratio definition

$$ratio = \frac{\text{Contact(Via) area}}{W2\cdot L2}$$

Layout for reliability: Antenna

- Fab. 2
  - Maximum floating (Poly,Metal) Edge area ratio to active area ratio.

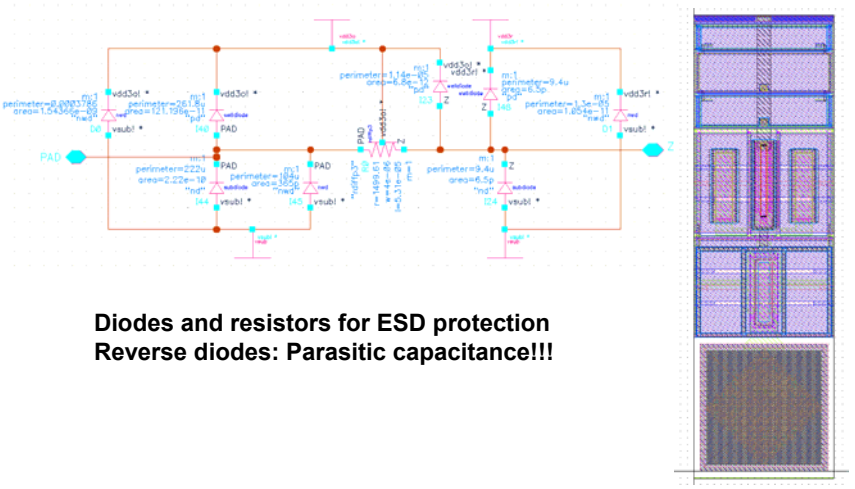


- Use of “leakers” and metal jumpers

Layout Strategies for circuit reliability (V)

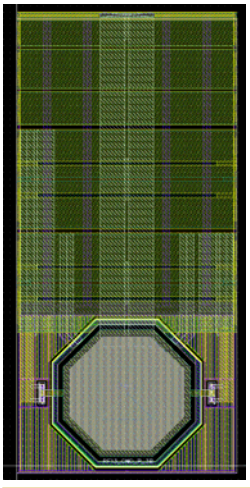
- ESD
  - Electrostatic Discharge
  - Damage in dielectrics due to IC manipulation (mainly gate oxide)

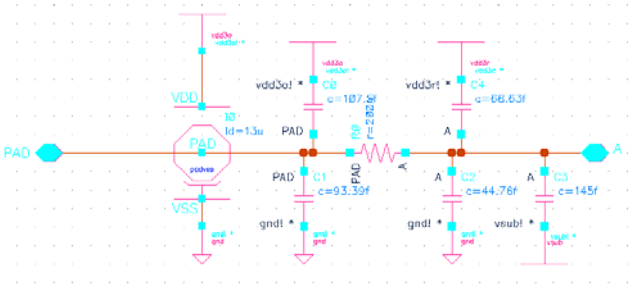
Layout for reliability: Analog PAD



Diodes and resistors for ESD protection
Reverse diodes: Parasitic capacitance!!!

Example of RF PAD without diodes





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