Implementation of Input Block of Minimally Buffered Deflection NoC Router

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***Abstract* - The traditional system on chip designs employ the shared bus architecture for data transfer in highly integrated Multiprocessor system on chips(MPSoC).Network on chip (NoC)is a new paradigm for on chip communication for Multiprocessor systems on chips(MPSoCs). NoCs replace the traditional shared buses system with routing switches. Heart of the NoC is the router and it consists of an input buffer, arbiter, crossbar and an output port. The NoC router uses a buffer to store the incoming packets. These buffers improve the performance but they consume more power and area. Bufferless deflection routing is the solution for improvement in energy efficiency. In this method deflections of the packets take place to overcome the contention problem. But at high network load, deflection routing degrades the performance because of unnecessary hopping of data packets.**

The MinBD (minimally buffered deflection) router is a new router design that uses a small buffer for bufferless deflection routing. In this paper the input block of MinBD router is implemented on FPGA which shows that a small buffer will help to reduce the network deflection rate. It also improves the performance and energy efficiency while buffering only deflected data packets.

***Keywords*-** MPSoC, NoC, Router, Minimally buffered deflection router (MinBD),FPGA

I. INTRODUCTION

As technology scaling allows the integration of billions of transistors on a chip, it evolves MPSoC architectures which allow more processors and more cores to be placed on a single chip. Usually for MPSoC architectures, interconnections among various devices or cores are based on shared bus. Share bus architecture allows only one communication transaction at a time. Hence scalability is a major concern with shared bus system. A solution for such communication bottleneck is use of switching network, NoC(Network on chip) to interconnect various cores of MPSoC [2] . NoC has emerged as scalable and suitable design approach to solve the interconnection problem for MPSoC architecture.

NoC architecture consists of three main parts, namely routers, link and network interface through which cores are interconnected to the NoC. Router is the heart of NoC as it coordinates data packet propagation from source to destination port based on information received from scheduler. Router consists of input port, arbiter, crossbar and output port. In most of the router design, input port is having buffer to temporarily store data packets and then transfer to destination port through crossbar. These buffers improve performance in term of increasing the bandwidth efficiency but consume significant power. These buffers consume dynamic power when read/ write operation is taking place and static energy when they are empty. Secondly buffers occupy more chip network area. In the TRIPS prototype chip, input buffers of routers were occupying 75% of total on chip network area. Hence there is a need for bufferless routers which eliminate input and output buffers [3].

Various bufferless routing algorithms have been proposed to overcome the disadvantages of a buffered router [4, 5, 6, 7, 8]. CHIPPER and BLESS are the best examples of bufferless routers [5, 7]. Yu Cai et al. Prove that bufferless routing saves up to 30% power consumption and 38% area reduction in mesh or tours topology compared with buffered architecture [9]. CHIPPER NoC implementation shows that when compare with buffered routing, it reduces average network power by 54% and area by 36.2% for 8X8 mesh topology [5].

The key idea for bufferless routing is that data packets are never buffered in the network. When two packets contend for the same link, one is deflected. Thus Bufferless deflection routing causes unnecessary hopping of data packets for high network utilization. It increases data packets traversals and reduces network throughput and also increases dynamic power. MinBD (minimally buffered deflection routing) provides the solution for bufferless deflection routing [4].

This paper is organized as follows. In section II, we discussed working principle of MinBD deflection router. Implementation of efficient input block of router is presented in section III. In section IV, we evaluate our proposed design for various test cases. Router input block is implemented on FPGA. The conclusions are given in section V.

II. MINIMALLY BUFFERED DEFLECTION ROUTING (MinBD)

MinBD routing is the solution for bufferless deflection router at high network load[4]. When the network is highly utilized, contention between data packets occurs quite often, and many data packets will get deflected when the destination port is not available. This unnecessary hopping will increase dynamic energy consumption and also the latency of the network. The key solution is provided for this problem by using a MinBD deflection router. In this router, small side buffer is added to reduce deflection rate. These side buffers are used to store data packets in case of the contention of data packets. This will reduce deflection caused by using small buffering. Key principles of working of MinBD router are

- In case of contention of data packets, it is better to buffer the data packets and arbitrate in a later cycle. In this case, small buffering can avoid many deflections. This helps us reducing in the power consumption and size of the chip.
- It may possible that data packets will be routed to destination port in first attempt. Hence in this scenario, buffering of data packets lead to unnecessary power overhead. So router should buffer a data packet if required. Thus data packets that would have been deflected in a bufferless deflection router are removed from the network temporarily into side buffer. It is called injection of data packets in side buffer. This reduces network deflection rates.
- Finally when the data packet arrives at its destination, it should be ejected from the network, so that it does not continue to contend with other data packets.

Following figure 1 shows the block diagram of MinBD deflection router.

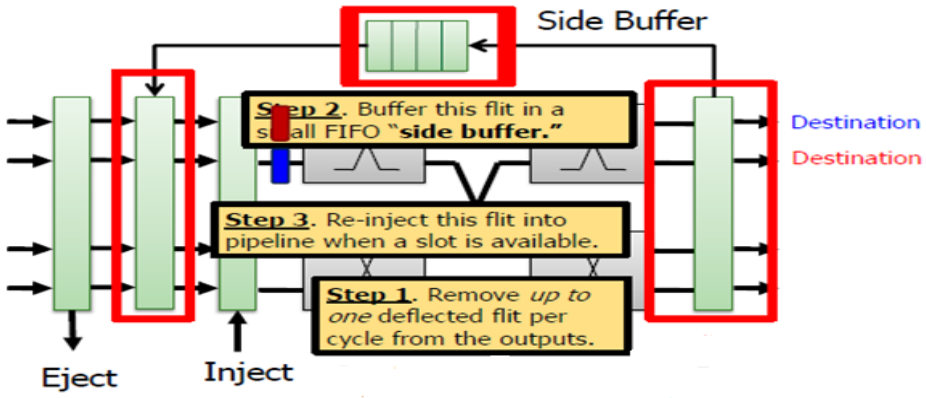

Fig 1: MinBD deflection router [4]

Following three steps are involved in MinBD deflection router:

1) Remove up to one deflected data packet per cycle from the outputs
2) Buffer this data packet in a small FIFO side buffer
3) Re inject this data packet into pipeline when a port is available

III. IMPLEMENTATION OF INPUT BLOCK OF MinBD ROUTER

Figure 2 shows the basic NoC structure with mesh topology. As shown in the figure, NoC is having some fundamental blocks such as network adaptors, network links and routing nodes. For NoC architectures, there are various topologies are available, such as mesh, torus, tree, butterfly, polygon, and star topology [10]. But mesh topology is recommended by many researchers because of its layout efficiency, scalability and low power consumption [1][11].

Design of NoC router consists of input port, arbiter, cross bar and output port. Each router node is consisting of 5 ports as shown in figure 3. In 5 port router data packets are coming from 4 directions such as North, East, West, South and the remaining one port is connected with processing element (PE). Processing unit sends the data to destination port through the required direction. Here the port can be shared in 2 directions. Data is transmitted in 2D (2-Dimensional) directions, such as X axis and Y axis directions. XY routing is more preferred for mesh topology. In this paper the design of input block with small buffer is explained and results for various test cases are validated.

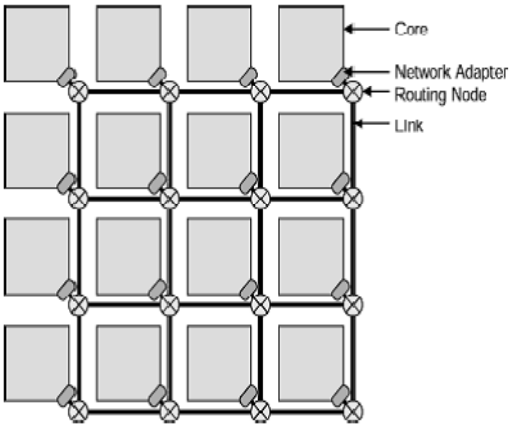

Fig 2: NoC structure with Mesh topology

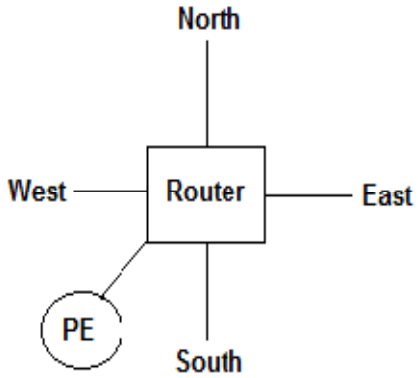

Fig 3: Five port NoC router

IV. DESIGN OF INPUT BLOCK OF ROUTER

As discussed in above sections, it is always better to have a small side buffer in router input port, which helps to improve the power efficiency and reduce the deflection rates. In the proposed design, for each router node in each direction, one buffer is used. Here buffer size is assumed as a single memory location in each direction of input port, but if required, we can use small FIFO as a side buffer. Data packets are having 22 bits which comprises 16 bits of data, 3 bits for source address and next 3 bits are of destination address. Here the assumption is that the scheduler will generate two control signals such as the grant signal for each direction of port and the control signal for side buffer to store data when destination port is not available. Following cases are considered in order to explain operation of input block with a side buffer.

Case I: If there is no contention of data packets

If there is no contention of data ports, in such condition data packet is directly transferred to destination port. There is no need to save data packet in the side buffer.

Case II: Use of side buffer when destination port is not available

If destination port is not free, then data packets will be stored in the side buffer. After few clock cycle there will be reinjection of data packets from the side buffer.

Case III: When side buffer is occupied with data and next data is also required side buffer

To solve this issue efficient design of scheduler is required. Scheduler will grant the access to re-inject the data packets after specific clock cycles. Always preference is given first for side buffer to re-inject the data and thereafter store the new data packets to the side buffer in case of contention.

The design is implemented using Verilog HDL on SPARTAN 3 family with XC3S4000 device, FG 456 package. Simulation is done by using ISIM simulator and synthesis is performed using XST tool of Xilinx ISE 14.2. Following table gives logic utilization for implemented input block of router.

Table I: Logic Utilization for Input Block of Router

Logic Utilization	Used	Available	Utilization
Number of Slice Flip Flops	190	7,168	2%
Number of 4 input LUTs	100	7,168	1%
Number of occupied Slices	100	3,584	2%
Number of Slices containing only related logic	100	100	100%
Number of Slices containing unrelated logic	0	100	0%
Total Number of 4 input LUTs	100	7,168	1%
Number of bonded IOBs	202	264	76%
Number of BUFGMUXs	1	8	12%
Average Fanout of Non-Clock Nets	2.82		

Power Dissipation Summary:

On chip power is calculated by using XPower analyser tool. Dynamic and static power is given in the following table.

Table II: On Chip Power Summary

On-Chip	Power (mW)
Clocks	3.40
Logic	2.02
Signals	3.67
IOs	373.75
Quiescent	61.95
Total	444.80

Following figure 4 shows the simulation results of input block of router for various test cases.

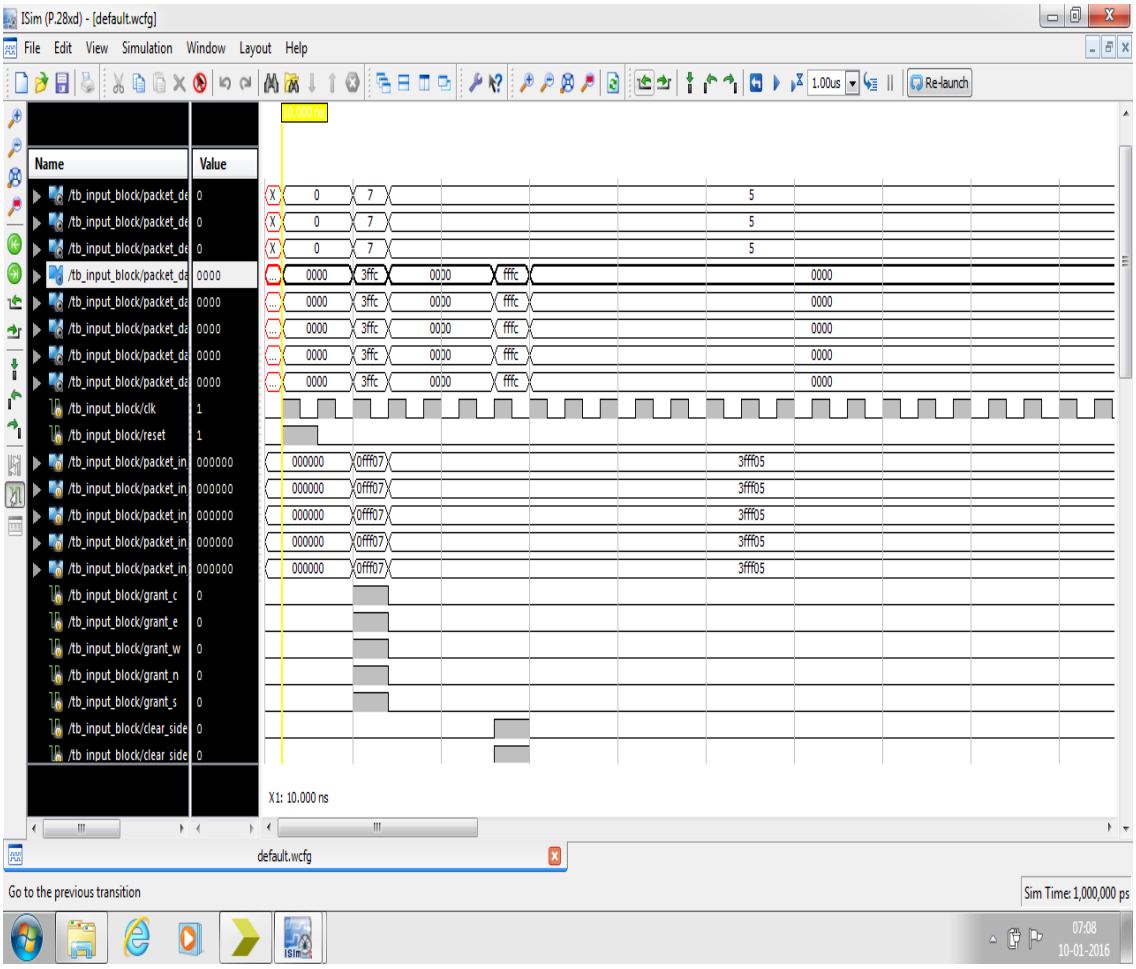

Fig 4: Simulation result of input block of router with small buffer

V. CONCLUSION

In this paper we have discussed the advantages of the MinBD router over the conventional buffered router. MinBD router stores only deflected data packets in small buffers instead of storing all data packets in input buffers. Hence it requires only a small buffer size for input port as compared to the conventional input buffered router. It saves significant energy and area of a router. Input block of the router with a single memory as a buffer is implemented using FPGA. We can increase the buffer size but effective reduction in power and area would not be achieved. Hence there is trade off between buffer size and performance of the router. We intend to work on an effective design of a scheduler to avoid data packet loss and also improve latency.

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AUTHOR PROFILE

Priti Shahane received Bachelor degree in Electronics engineering from Nagpur University and Master degree in Digital System from Pune University, India. She is pursuing Ph. D from Symbiosis International University, Pune. Her research interests include Network on chip router architectures, FPGA based dynamic partial reconfiguration.

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