Implementation of Integrated Circuits for Industrial Application using Gallium Arsenide Technology

Jugdutt Singh

B.Sc. (First Class Hons Electronic Eng.) UK, **M.Sc.** (Electrical Eng.) Canada

A thesis submitted for the research degree of

Doctor of Philosophy

to the Department of Electrical and Electronic Engineering

Faculty of Engineering and Science

Victoria University of Technology

AUSTRALIA

1997

To my wife, Dr. Mohini Singh and sons Deepak and Amrish

for their love and encouragement

in all my endeavors

Contents

Chapter One

Chapter Two

Chapter Three

Device Modelling and Performance Estimation 47

Chapter Four

GaAs MESFET Circuit Design Techniques 67

Chapter Seven

Data Converters and Overcurrent Protection Relays 188

Chapter Nine

VLSI Implementation of an Eight-bit Multi-Function Multi-Protection Relay 244

List of Figures

List of Tables

List of Principal Symbols and Abbreviations

ΔV_o	logic voltage swing
μ	electron mobility
β	HSPICE transconductance parameter
α	hyperbolic tangent drain voltage multiplier
Ω	ohm
λ	output conductance parameter
ε	permittivity
ϕ_B	barrier potential
δV_a	quantisation error
ADC	analog-to-digital converter
BiCMOS	bipolar CMOS
C_0	line capacitance per unit length
CDFL	capacitor diode MESFET logic
C_{ds}	drain-to-source capacitance
C_{gd}	gate-to-drain capacitance
C_{gs}	gate-to-source capacitance
C_L	load capacitance
CMOS	complementary metal oxide semiconductor
C_N	node capacitance

D-MESFET	depletion mode MESFET
DAC	digital-to-analog converter
DCFL	direct coupled MESFET logic
E-MESFET	enhancement mode MESFET
ECL	emitter coupled logic
eV	electron Volts
f	switching frequency
G	voltage gain
GaAs	gallium arsenide
g_m	transconductance
g_{nd}	ground bus
g_o	output conductance
HBT	hetrojunction bipolar transistor
HEMT	high electron mobility transistor
I	current
IC	integrated Circuit
I_{ds}	drain current
I_o	current through common source
k	boltzmann's constant
l	line length
L_0	line inductance per unit length
LSI	large scale integration
M	diode ideality factor
MESFET	metal semiconductor field effect transistor

MOS	metal oxide semiconductor
MSI	medium scale integration
q	electron charge
P_d	dynamic power dissipation
P_{st}	static power dissipation
R_0	line resistance per unit length
R_{ds}	drain-to-source resistance
ROM	read only memory
S/QN	signal-to-quantisation noise
SCFL	source coupled MESFET logic
SDCFL	source follower DCFL
SDFL	Schottky diode MESFET logic
SFFL	source follower MESFET logic
SRAM	static read access memory
SSI	small scale integration
T	temperature
t	time
t_a	sampling time
TDFL	two phase dynamic MESFET logic
t_m	time multiplier setting
$t_{pd(n)}$	propagation delay negative going transition
$t_{pd(p)}$	propagation delay positive going transition
t_{phl}	propagation delay, high to low
t_{plh}	propagation delay, low to high

ULSI	ultra large scale integration
Vout	output voltage
V_a	analog voltage
V_{dd}	supply voltage bus
V_{ds}	drain to source voltage
V_{gs}	gate to source voltage
V_{IH}	input high voltage
V_{IL}	input low voltage
V_{in}	input voltage
V_{inv}	inverter threshold voltage
VLSI	very large scale integration
V_{OH}	output voltage high
V_{OL}	output voltage low
V_{ref}	reference voltage
V_{SW}	switching voltage
V_t	device threshold voltage
V_{tdep}	threshold voltage D-MESFET
V_{tenh}	threshold voltage E-MESFET
W, L, and a	width, length and area of a MESFET
W_{pd}, L_{pd}	pull down MESFET width and length
W_{pu}, L_{pu}	pull up MESFET width and length
Z_0	line impedance per unit length

Abstract

The VLSI circuit normally has to meet the design requirements concerning the performance of the circuit, namely speed, power dissipation and size of the chip. The optimum design of the integrated circuit is the one that meets the speed requirements while dissipating the minimum possible power, without exceeding the power dissipation requirements and occupies the minimum possible area.

Silicon metal oxide semiconductor (MOS) technology has been the main medium for computer and system applications for a number of years and will continue to fill this role in a foreseeable future. However, the silicon logic has speed and power limitations that are already becoming apparent in the state-of-art fast integrated circuit design. Carrier mobility, saturation velocity and existence of semi-insulating substrate are the key factors in very high speed operation in a semiconductor medium.

Gallium Arsenide (GaAs) technology is attractive for the design and implementation of high speed digital ICs, mainly because of the inherent properties of the material, namely, high electron mobility, high peak electron velocity and low intrinsic carrier concentration, which yields semi-insulating substrates. Low intrinsic carrier concentration reduces device and interconnection capacitances, and is a requirement for high speed operation at reduced power dissipation. In this research GaAs was chosen as the semiconductor medium because it fulfils the above requirements and together with

low power dissipation, provide a technology base for new generation of integrated circuits.

The primary objective of this research is the design and implementation of a multi-channel data acquisition chip for measurement and instrumentation applications and a multi-function multi-protection relay chip for power systems protection. Real-time data processing systems operating in Gigabit rate are primarily limited by the analog-to-digital converter (ADC) performance. The four-bit data acquisition chip is based on very fast flash ADC with multiplexed inputs. In a flash ADC, the conversion time is equal to the propagation delays of the comparator and the encoding logic. However, the complexity of the circuit increases rapidly with the increase in the number of bits. For example, when an eight-bit flash ADC needs 255 comparators for its realisation, a nine-bit ADC requires 511 comparators for its implementation. This increase in complexity of the hardware discourages its feasibility of implementation for bigger number of bits.

The implementation of the ADC in this research is based on an algorithm that requires only $2^{(n-1)}$ comparators instead of (2^n-1) comparators for a n-bit conversion [117]. This approach thus reduces the complexity of multi-bit flash ADC design. The design of the ADC is module oriented [38], which enables multi-bit high resolution flash ADC to be implemented by cascading a number of n-bit flash modules.

Hardwired and microprocessor technologies have been used for over fifteen years, in the design and the implementation of digital relays for power systems protection. Initially the protection relays were based on 8-bit microprocessors, then 16-bit microprocessors and more recently 32-bit microprocessor has been used to provide multi-function multi-protection scheme [47]. Although these schemes provide a high level of reliability and security, they require complex hardware. Since the relay functions are usually software controlled, the protection schemes are slow, making it difficult to implement multi-channel multi-function multi-protection schemes. Recent developments in the microelectronic technology, in particular GaAs digital technology, has motivated the application of GaAs VLSI technology in the implementation of relaying techniques for power systems protection. The development of a multi-function multi-protection relay is aimed at improving the performance and reliability of the present protection schemes.

For the design and implementation of the above integrated circuits, the existing GaAs design techniques were analysed and appropriate static and dynamic design techniques were developed so as to take the maximum performance advantage of this technology. Multiple-output domino GaAs circuit design technique was developed in the design of dynamic integrated circuits. The most remarkable achievement using this technique is the reduction in the number of devices required to implement a given function resulting in improved performance. Merged logic design technique has been used for the design of static GaAs integrated circuits. In this technique, direct coupled MESFET logic is predominantly used to achieve higher packing density and improved performance, source follower direct coupled MESFET logic is used to drive large capacitive loads and realise And-Or-Invert functions and source follower MESFET logic is used to achieve large fan out. The performance of these two techniques has been demonstrated with the implementation of a Carry Lookahead Generator for a Carry Lookahead Adder and a power series evaluator circuits.

Four-bit multi-channel data acquisition chip was designed, implemented and analysed using the appropriate GaAs design techniques. Source coupled GaAs MESFET logic design technique was used in the design for a mix of analog and digital circuits on the same chip, mainly because of its wide tolerance to threshold voltage range and its immunity to temperature variations. The digital components of the chip were designed using the merged logic design technique. The four-bit multi-channel data acquisition chip was implemented with 397 GaAs devices and dissipated only 185.6 milliWatts of power with conversion time of 0.85 nanosecs.

An eight-bit multi-function multi-protection integrated circuit was designed using GaAs merged logic design technique. The digital chip was implemented with 400 GaAs MESFET devices and dissipated only 49.73 milliwatts of power.

The performance evaluation of the above ICs indicate the validation of the GaAs technology and design techniques developed in the implementation of the very fast low power integrated circuits.

Statement of Originality

I hereby certify that the work embodied in this thesis is the result of original research and has not been submitted for a higher degree to any other University or Institution.

This thesis may be made available for consultation within the University Library and may be photocopied or lent to libraries for the purpose of consultation if accepted for the award of the degree.

(Signed) Jugdutt Singh

Jugdutt Singh

Publications

Papers Presented and Published in Journals and Referred Conferences

The following papers are the direct outcome of this research.

[1] Zayegh, A., Kalam, A., Singh, J. and Malyniak, R., "Ultrafast multi-channel data acquisition chip implemented using GaAs MESFET technology", AMSE Press, International Journal for Modelling, Measurement and Control, Vol. 68, No. 1, pp 21 - 46, Oct. 1997.

[2] Kalam, A., Zayegh, A., Singh, J. and Malyniak, R., "Implementation of multifunction overcurrent relay using GaAs VLSI technology", IASTED Publications, International Journal of Power and Energy Systems, submitted 1997.

[3] Kalam, A., Zayegh, A., Singh, J. and Malyniak, R., "Multi channel hybrid chip for power protection using E-D GaAs MESFET technology", IEEE Transaction on Power Delivery, submitted 1997.

[4] Singh, J. and Malyniak, R., "The simulation and performance of source coupled GaAs MESFET circuits", Proceeding of International Conference on Modelling and Simulation, Melbourne, Australia, pp 259 - 266, 1993.

[5] Singh, J. and Malyniak, R., "A low power high speed dynamic domino decoder implemented with GaAs MESFETs", Proceeding of IEEE International Symposium on IC Technology, Systems and Applications, Singapore, pp 485 - 489, 1993.

[6] Singh, J. and Malyniak, R., "Comparison of CMOS and GaAs technologies", Proceeding of IEEE International Symposium on IC Technology, Systems and Applications, Singapore, pp 485 - 489, 1993.

[7] Singh, J. and Malyniak, R., "High speed adder implemented with GaAs MESFETs in multiple-output domino logic, Proceeding of IREE/IE(Aust) Microelectronics, Gold Coast, Australia, pp 233 - 238, 1993.

[8] Singh, J. and Malyniak, R., "The simulation and performance of dynamic GaAs MESFET circuit", Proceeding of Australasian Conference on Instrumentation and Measurement - Test and Evaluation, Adelaide, Australia, pp 405 - 410, 1994.

[9] Singh, J. and Malyniak, R., "GaAs MESFET dynamic and static circuit design techniques", Proceeding of Asean Regional Seminar on Microelectronics and Information Technology, Bangkok, Thailand, pp 105 - 109, 1994.

[10] Singh, J. and Malyniak, R., "0.2 nsec carry lookahead adder", Proceeding of Asean Regional Seminar on Microelectronics and Information Technology, Bangkok, Thailand, pp 91 - 94, 1994.

[11] Singh, J. and Malyniak, R., "GaAs ultrafast IC for high speed digital signal processing application", Proceeding of IE(Aust) Electrical Engineering Congress, Sydney, Australia, pp 385 - 390 , 1994.

[12] Singh, J. and Malyniak, R., "GaAs MESFET digital circuit techniques", Proceeding of IEEE Int. Symposium on IC Technology, Systems and Applications, Singapore, pp 233 - 237, 1995.

[13] Singh, J. and Malyniak, R., "Implementation of neural integrated circuits in GaAs technology", Proceeding of IEEE Int. Symposium on IC Technology, Systems and Applications, Singapore, pp 117 - 121, 1995.

[14] Kalam, A., Zayegh, A., Singh, J. and Malyniak, R., "VLSI implementation of high speed multi-function multi-protection relay for power protection", Proceeding of Australasian Universities Power Engineering Conference, Melbourne, Australia, pp 417 - 422, 1996.

[15] Singh, J., Zayegh, A., Kalam, A. and Malyniak, R., "New design approach for GaAs MESFET analog-to-digital converter", IEEE International Symposium on IC Technology, Systems and Applications, Singapore, pp 672 - 675, 1997.

[16] Singh, J., Malyniak, R., Zayegh, A. and Kalam, A., "Design methodology and performance estimation of GaAs MESFET logic", IEEE International Symposium on IC Technology, Systems and Applications, Singapore, pp 410 - 413, 1997.

[17] Kalam, A., Zayegh, A., Singh, J. and Malyniak, R., "Multi-function overcurrent relay implemented using E-D GaAs MESFETs", Universities Power Engineering Conference, Manchester, UK, pp 699 - 702, 1997.

[18] Singh, J., Zayegh, A., Kalam, A. and Malyniak, R., "Design, implementation and performance of multi-channel data acquisition chip", AMSE International Conference on Modelling and Simulation, Melbourne, Australia, pp 258 - 263, 1997.

[19] Singh, J., Malyniak, R., Kalam, A. and Zayegh, A., "GaAs VLSI implementation of a polynominal evaluator chip", AMSE International Conference on Modelling and Simulation, Melbourne, Australia, pp 252 - 257, 1997.

[20] Zayegh, A., Kalam, A., Singh, J. and Malyniak, R., "Low power ultrafast analog-to-digital converter implemented using GaAs MESFETs", Proceeding of International Conference on Electronic Measurements and Instruments, Beijing, China, 1997, (accepted - in press).

Acknowledgments

I wish to express my sincere appreciation to Professor Akhtar Kalam, Dr. Aladin Zayegh and Dr. Roman Malyniak for their encouragement, assistance and guidance during this research.

My acknowledgment and gratitude also goes to Professor Kamran Eshraghian and his research team at the Centre for Gallium Arsenide VLSI Technology for their assistance and guidance during this research.

I wish to thank the University of Adelaide and the Centre for Gallium Arsenide VLSI Technology, for providing me with the necessary VLSI design tools in the Gallium Arsenide technology.

My thanks also goes to the Commonwealth Government of Australia and the Victoria University of Technology for providing me with the scholarship to pursue this research.

Finally, I owe a debt of gratitude to my wife, Dr. Mohini Singh, and sons Deepak and Amrish, for their encouragement, patience and understanding during my course of study.

Chapter One

Thesis Overview

He that will not apply new remedies must expect new evils:
for time is the greatest innovator.

Francis Bacon.

1.0 Introduction

The enormous progress in integrated circuit (IC) technology in recent years has been changing many things in our daily lives because digital systems can be manufactured with much lower costs, lower power consumption, higher speed and smaller size. This is true in the domestic scene, professional disciplines, the workplace and the leisure activities. There is no doubt these revolutionary changes have taken place in a relatively short time and it is certain that even more dramatic advances will be made within the next decade, since the limit of miniaturisation of the transistors is not yet reached.

Up to 1950s, electronic active device technology was dominated by the vacuum tube. Although the measure of miniaturisation and circuit integration did take place, the technology did not lend itself to miniaturisation as we have come to accept it today [63, 74].

The invention of the transistor by Schokley, Brattain, and Bradeen of Bell Telephone Laboratories was followed by the development of the IC (also known as chip) [63 - 64]. The very first IC appeared around 1960, and since that time there already have been four generations of ICs, namely SSI (small scale integration), MSI (medium scale integration), LSI (large scale integration) and VLSI (very large scale integration). The emergence of the fifth generation, ULSI (ultra large scale integration) has been made possible by improvements in the fabrication technology and further miniaturisation of the devices. The ULSI is characterised by complexities in excess of three million devices on a single chip.

The revolutionary nature of this development is indicated by way in which the number of transistors integrated in circuits on a single chip has grown. This is highlighted in Figure 1.1 by Moore's first law. Table 1.1 illustrates the evolution of microelectronics over the last four decades [74].

The evolution of integrated circuit technology went through several phases starting with bipolar in the 1950s and 60s to n-type metal oxide semiconductor (NMOS) in the 70s until the 1980s when complementary MOS (CMOS) became the mainstream technology. The demand for superior performance, which has motivated the relentless search and development of new technologies, was behind the emergence of bipolar

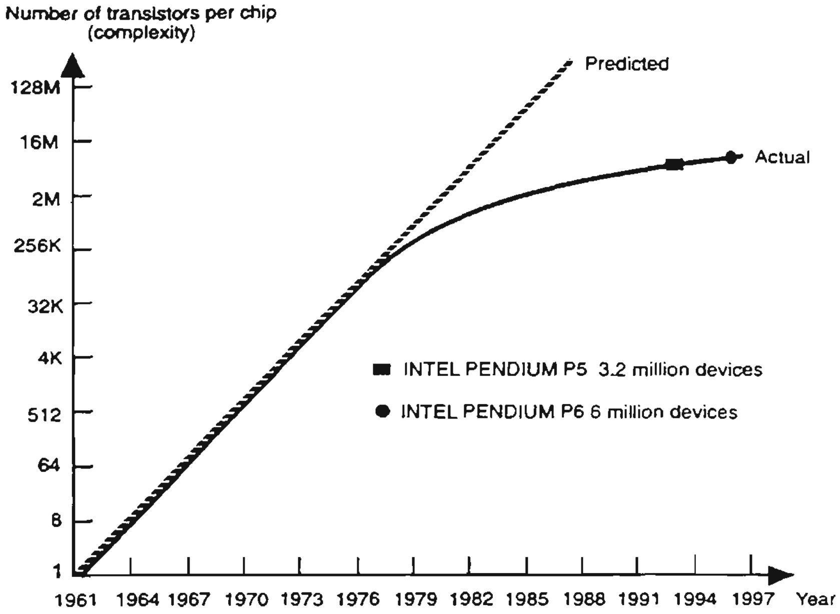


Figure 1.1 Transistor complexity on a single chip (Moore's law) [74].

Table 1.1 Microelectronics evolution

Year	1950	1961	1966	1971	1980	1990
Technology	Discrete components	SSI	MSI	LSI	VLSI	ULSI
Approx. number of transistors per chip	1	10	100 - 1000	1000 - 20,000	20000 - 1000000	100000+
Typical Products	Transistors and diodes	Gates	Adders	ROM RAM	Processors	Special Processors

CMOS (BiCMOS) and gallium arsenide (GaAs) technologies. The BiCMOS technology merged the old rivals, namely, CMOS and bipolar, to complement each other so that the strengths of one covers the weakness of the other. GaAs technology, on the other hand, possesses inherent superiority in electron mobility, saturation velocity, high temperature operation and radiation hardness. In research and development environment, GaAs digital integrated circuits have already out performed silicon circuits in power and delay performance [52 - 54].

1.1 VLSI Circuit Applications

The computerised acquisition of analog quantities is becoming very important in today's automated world. Computer based data acquisition systems are capable of scanning several analog inputs in a particular sequence to monitor critical quantities and acquire data for on line use and future recall. As speed is continuously increasing in electronic systems, especially in analog-to-digital converters (ADCs), data acquisition is becoming a real issue. With information processing technology becoming digital to the greatest possible extent, ADCs and digital-to-analog converters (DACs) are the core of the data acquisition system, operating as a peripheral to a data processing computer. Although much work has been performed in the design and implementation of silicon data converters [27 - 30], many system applications in the area of instrument and signal processing require much higher performance levels. The development of a multi-channel data acquisition chip, based on flash ADC, is aimed at addressing these applications with very high performance requirements.

Modern power systems are required to generate and supply high quality electric energy to the consumers. A growing demand for accurate, selective and reliable overcurrent relays has increased recently due to an increase in the complexity and capacity of power systems. Advancements in digital technology associated with power industry has had strong impact on the development of power system protection equipment and techniques.

Computer based digital relaying techniques have been well established in many aspects of power system protection. The availability of cheap and powerful microprocessors in recent years has led to their increasing use in power systems protection. Several types of microprocessors have been used to implement different type and level of relaying techniques. Initially the protection relays were based on 8-bit microprocessors, then 16-bit microprocessors and more recently 32-bit microprocessor has been used to provide multi-function multi-protection scheme [47]. Although these schemes provide a high level of reliability and security, they require large amounts of hardware. Since the relay functions are usually software controlled, the protection schemes are slow, and the reliability is highly dependent on the software performance, which makes it difficult to implement multi-channel multi-function multi-protection schemes.

Recent developments in microelectronic technology, in particular the GaAs digital technology, has led to the application of VLSI GaAs integrated circuits in high speed, low power relaying techniques for power system protection schemes. The development of a multi-function multi-protection relay is aimed at improving the performance, functionality and reliability of the present protection schemes.

1.2 Aims of this Research

Silicon MOS technology has been the main medium for ICs for industrial applications for many years and will continue to fill this role in the foreseeable future. However silicon logic has a number of limitations that are already becoming apparent in state-of-art fast IC design. While there has been a number of advancements in the material and fabrication processes, speed and power dissipation continue to be the major hurdle for VLSI design engineers. VLSI circuits with an excess of one million devices pose significant problems in relation to power dissipation, switching speed and gate delays. Presently the power dissipation is in the region of 20 microWatts per gate with gate speeds of a few nanoseconds. In order to facilitate the implementation of VLSI circuits that will be required for future industrial applications, a new design approach needs to be pursued that will reduce the gate power dissipation and at the same time improve the switching speeds and gate delays.

Within the scope of this research program a bottom up design philosophy is envisaged. It is anticipated that the result of this research will influence the architecture of the future ICs.

The overall aim of this research is to develop a multi-channel data acquisition chip for instrumentation and measurement applications and a multi-function multi-protection relay chip for power systems protection. The specific aims to achieve a successful implementation of the above ICs are:

(i) To investigate and choose an appropriate VLSI design technology for the implementation of high speed and low power ICs.

(ii) To analyse the available design techniques in the selected technology and access its suitability for the implementation of ICs.

(iii) Based on the above assessment, to develop design techniques using appropriate design methodology.

(iv) To analyse the performance of the above design techniques.

(v) To design, implement and evaluate the performance of a multi-channel data acquisition chip for instrumentation and measurement application.

(vi) To design, implement and evaluate the performance of a multi-function multi-protection relay for power systems protection.

1.3 Research Methodology and Techniques

The VLSI circuit normally has to meet the design requirements concerning the performance of the circuit, namely speed, power dissipation and size of the chip. The optimum design of the integrated circuit is the one that meets the speed requirements while dissipating the minimum possible power, without exceeding the power dissipation requirements and occupies the minimum possible area. Speed, power and area are all interdependent parameters, and therefore, trade off must be made to meet design requirements.

Logic design techniques have to be developed that will need to alleviate the power dissipation, switching speed, noise margin and loading effects encounted by the present day logic families. The techniques also will enable the mix of analog and digital circuits to be integrated on the same chip. In developing such design techniques a number of methodological questions in need of clarification are addressed. Specific investigation procedures are developed to answer each of the following:

(i) What is the best technology to use to alleviate the power dissipation problem and at the same time give good noise margins and fan out capabilities?

(ii) What is the best technology to use to obtain faster switching speed?

Having arrived at suitable answers to these questions the new circuit design techniques and the ICs are developed. This research is addressed as follows:

(i) Analysis of the present integrated circuit design techniques and the development of design techniques in both static and dynamic logic classes. Relative performance studies are carried out by way of case studies in static and dynamic circuit design.

(ii) Realisation of a four-bit multi-channel data acquisition chip using a mix of analog and digital circuit design techniques.

(iii) Realisation of an eight-bit multi-function multi-protection relay chip for power systems protection.

Several important issues are considered when designing very fast low power ICs. Interconnection of devices is a crucial issue because gate delays may be comparable to delays of the interconnections. Although on-chip speed is very high, this performance advantage can be lost at the system level by the interchip connections, which are significantly slower. Therefore, a different design approach to on-chip architecture is required for the very fast VLSI circuits. Exploitation of on-chip gate speed will be optimum when the functionality of the chip is increased for a given system application. This results in the implementation of the intended system function with as few chips as possible. Furthermore, optimum utilisation of the advantages offered by the technology requires a holistic approach to system design. The architectural design of the system is considered as a whole, including algorithm, architectures, device performance and interfacing with other technologies.

The primary objective in the design of the ICs is the optimum exploitation of the performance offered by a given technology. This is achieved only when the layout guarantees minimisation of parasitic capacitances. Full custom design approach has been used for all the design layout with the entire operation implemented on a single chip rather than on multiple chips. This allows the designer to maximise on the advantages of a given technology and reduce parasitic capacitances due to chip interconnections.

In developing the design techniques and the ICs extensive design, layout, simulation and analysis have been carried out using Integrated Silicon Design VLSI suite and HSPICE tools[1].

1.4 Originality of the Thesis

The contributions of this thesis are summarised as follows:

(i) Development of a static VLSI circuit design technique using GaAs technology. This approach is referred to as the Merged logic design technique.

(ii) Development of a dynamic VLSI circuit design technique using GaAs technology. This design approach is referred to as Multiple-output domino technique.

[1] Integrated Silicon Design VLSI suite is a state of the art custom integrated circuit design tool set catering for efficient design in a wide range of technologies. HSPICE is the Meta-Software's industrial grade circuit analysis tool for the simulation of electrical circuits.

(iii) Graded scaling of E-GaAs MESFET dynamic chain and comparative performance analysis.

(iv) Design, implementation and performance analysis of a ultra fast four-bit multi-channel data acquisition chip using GaAs technology. Analog-to-digital conversion is based on a technique that reduces circuit complexity.

(v) Integration of analog and digital GaAs devices on the same chip.

(vi) Design, implementation and performance analysis of an ultra fast eight-bit multi-function multi-protection relay chip for power systems protection using GaAs technology.

The merged logic approach to circuit design combines direct coupled MESFET logic (DCFL) with source follower DCFL (SDCFL) and source follower MESFET logic (SFFL) to exploit the advantages of each logic class and to achieve circuit performance which is superior to that obtained from the different individual design approaches. The merged logic static design approach, predominantly uses DCFL to achieve higher packing density and to improve circuit performance, SDCFL technique to provide drive for large capacitive loads and to realise the And-Or-Invert functions, and SFFL technique to implement large fan out.

This approach involves identifying critical parts of the circuit where SDCFL and SFFL techniques can be used to improve circuit performance. The performance of merged logic design approach is illustrated with the design and implementation of a power series evaluator chip. From the performance analysis it can be seen that this design approach demonstrates excellent performance including low power dissipation, large logic swings resulting in excellent noise margins and large fan in and fan out capabilities

The principle behind multiple-output domino technique is the utilisation of the sub-functions available in the logic tree of the domino gates. Multiple outputs are available by adding precharge devices at the corresponding intermediate nodes in the logic tree. Since nodes internal to the logic tree are being precharged for functional purposes, multiple-output domino logic is considerably less susceptive to charge sharing than domino logic. The saving in the area is mainly due to a reduction of replication of sub-circuits in the realisation of a logic functions. The actual advantage of this design technique over domino logic design technique is directly dependent upon the number of recurrence in a logic function being realised.

The improvement of performance is due to reduction of load capacitance for a given logic stage. This results from less overall device count and less parasitic wiring capacitance as a consequence of a smaller overall layout. This also leads to lower power consumption. The performance of multiple-output domino circuit is further improved by graded scaling of the domino chain.

The performance advantage of this design technique over dynamic domino technique has been demonstrated via the implementation of a four-bit Carry Lookahead Generator for a Carry Lookahead Adder. The most remarkable achievement using this technique is the reduction in the number of devices required to implement the carry generating circuit which leads to reduction in power dissipation.

The high speed, low power, four-bit multi-channel data acquisition chip was designed and implemented using mixed circuit design techniques. Source coupled MESFET logic (SCFL) technique was chosen for the design of mixed GaAs analog and digital circuits on the same chip, mainly because of its wide tolerance to threshold voltage range and its immunity to temperature variations. It also has an excellent fan out capability, a small input capacitance and a small discharging time permitting high speed operations. Digital components were designed using E-D GaAs merged logic design technique.

The four-bit multi-channel data acquisition chip is based on very fast flash analog-to-digital converter with multiplexed inputs. The analog-to-digital converter is based on an algorithm that requires only $2^{(n-1)}$ comparators instead of $(2^n - 1)$ comparators for a n-bit conversion. This approach, thus reduces the complexity of multi-bit flash analog-to-digital converter design. The design of the proposed analog-to-digital converter is module oriented, which enables multi-bit high resolution flash analog-to-digital converter to be developed by cascading a number of n-bit flash modules.

An eight-bit multi-function multi-protection digital relay was designed using E-D GaAs merged logic design technique. The single chip relay was implemented using an eight-bit comparator, programmable timer and a controller. Performance studies indicated very high speed operation of the relay with low power dissipation and respectable noise margin.

1.5 Organisation of the Thesis

This thesis contains ten chapters. Chapter 1 provides the aims of this research, the research methodology and the author's contribution to the field of study.

VLSI technology and literature review are presented in Chapter 2 of the thesis. Comparative studies of CMOS, BiCMOS and GaAs technologies indicate that GaAs technology mostly fulfils the high speed and low power requirements for the new generation of integrated circuits and systems. Literature review highlights that very limited research has been carried out in the implementation of a mix of analog and digital circuit on the same chip using GaAs technology. There are no reported literatures on the implementation of data acquisition circuit and multi-function multi-protection relay using E-D GaAs VLSI technology.

Having decided on the technology to be used for the implementation of integrated circuits for this research, the modelling and performance estimation of the GaAs MESFET are discussed in Chapter 3. In depth study of current voltage characteristic in the sub-threshold, linear and saturation regions, together with switching behaviour of GaAs MESFET are presented.

Chapter 4 is devoted to GaAs MESFET circuit design techniques using both static and dynamic design approaches. Comparative performance studies are made among different static and dynamic design approaches and this is highlighted through the GaAs VLSI implantation of SSI and MSI circuits.

GaAs integrated circuit design methodology and layout style are discussed in Chapter 5. Various design methodologies are presented and layout style adopted that allows the designer to layout the skeleton of the circuit rapidly, paying particular attention to signals, power and ground busses between adjacent circuitry.

Development of design techniques using E-D GaAs MESFETs are presented in Chapter 6. Two techniques are discussed, first using static design approach and the second using dynamic design approach. The static circuit design technique capitalises on the advantages of the static techniques presented in Chapter 4, and circuit performance is achieved that is superior to that obtained from different design approaches. The performance advantage is highlighted through the implementation of a power series evaluator chip. The dynamic circuit design technique utilises the sub-functions available in the logic tree, thus saving duplication of circuitry. The most remarkable achievement of the new design technique is the reduction in the number of devices required to implement integrated circuits with high recurrence in the logic function. The performance advantage of this technique over other well established dynamic techniques is highlighted through the implementation of a Carry Lookahead Generator for a Carry Lookahead Adder.

Data conversion techniques and principles of overcurrent relays for power systems protection are presented in Chapter 7.

Design, implementation and performance analysis of a four-bit multi-channel data acquisition chip is presented in Chapter 8. Appropriate design techniques have been chosen for the design of the mixed analog-digital GaAs chip. The methodology used for the design of the flash ADC greatly reduces the circuit complexity. The chip was implemented using 397 devices. The performance studies indicate a very high speed low power operation indicating the appropriateness of the design technology and techniques used for mixed analog-digital circuit design.

Chapter 9 is devoted to the design, implementation and performance studies of an eight-bit multi-function multi-protection relay for power systems protection. This design highlights the application and appropriateness of very fast GaAs VLSI technology in the design of dedicated chips.

The research conclusions and recommendations for future work are discussed in Chapter 10.

Chapter Two

VLSI Technology and Literature Review

Good things come in small packages.

Proverb.

2.0 Chapter Overview

In this chapter the following topics are discussed:

(i) comparison of silicon and GaAs based technologies,

(ii) review of GaAs circuit design techniques,

(iii) review of multi-channel data acquisition system, and

(iv) review of multi-function multi-protection relay systems for power protection.

In practical application environment, not only a small propagation delay and a fast access time is required, but also a low power dissipation is a important technological target.

2.1 Introduction

Since the invention of the transistor in 1947, and the development of the very first IC at the beginning of 1960 [63, 64], there have been four generations of ICs. The fifth generation of ICs, which are characterised by transistor complexities in excess of five and a half million devices on a single chip are emerging. Over the past several years, silicon CMOS technology has become a dominant fabrication process for relatively high performance and low cost effective VLSI circuits. Numerous silicon based technologies employing advanced process are emerging [48 - 51, 64], and have significantly improved the performance of silicon devices. The demand for superior performance, which has motivated the relentless search and development of new technologies, was behind the emergence of GaAs technology.

GaAs devices have higher electron mobility, saturation velocity, high temperature operation, and radiation hardness. In research and development environment, GaAs digital ICs have already out performed silicon circuits [52 - 54]. In addition to offering outstanding performance, the gate complexity of GaAs digital IC is increasing. However, compared with the matured silicon technologies, GaAs devices have some difficulties in their substrate material, and device structure.

2.2 Metal Oxide Semiconductor and Bipolar Technologies

Complementary metal oxide semiconductor (CMOS) and bipolar technologies have their weak and strong points. CMOS has emerged as the most appropriate choice for VLSI applications because of its low DC power dissipation and its high packing density. Yet, its speed is limited by the capacitive loading. On the other hand, bipolar digital circuits outperform CMOS in terms of speed, but consumes more power. Thus there is a performance gap between CMOS and bipolar technologies. The existence of this gap implies that neither CMOS nor bipolar technologies have the flexibility required to cover the full delay-power spectrum. The objective of the synergy of bipolar and CMOS technologies is to exploit the advantages of both at the circuit and system levels.

A variety of digital BiCMOS circuit structures have been developed [55 - 58, 65 -66]. The advantages of this circuits are, low DC power consumption, superior driving capability of on and off chip loads, and lower delay sensitivity to loading, which is important especially for semi-custom design.

BiCMOS has been exploited at the system level as well. It has been used for fast emitter coupled logic static memories, microprocessors, etc. [59 - 62]. The availability of CMOS and bipolar devices on the same chip can also be used for mixing slow/low power and fast/high power logic families, thus flexibility of optimising the overall system performance.

2.3 BiCMOS Technology

A known deficiency of MOS technology lies in the limited load driving capabilities of MOS transistors. This is due to limited current sourcing and current sinking abilities associated with both p- and n-transistors, and although it is possible to design super buffers using MOS transistors, such arrangements do not always compare well with the capabilities of bipolar transistors. Bipolar transistors always provide higher gain and have generally better noise and high frequency characteristics than MOS transistors and it may be seen that using BiCMOS gates may be an effective way of speeding up VLSI circuits. To take advantage of the BiCMOS process the whole functional entity, not just the logic gates, must be considered. The BiCMOS technology goes some way towards combining the virtues of the two technologies. Although the idea of merging bipolar and CMOS on the same chip originated twenty years ago [69], it was not feasible from the practical point of view because of the lack of adequate process technology. With the technological progress achieved in recent years, this idea has been revived. There are many techniques to merge bipolar and CMOS devices as reported in the literature [55-62] and [70 - 72]. There are two ways of classifying the BiCMOS process. One way is to classify according to the baseline process. A CMOS based BiCMOS process is a CMOS baseline process to which bipolar transistors are added. Similarly, a bipolar based BiCMOS process is a bipolar baseline process to which CMOS transistors are added. In both cases the added device would have to be compromised, which means that its characteristics can not be optimised. Alternatively, BiCMOS process can be classified according to their cost and performance. In this regard three categories can be identified, namely, low cost, medium performance, and high performance (high speed).

In low cost BiCMOS process, a bipolar transistor is added to a CMOS process with one additional process step. The process complexity is comparable to that of CMOS. However, there are many trade offs in designing the emitter, base, and collector of the NPN transistor. If the CMOS process is optimised, some of the bipolar device parameters will be degraded. For example, due to the absence of the buried layer and the deep n^+ collector in the NPN transistor, the collector resistance is high. This causes the cut-off frequency to be low, poor current drive, and high collector-emitter saturation voltage.

A medium performance BiCMOS process can be realised by adding a NPN transistor to a twin-tub CMOS process. The process uses three extra masks to form the bipolar transistor. The first mask is needed for n^+ buried layer, the second for n^+ deep collector and the third for the base implantation. This BiCMOS process is optimised to be used for high performance circuits. The collector resistance is low in comparison to the low cost process. For a 0.8 micron process the cut-off frequency can be as high as 5 GHz.

A high performance BiCMOS process is achieved by using a doped polysilicon emitter instead of n^+ implant for emitter. Four additional mask levels are required to form a high performance BiCMOS device. The bipolar transistors realised in the high performance BiCMOS process have low collector resistance (because of the buried layer and deep sink), high current gain (because of polysilicon emitter), and low parasitic capacitances (because of self-alignment). Cut-off frequency greater than 5 GHz can be achieved with this process [66 - 68].

In a BiCMOS technology, it is important to design high performance CMOS and bipolar transistors for minimum cost. The device design complexity depends on which bipolar structure is integrated with CMOS, or more precisely, the common process steps which can be shared by the CMOS and bipolar devices. One of the important design issues for BiCMOS devices is the latchup. The parasitic PNP and NPN transistors are inherent in the CMOS component of the BiCMOS structure. However, BiCMOS structures are less susceptible to latchup for the following reasons. The presence of buried layers under the CMOS devices reduce the parasitic significantly. Moreover, the parasitic bipolar transistors have reduced current gains.

2.4 Gallium Arsenide Technology

Silicon MOS technology has been the main medium for computer and system applications for a number of years and will continue to fill this role in the foreseeable future. However, silicon logic has speed limitations that are already becoming apparent in state-of-art fast digital system design. Paralleling developments in silicon technology, some very interesting results have emerged in GaAs based technology. GaAs will not replace silicon but will be used in conjunction with silicon based technology to satisfy the need for very high speed integrated technology.

The compound GaAs was discovered in 1926, however its potential as a high speed semiconductor was not realised until 1960s [73]. The high electron mobility of GaAs with respect to silicon, a semi-insulating substrate, its opto-electronics properties, as well as significant improvement in power dissipation and radiation hardness, have promised an ultimate system performance advantage for GaAs circuits. The developments in GaAs integrated circuit fabrication technology during 1970s and 80s, made the VLSI implementation of GaAs integrated circuits a reality.

2.4.1 GaAs Energy Band Structure

One of the important characteristics of GaAs is its superior electron mobility which is due to its energy band structure as shown in Figure 2.1 [73]. GaAs is a direct band gap material with valance band maximum and the conduction band minimum coinciding in ***k*** space at the Brillouim zone centres. Valleys in the band structure that are narrow and sharply curved correspond to electrons with low effective mass, while with gentle curvature correspond to higher effective electron mass. The minimum point of GaAs conduction band is near the zero point of crystal lattice momentum as opposed to silicon, where conduction band minimum occurs at higher momentum. The electron mobility, μ depends upon the impurity concentration, N, temperature, T, and electron effective mass, m.

For GaAs the effective mass of electron is $0.067m_e$, where m_e is the free electron rest mass. This implies that electrons travel faster in GaAs than in silicon as a result of their superior electron mobility brought about by the shapes of their conduction bands. Electrons in the higher valley have high mass and strong intervalley scattering and therefore exhibit very low mobility.

Since the conduction band minimum occurs at the same wave vector as the valance band maximum, little momentum change is required for the transition of an electron from the conduction band to the valance band. Probability of photon emission with energy nearly equal to the band gap is high in GaAs. This makes it an excellent light emitting diode.

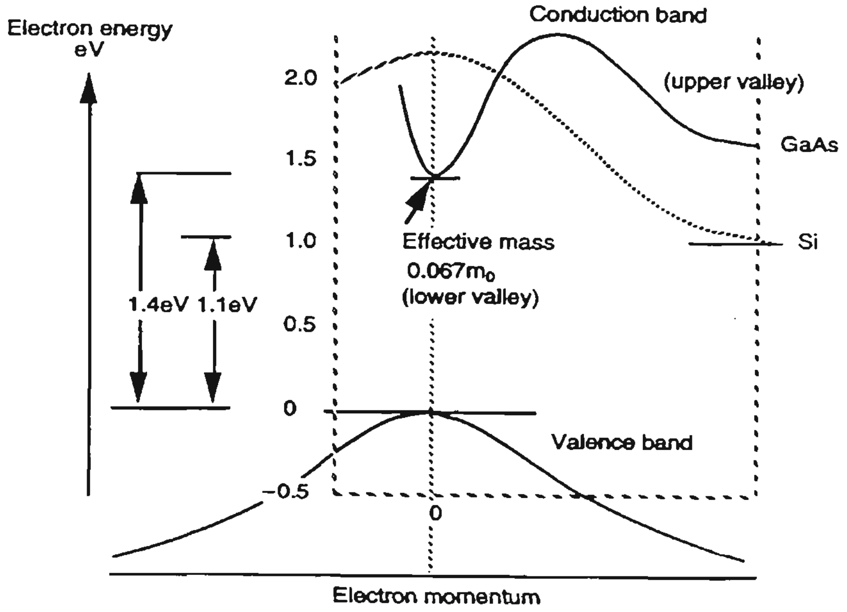


Figure 2.1 Energy band structure for GaAs and silicon.

2.4.2 Electron Velocity-Field Behaviour

As the applied field across the GaAs material is increased, the electron charge carriers gain energy from the applied field. At the same time, through collision with the lattice, the electrons also loose a small portion of this energy. So long as the resultant balance is positive, the energy and the drift velocity of the charge carriers increases with an increase in the applied electric field. At some point the energy gained from the electric field becomes equal to the energy lost as a result of collisions. This results in the drift velocity to approach a limiting value referred to as the saturation velocity.

Since GaAs is a multivalley semiconductor, when the energy of the lower valley electrons rises sufficiently, electrons become 'hot'. The region in the electron velocity field characteristics where some of the hot electrons populate the upper conduction band is characterised by the larger electron effective mass. The resultant effect is a reduction in the number of high mobility electrons and hence the drift velocity. In this region the drift velocity is no longer proportional to the electric field.

The velocity-field characteristics for GaAs and silicon are shown in Figure 2.2. From the graph it can be readily noted that in low electric field region, silicon has much lower electron mobility than GaAs. This increases monotonically until the drift velocity saturates at a value of about $1\text{x}10^7$ cm/sec.

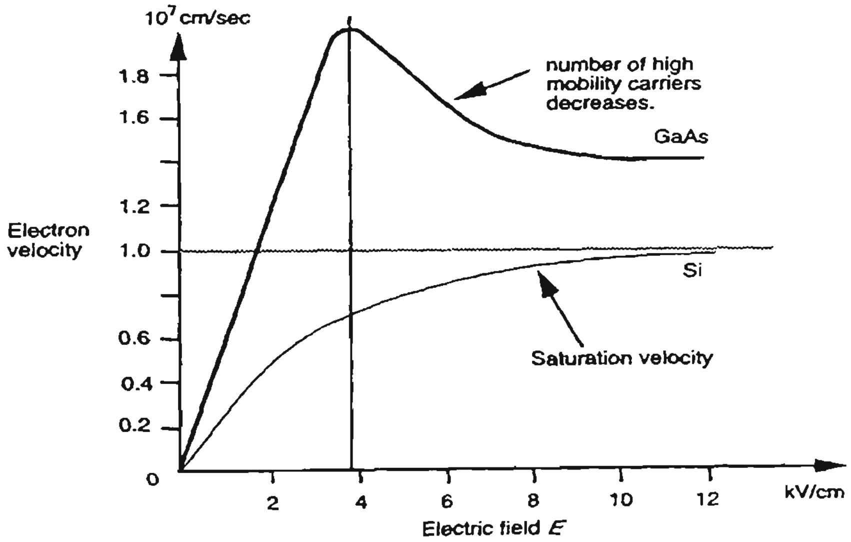


Figure 2.2 Velocity-field characteristic for GaAs and silicon [74].

2.4.3 GaAs Technology Development

Although the GaAs technology is confronted with similar technological problems as was silicon during 1970s, during the last few years considerable progress have been made in the GaAs integrated circuitry and the technology has progressed to the point where a number of foundries now provide GaAs fabrication facilities. The current foundry offerings have the following characteristics [74]:

(i) 0.8 micron gate geometry,

(ii) less than two micron metal pitch,

(iii) up to four layer metal,

(iv) four inch diameter wafer,

(v) suitability of clock rate in the range 1 - 5 GHz, and

(vi) both 'on' and 'off' devices.

GaAs technology is attractive for ultra high speed digital systems. This is mainly due to the higher mobility of electrons. Some of the salient features of the GaAs technology include:

(i) electron mobility of six to seven times that of silicon, resulting in very fast electron transit times,

(ii) saturated drift velocity of GaAs and silicon are approximately equal, but the GaAs saturation velocity occurs at a much lower threshold field than the silicon,

(iii) large energy bandgap offers bulk semi-insulating substrate with resistivities in the order of 10^7 to 10^8 ohm-cm. This minimises parasitic capacitances and allows easy electrical isolation of multiple devices on a single substrate,

(iv) radiation resistance is stronger due to absence of gate oxide to trap charges,

(v) a wider temperature range is possible due to larger bandgap. GaAs devices are tolerant to wide temperature variations over the range -200°C to +200°C,

(vi) up to 70% reduction in power dissipation can be obtained over the fastest of the silicon technology,

(vii) direct bandgap of GaAs allows efficient radiative recombination of electrons and holes. This means forward biased **pn** junctions can be used as light emitters. Thus the technology allows efficient integration of photonics with electronics.

The detailed comparison between GaAs and silicon technologies is presented in Table 2.1 [74 - 75].

Table 2.1 Comparison between silicon and gallium arsenide technologies

Properties	**Silicon**	**Gallium Arsenide**	**Units**
Mobility			
Electrons	1300	8000	$cm^2/V.sec$
Holes	500	400	$cm^2/V.sec$
Intrinsic resistivity	$2.2 * 10^5$	$1 * 10^8$	Ω-cm
Density	2.33	5.32	gm/cm^3
Effective electron mass	$0.97m_e$	$0.067m_e$	
Energy bandgap	1.12	1.43	eV
Thermal conductivity	1.5	0.46	W/cm^oK
Schottky barrier height	0.4 - 0.6	0.7 - 0.8	V
Dielectric constant	11.9	13.1	

2.4.4 GaAs Fabrication

Several GaAs process techniques have been developed, their differentiation depends on the technology various manufacturers utilise and on the trade offs they make in terms of circuit performance, level of integration, and process yield. Two basic requirements for any GaAs fabrication process are [78]:

(i) that the bulk resistivity be significantly high, even after the ion implantation anneal, to ensure acceptable low leakage current between circuit elements, and

(ii) the residual impurities be low enough to ensure uniform and repeatable implanted layer sheet resistance and acceptably low backgating.

The detailed GaAs E- and D-MESFET fabrication using planar and self-aligned gate processes are presented in Appendix A.

2.4.5 GaAs Devices

The speed advantage of GaAs over silicon must be translated into fast and useful devices and circuits. Devices need to be designed that will not only utilise the high velocity of the electrons to produce a high current density but will also provide a means to control the current so that such devices can act as switches and/or amplifiers. The GaAs devices used in the implementation of ICs are:

(i) depletion-mode metal semiconductor field effect transistor, D-MESFET,

(ii) enhancement-mode metal semiconductor field effect transistor, E-MESFET,

(iii) high electron mobility transistor, HEMT, and

(iv) hetrojunction bipolar transistor, HBT.

Two major GaAs devices, namely, the planer ion implanted D-MESFET and E-MESFET are widely used for IC applications with better fabrication yield and reliability than other devices.

2.4.5.1 Metal Semiconductor Field Effect Transistor (MESFET)

MESFETs are presently the predominantly used device for the design of GaAs ICs. This is mainly due to the simplicity of the Schottky barrier gate, which allows device fabrication to close geometrical tolerances. The structure of a basic GaAs MESFET is shown in Figure 2.3. It consists of a thin n-type active region joining two ohmic contacts with a narrow metal Schottky barrier gate that separates the more heavily doped drain and source.

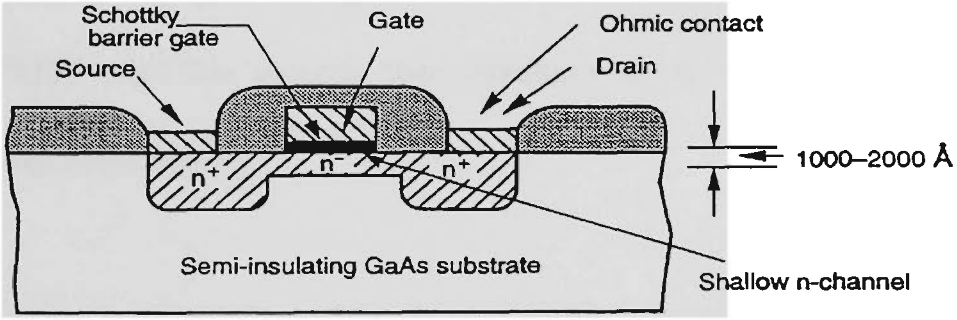


Figure 2.3 A GaAs MESFET structure [74].

GaAs MESFETs are similar to silicon MOSFETs. The major difference is the presence of Schottky diode at the gate region. The D-MESFET is normally a 'on' device and its threshold voltage V_{th} is negative. The threshold voltage is determined by the channel thickness, and the concentration density of the implanted impurity. A highly doped, thick channel exhibits a large negative threshold voltage. By reducing the channel thickness and the concentration density a normally 'off' E-MESFET with positive threshold voltage is formed.

A MESFET has a maximum gate-to-source voltage of 0.7 to 0.8 Volts owing to the diode action of the Schottky gate diode.

2.4.5.2 High Electron Mobility Transistors (HEMT)

The HEMT is a second generation of GaAs device that offers improved performance over a E-MESFET, particularly at low temperature. The concept behind this device is to place donor atoms in an AlGaAs layer adjacent to an undoped GaAs layer. The most widely used form of this device consists of a thick layer of GaAs covered with a thin layer of AlGaAs. The higher bandgap of the donor layer makes the HEMT similar to silicon MOSFET, and this physical correspondence allows a HEMT to be analysed using standard MOS theory.

The principle performance advantage of the HEMT over a MESFET is because the electron mobility in the channel of a HEMT is higher than in a MESFET. This is because there are no doping ions in the channel to scatter carriers. Some of the problems associated with this GaAs device to realise potential in the commercial market include light sensitivity, threshold voltage shift with temperature, and instability in the drain current characteristics which manifest in a hysteresis loop of I_{ds} curves as shown in Figure 2.4 [76]. Additional problems exist with the high channel resistance, voltage uniformity and control, and the thickness of the active layer, which is sensitive to process steps associated with heat and plasma kinetics. These issues together with still maturing fabrication technology, make this device unsuitable for commercial integrated circuit.

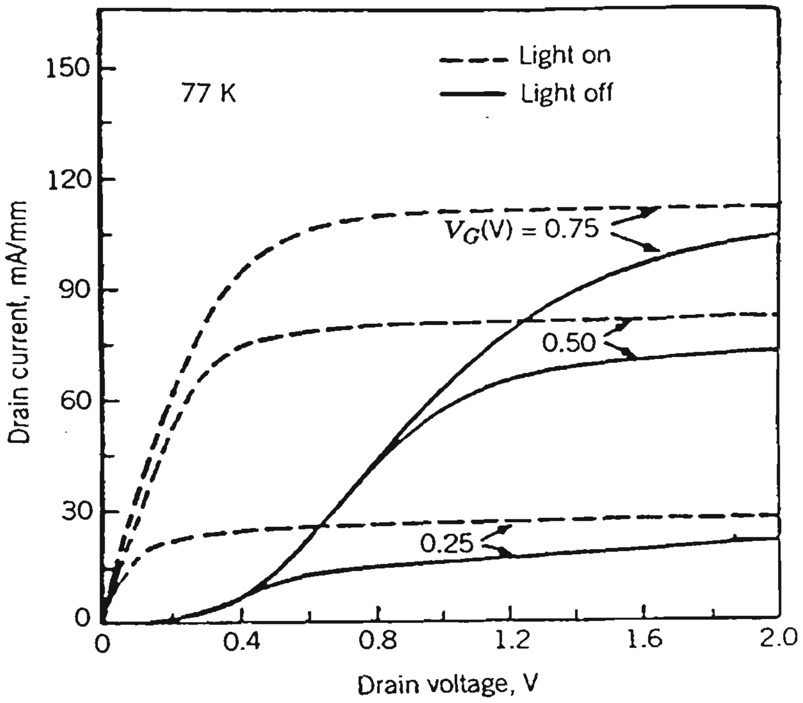


Figure 2.4 Drain current characteristics of a HEMT.

2.4.5.3 Hetrojunction Bipolar Transistor (HBT)

The main feature of the HBT relies upon a wide bandgap emitter, wherein part of the energy bandgap difference between the emitter and base, is used to control the flow and distribution of electrons and holes. The wide bandgap emitter allows the base to be more heavily doped than the emitter, leading to a low base resistance and emitter-base capacitance while maintaining a high emitter injection efficiency. Another advantage of

HBT technology is determination of the threshold voltage strictly by the inherent bandgap of the AlGaAs and GaAs, which varies very little compared to controlling the channel doping and layer thickness of MESFET structures.

Majority of research and development in HBT technology has been concentrated on the material and fabrication requirements. Molecular beam epitaxy (MBE) has been used in the development of HBT technology. A wide range of improvements in MBE material, device structures, and fabrication technologies must be achieved to make HBT technology a practical reality in VLSI circuits.

Performance of a HBT devices ultimately is projected to be in the 100 to 200 GHz range with gate delays in the range of 10 picosec. High current drive capability of this device coupled with their threshold voltage insensitivities make HBTs a prime candidate device for ultra high speed performance integrated circuits [77]. A wide range of improvements are needed in materials and fabrication processes before HBT technology can be used for commercial applications.

2.5 Technology Comparison

In view of rapid developments in GaAs and silicon technologies, Table 2.2 draws a comparison among GaAs, CMOS and bipolar technologies. Progress in terms of speed/power projections for GaAs and commonly used silicon technologies are accessed with reference to Figure 2.5 [74].

Table 2.2 Comparison between CMOS, bipolar and GaAs technologies

CMOS	**Bipolar**	**GaAs**
Low power dissipation	High power dissipation	Medium power dissipation
High input impedance	Low input impedance	High input impedance
High noise margin	Medium noise margin	Low noise margin
Medium speed - high voltage swing	High speed - low voltage swing	Very high speed - low voltage swing
High packing density	Low packing density	High packing density
Low output drive	High output drive	Low output drive
Bidirectional	Unidirectional	Bidirectional
Indirect bandgap	Indirect bandgap	direct bandgap - good light emitter
Ideal switching device	Non ideal switching device	Reasonable switching device
$g_m \alpha V_{in}$	$g_m \alpha e^{Vin}$	$g_m \alpha V_{in}$
Medium f_t	High f_t at low current	Very high f_t
Fabrication masks 12 to 16	Fabrication masks 12 to 20	Fabrication masks 6 to 10

where g_m is the transconductance, V_{in} is the input voltage and f_t is the cut-off frequency.

Technology comparison shows that circuit designed using CMOS technology has low power dissipation per gate but the propagation delay per gate is high. This is due to the large capacitances and resistances associated with circuits designed using this technology. BiCMOS technology offers improved propagation delay but suffers from high power dissipation per gate. The high power dissipation is mainly due to bipolar transistors used at the output using this technology. Circuit designed using GaAs

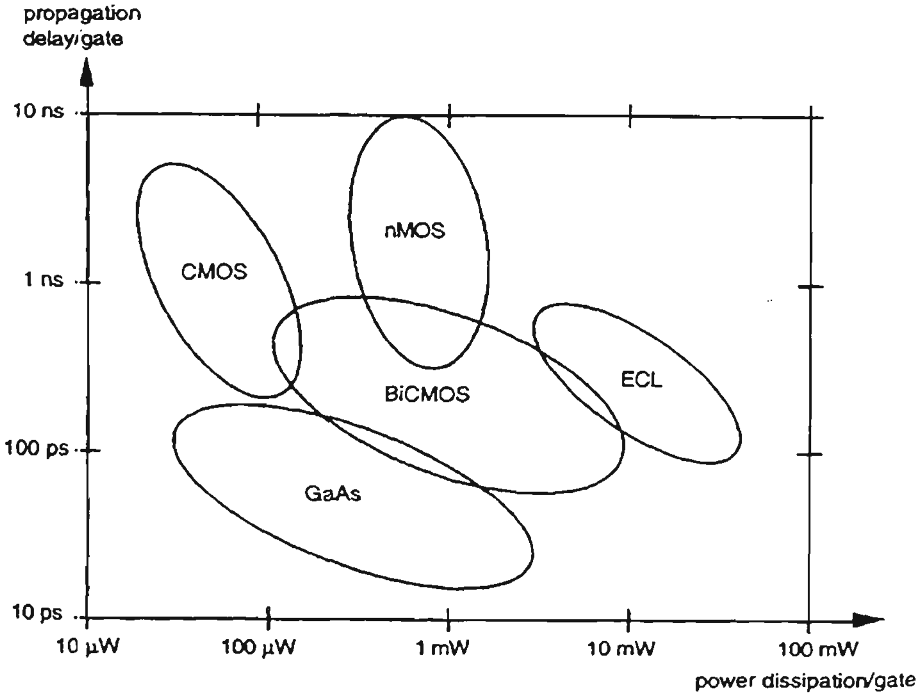


Figure 2.5 Power - speed performance of GaAs and silicon technologies.

technology has lowers propagation delay and power dissipation ranging from approximately 30 microWatts to 2 milliWatts. Recent research interests in GaAs technology is seeing new design techniques being developed with much improved circuit performance when compared with CMOS technology.

2.6 Literature Review

Education is a progressive discovery of our own ignorance.

Will Durant.

The review of the GaAs circuit design techniques, multi-channel data acquisition circuit and multi-function multi-protection relay systems are presented in the following section.

2.6.1 GaAs Design Techniques

Design and development of digital integrated circuits using GaAs MESFETs dates back to early 1980's. In 1982 *Suyama, et al.,* [1] presented a comprehensive paper on GaAs integrated circuit design. A GaAs four-bit arithmetic and logic unit was designed using buffered D-MESFET logic with gate lengths of two microns. The circuit was implemented with 854 devices (MESFETs and diodes) with delay time of 2.1 nanosec and dissipated 1.2 Watts. The chip required two power supplies of +5 Volts and -3 Volts.

Soon after *Demin, et al.,* [2] reported a GaAs configurable cell array using buffered logic. The cells were designed using D-MESFETs and allowed multiple implementation of multiple logic functions within each cell. The power dissipation per cell was 2.8 milliWatts and required dual power supply.

Rocchi and Gabillard [3] presented a GaAs digital dynamic IC's for applications up to 10 GHz. Flip flops were designed using transmitting gates with BFL logic and fabricated using self aligned planar process. Two phase dynamic approach applied to SSI circuits allowed the reduction of chip size per gate without loss of speed and with reduced power dissipation. Though the circuits showed high operating speed, they required two power supplies.

Hirayama, et al., [4] developed a GaAs four-bit static memory (SRAM) using direct coupled MESFET logic. The circuit was fabricated using 1.0 micron SAINT FET process. The minimum address access time reported was 2.8 nanosec with power dissipation of 1.2 Watts. The difficulty in fabricating E-MESFETs with precise threshold voltage posed difficulties in designing GaAs integrated circuits using both D- and E-MESFETs.

In 1986, *Osafune, et al.,* [5] reported the design and fabrication of an ultra high frequency divider using buffered MESFET logic. With improved SAINT fabrication process, much lower power dissipation was achieved. The circuit was implemented with 0.5 micron D-MESFETs using dual power supplies.

With improvements in GaAs technology fabrication process, especially E-MESFETs, the emergence of GaAs digital integrated circuits using DCFL technique was noticed. *Singh, et al.,* [6] presented a comprehensive papers on GaAs low power integrated circuits for high speed digital signal processor. The circuit was designed using low power GaAs E-D direct coupled MESFET logic. The DSP consisted of a four-bit arithmetic and logic unit, 4x4-bit multiplier and 8x8-bit multiplier/accumulator. The subsystem consisted of seven packaged integrated circuits which were interconnected on PCB. The individual integrated circuits showed marked improvements in speed and power dissipation. The overall performance of the system was degraded due to interconnection capacitances.

Katsu, et al., [7, 8], *Idda, et al.,* [9] and *Vu, et al.,* [10] reported GaAs integrated circuits designed using source coupled MESFET logic. The circuits demonstrated a wide range of tolerance to threshold voltage and a partial immunity to temperature variations. Number of designs using this technique were reported by *Ohta, et al.,* [11] and *Shimizu, et al.,* [12] - all highlighting the advantages of this technique in respect to its tolerance to threshold voltage variation and immunity to temperature variations.

Vu, et al., [13, 14] reported the design of gate array using Schottky diode MESFET logic (SDFL). Propagation delays of 1.6 nanosec and power dissipation of 108 microwatts per gate were obtained using SDFL logic. Number of circuit design were reported by *Shur,* [15] and *Srivastava, et al.,* [16]. Srivastava presented a review of designing ultra fast VLSI circuits from silicon point of view.

During 1990's, the some emphasis was placed on GaAs VLSI circuit design using DCFL technique, mainly due to the refinement of the E-D MESFET fabrication process. *Higashisaka, et al.,* [17] reported a 2.5 Gbps 16-bit multiplexer - demultiplexer using GaAs DCFL design technique. To avoid the speed degradation caused by using DCFL, various techniques such as 8x2 data conversion processes, selector merged shift register and clock overlapping were used. Although the circuit operated at very high speed, the power dissipation was considerable. *Singh, et al.,* [18, 19] also reported integrated circuit design using GaAs DCFL technique.

Implementation of dynamic circuits using GaAs MESFETs have not been as well developed as its static counterpart due to the leakage of the Schottky gate of the

MESFET and the often critical timing requirements of the clock. The dynamic frequency divider which was reported by *Rocchi, et al.,* [3] used only the concept of the pass transistor in combination with GaAs MESFET buffered logic. The charge storage, which is the main feature of the dynamic circuit, was not fully utilised in this approach. *Pasternak, et al.,* [20] utilised this approach and developed the differential pass transistor logic technique. Charge control devices (CCDs) have been implemented using GaAs MESFETs devices and show very fast operation as reported by *Hoe, et al.,* [21]. However, the circuit applications available to the CCD are limited, and the need for three or four phase clocks increase the complexity and power dissipation.

Yang, et al., [22] and *Nary, et al.,* [23] and reported a high speed dynamic domino circuit. The circuits were implemented using GaAs D-MESFETs only. Level shifting diodes and coupling capacitor were used due to negative threshold voltage of the D-MESFET. The circuit required two voltage level single phase clock signals. The design was based on the technique developed by *Krambeck, et al.,* [24] using CMOS technology.

Lassen, et al., [25] and *Nary, et al.,* [26] presented two phase dynamic MESFET logic gate which dissipated very low power. The circuit operated from two nonoverlapping clocks and a single power supply. This technique is self latching, lending itself to highly efficient pipelined architectures. Although this technique was demonstrated to be compatible with the static design techniques making its introduction into high speed systems very straightforward, it had very poor drive capability and required two clock signals which could lead to problems in VLSI design.

2.6.2 Data Converters

Data converters are one of the most widely used linear integrated circuits. With digital information processing technology, analog-to-digital converters (ADCs) are the core of a data acquisition system, operating as a input peripheral to a data processing computer. Although much work has been performed in the design and implementation of silicon data converters, and many commercially available monolithic data conversion circuits exist, many system applications in the areas of instrumentation and signal processing require performance level even higher than what is available today in silicon. GaAs data conversion circuits are aimed at addressing these applications with very high performance requirements. The review of data acquisition circuit and ADCs are presented in this section.

Real-time signal and data processing systems operating at gigabit rates are primarily limited by ADC performance. A six-bit, 1-GHz, full Nyquist, hybrid data acquisition system was reported by *Corcoran, et al.*, [27] using an interleaved silicon ADC driven by GaAs sample and hold (S/H) circuits. 1-GHz GaAs ADC building blocks was reported by *Thomas, et al.*, [28] using low cost D-MESFET technology. A four-bit, 1-GHz full Nyquist single chip ADC including S/H circuits was realised. The chip offered 0.8 LSB integral linearity and was demonstrated to as high as 500 Ms/s in the full Nyquist condition. A 4-bit and 5-bit flash ADCs implemented in GaAs technology were reported by *Ducourand, et al.*, [29, 30]. The 4-bit chip dissipated 150 milliwatts of power and operated up to 3 GHz and the 5-bit chip operated up to 2.2 Gs/s. A number of other 4-bit flash ADC chips were implemented by *Naber, et al.,* [31] and *Kleks, et al.,* [32] using GaAs technology operating in GHz range.

A 5-bit flash ADC with excellent accuracy was developed by *Hagelauer, et al.,* [33] using one micron E-D MESFET process. The chip employed S/H circuit in front of the converter to improve the performance at higher frequencies. It was reported that dynamic characterisation was performed up to 1 Gs/s and an accuracy of 4.4 effective bits with full Nyquist input was achieved at this frequency. The performance was attributed to S/H circuit and the use of differential SCFL in the converter.

Different ADC algorithms were investigated by *Sauerer, et al.,* [34] to find an architecture suited for high speed high resolution converters based on MESFET technology. System architecture and key components for an 8-bit 1-GHz GaAs MESFET ADC were developed, fabricated and characterised.

Doernberg, et al., [35] reported the design of flash ADC using two step flash conversion and pipelining technique for the design of a 10-bit CMOS flash ADC with sampling speed of up to 5 Ms/s. *Kerth, et al.,* [36] reported using the same technique in the design of a 667 nanosec, 12-bit flash ADC. Though the comparator count is reduced using this design approach, the scheme generally requires DACs, amplifiers and other additional circuitry.

Investigations and measurements of the dynamic performance of high speed ADCs reported by *Hagelaur, et al.,* [37]. The accuracy of ultra high speed ADCs decreases at higher input frequencies, mainly due to timing mismatches, which cause the comparators to sample different time points of the input signal. This was highlighted by on-chip E-beam measurements on a 4-bit flash ADC.

Recently *Balasubramanian,* [38] reported an architecture for flash ADC with reduced circuit complexity. The design of this ADC was modular oriented, ie. a k-bit ADC was developed by cascading a number of n-bit flash modules. Using this approach, high resolution flash ADC could easily be implemented with low resolution modules.

2.6.3 Power Systems Protection

Power system occasionally experiences faults and abnormal operating conditions. Protective relays are used to avoid damage to the equipment of the utilities and consumers. In the early developments of power systems, protection functions were performed by electro-mechanical relays and many such relays are still used in power systems protection. Solid state relays were introduced in 1950s and the last thirty years has seen the development of digital relaying techniques. Some of the advantages of digital relaying techniques highlighted by *Sachdev,* [39] are:

(i) The equipment design based on digital technology generally use fewer parts.

(ii) The digital devices are not required to be tuned individually to obtain consistent results.

(iii) The characteristics of digital devices do not drift with temperature, supply voltage changes or aging.

(iv) The resolution of the solutions provided by digital systems depend on the number of bits per word.

(v) Most design changes can be made by changing the software only.

Properly designed microprocessor based relays and systems are being increasingly accepted for general use in the power industry. The review of digital relaying techniques are presented in this section.

Protective relay developed for power system protection by *Kramer and Elmore* [40] describes the availability of a microprocessor based inverse time overcurrent relay having selectable characteristic which greatly relieves the application difficulties that have been associated with fixed characteristic electromechanical counterpart. *Sidhu, et al.,* [41] reported design, implementation and testing of a microprocessor based relay for detecting transformer winding faults by using sixteen-bit microprocessor.

In recent years, various researchers have applied the concept of multi-function to protective relay. *Manzoul,* [42] described the implementation of several independent overcurrent relays using a single 8085 microprocessor. The implementation was based on the concept of multi-tasking and time sharing in microprocessors. Each relay was implemented by a combination of a lookup table and a counter. The software development and hardware testing were carried out using HP-64000 UX Microprocessor Development Kit.

Harlow, [43] applied a multi-function protective relay to a cogeneration industry. His concept was to incorporate as many of the required protection function as was feasible into one package. The complete package was versatile, compact and user friendly. *Gillany, et al.,* [44] developed a new digital relaying technique for parallel transmission lines using a single relay at each end.

Yalla, [45] described the development of digital multi-function relay for the protection of the intertie between a customer owned generator and a utility system. The relay used digital signal processing techniques to measure the relay parameters, thereby eliminating analog hardware. The hardware design was based on the use of dual microprocessor architecture to achieve flexibility and high speed operation. *Balasubramanian, et al.,* [46] proposed a microprocessor controlled general purpose multi-function relay switching system. The was designed to switch independently multiple electronic devices at desired times and duration with day and night intensities control.

More recently, a 32-bit relaying technique for power system protection has been reported by *Zayegh, et al.,* [47], where Motorola MC68020 microprocessor was used to provide multi-function multi-protection scheme with high speed, accuracy and reliability.

2.7 Conclusions

For very high speed operation in a semiconductor medium, three factors become significant, namely, carrier mobility, carrier saturation velocity, and existence of semi-insulating substrate. GaAs technology mostly fulfils the requirements, and together with low power dissipation, provides a technology base for a new generation of integrated circuits and systems.

GaAs technology has been confronted with similar technological problems as was silicon technology in 1970s. This has been the main reason for limited research in GaAs VLSI circuit design as compared with silicon based technology. During the last few years considerable progress has been made in the GaAs material and fabrication process which has led to research interests in GaAs VLSI circuit design.

The fastest ADC available in practice is the flash ADC involving a conversion time equal to the propagation delays of the comparator and the encoding logic. However, the complexity of the circuit increases rapidly with the increase in the number of bits. An increase in one bit in the digital output nearly doubles the circuit complexity. For instance, when an eight-bit ADC needs 255 comparators for its realisation, a nine-bit ADC requires 511 comparators for its implementation. This increase in the complexity of the hardware discourages its feasibility of implementation for more number of bits. Flash converters using GaAs technology are limited to about four to five-bits due to this problem. There has been no reports on a single chip multi-bit multi-channel data acquisition circuit using E-D GaAs MESFET technology.

Literature survey shows that digital and microprocessor technologies have been used for over fifteen years in the design and implementation of the protection equipment with very good results. Initially the protection relays were based on 8-bit microprocessors, then 16-bit microprocessors were used which gave increased flexibility, with high level of reliability, security and repeatability and recently 32-bit microprocessor has been used to provide multi-function multi-protection scheme with required speed, accuracy and reliability.

There has been no reported material related to the VLSI implementation of the digital protection scheme for power systems protection. Recent developments in the microelectronic technology, in particular GaAs digital technology, has motivated the application of GaAs VLSI integrated circuits in the implementation relaying techniques for power systems protection schemes. High speed and low power dissipation features of GaAs devices will enable the design and implementation of a single chip of multi-channel multi-function digital relay with respectable performance.

Chapter Three

Device Modelling and Performance Estimation

3.0 Chapter Overview

This chapter reviews a number of currently available GaAs MESFET models and presents a criterion for accurate modelling.

3.1 Introduction

When designing circuit to meet its given performance and specifications, VLSI design engineers should have a thorough understanding of its behaviour, particularly of the component devices, and a sound methodology. The prime consideration in this chapter is to describe a model for the MESFET which will not only preserve the essential features of the device, but also assists the VLSI systems designer with performance estimations and optimisation processes.

The discussed analytical models for self-aligned gate, GaAs MESFET predict the static current-voltage characteristics in the sub-threshold, linear and saturation regions of operation. The model equations are explicit, closed form analytical expressions in terms of terminal voltages. Throughout, the model derivations, uniform doping is assumed for all regions.

3.2 GaAs MESFET Model

An idealised MESFET (metal-semiconductor field effect transistor) structure is shown in Figure 3.1. An active layer of n-type GaAs is grown on top of a semi-insulating GaAs structure. The drain and source electrodes make contact with the active layer through the n+ region under each. The third electrode, which is the gate, is placed directly on the active layer.

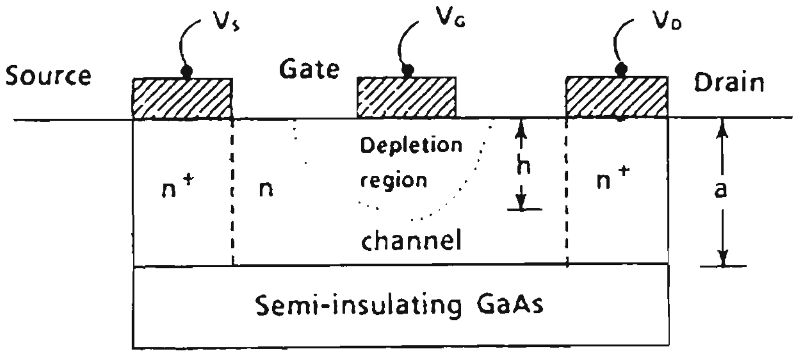


Figure 3.1 An idealised GaAs MESFET structure.

From the consideration of the energy band diagram at the metal-semiconductor interface, a depletion region under the gate whose height is controlled by the transverse electric field created by an applied gate voltage. The undepleted region is called the channel. When a positive gate voltage is applied to the drain with respect to the source, a longitudinal electric field is created that accelerates electrons in the channel from the source towards the drain. The resulting current in the channel, called the drain current, will depend on the gate voltage and drain to source voltage.

GaAs MESFET is a channel-area modulated device, that is, it depends upon the capacitance of the Schottky barrier to control the effective charge in the channel. Three distinct regions of operation, model the drain current in GaAs MESFET devices, namely:

(i) sub-threshold or cut-off region where the gate to source voltage is less than the device threshold voltage, with a closed channel from source to drain;

(ii) linear region where the gate to source voltage is greater than the device threshold voltage and the drain to source voltage is less than the drain saturation voltage with a open channel from source to drain;

(iii) saturation region, where the gate to source voltage is greater than the device threshold voltage and the drain to source voltage is greater than the drain saturation voltage, closed channel at the drain end and an opened channel at the source end.

A simplified analytical model has been formulated by *Shur* [79]. He used Shockley's equations and the assumptions that current saturation occurred due to the formation of a stationary Gunn domain at the drain side of the gate when the average electric field under the gate equalled the domain sustaining field. The MESFET equivalent circuit is similar to the circuit to be described here, however, electron transit time effects under the gate have been omitted. The most complete analytical model was presented by *Van Tuyl* and *Liechti* [80]. *Pucel et al,* [81] presented a small signal model and showed how to derive the element values. *Krumm et al.,* [82] used a similar model but included electron transit-time effects as a time delay factor associated with the drain current source. Figure 3.2 illustrates the GaAs MESFET model used in this work. It consists primarily of a voltage-controlled current source, three interelectrode capacitors, drain to source resistance, and diodes between the gate and source and between the gate and drain. Resistors R_g, R_s, and R_d represent resistance of gate, source and drain contact regions. This is referred to as the Curtice model [83].

3.2.1 On Region Drain Current Derivation

To appreciate some of the features that characterise the drain current I_{ds}, without losing the objective of simplicity which is so critical for VLSI system designer, a simple model will firstly be used to highlight the first order effects in I_{ds}, and then attention will be focussed on the more complex Curtice model.

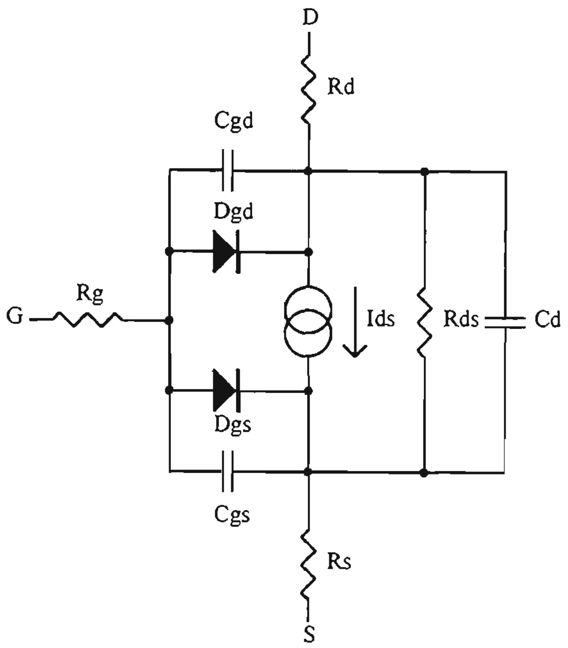


Figure 3.2 Circuit model for GaAs MESFET.

Consider a typical GaAs MESFET structure as shown in Figure 3.1, where the majority carriers flow from source to drain. The equation of the drain current, I_{ds}, which results from this movement, is:

$$I_{ds} = \frac{\mu.\varepsilon.W}{2.a.L}(V_{gs} - V_t)^2 \qquad \textbf{(3.0)}$$

and can be rewritten as:

$$I_{ds} = \beta.[V_{gs} - V_t]^2 \qquad \textbf{(3.1)}$$

where $$\beta = \frac{\mu.\varepsilon.W}{2.a.L} \qquad \textbf{(3.2)}$$

V_{gs} is the gate to source voltage

V_t is the device threshold voltage

W, L and a are the width, length and the area of the MESFET

μ is the electron mobility, and

ε is the permittivity of the material between gate and the channel.

β is a transconductance parameter used in the HSPICE MESFET model specification, denoted by Kp. It consists of process dependent factor [$\mu\varepsilon/2a$] and the geometry dependent term [W/L], which depends on the actual layout of the transistor. Sometimes the process determines the channel length of the transistor, which means the designer can control the gain factor through varying the channel width only.

Equation 3.0 describes the behaviour of the GaAs MESFET in the saturation region only. Equation 3.3 describes the linear region of the current model.

$$I_{ds} = \beta[2(V_{gs} - V_t)V_{ds} - V_{ds}{}^2] \qquad \textbf{(3.3)}$$

where V_{ds} is the drain to source voltage.

Special note should be made here that in the GaAs MESFET the saturation of drain current, I_{ds}, with an increasing drain to source voltage, V_{ds}, is due to carrier velocity saturation, whereas in silicon the saturation is due to channel pinch-off.

The model described by equation 3.3 unfortunately does not provide for the smooth transition between the saturation and the linear regions of MESFET operation. The modified model describing the behaviour of a GaAs MESFET in linear and saturation regions, referred to as the Curtice "square law" model, gives the equation:

$$I_{ds} = \beta(V_{gs} - V_t)^2.(1+\lambda.V_{ds}).\tanh(\alpha.V_{ds}) \tag{3.4}$$

where λ is the output conductance parameter, and

α is the hyperbolic tangent drain voltage multiplier.

While the proposed "square law" model has generally proved accurate, some MESFETs show a deviation from "square law" behaviour. The deviation has been attributed to velocity saturation and to mobility and saturation velocity reduction due to thermal heating effects at high current levels [84]. In order to simplify the characterisation process and still accurately model the MESFET characteristics, a modified version of *Sakurai et al.,* [85] is used. This model accurately simulates both "square law" and "velocity saturated" MESFETs. In MESFET power law model, the drain current is given by:

$$I_{ds} = \beta(V_{gs} - V_t)^n.(1+\lambda.V_{ds}).\tanh(\frac{V_{ds}}{V_{ss}}) \tag{3.5}$$

where n is the power exponent, and

V_{ss} is a constant to fit the knee region of operation.

The hyperbolic tangent function is used to model the drain current continuously from the linear to saturation region. Generally devices with small pinch-off voltages (less than 1.0 volts) may be described by an *n* value of 2.0.

The model described above does not include short-channel effects, namely, threshold voltage shift, field dependence of mobility, high field velocity saturation and channel length modulation. In the linear and saturation regions the modified drain currents, I_{dsn}, due to short-channel effects, are described, respectively, by the following expressions [86]:

$$I_{dsn} = \frac{I_{ds}}{(1+\frac{V_{ds}}{E_c.L})} \qquad \textbf{(3.6)}$$

and

$$I_{dsn} = \frac{I_{ds}}{(1-\frac{\Delta L}{L}).[1+\frac{\min(V_{dsv})}{E_c(L-\Delta L)}]} \qquad \textbf{(3.7)}$$

where E_c is the electric field at which the drift velocity saturates,

V_{dsv} is the saturation voltage due to velocity saturation, and

ΔL is the distance from the drain end to the point of velocity saturation.

In the derivation of the drain current, it was assumed that the gate voltage is sufficiently low so that the thermionic emission current across the Schottky junction is negligible. In digital circuits the gate voltage takes on extreme values, from a low value near the threshold voltage to a value comparable to the supply voltage. When the gate is driven to a large positive voltage, gate current will flow and degrade the circuit performance in a significant way. This is particularly troublesome for enhancement transistors. In order to counter this, special design techniques need to be developed.

3.2.2 Transconductance and Output Conductance

The two parameters, transconductance, g_m, and output conductance, g_o, are important since they are directly related to the gain of the MESFET. The transconductance describes the relationship between the drain current, I_{ds}, and the input control voltage, V_{gs}, and measures the gain of the MESFET, while the output conductance determines the slope of the output characteristics [74].

3.2.2.1 Transconductance Parameter, g_m

Equations 3.8 and 3.9 define the transconductance parameter, g_m, for linear and saturation regions:

$$g_m = \frac{\Delta I_{ds}}{\Delta V_{gs}} | V_{ds} = \text{ constant} \qquad \textbf{(3.8)}$$

Differentiating equation 3.5, for n = 2 gives g_m as:

$$g_m = 2\beta(V_{gs} - V_t).(1 + \lambda.V_{ds}).\tanh(\frac{V_{ds}}{V_{ss}}) \qquad \textbf{(3.9)}$$

The major difference to note between GaAs and Si devices is the transconductance. For GaAs MESFET, the transconductance is high with a very low gate capacitance. Figure 3.3 [74] shows typical transconductance for several types of devices, both GaAs and silicon, primarily for comparison purposes. From equation 3.9 it can be seen that for GaAs MESFETs the transconductance is both process-dependent and size-dependent.

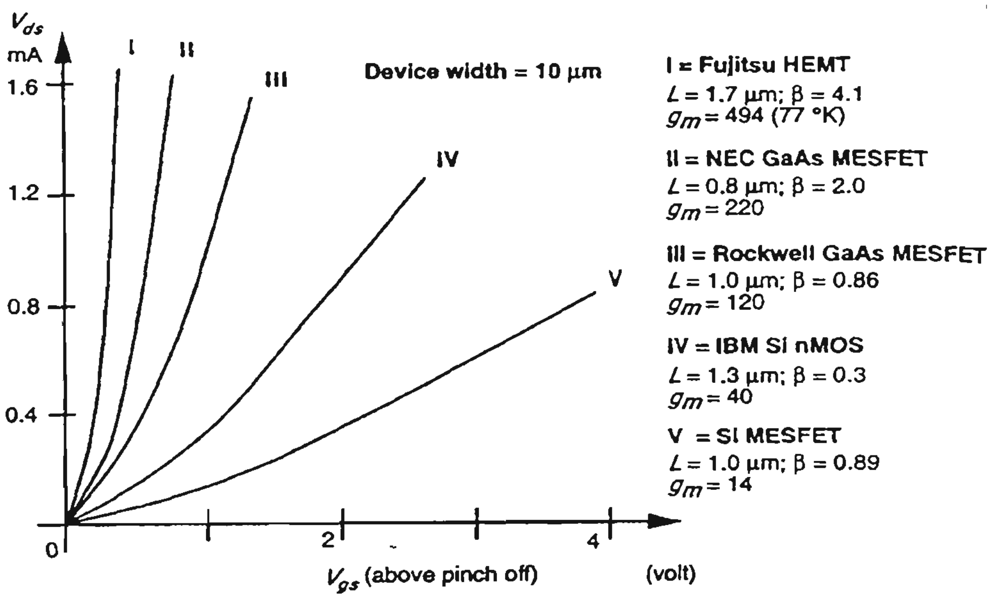


Figure 3.3 Transconductance variation for several devices.

3.2.2.2 Output Conductance, g_o

The output conductance, g_o, can be determined by differentiating equation 3.5 with respect to drain voltage, V_{ds}, and for n = 2, g_o is expressed as:

$$g_o = \lambda.\beta(V_{gs} - V_t)^2.\tanh(\frac{V_{ds}}{V_{ss}}) + (\frac{\beta}{V_{ss}}).(V_{gs} - V_t)^2.(1 - \lambda.V_{ds}).\sec h^2(\frac{V_{ds}}{V_{ss}}) \qquad (3.10)$$

3.2.3 Logic Voltage Swing

The switching speed of MESFET devices can be improved by, (i) increase in logic voltage swing, and (ii) a reduction in gate length. Although the former option is possible, it increases the switching energy, resulting in an increase in power dissipation. The dynamic power dissipation, P_g, can be expressed in terms of the logic voltage swing, ΔV_o as [74]:

$$P_g = \frac{C_L(\Delta V_o)^2 f}{2} \qquad \textbf{(3.11)}$$

where P_g is the dynamic dissipation,

C_L is the load capacitance,

ΔV_o is the logic voltage swing, and

f is the switching frequency.

To exhibit small dynamic switching energy, devices must develop their transconductance at control voltages with only a small logic swing above the threshold voltage. To establish the logic voltage swing, ΔV_o, two conditions must be satisfied:

(i) the low logic voltage level V_{low} must satisfy the relationship $\mathbf{V_{low} < V_t}$, which ensures the device turn off,

(ii) the gate should not be driven higher than the barrier potential, ϕ_B.

The logic high level, V_{high}, should therefore satisfy the relationship: $\mathbf{V_{high}} < \phi_B$. Thus, the logic voltage swing can be expressed as:

$$\Delta V_o = V_{high} - V_{low}$$
$$= \phi_B - V_t \qquad \textbf{(3.12)}$$

which is the channel pinch-off voltage.

3.2.4 Device Parameters

In order to appreciate the interrelation between the parameters which must be optimised, or alternatively controlled, when fabricating MESFETs, it is important to consider other device parameters, besides I_{ds} and V_t, which ultimately characterise the performance of MESFETs. These parameters include:

(i) gate-to-source capacitance, C_{gs},

(ii) gate-to-drain capacitance, C_{gd}, and

(iii) drain-to-source capacitance, C_{ds}.

The depletion region beneath the gate produces the gate capacitances between the gate and the source, C_{gs}, and between gate and the drain, C_{gd}. Making the following assumptions

(i) for V_{gs} negative and small V_{ds}, then $C_{gs} \cong C_{gd}$ since each diode is reversed biased by approximately the same amount, and

(ii) for increasing V_{ds}, then the depletion layer at the drain end is greater, so $C_{gd} < C_{gs}$.

These two capacitances depend on the device terminal voltage, the relationships being:

$$C_{gs} = \frac{C_{gso}}{(1 - \frac{\phi_B}{V_{gs}})^{M_{gs}}} \tag{3.13}$$

$$C_{ds} = \frac{C_{gdo}}{(1 - \frac{\phi_B}{V_{ds}})^{Mgd}} \tag{3.14}$$

where C_{gs0} and C_{gd0} are zero bias capacitances at source and drain respectively,

ϕ_B is the built-in potential, and

M_{gs} and M_{gd} are the diode ideality factors.

The drain-to-source capacitance, C_{ds}, is constant over the operating voltage range.

3.2.5 Switching Behaviour

The switching characteristics of a MESFET is limited by the time the gate takes to charge and discharge load capacitance C_L. Some of the terms used to describe the switching behaviour of a MESFET are defined as follows:

(i) rise time, t_r, is defined as the time for the waveform to rise from 10% to 90% of its steady-state value.

(ii) fall time, t_f, is defined as the time for the waveform to fall from 90% to 10% of its steady-state value.

(iii) delay time, t_d, is defined as the time difference between the input and output transitions at 50% level.

The above parameters are illustrated in Figure 3.4.

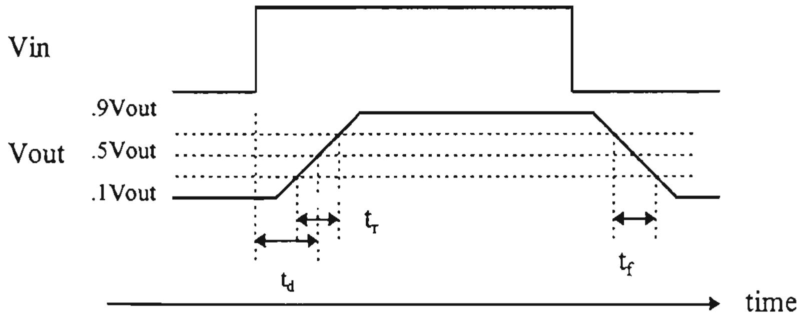


Figure 3.4 Switching characteristics of a MESFET.

A generalised expression that describes the change in rise and fall times, Δt_x, is given by:

$$\Delta t_x = C_L(\frac{\Delta V_o}{\Delta I_{ds}}) \quad \textbf{(3.15)}$$

where 'x' denotes for either the rise or the fall time and ΔV_o is the output logic swing.

3.2.6 Sub-threshold or Cut-Off Region

As the integrated circuit density increases, sub-threshold conduction, especially in normally-off MESFET devices, becomes increasingly important. While extensive attention has been given to modeling of MOSFET's in the sub-threshold region, only empirical models have been proposed for MESFET sub-threshold behaviour, [87 - 89], even though this region of operation is extremely important for calculating the performance parameters (power, noise margin, transfer characteristics) in high performance digital MESFET circuits. In low voltage MESFET digital circuits the logic swing and, consequently, the maximum drain-to-source voltage is limited to, typically, 0.7 Volts by the Schottky gate conduction. As a result, the device characteristic's in the vicinity of threshold are critical to circuit behaviour. In the sub-threshold region the drain current, I_{ds}, is described by the following expression [84]:

$$I_{ds} = \beta(\frac{k.T}{q})^2.\exp[(\frac{q}{k.T}).(V_{gs} - V_t)].[1 - \exp(\frac{-q.V_{ds}}{k.T})] \quad \textbf{(3.16)}$$

where k is the boltzmann's constant,

T is the temperature in ^{o}K, and

q is the electron charge.

The above expression for sub-threshold current is similar in form to the empirical relations for sub-threshold current in references [88] and [89]. The noticeable features of the sub-threshold region are the exponential dependence of the drain current on the gate and drain voltages and the exponential transition of the drain current into the saturation region.

The switching characteristics of low-voltage MESFET digital circuits are influenced critically by two device parameters, namely, the sub-threshold swing and the large-signal transcoductance. Sub-threshold swing, which is related inversely to the sub-threshold slope, is defined as the change in the gate bias that produces a decade of change in the drain current below threshold and should be made as small as possible in order to ensure sharp turn-off of the device. The sub-threshold swing, essentially, is inversely proportional to the rate of change of channel potential with gate bias. By examining the behaviour of the equivalent capacitive divider circuit across the gate and the substrate, it is evident that the sub-threshold swing will decrease as the gate-channel depletion capacitance is made larger and the channel-substrate depletion capacitance is reduced.

The large-signal transconductance is defined as the ratio of current in the ON state to half the logic swing. This parameter is the measure of the capacity of the logic gate to drive a capacitive load and must be made as large as possible. Calculations based on transconductance [86] indicate that for a logic swing of 0.5 Volts and the threshold voltage of 0.2 Volts, the large-signal transconductance of a MESFET with doped substrate reduces substantially as the substrate doping concentration is lowered and eventually approaches that for a MESFET with undoped substrate. Furthermore, for identical threshold voltage and logic swing values, a MESFET with highly doped substrate has a higher large-signal transconductance than one with an undoped substrate. Hence, it is clear that in very low voltage circuits, while using a MESFET with undoped substrate instead of one with doped substrate will lead to a larger circuit noise margin (smaller sub-threshold swing), the drive capacity of the gate (large-signal transconductance), will be correspondingly reduced. In a typical GaAs MESFET DCFL circuit the logic swing can be as high as 0.7 Volts and in such case the large signal transconductance will be virtually invariant with substrate doping.

3.2.7 Results and Discussion

A GaAs MESFET with gate length, L, of 0.8 micron and width, W, of 10 microns was characterised and simulated using HSPICE circuit simulation package. Table 3.1 lists the model parameters used for the simulations. Figures 3.5 and 3.6 show the simulated drain current characteristics for the device in the ON and sub-threshold regions. The results show a good fit of our model calculations with the drain characteristics of a short channel GaAs MESFET in the three regions.

Table 3.1 Power law MESFET model parameters used for simulation

Parameters	Units	D-MESFET	E-MESFET
Threshold Voltage	Volts	-0.545	0.15
Transconductance Parameter β	mA/	2.13E-04	3.628E-04
Exponent n	-	1.169	1.169
Built-in voltage, Vbi	V	0.85	0.85
Drain series resistance	Ω	1150	1500
Source series resistance	Ω	1150	1500
Output conductance parameter, λ	1/V	0.13	0.10
Threshold voltage modulation parameter, γ	-	-0.04	
Linear region fitting parameter, Vss	V	0.50	
Junction capacitance gate-drain	F	6.5E-16	7.5E-16
Junction capacitance gate-source	F	1.3E-15	1.5E-15
Alpha	1/V	2.0	2.0
Bandgap correction factor - Gap1	eV/deg	5.14E-4	5.14E-4
Bandgap correction factor - Gap2	deg	204	204
Junction saturation current	Amps	2.0E-14	2.0E-14
Gate and drain sub-threshold factors	1/V	default	1.0
Energy gap	eV	1.52	1.52

3.3 Conclusions

In this chapter an analytical model of the GaAs MESFET based on a three region current conduction has been discussed. The closed form analytical model for GaAs MESFET successfully predicted the static current-voltage characteristics in sub-

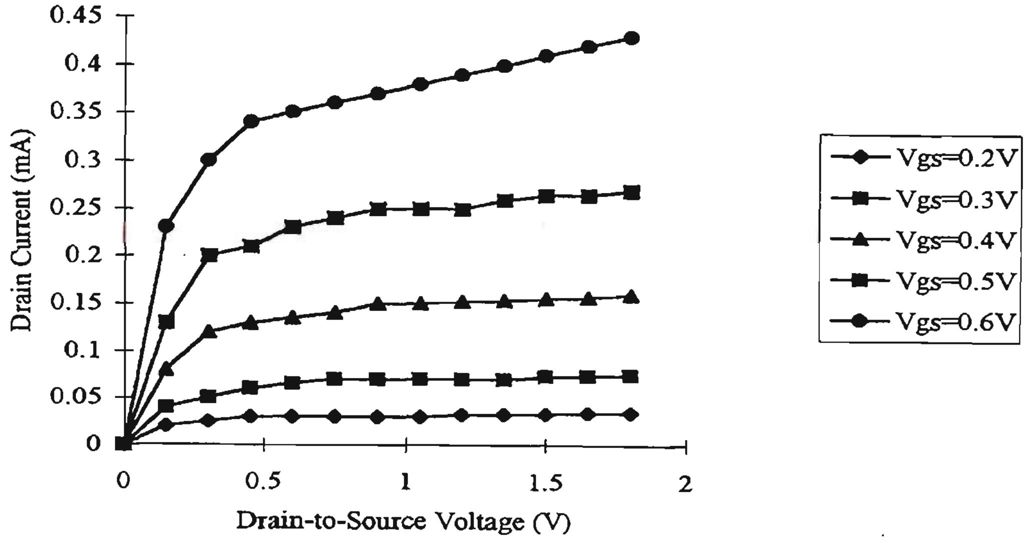


Figure 3.5 Simulated drain current characteristic for GaAs MESFET.

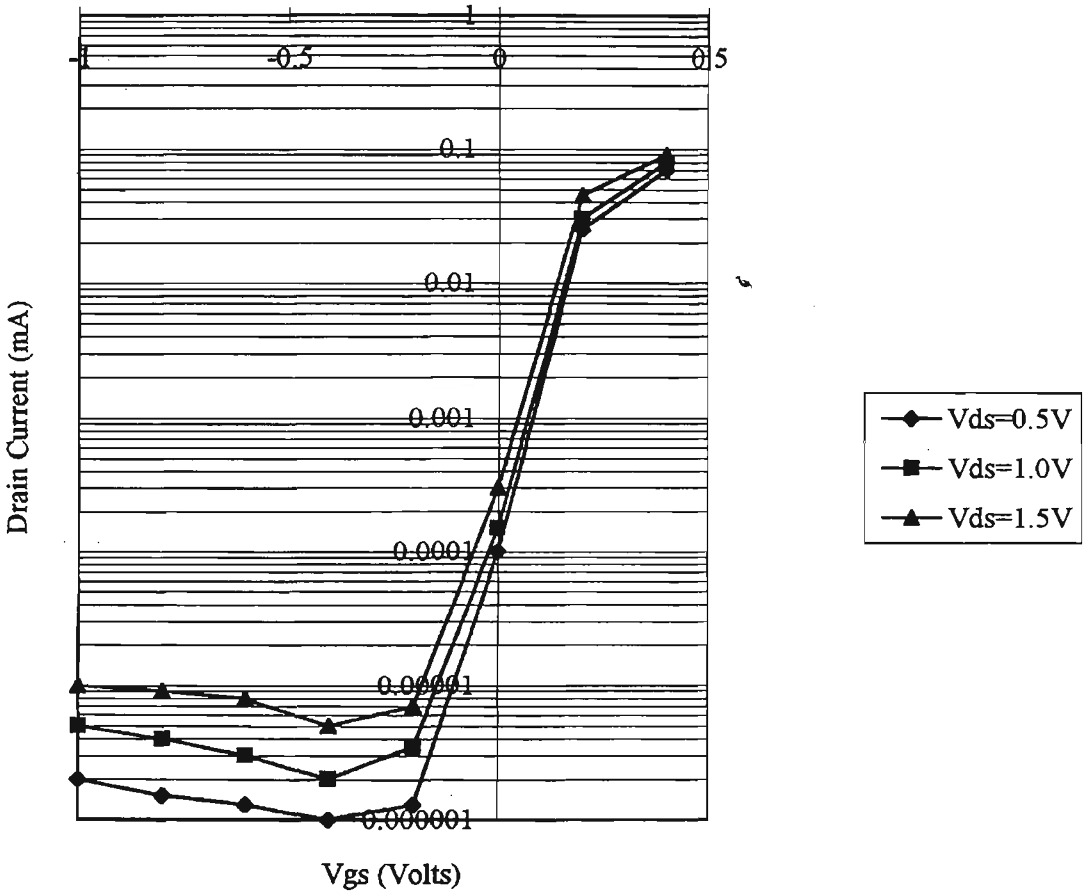


Figure 3.6 Sub-threshold current characteristics for GaAs MESFET.

threshold, linear and saturation regions of operation. Since most of the MESFET digital circuits use 0.8 micron channel length GaAs MESFETs, using the model described in this chapter will avoid large errors in the analysis of many GaAs MESFET circuits. Because of their relative simplicity, the models retained the physical basis of device operation and at the same time offered a more efficient method of simulating MESFET digital circuits.

Chapter Four

GaAs MESFET Circuit Design Techniques

4.0 Chapter Overview

The following topics are discussed in this chapter:

(i) design and performance of GaAs MESFET static design techniques,

(ii) design and performance of source-coupled E-D GaAs MESFET logic,

(iii) design and performance of E-D GaAs MESFET dynamic design techniques, and

(iv) analysis of normally-off E-D GaAs MESFET logic.

4.1 Introduction

The low field mobility and peak electron velocity in GaAs are each several times greater than their respective values in silicon. Also, in GaAs devices there is no ground plane and all capacitances between conductors and device terminals are lateral. Moreover, there is no junction capacitance between the drain or source and the substrate as in MOS devices. The lower parasitic results in significant reduction in the dynamic power dissipation when compared with silicon devices. With the availability of foundries offering an Enhancement - Depletion (E-D) Self-Aligned process, with a sub-micron feature size, GaAs VLSI digital circuits in a true sense are now available. Since there is no native insulating oxide between the transistor gate and the substrate channel, only MESFET structures are available in GaAs technology.

The current-voltage characteristics of a GaAs MESFET are similar to those of a NMOS transistor. This suggests that many of the design techniques that have been developed for NMOS digital circuits can be applied directly to the design of GaAs digital circuits. However, there are fundamental differences between a GaAs and a MOS transistors. In a GaAs device, when the gate voltage exceeds the Schottky barrier voltage, the gate becomes conducting and the gate current has detrimental effects on circuit performance. Special digital circuit design techniques have to be developed to counter this effect and this makes the GaAs logic circuits more complicated. In addition, when the MESFET gate becomes conducting, the voltage is clamped to a value equal to the Schottky barrier voltage. This limits the logic swing and places severe requirements on the noise margins of logic circuits.

4.2 GaAs Logic Gate Design

The choice of a particular GaAs MESFET device for implementing integrated circuits is dependent on the circuit performance requirements of the IC and the fabrication process of the device. Table 4.1 relates the circuit and the consequent device requirements for high speed, low power integrated circuits while Table 4.2 relates the device characteristics and the consequent physical parameters of the device for high speed low power integrated circuits [75].

The depletion mode metal semiconductor FET (D-MESFET) was the most widely used device in the 1980s for implementing GaAs ICs. Circuits employing D-MESFETs pose least fabrication problems, since Schottky barriers on GaAs ICs are easier to

Table 4.1 Circuit and device requirements for high speed low power GaAs integrated circuits

Circuit Requirements	**Consequent Device Requirements**
1. Small logic voltage swings	Very uniform threshold voltage for active devices (particularly for VLSI).
2. Low device and parasitic capacitances	Low input capacitance devices and semi-insulating substrate for low parasitics.
3. High switching speeds with reasonable fan out loadings at low switching voltages	Very high current gain bandwidth, very high power gain bandwidth, and fast increase in transconductance above threshold.

fabricate than **pn** junctions. Further, the large voltage swing associated with D-MESFET circuits relax the requirements for MESFET threshold voltage uniformity. In D-MESFET any region of the source-drain channel not under the gate are conductive. This eases the requirements for precise gate alignments and special gate-recesses and etch processes that are necessary for avoiding parasitic source and drain resistances. The relative simplicity of fabricating D-MESFET circuits result in acceptable yields for commercial production of D-MESFET GaAs integrated circuits. However, for proper logic switching of circuits designed with depletion mode active devices, voltage level shifting between D-MESFET drain and the next stage gate is necessary. The voltage shift is necessary to meet device turn-off requirements, and requires two power supplies. The two power supplies impose a severe penalty in terms of circuit area and chip interface-overhead, since most circuit logic families require only one power supply.

Table 4.2 Device characteristics desired for high speed low power switching

Desired device electrical characteristics	**Consequent physical parameters.**
1. High transconductance	High carrier mobilities. Very short channel.
2. uniform threshold voltage	Low threshold voltage sensitivity to horizontal and vertical geometry variations and doping variations.
3. Low input capacitance	Small geometries and low carrier storage effects.
4. High current and low gain bandwidth	High carrier mobilities and saturation velocities.

Enhancement mode MESFET (E-MESFET) circuits avoid the need for dual power supply and level shifting circuits, because the E-MESFETs have positive threshold voltage. However, E-MESFETs must have to small voltage swings because their gates cannot be forward biased above 0.6 to 0.8 Volts without drawing excessive gate current. Since the differences between logic 1 and 0 must be approximately twenty times the standard deviation of the threshold voltages to allow adequate noise margins in implementing ICs, E-MESFET threshold voltage must be uniform to within 25 milliVolts. Recent refinements in GaAs fabrication technology has made it possible to commercially produce reliable E-MESFET devices and analog and digital ICs [73].

4.3 GaAs Static Circuit Design Techniques

There are two main approaches to static digital logic design using GaAs technology, namely:

(i) normally-on logic, and

(ii) normally-off logic.

4.3.1 Normally-On Logic

The normally-on logic uses depletion mode MESFETs which are 'ON' devices and when used as switching elements are required to be turned 'OFF'. A number of circuit techniques have been developed to facilitate logic turn-off. The approaches in this class of logic include:

(i) buffered MESFET logic,

(ii) unbuffered MESFET logic,

(iii) Schottky diode MESFET logic, and

(iv) Capacitor-Diode MESFET logic.

Since D-MESFETs are 'ON' devices, they need negative potential at the gate to facilitate logic turn-off. This means that dual supply rails, together with level shifting networks, are necessary for proper circuit operation.

4.3.1.1 Buffered MESFET Logic

Buffered MESFET logic circuit design has been extensively employed for the design of depletion mode GaAs ICs [2]. This design technique uses depletion mode transistors together with Schottky diodes to perform the logic function. Figure 4.1 shows the circuit configuration of a Buffered MESFET logic inverter. The logic is implemented with transistors in the inverting stage, while the output is driven by a source follower with a level shifting diodes to restore the required logic levels of +0.7 Volts (high) to -

V_t (-0.5 Volts - low) or below, voltages required by the input MESFETs. The source follower has relatively low sensitivity to fan out loading and loading capacitance. Also, no DC current is required to drive subsequent gate inputs. However, since the circuit operation relies on the use of forward biased, level shifting diodes, this approach to logic design results in relatively high power consumption (typically 10 - 50 milliWatts per gate). The circuit exhibits an excellent speed performance [1 - 2], (typical gate delay is in the order of 50 picosec) as well as providing a reasonable fan out capability. The noise margin for buffered MESFET logic is determined by the Schottky turn on voltage, which is typically 0.75 Volts.

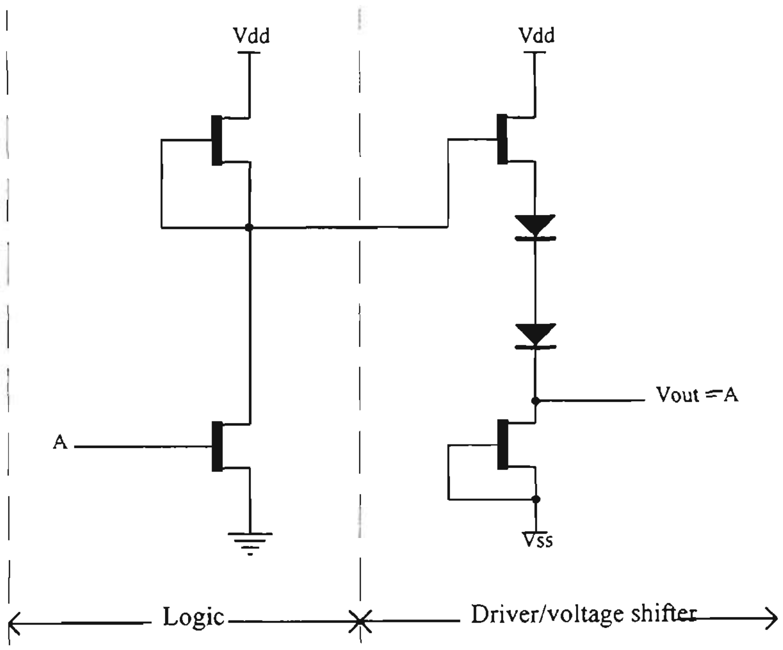


Figure 4.1 Buffered MESFET logic inverter.

Since this class of logic uses depletion mode MESFETs, it therefore needs a negative voltage supply to ensure that the depletion mode driver MESFETs can be switched off. This means there is a need for dual power supplies (+ and -) for the proper operation of circuits designed using this technique. Logic function can be realised by simply modifying the input logic circuitry. Figure 4.2 illustrates the realisation of a two input NOR gate.

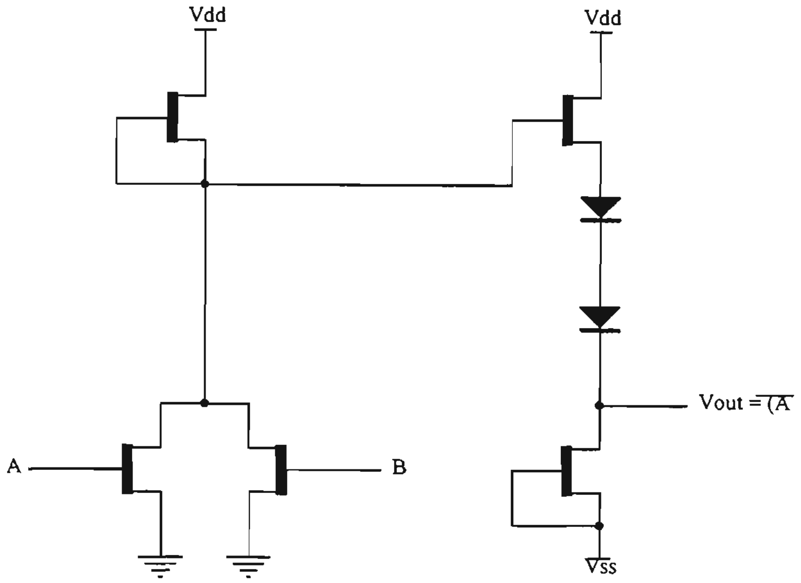


Figure 4.2 Buffered MESFET two input NOR gate.

4.3.1.2 Unbuffered MESFET Logic

The circuit structure shown in Figure 4.3 can reduce the high power consumption of the buffered MESFET logic. This circuit configuration, known as unbuffered MESFET logic, consumes less power by omitting the load driver source follower. In this case, however, the circuit is sensitive to high fan out load because there is no buffer between the switching transistor and the output node. The output node is loaded by the input impedance at connected stages and its capacitance increases linearly with the fan out as do the rise, fall and delay times. The unbuffered MESFET logic offers good noise margin but as with buffered MESFET logic requires dual power supply.

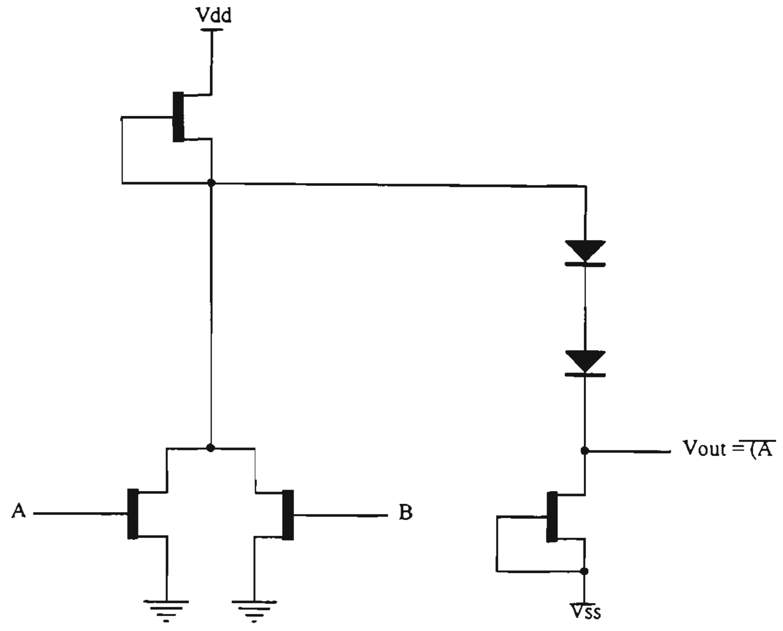


Figure 4.3 Unbuffered MESFET logic inverter.

4.3.1.3 Schottky Diode MESFET Logic (SDFL)

Another approach for minimising circuit area and power dissipation is to use Schottky diodes to perform the logic function of a logic gate and the D-MESFET to provide the load-driving capability [13]. Figure 4.4 presents the design of a basic SDFL inverter. The SDFL design offers saving in power, as the input diodes are not always forward biased, and in circuit area, since diodes, which occupy less area than MESFETs, implement the logic function. The use of smaller, low capacitance diodes for switching and input level shifting allows the construction of higher fan in, logic gates in SDFL. The logic gate delay depends on the fan out and capacitance loading, as does the noise margin. High fan in limits the noise margin due to the division of the high pull down current among many pull ups of the drivers.

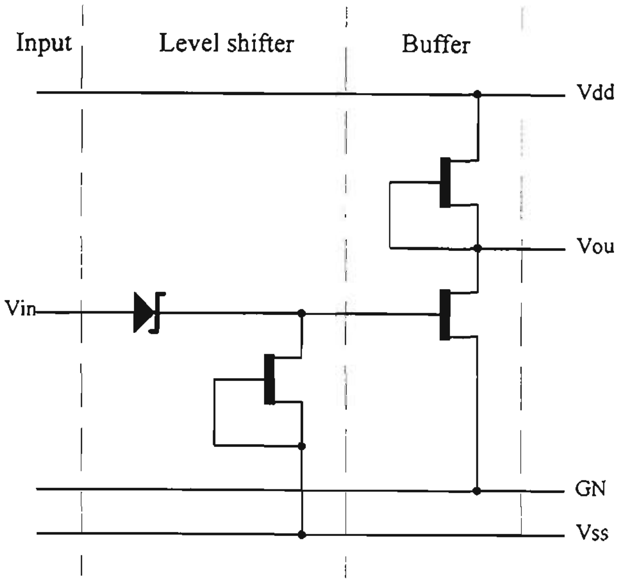


Figure 4.4 Schottky diode MESFET logic inverter.

To overcome fan out problems, a push pull output driver for the SDFL circuit has been suggested [90]. The driver includes a source follower plus a switched pull down MESFET, as illustrated in Figure 4.5. The source follower has very good current sourcing capabilities and is relatively insensitive to loading. The pull down current available for a given logic gate depends on the input states of the gates' loading, and, adding a switched pull down MESFET to the driver addresses this problem. When the output is high, this device is off, and therefore, does not add any more loading or draws any more power. When turned on, it helps to pull down the output node irrespective of the state of the inputs of the loading gates. The push pull driver results in SDFL circuits that are relatively insensitive to fan out, but at the expense of extra area and power requirements.

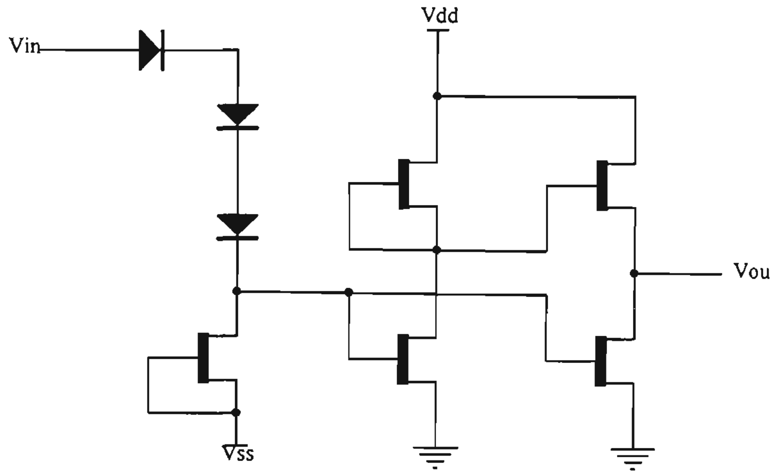


Figure 4.5 Schottky diode MESFET logic inverter with push pull driver.

4.3.1.4 Capacitor Diode MESFET Logic (CDFL)

CDFL logic family takes a different approach to reducing buffered MESFET logic power consumption by being introduced as feed forward, static logic [91]. Figure 4.6 illustrates the inverter configuration in CDFL. The Schottky diode added to the voltage shift section of the circuit is always reversed biased and acts as a capacitor providing capacitive coupling between stages, which, transmits the high frequency signal. The transmission of high frequency signal through the capacitor diode (CD) allows for smaller device width of the current source in the voltage shift section and also for wider tolerance to pinch off voltage variations' than is the case for the buffered MESFET logic without performance degradation. While buffered MESFET circuits have to retain internal logic levels to achieve a certain performance, in CDFL there is no need to bias the voltage shift section for optimal speed but only for the correct DC levels.

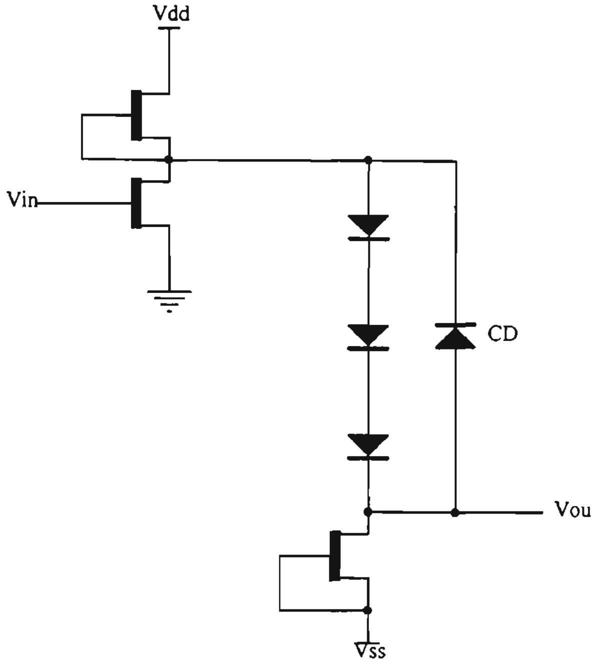


Figure 4.6 Capacitor diode MESFET logic inverter.

Two factors must be considered when designing CDFL circuits. First, the CD must not be punched through under operating conditions. This implies that the charge flow to the depletion edge of the capacitor must not be excessively hindered. Second, the capacitance of the CD must be significantly greater than the maximum capacitive load of the output node. Since the two capacitors act as a divider network, it will not excessively attenuate the high frequency signal.

4.3.2 Normally-Off Logic

The normally-off logic uses enhancement mode MESFETs as switching elements. In this section the following GaAs design approaches are investigated:

(i) direct coupled MESFET logic (DCFL),

(ii) source-follower DCFL (SDCFL), and

(iii) source-follower MESFET logic (SFFL);

4.3.2.1 Direct Coupled MESFET Logic (DCFL)

DCFL class of logic uses both E- and D-MESFETs. This class of logic resembles the structure of NMOS logic with which the present generation of VLSI designers are most familiar with. Because of the structure of the gate, ratio rules which establishes the device size applies. The sizing determines the performance of the basic gate both in terms of power-speed product and noise margin. Figure 4.7 illustrates the DCFL inverter structure where the designer must select the transistor size of each MESFET to achieve the required performance. For the inverter circuit the following expression define the pull-up, Z_{pu}, to pull-down Z_{pd}, ratio [74]:

$$Z_{pu} = \frac{L_{pu}}{W_{pu}} \qquad \textbf{(4.0)}$$

$$Z_{pd} = \frac{L_{pd}}{W_{pd}} \qquad \textbf{(4.1)}$$

and

$$\frac{Z_{pu}}{Z_{pd}} = \frac{a_{pd}}{a_{pu}}.[\frac{-V_{tdep}}{(V_{inv} - V_{tenh})}] \qquad \textbf{(4.2)}$$

where Z_{pu} and Z_{pd} are the pull-up and pull-down aspect ratios of the transistors respectively,

L and W are the length and width of the transistors,

a is the area of the transistor,

V_{tdep} and V_{tenh} are the threshold voltages for the D- and E-MESFETs respectively, and

V_{inv} is the inverter threshold voltage.

The following expression describes the inverter threshold voltage:

$$V_{inv} = V_{tenh} - \sqrt{\frac{a_{pd}}{a_{pu}}}.(\frac{V_{tdep}}{\sqrt{Z_{pu}/Z_{pd}}}) \qquad \textbf{(4.3)}$$

An optimal DCFL inverter with satisfactory logic levels and noise margins at different process spread has been found to have a pull-up to pull-down aspect ratio in the range 10 - 12 [91].

From the circuit it is evident that there is no need for level shifting circuitry as was the case for normally-on logic. Also, a single power supply bus is necessary. Although DCFL is the simplest and fastest of the static classes it has several disadvantages. The most notable being the low noise margin (100 mV) [91]. This is due to the allowable output voltage being limited by the barrier height of the MESFET Schottky diode at the input of the next DCFL stage (650 mV). From a static point of view, DCFL has very good fan out capability, determined by the very low leakage currents. From dynamic point of view, however, the switching speed of a DCFL gate is reduced by the gate capacitance loading of the output node. The factor of switching speed reduction is approximately **1/n,** where **n** is the number of loading gates. The current through the D-MESFET load is kept fairly low in order to reduce static power dissipation and to improve noise margin by reducing the output logic low of the E-MESFET. As a consequence, the output rise time of the circuit with high fan out is slow. Other limitations include the sensitivity of the gate delay to fan in, load capacitance and the small temperature stability margin.

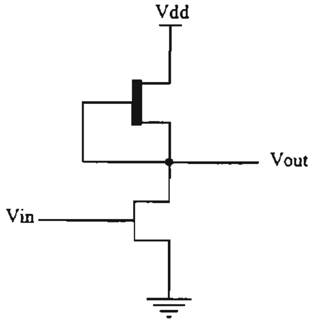


Figure 4.7 Direct coupled MESFET logic inverter.

4.3.2.2 Source-Follower Direct Coupled MESFET Logic (SDCFL)

The source-follower DCFL, as the name imply, consists of a DCFL stage using a source-follower as a buffer on the output. This approach utilises two distinct features of the source-follower to improve the noise margin of the DCFL circuit. The two features are that: (i) the input transistor of the source-follower does not draw any gate current even when the input voltage is as high as the supply voltage, V_{dd}, and (ii) the minimum output voltage is lower than the threshold voltage of an enhancement transistor. Figure 4.8 illustrates the structure of a SDCFL inverter.

In SDCFL circuits, the voltage levels at the input and output terminals are DCFL compatible. Simulation results on optimal SDCFL inverter show that low level output voltage is much lower than that for the DCFL inverter, thus, giving a marked improvement in noise margins. As expected, the propagation delay and power dissipation for this circuit are much greater than DCFL circuit. Table 4.3 summarises the performance of an optimal SDCFL inverter.

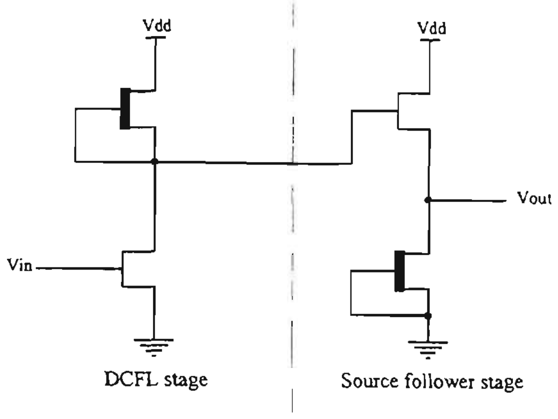


Figure 4.8 Source-follower direct coupled MESFET logic inverter.

4.3.2.3 Source-Follower MESFET Logic (SFFL)

In DCFL and SDCFL design techniques, the input stage is an E-D GaAs MESFET inverter. When a buffered inverter with an E-D inverter as the input stage is loaded by another, the output voltage is limited to the value of the Schottky barrier voltage because of gate conduction. It will be desirable if this limitation is removed. As mentioned earlier, a source-follower has a property that its input transistor does not draw any gate current even when the input voltage is as high as V_{dd}. This suggests that a source-follower can be used as an input stage and an E-D inverter as an output stage.

Figure 4.9 presents such an inverter, known as SFFL inverter. This design approach gives a large output voltage swing and good noise margins and it is ideal for driving large fan-out loads. Table 4.3 tabulates the performance of an optimal SFFL inverter.

The basic structure of these classes of logic can be expanded to perform other logic functions. Figure 4.10 shows a structure for a three input NOR gates with DCFL, SDCFL and SFFL design techniques. Proper NAND gate operation is difficult to achieve in these design techniques because, when both the inputs are high (i.e. logic '1'), static current flows through the input transistors, thus degrading the performance of the gates. Circuits in our design methodology are restricted to parallel branches in the input path, that is, OR/NOR gates.

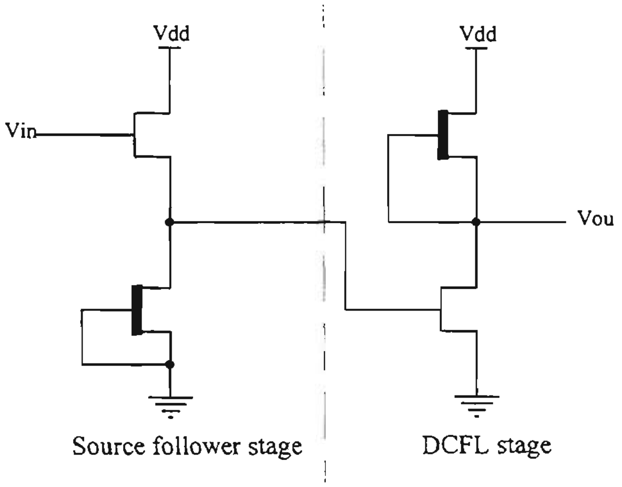


Figure 4.9 A source-follower MESFET logic inverter.

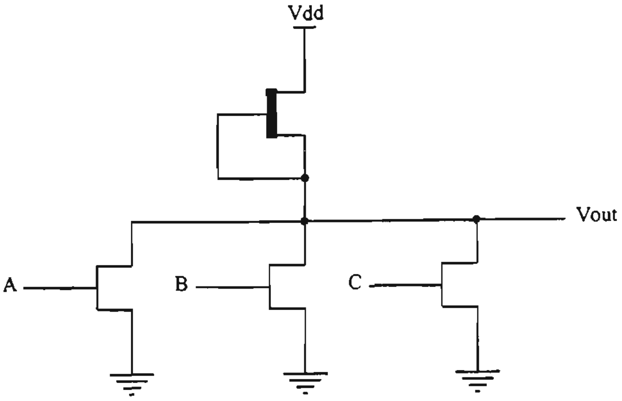


Figure 4.10 (a) Three input NOR gate using direct coupled MESFET logic design technique.

Table 4.3 Performance of optimal DCFL, SDCFL and SFFL inverters

Description	Logic Classes		
	DCFL	SDCFL	SFFL
Power dissipation (μW)	200	590	650
Noise Margin (mV)	100	350	350
V_{HIGH} (mV)	650	700	750
V_{LOW} (mV)	100	20	100
$t_{pd(p)}$ (picosec)	70	90	80
$t_{pd(n)}$ (picosec)	30	70	80

where V_{HIGH} and V_{LOW} are the high and low output voltages respectively, $t_{pd(p)}$ and $t_{pd(n)}$ are the propagation delays during positive and negative going transition respectively.

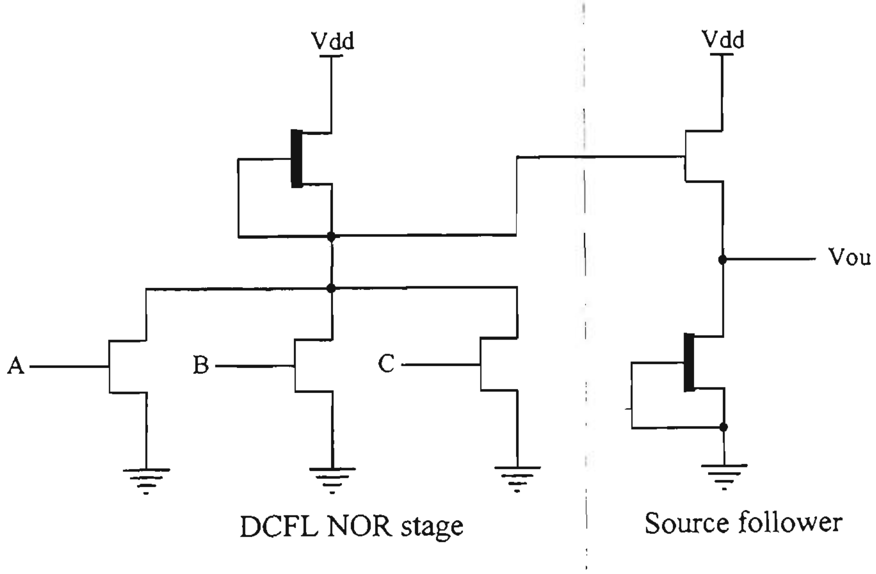


Figure 4.10 (b) Three input NOR gate using source follower direct coupled MESFET logic design technique.

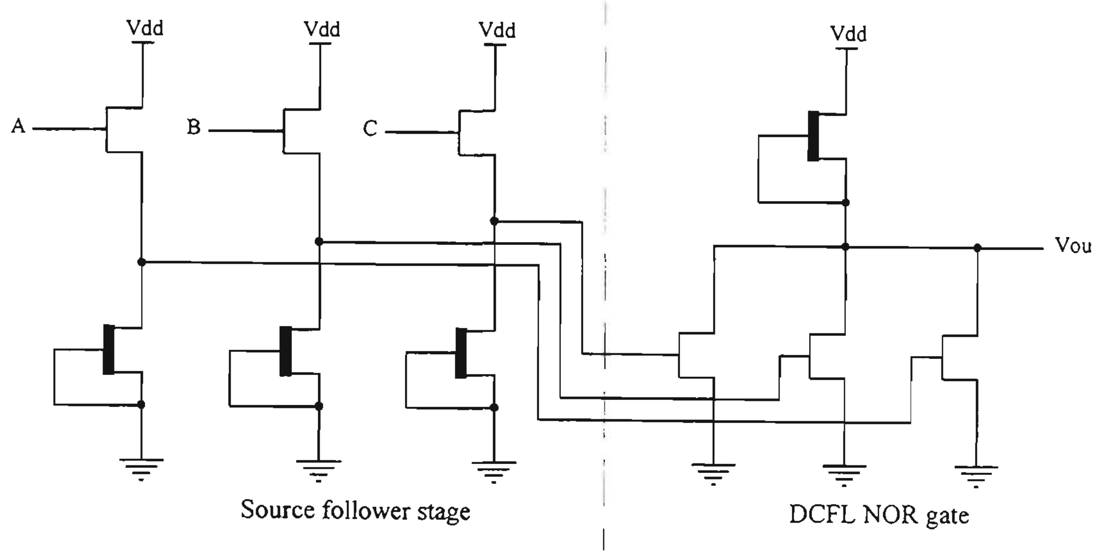


Figure 4.10 (c) Three input NOR gate using source follower MESFET logic design technique.

4.4 Propagation Delays and Power Dissipations

The charge required to move the output voltage of a logic gate by half of the logic swing, $V_o/2$ is given by $(C_N V_o)/2$ in a linear circuit with a constant output node capacitance C_N. Experimental measurements on fabricated MESFETs have shown a weak and similar dependence of the device transconductance g_m and gate-to-source capacitance, C_{gs}, on the operating current I_{DS} [92]. The dependence is attributed to non-linear charge storage and a low and high drain currents in the gate-to-source capacitance. It is found that this excess charge is only 27 percent of the nominal charge and therefore its influence, although significant, is not dominant. The contribution of non linear charges to propagation delay can be taken into account as a correction, after the propagation delay of the logic gate is computed with constant capacitances and transconductances. The propagation average delay, $\mathbf{t_{pd}}$, of a E-D GaAs MESFET gate is given by [92]:

$$t_{pd} = \frac{t_{pd(n)} + t_{pd(p)}}{2} \qquad (4.4)$$

where $$t_{pd(p)} = R_G.C_N.\ln(\frac{V_G - V_{LOW}}{V_G - V_T}) \qquad (4.5)$$

and $$t_{pd(p)} = R_G.C_N.\ln(\frac{V_G - V_{HIGH}}{V_G - V_T}) \qquad (4.6)$$

R_G is the source resistance,

C_N is the load capacitance,

V_G is the voltage source representing D-MESFET,

V_{LOW} is the output low voltage,

V_{HIGH} is the output high voltage, and

V_T is the gate threshold voltage.

Assuming the initial value of the output voltage is $\mathbf{V_{LOW}}$, than the output voltage, V_{OUT}, as a function of time can be expressed as:

$$V_{OUT} = V_{LOW} + (V_G - V_{LOW}).[1 - \exp(-t/_{R_G C_N})] \qquad (4.7)$$

.

and at the time $t_{pd(p)}$, $V_T = V_{OUT}$.

The power dissipation of a DCFL inverter, switching at a frequency *f*, has a static component $\mathbf{P_{st}}$ (which is independent of *f*) and dynamic component $\mathbf{P_d}$ (which is proportional to *f*). The following expression defines the static component of power, $\mathbf{P_{st}}$, [92]:

$$P_{st} = \frac{I_{DS}.V_{dd}.(V_{dd} - V_{LOW})}{2} \tag{4.8}$$

The dynamic power dissipation, **P**$_{\mathbf{d}}$, results from the periodic charge and discharge of the output node capacitance C_N. The following expression defines the dynamic component of power:

$$P_d = C_N.V_{OUT}^2.f \tag{4.9}$$

where f is the switching frequency,

V_{dd} is the supply voltage, and

I_{DS} is the drain current.

Table 4.3 summarises the results for power dissipation and propagation delays for E-D GaAs MESFET circuits. Appendix B presents the derivation of expressions for propagation delays and power dissipation for a E-D GaAs MESFET circuit.

4.5 Noise Margin

Noise margin of a circuit is a measure of its immunity against the possibility of producing a logical error owing to impulsive noise injected at a node and can be defined as the voltage difference between the operating point and the nearest unity gain point. The unity gain is defined on the transfer characteristic where the slope is equal to one.

Noise margin calculations for E-D GaAs MESFET circuits is usually based on the widely used "largest square" definition [93 -94]. The diagonal corresponding to the largest square is defined by the two points on the normal and mirror transfer curves where the slope are equal. Hence for a E-D GaAs MESFET circuits, from simple geometrical considerations the noise margin is given by:

$$\textbf{NML (noise margin low)} = \mathbf{V_{IL} - V_{OL}} \quad \text{for } V_{SW} < V_{IH} \qquad \textbf{(4.10)}$$

$$\textbf{NMH (noise margin high)} = \mathbf{V_{OH} - V_{IH}} \quad \text{for } V_{SW} > V_{IH} \qquad \textbf{(4.11)}$$

The intercept voltages V_{IH} and V_{IL} are defined as:

$$V_{IH} = \frac{V_{OH} + G.V_{SW} + V_{OL} - V_{1SW}}{1+G} \qquad \textbf{(4.12)}$$

$$V_{IL} = \frac{2V_{OH} + (G-1)V_{SW}}{1+G} \qquad \textbf{(4.13)}$$

where $$V_{1SW} = V_{SW} + \frac{(V_{OH} - V_{OL})}{G}$$

G is the voltage gain,

V_{SW} is the switching voltage

V_{OH} is the output high voltage,

V_{OL} is the output low voltage,

V_{IH} is the input high voltage, and

V_{IL} is the input low voltage,

The results for noise margin for different E-D GaAs MESFET circuits are presented in Table 4.3. The derivation of analytical expressions for noise margins are discussed in Appendix C.

4.6 Source Coupled GaAs MESFET Logic (SCFL)

To realise high speed GaAs integrated circuits a suitable logic family should be chosen to meet the noise margin, power, speed and the interface requirements with the tolerance to the fabrication process and temperature variations. One of the biggest problem in realising ICs in GaAs technology is caused by the dispersion of device characteristics throughout the chip and wafer [7 - 12]. The threshold voltage of a GaAs MESFET is the difference of the Schottky barrier voltage and the pinch-off voltage. The latter being proportional to the square of the thickness of the active layer. This implies that the threshold is very sensitive to geometric variations. In SCFL, the circuitry of the logic gate is such that only the relative variations of threshold voltages is important. Hence, the input level required for switching is only dependent on the difference between the threshold voltages of the MESFETs. In most cases the threshold voltage difference between neighbouring MESFETs on a chip is small.

4.6.1 SCFL Circuit Configuration

Source-coupled MESFET inverter is shown in Figure 4.11. The circuit consists of a E-D GaAs MESFET differential amplifier and source follower buffer. The input voltage,

V_{in}, is applied to MESFET1 of the differential pair with the fixed reference voltage, V_{ref}, applied to MESFET2. When MESFET1 gate voltage is equal to V_{ref}, the same magnitude of current flows through the two branches of the differential pair. For an input voltage higher than the reference voltage, the current mostly flows through MESFET1 and with the input voltage lower than the reference voltage, the current mostly flows through MESFET2. The reference voltage sets the logic threshold level. The state of the SCFL circuit can be detected from the resultant voltage drop across MESFET3 and MESFET4. The size of these two MESFETs are chosen to accomplish charging and discharging of all the parasitic capacitances at a desired switching rate.

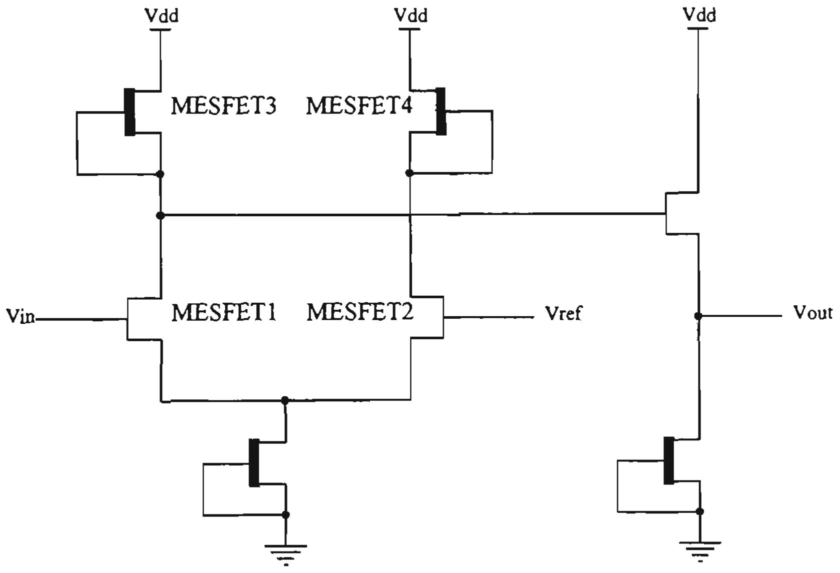


Figure 4.11 Source coupled MESFET logic inverter.

The features of a SCFL circuit are as follows:

(i) If the MESFET threshold voltage is scattered from wafer to wafer, the operating point and the output voltage can be optimised by controlling the reference voltage.

(ii) Due to the source follower buffer, the SCFL circuits are capable of driving many gates.

(iii) Increasing the fan-in reduces the transition region in transfer characteristic and thus increases the transfer gain. The output voltage swing and level are unaffected due to the use of constant current source.

A GaAs MESFET SCFL two input NOR gate is shown in Figure 4.12. The circuit includes a MESFET differential amplifier and a source follower buffer stage.

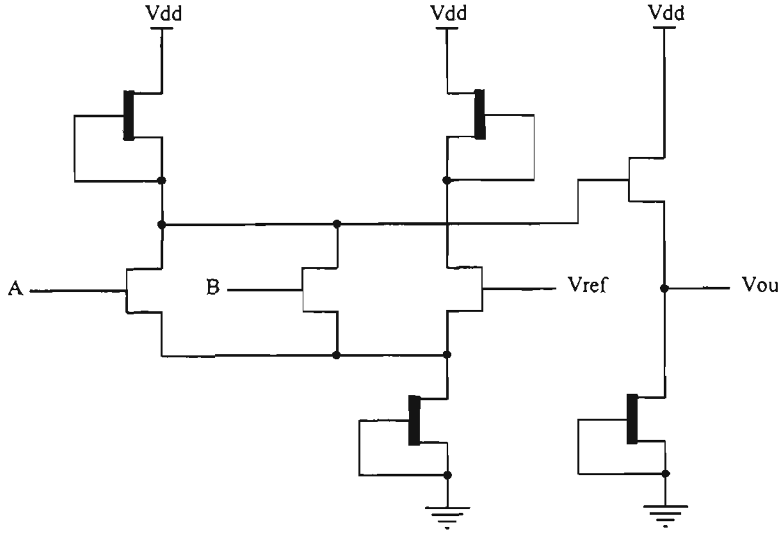


Figure 4.12 Source coupled MESFET logic NOR gate.

4.6.2 DC Characteristics

When the input voltage is applied to MESFET1 in the differential pair (Figure 4.11), the voltage, V_{in}, is compared with the fixed reference voltage, V_{ref}, so that either MESFET1 or MESFET2 can turn "on" in a current mode . The characteristics of a

SCFL circuit is characterised by the switching behaviour of the differential pair. The drain-source current flow for the differential pair, $\mathbf{I_{ds1}}$ and $\mathbf{I_{ds2}}$, are given by [8]:

$$I_{ds1} = \frac{I_0}{2} + \frac{\beta_1 (V_{in} - V_{ref})}{2} . \sqrt{\frac{2.I_0}{\beta_1} - (V_{in} - V_{ref})^2} \qquad \textbf{(4.14)}$$

$$I_{ds2} = \frac{I_0}{2} + \frac{\beta_2 (V_{in} - V_{ref})}{2} . \sqrt{\frac{2.I_0}{\beta_2} - (V_{in} - V_{ref})^2} \qquad \textbf{(4.15)}$$

where I_{ds1} and I_{ds2} are the drain currents for MESFET1 and MESFET2 respectively,

β_1 and β_2 are the HSPICE parameters dependent on the process and geometry of E-MESFET1 and E-MESFET2 respectively,

I_0 is the current flow through the common source.

V_{in} is the input voltage applied to the circuit, and

V_{ref} is the circuit reference voltage.

The DC switching characteristic described by expressions (4.14) and (4.15) provide with the following features exclusively found in SCFL circuits:

(i) switching of the differential amplifier occurs independently of the threshold voltage, and

(ii) complementary outputs are available from the circuit.

For high speed operation one of the most important parameters is the transition frequency, f_T. A MESFET with high f_T can quickly steer the current in the SCFL circuits. The transition frequency, f_T, is described by the following expression:

$$f_T = \frac{g_m}{2\pi(C_{gs} + C_{gd})} \qquad \textbf{(4.16)}$$

where g_m is the transconductance,

C_{gs} is the gate-to-source capacitance, which depends on gate-to-source bias voltage, and

C_{gd} is the gate-to-drain capacitance, which depends on gate-to-drain voltage.

High speed is a feature of SCFL circuits due to the following reasons:

(i) the gate-to-drain capacitance is essentially small because the drain voltage at the ON state is designed to be higher than for any other logic,

(ii) the discharging time of the differential amplifier outputs is short because the discharging current is dominated by the current in the saturation region of the MESFET, and

(iii) the fan out capability is excellent because the source follower buffers enable quick charging up of the load capacitors.

4.6.3 SCFL Circuit Performance

The performance analysis of SCFL circuit was carried out using HSPICE circuit simulation tool. Performance of two input SCFL NOR gate is summarised in Table 4.4. The result shows significant improvement in speed as compared with the normally-on and normally-off logic families. The circuit threshold voltage has a wide range of tolerance and is independent of the threshold voltage of the MESFETs as evident from Figure 4.13. The circuit threshold voltage hardly changes as the threshold voltage of the E-MESFET changes from 0.05 V to 0.3 V. The DC, transient, and the effects of device threshold voltage on the SCFL circuit are analysed in Appendix D.

Table 4.4 Performance of a two input GaAs SCFL NOR gate

Description	Value
Number of devices	10
E-MESFET	5
D-MESFET	5
Gate length	0.8 micron
Propagation delay	
Fan out = 1	30 psec
Fan out = 2	40 psec
Fan out = 3	45 psec
Noise margins	
Low	650 milliVolts
High	480 milliVolts
Power dissipation	0.56 milliwatts

The noise margins were calculated from the transfer characteristics using the largest square noise margin definition. From Figure 4.14 it can be seen that SCFL circuit has an excellent noise margins when compared with DCFL circuits. The improvement in noise margins is mainly due to large logic swings and the differential operation of SCFL circuits.

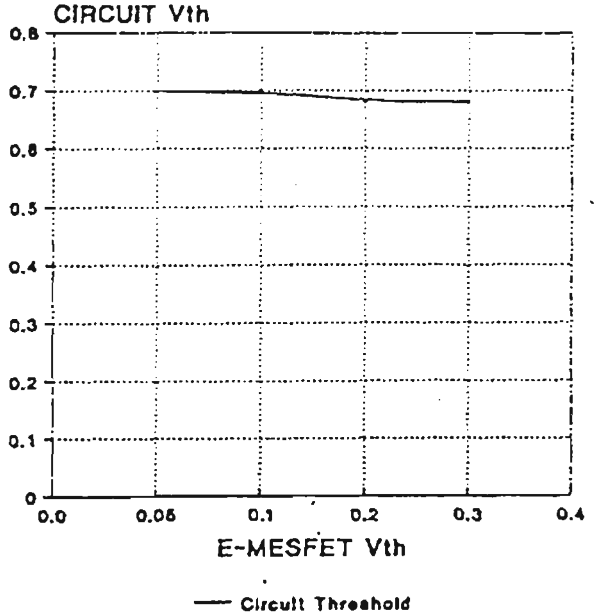
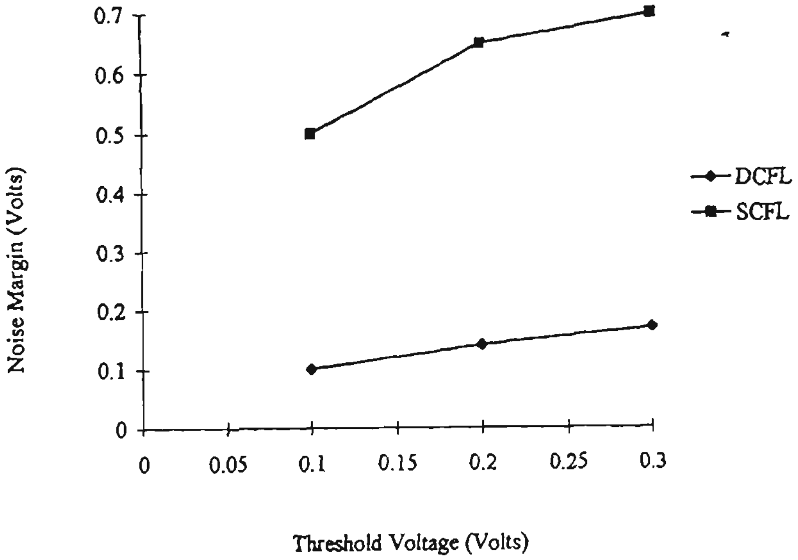


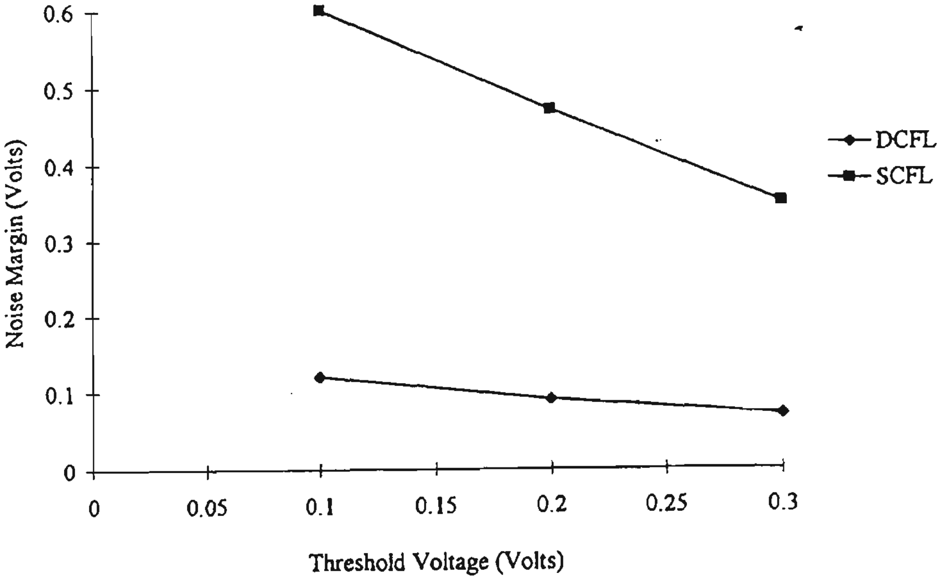
Figure 4.13 Effect of E-MESFET threshold voltage on SCFL NOR gate.

The fan out performance of SCFL circuit was analysed and compared with DCFL circuit. Figure 4.15 indicates propagation delay for the SCFL circuit is remarkably less than the DCFL circuit. This excellent fan out capability of SCFL circuit greatly contributes to the high speed operation in complex logic circuits.

In a SCFL circuit to obtain a complementary outputs, the inputs must also be complementary. A logic variable and its complement must be available throughout the circuit and the logic gates tend to be more complicated than the DCFL circuits. However, series gating, commonly used in ECL, can also be used to implement complex gates.



(a) Low noise margin



(b) High noise margin

Figure 4.14 Comparison of noise margins.

As for power consumption, the SCFL circuit is not necessarily as good as the DCFL circuit. This is because the SCFL circuit has more devices than the DCFL circuit and it is a normally-on logic. The circuit has large voltage swing and relative large incremental gain. The circuit exhibits an excellent symmetry in the two outputs even though the input is only single rail.

SCFL circuits are compatible with bipolar ECL logic. MESFET differential amplifiers usually exhibit smaller voltage gain than bipolar amplifiers. Nevertheless, SCFL circuits are quite fast because the MESFETs operate in the saturation region of the current voltage characteristic where the drain-to-gate capacitance is small. A comparison of SCFL and DCFL circuits is given in Table 4.5.

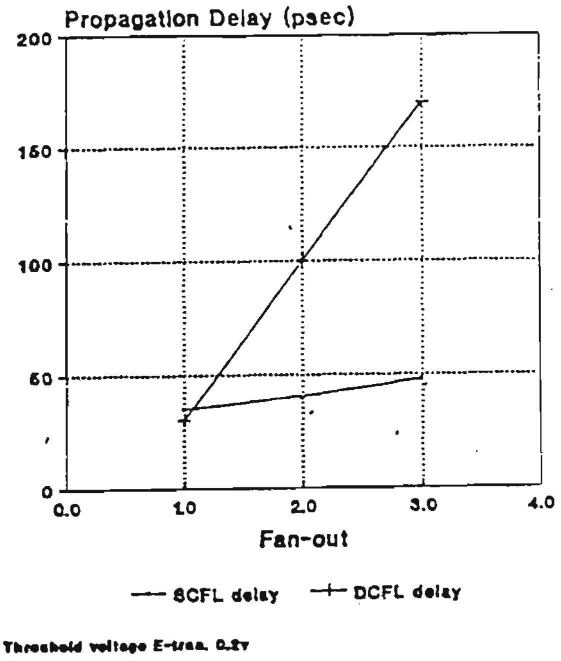


Figure 4.15 Effects of fan out on propagation delay.

SCFL technique seems to be the best choice in the MESFET process for a mix of GaAs digital and analog ICs on the same chip, mainly because of its wide tolerance to threshold voltage range and its immunity to temperature variations. It also has an excellent fan out capability, a small input capacitance and a small discharging time permitting high speed operations.

Table 4.5 Comparison of DCFL and SCFL circuits

Design Technique	Advantages	Disadvantages
DCFL	Simple NMOS circuit style	Small noise margins
	No level shifting	NOR gate is the fundamental logic unit
	Low power dissipation	Inefficient for large macrocells
	Medium performance	
SCFL	Differential circuit technique, therefore independent of threshold variations	Requires level shifting
	Excellent noise margins over temperature, voltage and process variations	Requires twice the number of signals to be routed
	True and complement signals available	High power dissipation
	Low switching noise	

4.7 GaAs Dynamic Circuit Design Techniques

GaAs MESFETs have been used to implement static logic and memory circuits in various applications (adders, multipliers, etc.) [95 - 98]. The implementation of dynamic circuits using GaAs MESFETs have not been as well developed as its static counterpart basically, due to the leakage of the Schottky gate of the MESFETs and the often critical timing requirements on the clock. To realise dynamic GaAs MESFET circuits a suitable design technique should be chosen to satisfy the noise margin, power, speed and interface requirements. Two phase dynamic approaches, as applied to MSI/LSI circuits, has allowed the reduction of chip size per function without loss of speed and with reduced power dissipation [26]. The domino technique has been very suitable for implementing circuits with high fan in and fan out, despite its limitation of providing only non-inverting output. This section presents the two phase and domino dynamic techniques. Other dynamic circuit design approaches have been evaluated, but most were found inconvenient in their implementation or lacking performance. For example, circuits employing transmission gates and precharge devices lacked performance and have been deemed impractical in comparison to the above two approaches.

4.7.1 Dynamic Two Phase MESFET Logic (TDFL)

Two phase dynamic MESFET logic is a ratio-less dynamic logic family which uses two nonoverlapping clocks and dissipates power only during clock level transitions [25 - 26]. TDFL provides all standard logic functions and is directly compatible with static DCFL. In addition, because dynamic nodes store data for one half clock cycle, there is a need for static latches for synchronisation or pipelining. This 'self-latching' feature enables very efficient implementations of pipelined circuits. Because of its low power dissipation and its flexibility in logic circuit design, TDFL is an excellent candidate for GaAs VLSI design.

The schematic of a two TDFL inverters is shown in Figure 4.16(a) and their operation depicted graphically in Figure 4.16(b) [116]. All TDFL gates operate from a single power supply and two nonoverlapping clocks ϕ_1 and ϕ_2. When ϕ_1 is high, the output of inverter #1 is charged to V_{dd} while the input value is passed to node A. Node A is charged to approximately 0.6 Volts if the input is high, or it is discharged to ground if the input is low. During the evaluation phase of operation of inverter #1, ϕ_2 is high, and the value at the output is passed to node C of inverter # 2.

As can be seen from Figure 4.16 (b) that TDFL gates are sequential. That is, the output of an inverter is the inverse of its input at one half clock cycle (T/2) later. While this property limits propagation delay to T/2, it also provides a latched output at no extra cost in area or power. This is a distinct advantage in pipelined or sequential circuit applications.

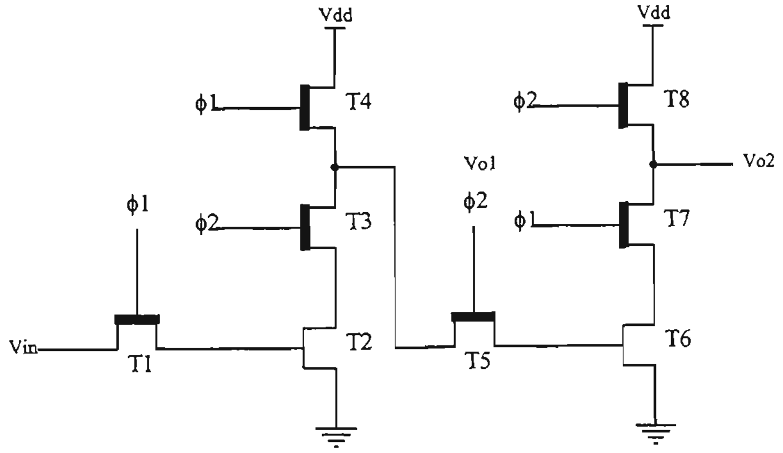


Figure 4.16(a) Schematic of two TDFL inverters in series.

Figure 4.17(a) and (b) depict the schematics of TDFL NAND and NOR gates. Unlike DCFL, NAND gates are reliable in TDFL because there is never any static current flow in the input transistors (Q_3 and Q_4 of Figure 4.17(a)).

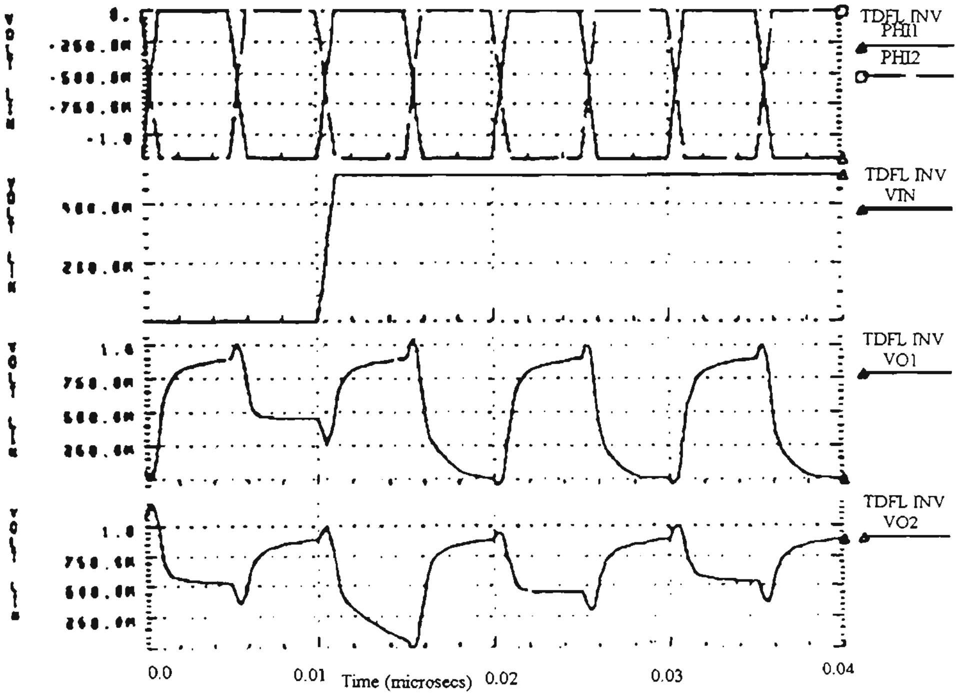


Figure 4.16(b) Simulated operation of TDFL inverter.

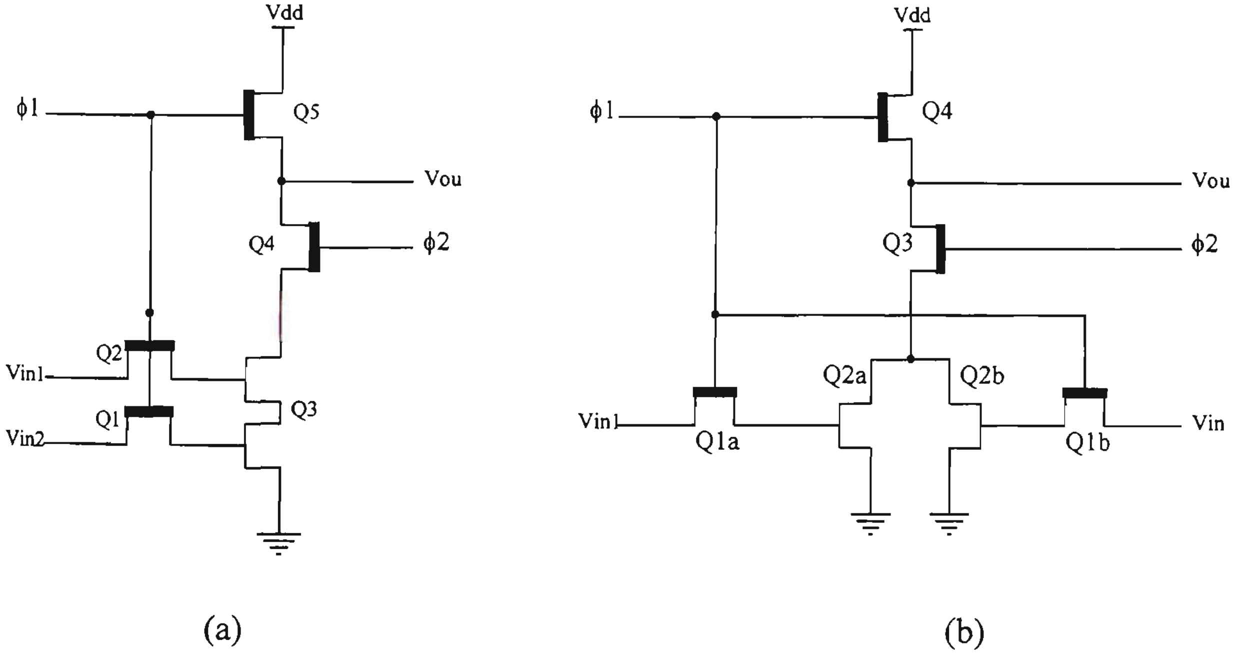


Figure 17 Two input TDFL (a) NAND and (b) NOR gates

This design approach uses nonoverlapping clocks to eliminate static power dissipation. By sequentially toggling transistors Q_4 and Q_5 in Figure 4.17(a), a direct current path from V_{dd} to ground is prevented. Since TDFL uses D-MESFETs as pass transistors, the overlapping clock voltage level is determined as follows:

$$V_{td} < V_{clk}(on) - V_{in} < 0.8$$

$$V_{clk}(off) - V_{in} < V_{td}$$

where $0 < V_{in} < 0.5$

For typical threshold voltage $V_{td} = -0.88$ Volts, the region of clock voltage level is:

$$-0.38 < V_{clk}(on) < 0.8$$

and

$$V_{clk}(off) < -0.88.$$

Table 4.6 tabulates the performance of a TDFL and DCFL registers. It can be seen that TDFL circuit saves up to 90% on power dissipation. Another advantage is that the delay of a TDFL register is one clock cycle, while that of a DCFL register is one clock cycle plus added gate delays. It is important to note that the TDFL logic levels are compatible with DCFL and buffered MESFET logic levels. This compatibility can be used to great advantage in chip design. This fact is used to advantage the construction of EXCLUSIVE-OR gate, as shown in Figure 4.18. However, the drive capability of TDFL logic is poor because the low voltage swing of TDFL ($0 < V < 0.6$ Volts). When

TDFL drives a long wire, the output capacitance is large and charge sharing can be a problem.

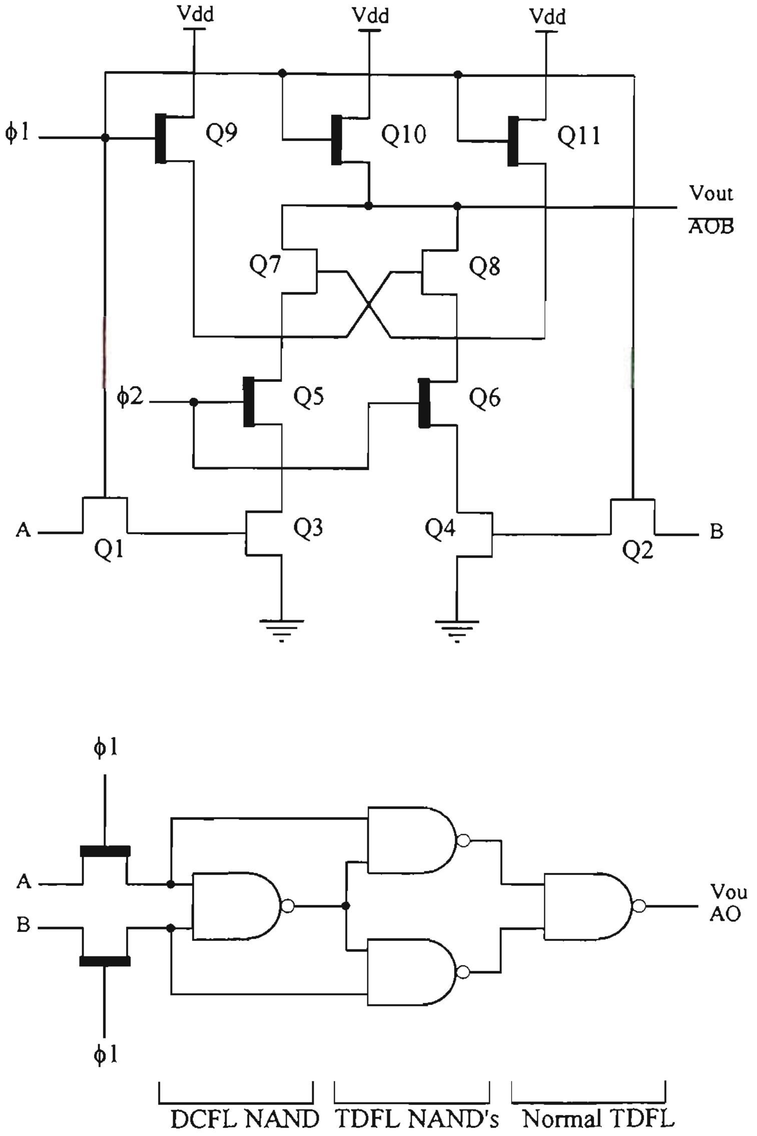


Figure 4.18 TDFL XOR gate made from DCFL and TDFL gates.

Table 4.6 Comparison between DCFL and TDFL registers

Description	Logic Type	
	DCFL	TDFL
Device count	27	16
Propagation delay	1.5 nanosec	1.2 nanosec
Power dissipation	2.0 milliWatts	0.2 milliWatts

4.7.2 Dynamic Domino Logic

Dynamic domino CMOS circuits [24, 99, 100] have found widespread applications due to many performance advantages provided by this approach. By incorporating a static inverter in each gate structure, as shown in Figure 4.19, the output will remain low during the precharge clock phase. Thus, the combinational input structure has no DC current flow even though there is only one clock phase. The speed of the gate is enhanced because the full pull-up current of the precharge device is available for charging the gate node capacitance. Also, the full pull-down current of the combinational logic tree is available during the evaluation phase for discharging this node. Because the logic is no longer ratioed, very complex combinational functions can be accomplished in a single logic gate structure.

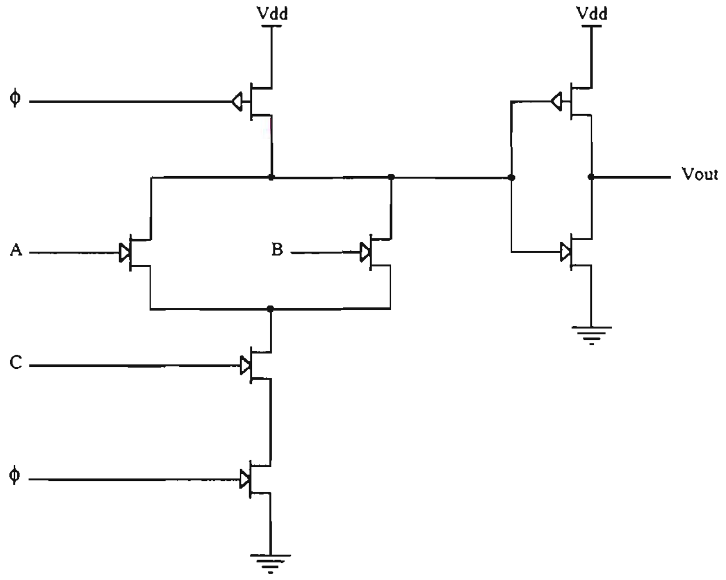


Figure 4.19 CMOS domino dynamic logic.

Many of the advantages of the CMOS domino approach also are possible when circuits are implemented with GaAs MESFET devices. In this section presents a dynamic domino design approach to circuit design using E-D GaAs MESFET devices. A building block of a GaAs domino circuit is shown in Figure 4.20. The input stage is used to compute the combinational logic and the inverter stage is used to store the charge on the gate capacitance and predischarge the input of the next building block. The DCFL inverter stage eliminates the need for any level shifting between the stages and is also suitable for driving domino outputs off-chip.

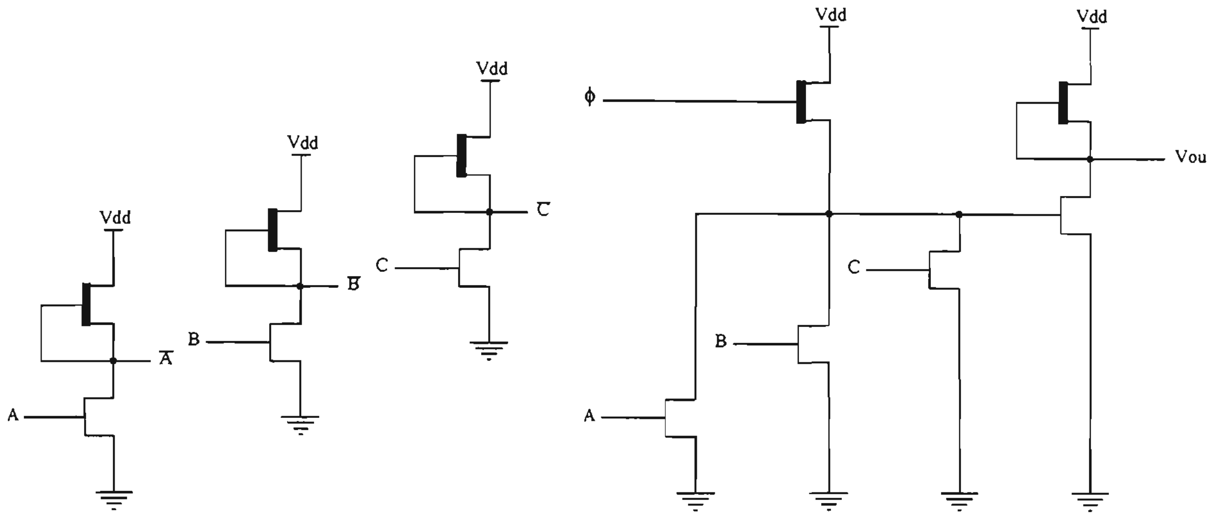


Figure 4.20 Domino GaAs MESFET OR gate.

The circuit operation is as follows: When the clock is high (precharge phase), node N_l is charged and V_l is close to V_{dd}. The output voltage, V_{out}, will be low. When the clock is low (evaluation phase), the precharge device, D-MESFET, is cut-off. The charge on the internal node N_l may be conditionally discharged through the E-MESFET structure in the input stage depending on the outputs of the previous stages. The information propagates, rippling stage to stage as in a chain of dominos. It is important that for proper operation of this type of logic, all the inputs must be kept low during the precharge phase.

To evaluate the properties of this design approach, three input NOR gate and a three-to-eight decoder has been implemented, with the output DCFL inverter being replaced by an E-D source follower stage. The structure utilised two distinct properties of the source follower, which also had better noise margin: (i) the input transistor of the source follower does not draw any gate current even when the input voltage is as high as the supply voltage, and (ii) the minimum output voltage is usually lower than the threshold voltage of an enhancement transistor. The E-D source follower stage eliminates the need for any level shifting between the stages and is more suitable for driving domino outputs off-chip and also driving large capacitive loads on-chip.

The three input dynamic domino NOR gate has been designed, analysed and evaluated using VLSI design suite and HSPICE circuit simulation tools. Table 4.7 summarises the simulated results. The propagation delay for the three input domino NOR gate is 100 psec and the power dissipation is 0.09 milliWatts. The simulated results indicate that variations in threshold voltage have only a very slight effect on the delay except that the voltage swing is reduced. The fall time increases with increasing fan out but the rise time remains relatively unchanged. Because of the nature of the dynamic circuit, the width ratio of the pull up and pull down MESFETs is not required for the optimisation of the noise margin. Therefore, increased number of MESFETs in the input structure will only increase the delay of this stage because of the increased capacitance and resistance. Since the logic swing of the domino circuit is about the same as that of buffered MESFET logic, the yield of functional logic circuits, in an environment in which device parameters vary randomly across or between wafers, is expected to be high than that of a low noise margin design such as DCFL circuits.

Power dissipation per stage is much smaller than for DCFL circuit, therefore circuit complexity in the LSI and VLSI range would be feasible. The noise margin can be about 0.5 Volts or larger depending on the circuit design and choice of V_{dd}. The results of Figure 4.21 shows that a circuit with a E-D source follower structure has better noise margins.

The minimum frequency of operation depends on the storage time, which can be modelled as a RC network. The minimum operating frequency is the lowest clock frequency at which the output of the domino circuit switches while all of the inputs are held low. Therefore, the switching is due to the discharge of the internal node capacitance by the leakage current. From the result it has been found that the lowest frequency at which the circuit will operate reliably is 100 kHz. Further reduction in the lowest frequency can be achieved by adding a resistance across D-MESFET load of the NOR gate. Normally the low frequency is not the limitation when a high speed is desired.

Three-to-eight decoder has been designed using the three input domino NOR gates and implemented with MESFET gate lengths of 0.8 micron, using ISD VLSI design suite. The mask layout for the three-to-eight decoder is shown in Figure 4.22. The circuit has been simulated using GAASNET net extractor and HSPICE circuit simulation tools. The simulated circuit results show higher speed and lower power dissipation when compared with DCFL circuits. Table 4.8 tabulates the results.

Table 4.7 **Performance of dynamic domino three input NOR gate**

Description	Values
Device width	
E-MESFET	50 microns
D-MESFET	20 microns
Gate length	0.8 micron
Propagation delay	100 psec
Power dissipation	0.09 milliWatts
Noise margins	
Low (V_t = 0.2 Volts)	0.60 Volts
High (V_t = 0.2 Volts)	0.45 Volts

The rise in the transfer curve of the domino circuit, as the input voltage increases beyond the turn-on of the input gate diode, can cause logic errors. Secondly, when the input is low, the output will cause the input gate diode of the following stage to conduct in a cascaded domino circuit. Both these problems can be avoided if a diode is

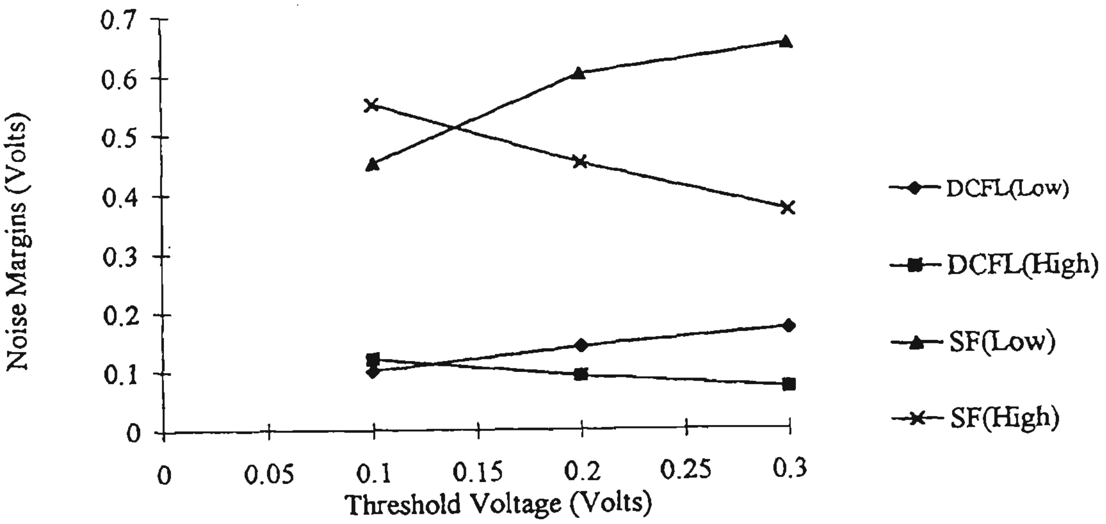


Figure 4.21 Noise Margins for DCFL and dynamic source follower NOR gate.

inserted in series with the E-MESFET of the source-follower stage, as shown in Figure 4.23

Table 4.8 Performance of Domino three-to-eight decoder with source-follower output stage

Description	Domino	DCFL
Device gate length	0.8 micron	0.8 micron
Power dissipation	0.85 milliwatts	2.4 milliwatts
Noise Margins	0.45 volts	0.1 volts
Propagation delays	100 psec	350 psec

With this arrangement it is possible to select suitable widths for the MESFET so that V_{out} is less than the turn-on voltage of the input gate diode. During the evaluation phase, when the input is high, voltage at node N_1 (Figure 4.19) will be sufficiently low, the series diode will not conduct and the output voltage, V_{out}, will drop to zero Volts.

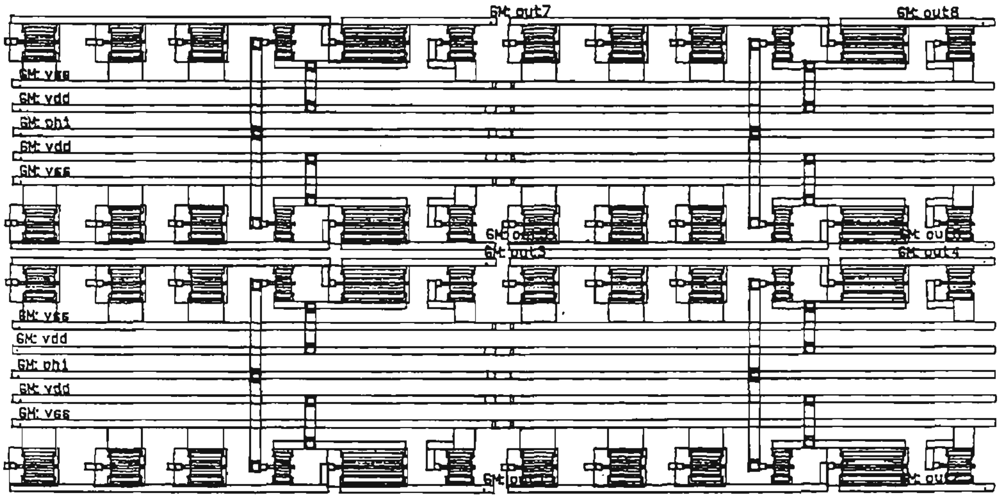


Figure 4.22 The mask layout of the three-to-eight domino GaAs decoder.

This circuit modification will result in better noise margins. The propagation delay should also be lower than the domino source follower circuit because during pull up the output never exceeds the turn on voltage of the input gate diode so that all the current from the source follower goes to charge the output node capacitance. During pull down all the capacitor current goes to the source follower D-MESFET and the discharge current is not reduced by the current from the E-MESFET.

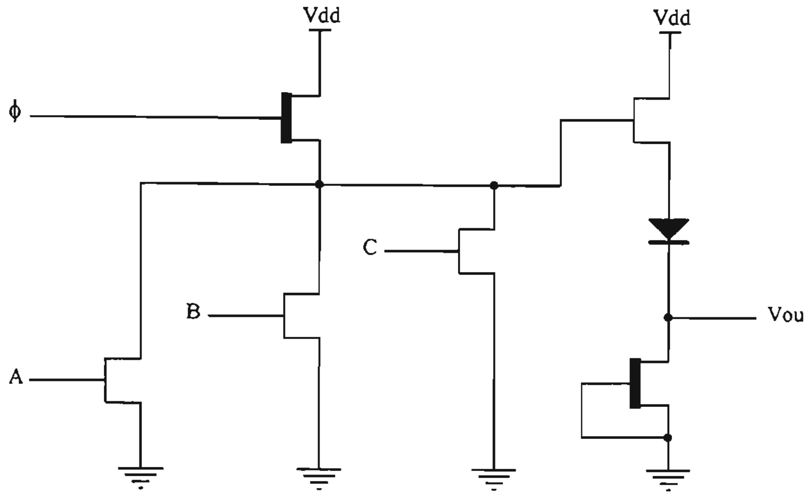


Figure 4.23 Modified output stage of a three-to-eight decoder.

4.8 Conclusions

The choice of a particular GaAs MESFET device for implementing ICs depends on the circuit performance requirements of the circuit and the fabrication process for the device. The relative simplicity of fabricating D-MESFET circuit results in acceptable yields, however, the circuit requires appropriate voltage shifting between stages for proper operation. On the other hand, E-MESFET circuits do not require level shifting, but, these circuits have small voltage swing.

Buffered MESFET logic circuit operation relies on the use of forward biased, level shifting diodes. Although this design technique has excellent speed performance and fan out capabilities, it suffers from relatively high power consumption. Unbuffered

MESFET logic overcomes the power dissipation problem by omitting the load driver source follower but the logic is sensitive to large fan out loads. Other design techniques such as SDFL and CDFL have been developed to overcome the high power consumption of Buffered logic. All the above design techniques require dual power supplies for proper operation, making it unattractive for VLSI design.

The normally-off logic families (DCFL, SDCFL, and SFFL) use E-MESFETs as switching elements and require only one power supply. Although DCFL is the simplest and the fastest of this logic class, it has several shortcomings, the most noticeable being the low noise margin. Other limitations include the sensitivity of the gate delay to fan in, fan out and the load capacitance. SDCFL design technique is suitable for driving large capacitive loads and realising the And-Or-Invert functions, while SFFL provides large fan out capability.

One of the major problems in realising ICs in GaAs MESFET technology is caused by the dispersion of the device characteristics throughout the chip and wafer. In SCFL the circuitry of the logic gate is such that only the relative variations of the threshold voltage is important. SCFL technique is the best choice in the MESFET process for a mix of GaAs digital and analog circuits on the same chip, mainly because of its wide tolerance to threshold voltage range and its immunity to temperature variations. It also has an excellent fan out capability, a small input capacitance and a small discharging time which permits high speed operations. This technique exhibits excellent noise margins over temperature, voltage, and process variations.

TDFL dynamic approach to circuit design allows the reduction of chip size per function, without loss of speed, and has much lower power dissipation. TDFL circuits are compatible with DCFL circuits. This compatibility can be of great advantage in chip design, but the technique has very poor drive capability. On the other hand the domino dynamic approach is very suitable for implementing circuits with high fan in and fan out despite, its limitations of providing only non-inverting output.

Chapter Five

GaAs Integrated Circuit Design Methodology and Layout Style

The artist must understand that he does not (only) create - he materialises.
Horia Bernea.

Style, like sheer silk, too often hides eczema.
Albert Camus.

5.0 Chapter Overview

This chapter presents GaAs IC design methodologies and layout styles used to produce various designs. Full custom design approach has been used for all the design layout with the entire operation implemented on a single chip rather than on multiple chips. This allows the designer to take maximum performance advantage of the GaAs technology.

5.1 Introduction

GaAs technology is attractive for the design and implementation of high speed digital ICs, mainly because of the inherent properties of the material, namely, high electron mobility, high peak electron velocity and low intrinsic carrier concentration, which yields semi-insulating substrates. Low intrinsic carrier concentration reduces device and interconnection capacitances, and is a requirement for high speed operation at reduced power dissipation.

Several issues should be considered when designing GaAs digital integrated circuits. The interconnection of devices is a crucial issue because logic gate delays may be comparable to the delays introduced by interconnections. At the systems level, although on-chip speed is very high, this performance advantage can be lost by the slowing action of interchip connections. Therefore, this requires a different approach to on-chip GaAs architecture than to that of silicon based VLSI ICs. Exploitation of on-chip gate speed will be optimum when the functionality of the chip is increased for a given system application. This results in the implementation of the intended system function with as few chips as possible. Furthermore, the optimum utilisation of the advantages offered by the GaAs technology requires a holistic approach to system design. The architectural design of the system should be considered as a whole, including the algorithm, architecture and device performance. The fast rise times generated by GaAs circuits and the small logic swings make their interface with silicon ICs difficult and the design of on-chip input/output drivers crucial.

5.2 GaAs MESFET Design Methodologies

The VLSI era has brought with it the concept of design methodology that has for some years facilitated rapid development of complex integrated circuits. The major task facing circuit designer is to turn circuit specifications into masks for processing. The objective is to develop an approach to capture the topology of the actual layout so that through a simple representation, both layer information and topology can be described. At the same time, interaction between signal and power busses is minimised to guard against degradation of noise margin.

Three generic design methodologies apply to the development of high performance GaAs digital ICs [101]. These design methodologies are: full custom design, standard cell design, and gate array design. All these approaches have been used to design GaAs ICs and the selection of one approach over the other depends on its performance, schedule, and budget requirements.

5.2.1 Full Custom Design

Full custom design is the best known methodology for GaAs IC design [102]. The full custom approach gives the designer the full freedom to design the intended structure for the circuit using transistors and diodes of any size, placed at any position allowed by the design rules, and interconnected in any way that does not violate the design rules. Following this approach, the designer can take maximum advantage of the technology, thus producing a circuit that meets the required speed, power, noise margin and input/output driving specifications while still maintaining the best possible utilisation of GaAs area. Minimising the area occupied by the circuit is important because the chip die size affects the process yield. Utilising the fewest devices for performing a required function results in small area die, as well as low power dissipation. Sizing each device independently yields faster circuits as compared to circuits where sizing restrictions apply.

On the other hand, full custom design is a laborious process, requiring very good knowledge of circuit design and understanding of the GaAs fabrication process and device characteristics. Designing at the transistor level, means that the design time is the longest compared to any other design approach. The final design has to be verified exhaustively before fabrication. The implication of long design times, is of course, high development cost, both being important issues in a competitive semiconductor market.

Designers mainly use the full custom design approach for medium scale integration circuits where the number of transistors yield a acceptable design time and a manageable design verification process. With increasing level of integration, full custom approach is used to design functional modules which can be repeatedly interconnected to complete the overall circuit function. An example being a memory circuit where its storage cell is usually full custom designed and repeated thousands of time to produce the storage section of the memory circuit.

As both level of integration and demand for GaAs chips increase, there are requirements for rapid turnaround may preclude the use of the full custom design approach. For these complex type of circuits, standard cells or gate array approaches will be more attractive, mainly because they offer shorter turnaround times at lower cost [101]. Full custom design will continue to be employed in memory and microprocessor components where the chip quantities produced can justify the development cost. Finally, full custom design will always be used for special circuits where performance and reliability outweigh any other considerations.

5.2.2 Standard Cell Design

The standard cell approach is the best way to achieve the maximum speed performance, short of a full custom chip design, without paying the penalty of long turnaround times and high development costs [103]. This approach to IC design is similar to board design using off-the-shelf standard parts. The standard cells are functional building blocks of various complexities, fully custom designed at the transistor level, and having their functions and performance verified through implementation and testing. The designer knows the performance characteristics and the electrical parameters of each cell are known to the designer. In most cases, standard cells which normally has a standard dimension. This facilitates efficient layouts because the cells can be butted at the standard dimension when they are connected.

The individual standard cells are full custom designs of all mask levels, but their layout and functions remain constant over time. As a result, their layout can be stored in a database, usually called a standard cell library, and can be recalled for repeated use. A number of standard cells can be interconnected to realise a complete functional entity on a chip. Since the function and performance of the cells have been verified, the designer need only verify the correctness of the interconnection and the performance of the interconnected cells.

The standard cell design approach provides a low risk, rapid turnaround method for designing high performance integrated circuits. However, the penalty paid, compared to full custom design, is the poor area utilisation and the reduced performance allowed by the GaAs technology. Standard cell designs occupy more area than full custom designs, for two reasons. The first is that one of its dimensions is kept constant independent of the circuit complexity in a cell and this leads to sub-optimal utilisation of GaAs area. The cell structure also affects the interconnect patterns, which is another area consuming factor attributed to the constant layout of the cells. The second reason is that quite frequently the designer has to use a cell but not all of its functions and therefore has more devices than are actually needed to perform the intended function. Extra devices actually imply extra area and greater power dissipation.

Designing with standard cell makes the technology available to the wide spectrum of designers who are not necessarily experts in GaAs device operation. This is a major advantage for logic and system designers who intend to design special purpose ICs to impact the performance of the systems. This approach is particularly attractive in the design of high throughput signal processors where there is often a high speed requirement for the circuit. The computational structures of these signal processors are very regular and can be implemented using only a few different cells replicated over the chip. As GaAs technology matures and the yield from the fabrication process increases, the utilisation of standard cells will continue to expand. On the other hand, for components that have to be produced in large quantities, as well as components for military applications with special performance requirements, full custom design will continue to be a viable approach.

Some applications call for a combination of standard cells and full custom design to produce a chip with certain specifications. The combination of two methodologies is often referred to as semi-custom design. This approach uses standard cells wherever possible and full custom design for subsections requiring high performance or area efficiency. The non-standard dimensions of the full custom designed parts of the circuit need hand crafting into the final circuit. This approach resolves the design bottlenecks due to performance or area requirements that cannot be met by standard cells, while maintaining the benefits of rapid turnaround and low design risks.

5.2.3 Gate Array

The gate array approach became popular with silicon technologies because it offered low cost and rapid turn around development of ICs with no stringent performance requirements. This design methodology continues for GāAs technology.

Gate arrays are dies containing collections of prefabricated transistors and diodes placed in fixed positions on the dies, along with suitable general purpose input/output structures and associated bonding pads. The transistors and diodes form an array of active islands with regions around the islands provided for interconnection. A design on a gate array, often called the array personalisation, entails the interconnection of the prefabricated fixed transistors and diodes that provide the required function. The designer in this case defines only the interconnection pattern, which determines the logic function the gate array will perform. By varying the interconnect pattern, a gate array can be configured to a virtually unlimited number of circuits. This approach significantly reduces the cost and turn around time. Since the gate array structure is fixed, the array is prefabricated up to the metallisation step, therefore, only these steps need to be performed when a design is being fabricated.

The trade-offs the designer needs to make when using gate array mainly concern the circuit performance and input/output structure. The fixed transistor sizes and placement may result in the designed circuit not meeting its performance specifications, necessitating modifications in them. Also trade offs may have to be made about the input/output structure intended for the design if the gate array does not offer as many input/output ports as the design may require.

Advances in application specific integrated circuits (ASIC) technology have ushered a whole new way of designing electronic systems with significant advantages, but at the expense of placing severe demands on design engineers, tool developers and ASIC semiconductor vendors. The benefits provided by the use of ASICs, as compared with using the full custom design include reduced design cycle and cost, and improved reliability and testability.

Logic synthesis tools and hardware descriptive languages are revolutionising the design of ASIC systems [104 - 105]. The major change is primarily the result of rapidly moving developments in semiconductor technology and design processes as well as the general need for improving both design quality and productivity. In contrast with the traditional, schematic-based, digital design process, logic synthesis software tools use a specialised language such as VHDL (very high speed integrated circuit hardware descriptive language) to efficiently describe and simulate the desired operation of the circuit. As the availability of GaAs gate arrays increases, this design approach will be very effective in implementing GaAs ASICs and testing of the design specifications at prototype stage.

5.3 Architectures Attractive for GaAs Implementation

The higher gate speed offered by the GaAs technology makes it attractive for utilisation in high performance system design. Optimum exploitation of gate speeds, leading to significant impact on the system performance, requires a different approach to on-chip architectures than those used in silicon VLSI chips. The main reason for this different approach is that the logic gate delays of GaAs circuits compare, in magnitude, with the delays of chip-to-chip interconnections and the latter, being constant, limits the system's performance. Therefore, decreasing the on-chip gate delays by using improved technology, while at the same time requiring more chips to perform a given function, will offer no improvement to the system's performance. Also, the result will be a system performance degradation, since interconnect delays rather than the component delay become the predominant limiting factor on performance.

Optimum use of silicon circuit depends on the availability of the large number of gates on each chip, while the effect of gate speed is a secondary consideration. The designer, in this case, turns to parallel architectures to obtain high performance, and places less emphasis on the structures that exploit gate speed. On the other hand, GaAs technology offers very high gate speeds but significantly a lower level of integration. The on-chip architecture, therefore, should focus on maximising the performance while minimising the amount of system performance degradation, due to inter component communication delays as well as on-chip propagation delays. A generic approach to achieving this is to maximise the fraction of the system function performed by the GaAs chip, and not simply to minimise the time required for a simple logic operation. For example, consider one of the most widely performed operations in many signal processing applications, namely, the Fast Fourier Transform (FFT). The basic operations in FFT are:

$$\mathbf{A_1 = A + B}$$

$$\mathbf{B_1 = (A - B).W}$$

where A, and B are the input operands, A_1, and B_1 are the outputs and W is a constant coefficient. One implementation approach would be to implement individual operators (multiplier, adder) on single chips and use these set of chip to perform the required computations. Although the individual components will have high throughput, the chip set performance will be dominated by interconnect communication delays. An alternative approach would be to implement the whole operation on a single chip. This approach will use very short on-chip interconnection, thus allowing for optimum exploitation of the gate speeds the technology can provide. Therefore, it is conceivable that the overall function can be performed in a shorter time on a single chip than on the set of chips employing individual operator chips.

5.4 GaAs MESFET Layer Representation

The advances that are taking place in the GaAs process are very complex and sometimes inhibit the visualisation of all the mask levels used in the actual fabrication process. Nevertheless, the design process can be abstracted to a manageable number of conceptual levels that represent the physical features one observes in the final GaAs wafer.

The GaAs MESFET circuits are formed basically by two layers, namely, green implant layer, and red gate-metal layer. If the gate metal layer is in contact with the green implant layer a GaAs MESFET transistor is formed. The implant layer and the gate-metal layer interact to form a Schottky gate where the layers intersect. However, if an insulating layer is introduced between the implant and the gate-metal layer, then there is no interaction between the two layers and in this case the gate-metal layer can be used as an interconnect.

The GaAs MESFET properties can be modified by varying the density of the implant dopant. By using the simple colour scheme the topology of actual layout in GaAs can be captured so that circuit diagrams which convey both layer information and topology for different layers can be set out. Through colour encoding and symbolic representation of layers it is possible to remove much of the complexity associated with a given design. To convey layer information, the colour encoding used in GaAs MESFET circuit design are [74]:

(i) green (implant) for active implant region,

(ii) red (gate-metal) for Schottky gate and short interconnections,

(iii) yellow (n^+) for the more heavily doped shallow n channel implant,

(iv) blue (metal 1) for first level metal, and

(v) dark blue (metal 2) for second level metal.

Transistors are formed by the intersection of green and red masks. The devices so formed can either be: (i) a enhancement mode MESFET, if there is no yellow implant, or (ii) a depletion mode MESFET if there is such an implant. Table 5.1 summarises the layers of typical E-D GaAs MESFET process. The green layer mask identifies all the active regions, that is, areas that eventually form D and E MESFETs, active loads, Schottky diodes, and implant resistors. Green region that are inside the yellow layer mask form a more heavily doped channel for D-MESFET and green region outside the yellow layer form the lightly doped channel for the E-MESFET.

Table 5.1 Layer representation for E-D GaAs MESFET process

Layer	**Colour**	**Symbolic**
Implant	Green	E-MESFET
Depletion implant n^+	Yellow	D-MESFET
Ohmic contact	Brown	
Gate-metal	Red	Gate-metal
Metal 1	Blue	Metal 1
Metal 2	Dark blue	Metal 2
Contact	Black	Contact
Via	Gray	Via
Passivation	White stripes	

5.5 Ring Notation for GaAs MESFET Circuit Design

Communication paths between cells or group of cells and positioning of power and ground buses have significant influence upon the performance of very high speed VLSI systems. The designers of high performance digital systems need to appreciate the bandwidth requirements of high speed signal and the related constraints such as crosstalk, reflection, attenuation and distortion when a communication path acts as a transmission line. Fast transitions on the signal bus could also bring about significant noise on the power bus. Thus, both the design methodology and layout will have to address the influence of the coupling between busses on the performance of a device.

The placement of power and ground lines must be such as to reduce the lines' self inductance and hence their susceptibility to current transients. From the results of Coplanar Strip Line and Coplanar Waveguide models, power busses placed in the proximity of one another have their inductances reduced by a factor of two to three [106].

This leads to the concept of ring notation, a generic term given to a free form topological symbolic layout, which places graphical symbols relative to each other rather than in an absolute manner. These are subsequently interconnected by coloured sticks representing mask level interconnecting layers, paying particular attention to organisational aspects of power and ground busses in relation to high speed signal carrying paths.

The ring diagram can be turned into mask layout either directly or through an intermediate symbolic representation stage of grid assignment which converts rings into circuit elements. Figure 5.1 illustrates this phase. For the mask layouts produced during design to be compatible with the fabrication processes, a set of generic design rules are set out for layouts so that, if obeyed, the rules will produce layouts which will work in practice. Therefore, with the aid of ring notation the designer can layout the

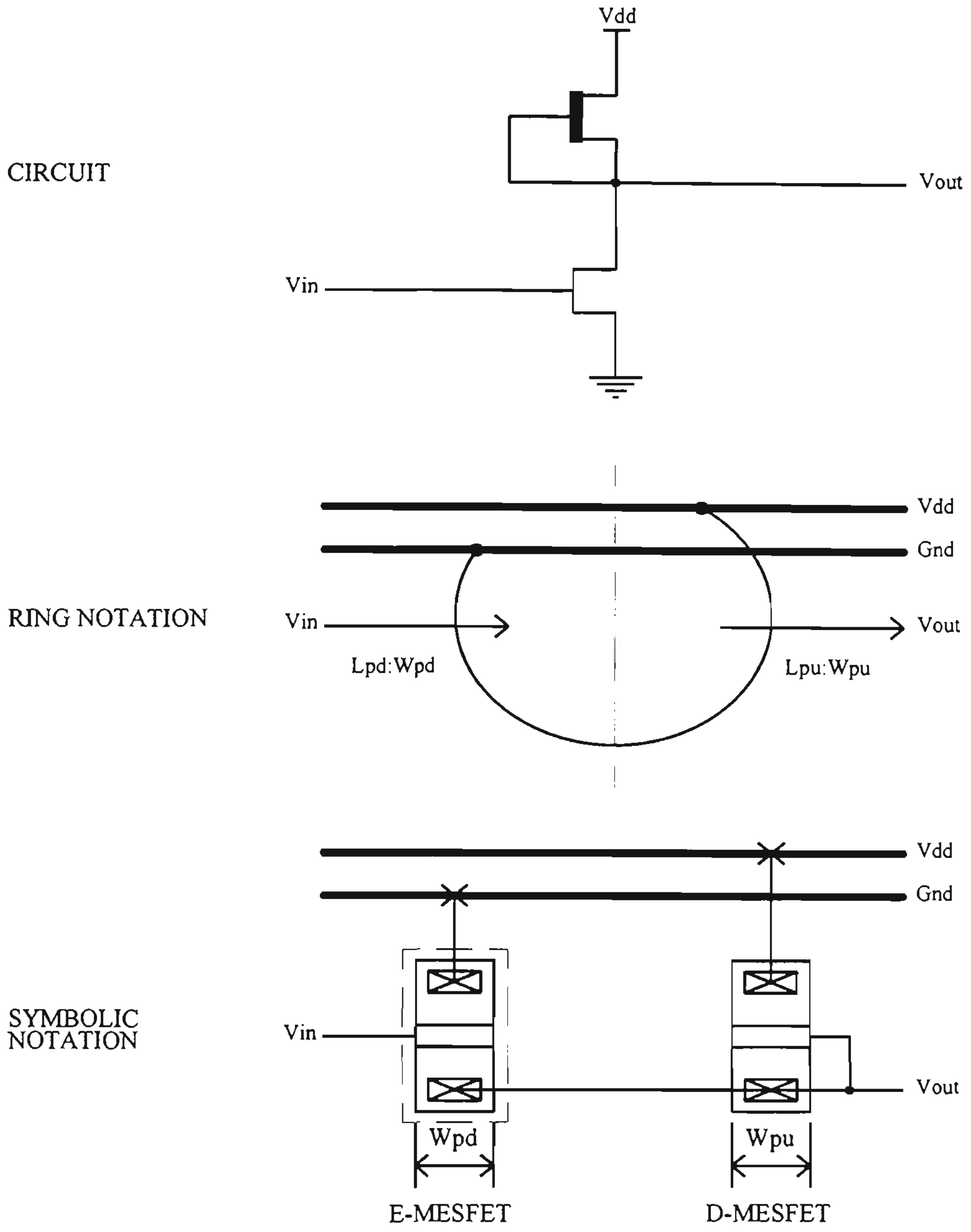


Figure 5.1 Translation of DCFL inverter to ring and symbolic forms [74].

skeleton of a circuit quickly, paying particular attention to interconnects between adjacent circuitry as well as to the positioning of signal busses in relation to both power and ground busses. When starting the layout, the first step is normally to draw the metal 2 power and ground rails in parallel and in the close proximity of one another. Green layer followed by yellow layer are drawn next for inverters and inverter based logic (NOR gates). Inverters and inverter based logic comprise a pull-up structure, usually a depletion mode transistor, connected from output to the power rail and a pull-down structure of enhancement mode transistors suitably interconnected between the output and the ground. Long signal and global control paths are conveniently run in metal 2, parallel with the power rails with the ground bus located in between the two to reduce the coupling of fast transients into the power bus. The remaining interconnects are made in either metal 1 or metal 2. It is also possible to use gate-metal for very short paths.

Since the design of Merged logic circuits are restricted to parallel branches in the input path (NOR gate), the ring notation for NOR gate can be simplified by eliminating parallel input branches as shown in Figure 5.2. Figure 5.3 shows the transformation of a NOR gate into symbolic form [74 - 106].

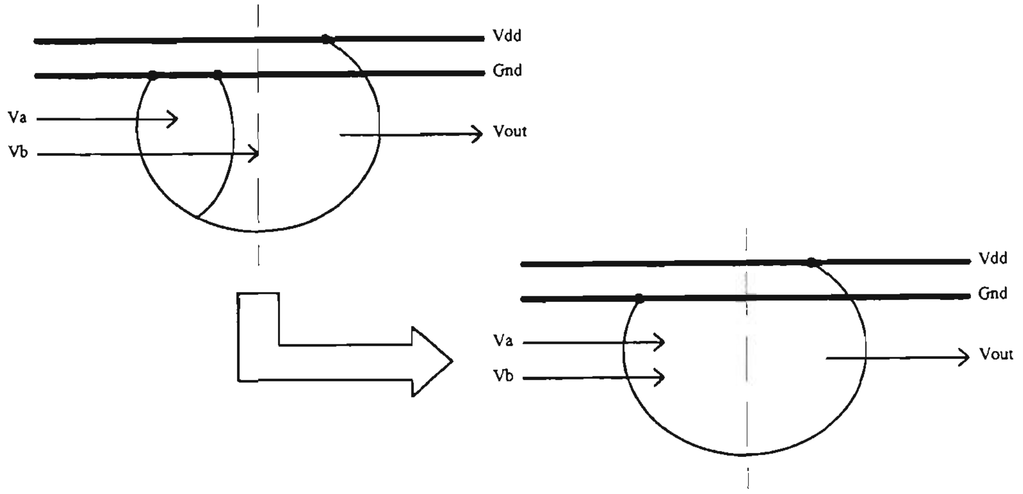


Figure 5.2 Ring notation for two input NOR gate.

During the translation of circuit description into layout, the related issues of electrical equivalence must be addressed. The layout strategy must take into consideration the signal paths to minimise the skew.

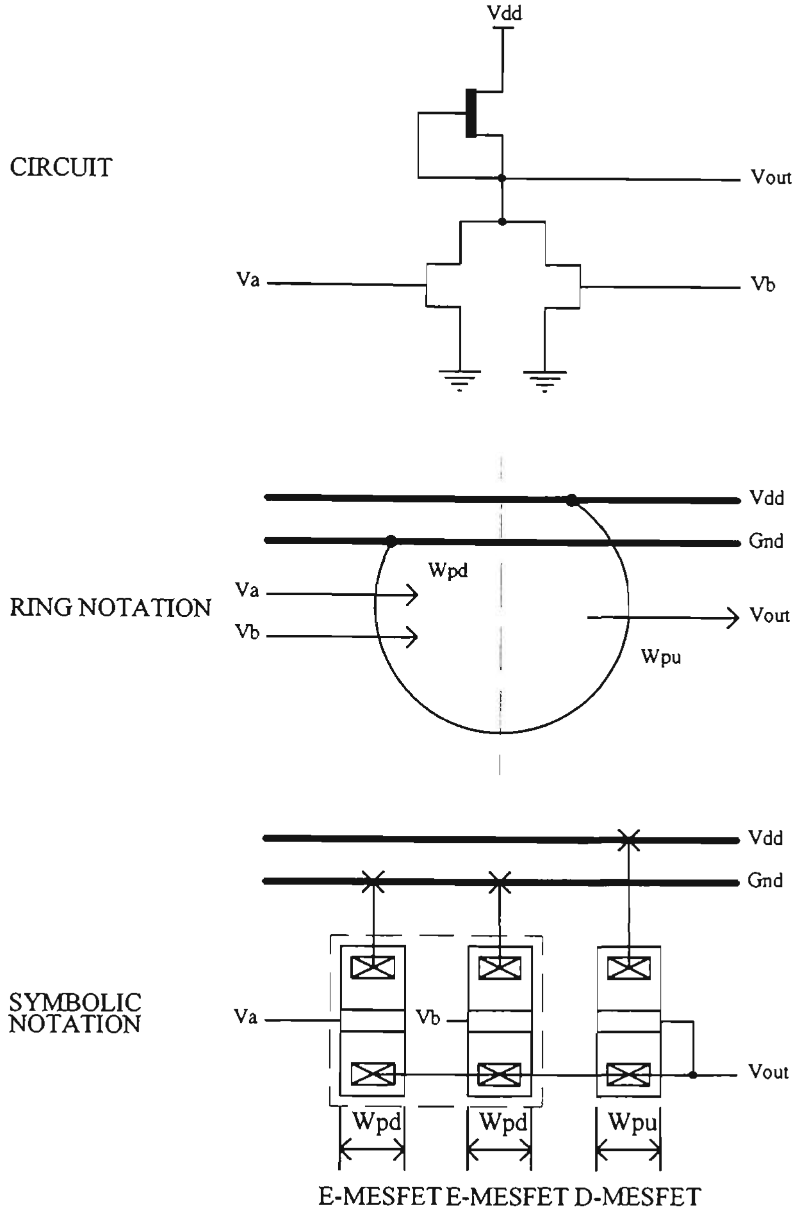


Figure 5.3 Translation of a NOR gate into ring and symbolic layouts.

5.6 GaAs MESFET Layout Design Rules

Layout is the process of translating a design from its logic and circuit representation to its physical representation. The way layout is performed depends on the design methodology used for implementing the integrated circuit and the capability of the layout system. In the full custom design approach, layout is performed for all circuits included in the design on a per gate basis, and all the gates are manually interconnected. This allows the designer to optimise the utilisation of area. Since each gate is laid out individually, close attention is paid to the layout rules during the entire process of chip layout. The design rules are based on the fabrication process and the capabilities of the available lithography system. The main objective associated with the design rules is to obtain the circuit with optimum yield in as small a geometry as possible, without compromising reliability of the circuit. Design rules can also be influenced by the maturity of the process.

Layout rules address two main issues, namely, geometrical reproduction of features that can be reproduced by the mask making and the lithographical process, and interaction between different layers.

Over the years several approaches have been used to describe the design rules. The design of GaAs MESFET circuits is mostly concentrated on lambda based rule. The lambda based rule is based on a single parameter, lambda (λ), which characterises the linear features as well as the resolution of the complete wafer implementation process [107].

Appendix E presents the GaAs MESFET layer colour coding, layer connectivity and lambda based rules.

5.7 Interconnection Lines

Interconnection lines play a major role in integrated circuits with regard to both chip area and dynamic behaviour. In digital circuits the required number of interconnection networks equals approximately the number of gates. Furthermore, the average interconnection line length increases with the complexity of logic circuitry.

The major role of the interconnection networks is reflected, in addition to the required chip area, in the electrical properties of a logic circuit. The interconnection lines pass signals from one logic gate to the next and the rate of signal propagation is limited by delays occurring during the propagation through the interconnection. This delays, and at the same time band limiting effect of interconnection lines, is due to their electrical characteristics.

5.7.1 Electrical Properties of On-Chip Interconnection Lines

The interconnection lines have distributed capacitance, inductance and resistance (C_0, L_0 and R_0 respectively). In high speed systems, interchip interconnection lines have to be terminated with a resistance equal to the characteristic impedance, Z_0, to avoid reflections. On-chip interconnections are unmatched. An equivalent circuit representation of a signal line between two active elements is shown in Figure 5.4.

Normally in VLSI circuits, interest is in the line response in the frequency region below the cut-off frequency of the active devices.

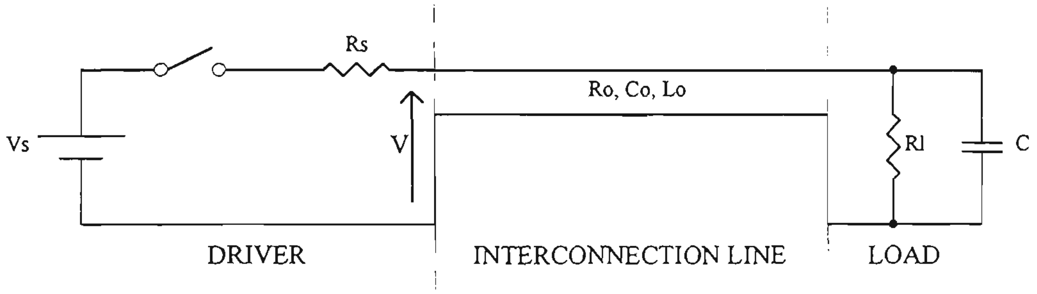


Figure 5.4 On-chip unterminated interconnection line.

The transfer function for the line in Figure 5.4 is given by:

$$\frac{V_s}{V} = \cosh(\gamma l) + \frac{R_s}{Z_0}\sinh(\gamma l) \tag{5.0}$$

where $$Z_0 = \sqrt{\frac{R_0 + j\omega . L_0}{j\omega . C_0}} \tag{5.1}$$

and $$\gamma = \sqrt{j\omega . C_0 (R_0 + j\omega . L_0)} \tag{5.2}$$

$$= Z_0 \cdot j\omega . C_0 \tag{5.3}$$

R_0 is the line resistance per unit length

L_0 is the line inductance per unit length

C_0 is the line capacitance per unit length

l is the line length

If $\mathbf{L_0}$ term is neglected, then the transient line response approaches the exponential charging of a capacitor C = $C_0.l$ through the resistor R_s. Using this approximation, the line propagation delay can be calculated as [73]:

$$T_d = 0.7 R_s . C_0 . l + 0.4 R_0 . C_0 . l^2 \qquad \textbf{(5.4)}$$

The first term simulates the recharging of the line capacitance through the source resistance $\mathbf{R_s}$. This fraction of $\mathbf{T_d}$ is proportional to the line length. The second term simulates the characteristic of RC lines and it increases with the square of the line length.

The principal contributing factor in this line response is the capacitance per unit length, $\mathbf{C_0}$, of the line. When it becomes possible to make this capacitance arbitrarily small, fast and low power circuits will result. The extent of the reduction of this capacitance, however, is limited to the geometry of the lines and the fabrication process.

5.7.2 Solutions To Interconnection Line Problems

Line propagation delays and band limiting occur irrespective of the semi-conductor technology used in the VLSI circuit design. A particularly effective approach for keeping propagation delays of interconnection lines within desirable limits is the utilisation of two or three interconnection layers. The utilisation of multiple layers of interconnect allows higher packing density of the active circuitry and reduces the average line length.

Another option for reducing propagation delays and synchronising signals of different length paths is to include active elements in the interconnection line. The repeated regeneration of signal by the active elements can eliminate the l^2 term from the expression for $\mathbf{T_d}$. The active elements, in this case buffers/inverters, introduce propagation delays. However, a minimum propagation delay can be realised by a trade off between the number of buffers/inverters used and the l^2 term of the propagation delay, $\mathbf{T_d}$.

5.8 GaAs Chip Design Sequence

Regardless of the design approach chosen for developing a GaAs integrated circuit, the designer must take a sequence of steps, from the development of design concept to the final pattern generation that is used for mask fabrication, for a chip design. The work involved in the process of the design sequence is normally supported by a number of Computer Aided Design (CAD) tools and the designer can use these tools to maximise the probability of a successful design with the first fabrication run.

An overview of the stages of integrated circuit design, layout, and implementation is shown in Figure 5.5. The first step in VLSI design is to transforms the circuit and topology level designs into a geometrical layout of the system using appropriate CAD tools. In order to optimise the layout, several iterations of design rule checks and simulations are carried out between the design and the layout steps. The design files are converted to pattern generator (PG) files for use by the mask making firm. By a sequence of photographic steps, the mask house produces a set of masks, which a commercial wafer fabrication firm uses to pattern wafers. Each finished wafer contains an array of system chips. The wafer is then diced into separate chips, which are packaged and tested to yield working systems.

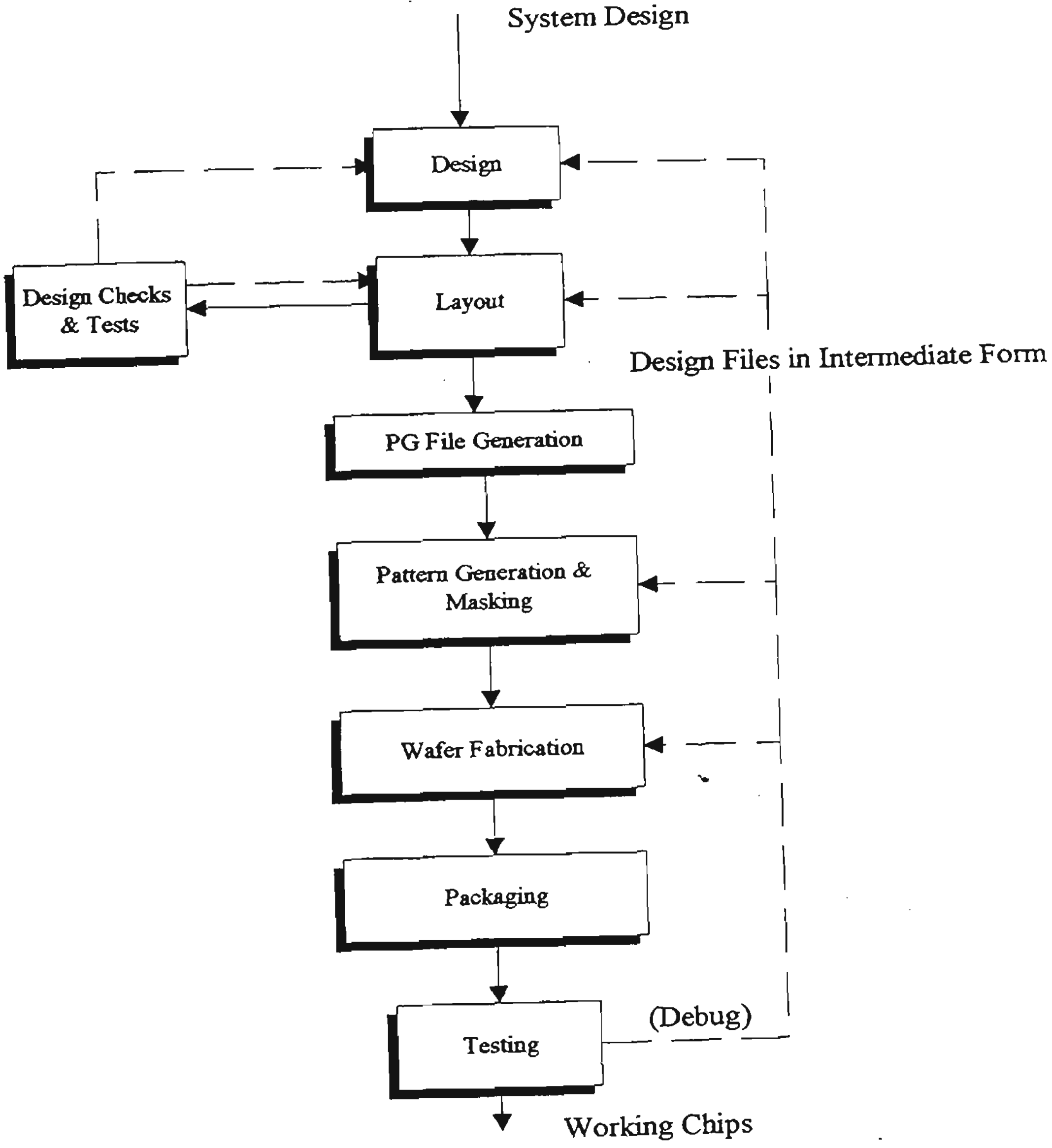


Figure 5.5 Overview of implementation of an integrated circuit.

5.8.1 Circuit Design

The initial task in designing an integrated circuit is to capture the overall logic function by interconnecting logic circuits such as gates, flip flops, registers, etc. The schematic capture of the design is usually independent of the design methodology used to implement the design, its purpose being the logical representation of the function to be performed. The logic circuits are simulated using logical simulators. The purpose of logic simulation is to verify that the circuit to be implemented on a chip perform its intended logic function correctly. The logic simulator operates at the gate level and predicts the output of the circuit, statistically and dynamically as a function of time. It is important to note that the logic simulator does not account for circuit characteristics dependent on the technology used, device geometry, bias or loading. Logic simulation is a design step necessary to ensure correct logic operation for wide range input logic variations. The need becomes greater as the number of state increases and when asynchronous logic is used. The latter is difficult to handle manually, and it will be hard to guarantee an error free logic operation, even for relatively small circuits. Once the circuit has been proved to logically function as intended, the next major step in VLSI circuit design is the selection of circuit design techniques and methodology to meet the design requirements.

The GaAs VLSI design of an integrated circuit has to meet design requirements such as speed, power dissipation and size of the chip. The optimum design of an integrated circuit is the one that meets the speed requirements while dissipating the minimum possible power, without exceeding the power dissipation requirements and occupies the minimum possible area. Speed, power and area, however, are all independent design parameters, and therefore, certain trade off must be made to meet design requirements.

The placement of power and ground lines must be such as to, reduce their self inductance and hence their susceptibility to current transients. Ring notation approach to symbolic design allows the designer to exploit this advantage and layout the skeleton of the GaAs circuit rapidly, paying particular attention to power and signal busses between adjacent circuitry.

For a given minimum gate length, the circuit designer can only choose an appropriate design techniques, device widths, geometry of the interconnects, and layout methodology to achieve the circuit design requirements.

5.8.2 Layout

Layout is the process of translating a design from its circuit representation to its physical representation. The layout depends on the design methodology used for implementing an integrated circuit and the capability of the layout system. To maximise the performance of the GaAs integrated circuits, full custom design approach is used to translate the circuit into physical representation. Using this approach, the layout is performed for all circuits included in the design on a per gate basis. The designer in this case has full freedom concerning the layout style and the arrangement of gates and interconnects. The freedom allows to optimise the utilisation of die area. Since each device is laid out individually, close attention is paid to the layout design rules during the entire process of full custom layout. The layout rules are established based on the fabrication process used and the capabilities of the available lithography system. These rules define limits for the mechanical dimensions of, and spacing between, different features on the various layers in order to ensure maximum circuit reliability for a given process technology.

The primary objective during full custom layout is efficient utilisation of chip area. However, consideration should be given to all aspects of circuit performance during layout. Frequently, trade off must be made among optimum area utilisation, performance, yield and turn around time. Such trade off involve a careful examination of circuit design, device parameters, and layout rules. Optimum exploitation of the performance offered by GaAs technology can be achieved only when the layout guarantees minimisation of parasitic capacitances. In addition, a very important consideration in layout is simplicity. To reduce the possibility of errors in mask fabrication and to increase the accuracy of parameter extraction and, therefore, circuit performance calculations, the layout should be as simple as possible to accomplish the function in the chip design specification.

A multitude of available CAD layout systems support full custom design layout methodology. The CAD tool used for the implementation of the GaAs integrated circuits is the Integrated Silicon Design (ISD) VLSI suite, comprising of:

(i) **PLAN** a powerful mask level graphic full custom layout tool,

(ii) **SEE** a general purpose graphic display tool,

(iii) **CHECK** a fast corner based design rule checker,

(iv) **GAASNET** an accurate and efficient GaAs circuit extractor, and

(v) **ELEC** a versatile electrical rules checker,

together with three utility programs **P2C**, **C2P**, and **POINTS**.

The full custom layout design tool, **PLAN,** is a menu driven, fixed grid, lambda based interactive graphic screen editing tool for Manhattan geometry VLSI design. The output from **PLAN** is a file defining the mask layout description of the circuit. Two utilities **P2C** and **C2P** enable conversion between **PLAN** format and the Caltech Intermediate Form (CIF). Figure 5.6 illustrates the design cycle followed when using this design suite. Appendix E presents the detailed design process based on this suite.

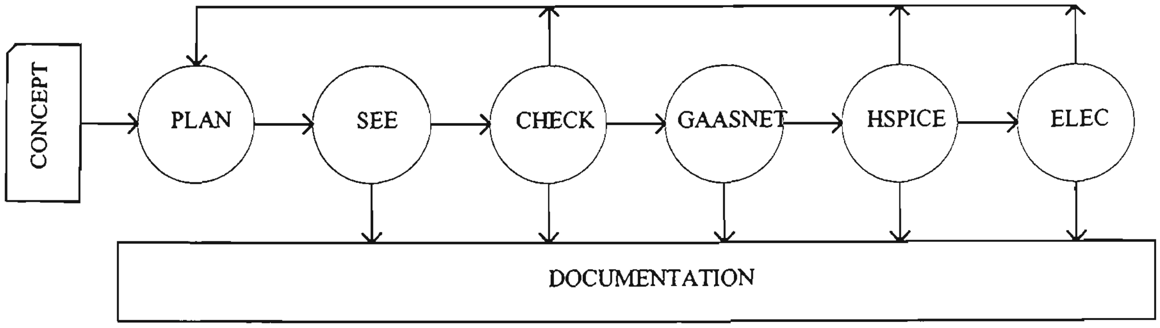


Figure 5.6 GaAs design cycle using ISD VLSI design suite.

5.8.3 Design Rule Checking

When the layout is completed, it must conform to the geometric design rules determined by photolithography requirements and the fabrication process used in implementing the design. The design rule checking is performed by a tool called **CHECK,** which checks for possible violation of minimum dimensions of structures allowed in each layer and also for minimum spacing violation of both unrelated and related structures. Design rule checking is a computer time intensive process but it is very important design step and should never be omitted.

If design rules are violated and the violations are undetected, the resulting circuit will either malfunction or will have very low reliability. This is because the geometry of the devices and interconnections is directly related to their electrical characteristics and also to the capability of the fabrication processing technology.

5.8.4 Circuit Extraction

Circuit extraction ensures logic and electrical performance correctness of the circuit after layout. The circuit extraction program examines the inter-relationship of mask layers to infer the existence of transistors and other components. In addition to device connectivity, the circuit extractor reports parasitic capacitances and resistances at all nodes. This information is extremely valuable because it can be used to perform circuit simulations on various section of the circuit with actual values of parasitics derived from the layout. Circuit simulation including these parasitics is the closest prediction or indication of how the fabricated circuit will behave. Depending on the values of circuit parasitics, the circuit layout or device and interconnect size may have to be changed if the circuit simulation including these values of parasitics produces results that do not meet the circuit design requirements.

The need for circuit extraction increases as performance requirements for a circuit become higher, thus allowing for smaller design margins. Given the relatively high cost of full custom design of GaAs integrated circuits, this design step should be performed to ensure compatibility of design requirements and circuit performance after layout.

The ISD VLSI tool **GAASNET** is a VLSI circuit verification tool used to extract a netlist description and other relevant design information from the circuit description file. It produces connectivity information by identifying where in the mask layout transistors are formed, and how they are interconnected. It also calculates the capacitance associated with each connection. These informations are recorded together with additional information on transistor characteristic and substrate connections in a netlisting file in the appropriate format.

5.8.5 Circuit Simulation

Circuit simulation is performed at the transistor level by taking into consideration device characteristic dependent on the technology of implementation, active and passive device sizes, and parasitics. Since device sizes and technology factors are taken into consideration, there is a strong link between the simulated and the physical structure, and consequently there is a high accuracy in the simulation output that presents the circuit node behaviour as a function of time.

The simulation output is used to derive the propagation delays, rise and fall times and power dissipation as a function of device size, temperature and fan out. In addition, numerous circuit analysis can be carried out to determine the circuit performance.

The most widely used circuit simulator used for GaAs VLSI circuits is the **HSPICE** circuit simulation tool. The **HSPICE** optimising circuit simulator is Meta-Software's industrial grade circuit analysis product for the simulation of electrical circuits in steady state, transient, and frequency domain. This simulator is capable of accurately simulating, analysing, and optimising circuits from DC to microwave frequencies greater than 100 GHz.

The input parameters specified for **HSPICE** simulation include device models indicating the electrical characteristics of the GaAs devices, parameters characterising the device geometry, and input conditions indicating the circuit bias, clocking, and input signals. One of the most important aspects of an accurate simulation concerns the device models. Since some of the device parameters include intrinsic properties of GaAs and the fabrication process, it is very important to include the actual parameters provided by the fabrication house for reliable simulation.

5.9 Conclusions

The VLSI circuit normally has to meet the design requirements concerning the performance of the circuit, namely speed, power dissipation and size of the chip. The optimum design of the integrated circuit is the one that meets the speed requirements while dissipating the minimum possible power, without exceeding the power dissipation requirements and occupies the minimum possible area. Speed, power and speed are all interdependent parameters, and therefore, trade off must be made to meet design requirements.

One of the important considerations during the design of the high speed, low power VLSI circuits is the minimisation of the parasitic capacitance throughout the chip, and the layout should be dedicated by this consideration

Full custom design approach allows the designer the maximum freedom in choosing the layout style and the arrangement of gates and interconnects. This means the designer can take the maximum advantage of the technology, thus producing a circuit that meets the required speed, power, noise margin and input/output driving specifications while still maintaining the best possible utilisation of area devoted to active logic and, most importantly, to interconnections.

In the standard cell design approach, the designer concentrates on placing the cells and interconnecting them in a way that minimises overall chip area, assuming that the selected cells provide the performance required by the chip design specification. The arrangement of the interconnections is the most important aspect of the layout in standard cell design.

Gate arrays have their device sizes, their placement and the routing channels for interconnections fixed. The designer only decides how to map the functional partition of the design onto the array. The trade off the designer has to make when using gate array mainly concern the circuit performance and the input/output structure. The benefits provided by this approach, as compared with using the full custom design include, reduced design cycle time and cost, and improved reliability and testability.

Communication paths between cells or group of cells and positioning of power and ground buses have significant influence upon the performance of very high speed VLSI systems. Fast transitions on a signal bus could cause significant noise on the power bus. The placement of power and ground lines must be placed such as to, reduce their self inductance and hence their susceptibility to current transients. The ring notation approach to symbolic layout allows the designer to exploit this advantage and layout the skeleton of the GaAs circuit rapidly, paying particular attention to power and signal busses between adjacent circuitry.

The primary objective in the layout of GaAs circuits is optimum exploitation of the performance offered by the GaAs technology. This can be achieved only when the layout guarantees the minimisation of parasitic capacitances. Full custom design approach has been used for all the design layouts in this thesis, with the entire operation implemented on a single chip rather than on multiple chips. This allows the designer to maximise on the advantages of the GaAs technology and reduce parasitic capacitances due to chip interconnections.

Chapter Six

Development of GaAs MESFET Integrated Circuit Design Techniques

Nothing great was ever achieved without enthusiasm.

R.W. Emerson.

6.0 Chapter Overview

The following topics are discussed in this chapter:

(i) design and performance of dynamic multiple-output domino technique,

(ii) design and performance of merged logic design technique,

(iii) design and performance of carry generating circuit using domino and multiple-output domino techniques, and

(iv) design and performance of power series evaluator using merged logic design technique.

6.1 Introduction

Multiple-output domino design technique, which is highlighted in this chapter, is a new dynamic GaAs MESFET logic design style which allows single logic gate to produce multiple functions. This design technique is particularly attractive for recurrent logic circuits where reductions in device count by a factor of two or more are achievable. A four-bit, carry generating circuit for a Carry Lookahead Adder implemented by this method demonstrates a performance advantage over one implemented using domino method.

The static design technique, referred to as Merged logic, combines the normally-off static design techniques discussed in Chapter 4, namely DCFL, SDCFL and SFFL to exploit the advantages of each logic class. Such a circuit achieves a superior performance to that obtained by the same circuit exclusively implemented with any one of the separate logic classes. Merged logic predominantly use DCFL stages to achieve high packing density and maximum circuit performance. One then merges SDCFL and SFFL stages with the DCFL stage to drive the capacitive loads and give large fan outs.

Part I Dynamic Design Technique

6.2 Multiple-Output Domino Logic

To improve the performance of GaAs MESFET logic (speed, area and power dissipation), many of the recent GaAs MESFET logic design techniques exploit non-complementary circuit structures [22]. In particular the dynamic domino technique is very suitable for implementing arithmetic and other circuits involving complex gates with high fan in and fan out, despite the limitation that it can only provide non-inverting gates [24]. This is in spite of the fact that multiple functions are often implemented in the logic tree with one being the sub-function of another. Therefore, if one or more of these sub-functions are needed as separate output signals, they have to be implemented in several additional gates, resulting in a replication of circuitry. For example, in the dynamic domino circuits shown in Figure 6.1, the functions **F** and $\mathbf{F_2}$ require two logic tree gates to implement themselves, with duplication of the $\mathbf{F_2}$ logic tree.

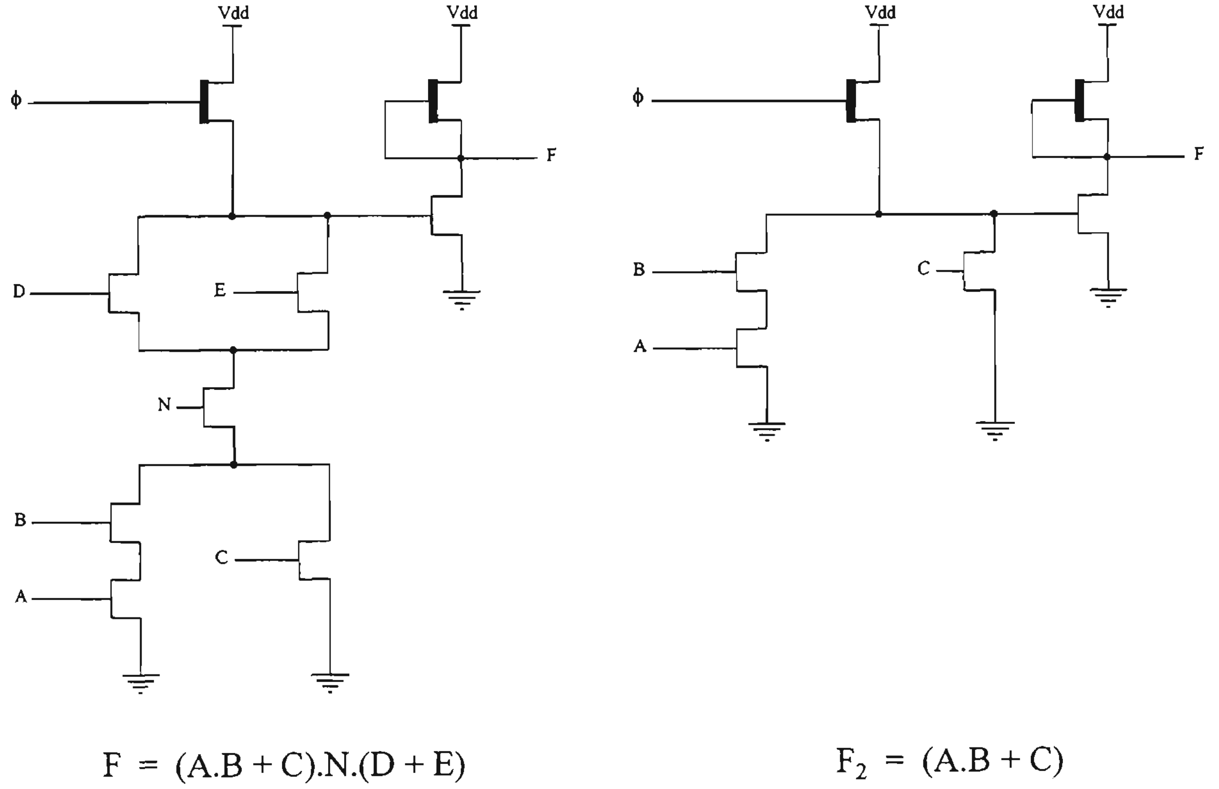


Figure 6.1 Function implementation using dynamic domino technique.

The principle behind multiple-output domino technique is to utilise the sub-functions available in the logic tree of the domino gates, thus saving duplication of circuitry. Multiple outputs are available by adding precharge devices at the corresponding intermediate nodes in the logic tree. Figure 6.2 illustrates the technique for producing both functions **F** and $\mathbf{F_2}$ from a single logic tree structure without duplicating the logic tree for $\mathbf{F_2}$.

In addition, since nodes internal to the logic tree need to be precharged for functional purposes, multiple-output domino logic is, by construction, considerably less susceptive to charge sharing than domino logic. In fact, as shown in Figure 6.2, the added precharge devices to the internal nodes of the logic tree are also the principal means used to prevent the charge sharing - an essential requirement for dynamic circuits. Therefore, these additional precharge devices already exist in the domino implementation of the circuit. From this perspective, multiple-output domino logic requires fewer extra precharge devices and this saves on additional devices.

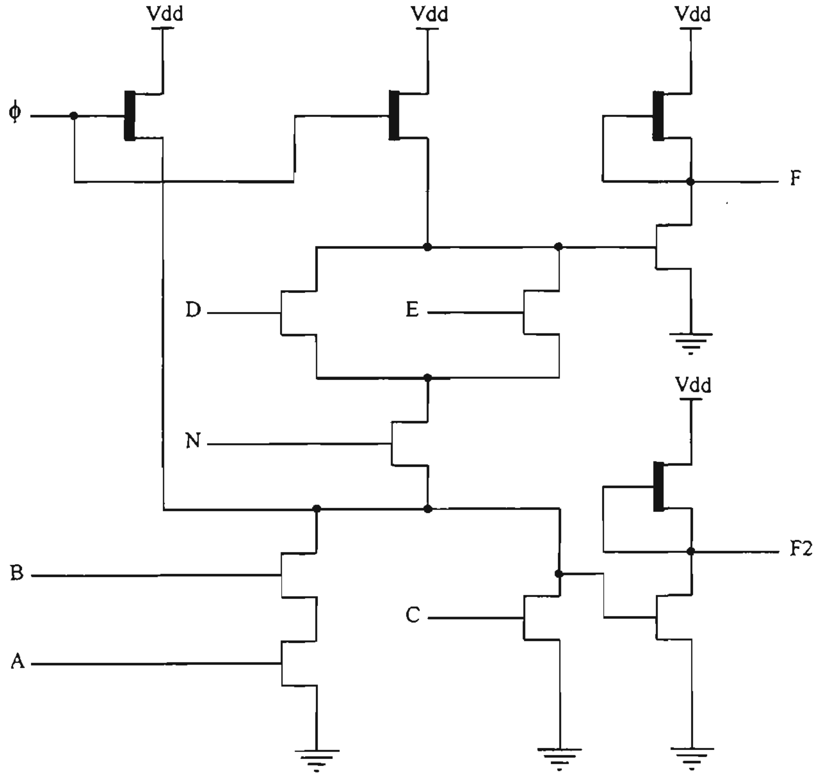


Figure 6.2 Function implementation using multiple-output domino technique.

Since the saving in the circuit area is mainly due to a reduction in the replication of sub-circuits, the actual advantage of this design technique over domino logic design technique directly depends upon the number of recurrence in a logic function being realised. For carry generating circuits, the degree of recurrence is very high, therefore the number of devices used in a multiple-output domino logic version of the circuit should be much lower than in a domino logic version.

As the dynamic portion of each gate drives more than one static inverter, there is an overall increase in capacitive loading compared to that found in domino gates. Larger capacitive loads need slightly large pull down devices. In the actual layout of non-complementary circuits, however, the area saving due to the reduction of gate count overwhelms the area increase due to incrementally larger device sizes.

Although the circuit area saving advantage of this technique is apparent, the speed advantage is not that obvious, especially at the gate level. This is because each multiple-output domino logic gate implements more than one function, and performance improvement is achieved by capitalising on this fact at a higher level. Therefore, an overall organisation of a given block of logic needs to be developed with an intention to use this technique.

In an organisation optimised with respect to this technique, the improvement of performance is due to a reduction of a load capacitance for a given logic stage. This results from less overall device count and less parasitic wiring capacitance as a consequence of a smaller overall layout. In addition, the reduction of capacitance results in a reduction in power consumption as well.

Constructing and cascading AND-OR (sum-of-product) structures in multiple-output domino logic, such as the one shown in Figure 6.3, requires care so as to prevent false discharge at a lower AND dynamic output node by a pull downed OR dynamic node.

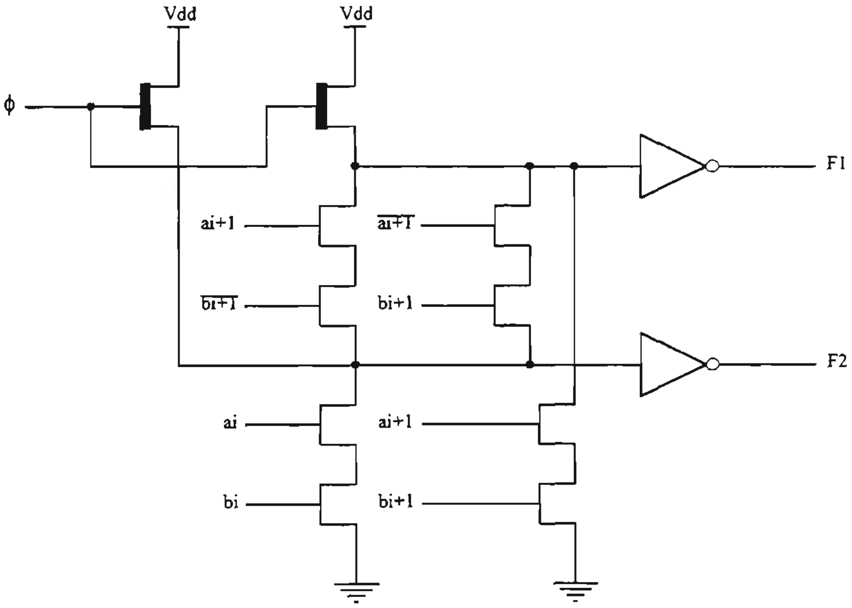


Figure 6.3 Multiple-output domino AND-OR structure.

A reverse current path can occur from the lower node through the higher node to ground depending on the inputs to the logic tree. Boolean simplification or by restructuring the complex AND-OR structure can remove such a current path.

6.2.1 GaAs MESFET Scaling

Dynamic logic circuit are now increasingly becoming an integral part of GaAs VLSI technology. Recently, the advantages of using dynamic logic circuits in GaAs MESFET technology have been demonstrated in References [23, 25 and 26]. Unlike conventional static GaAs gate designs, such as buffered MESFET logic (BFL) and direct coupled MESFET logic (DCFL), GaAs dynamic structures allow ratioless circuit operation, which significantly increases the amount of logic implementable per gate. Cascading of many dynamic GaAs MESFET gates to make either a domino or multiple-output domino circuit, enables the circuit to execute many data path operations of a microprocessor, like: addition, shift, rotation etc. at very high speed. The speed of the GaAs MESFET dynamic chain can be further improved by scaling the MESFETs in the dynamic chain. Figure 6.4(a) shows a structure of a domino four-input GaAs AND gate. The chain of GaAs E-MESFETs were laid out using VLSI design suite as shown by layout 'A - D' in Figure 6.4(b). The gate propagation delays for the four structures were analysed using the GaAs net extractor and HSPICE simulation tools and are tabulated in Table 6.1. The width of the MESFETs of the unscaled chain (layout A) were eight microns with 0.8 micron gate length.

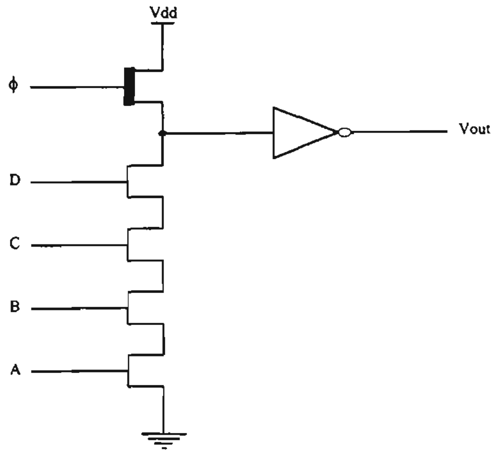


Figure 6.4(a) Four input domino GaAs MESFET AND gate.

For each layout the precharge D-MESFET was four microns and the buffer E-MESFET and D-MESFET were twelve microns and four microns respectively. From the results it can be seen that the propagation delay decreased by 54 percent by scaling

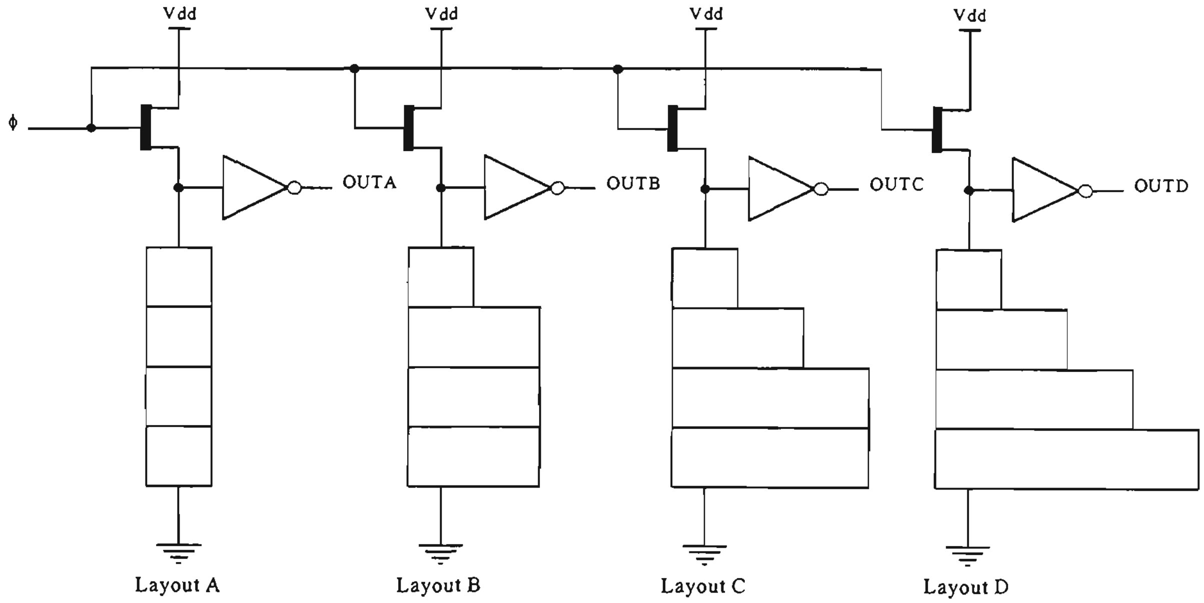


Figure 6.4(b) Domino scaling layouts A to D.

the E-MESFET chain. The HSPICE simulation results for the four layout are shown in Figures 6.5 where VIN1, VIN2, VIN3 and VIN4 represent the outputs of layout D, A, B and C respectively. The fall time for the four layouts are same because all the structures are in the precharge mode. During evaluation phase, the graded scaling of the E-MESFETs affects the rise time. The propagation delay for layout D is 0.4556 nanosec as compared with unscaled layout A of 0.996 nanosec.

6.2.1.1 Scaling Mechanism

When the size of E-MESFET1 is made smaller, two effects are seen: one tends to increase the delay, and the other tends to decrease the delay. First, the resistance of E-MESFET increases, and therefore the charge on the output node takes more time to be

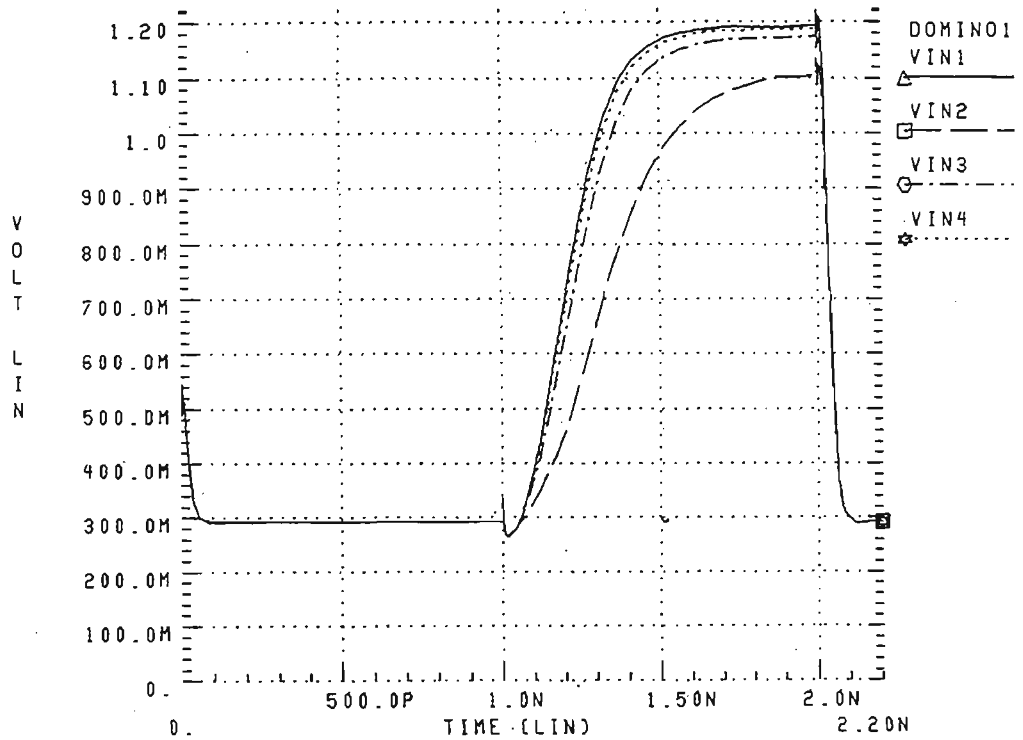


Figure 6.5 Simulation results for layouts A - D.
VIN1, VIN2, VIN3 and VIN4 represent the outputs of layout D, A, B and C respectively.

discharged to ground. This mechanism increases the delay. If the length of the E-MESFET chain is long, the increase in resistance of only one E-MESFET becomes less important, and therefore the effect becomes less significant. Second, the parasitic capacitance of E-MESFET1 decreases. Since the charge stored in the parasitic capacitance decreases, the delay time decreases as well. Since the charge drains through the summed resistance of E-MESFET1 - 4, the effect is more significant when the length of the E-MESFET chain is long. Since the first effect is minimised in a long E-MESFET chain while the second effect is maximised, it is expected that the second effect predominates if the E-MESFET chain is long, and that the delay time can be decreased by decreasing the size of E-MESFET1.

Table 6.1 Effect of scaling MESFETs on propagation delay

Layout	Propagation Delay
Device size - Buffer D-MESFET E-MESFET	 4 microns 12 microns
Precharge D-MESFET	4 microns
Layout A MESFET1 - 4 = 8 microns	0.996 nanosec
Layout B MESFET1 = 8 microns MESFET2 - 4 = 16 microns	0.5338 nanosec

Layout C
MESFET1 = 8 microns
MESFET2 = 16 microns
MESFET3 - 4 = 24 microns
	0.4738 nanosec

Layout D
MESFET1 = 8 microns
MESFET2 = 16 microns
MESFET3 = 24 microns
MESFET4 = 32 microns
	0.4556 nanosec

It is possible to get a deeper insight into the delay mechanism by studying the simple RC low-pass filter model, in which each MESFET is replaced by one link of the RC chain consisting of channel resistance and parasitic capacitance. Such a chain model is shown in Figure 6.6.

In the above model all the components are assumed to be linear devices having two terminals. All the resistances and capacitances of the RC chain except for the last link are lumped together into single component R_0 and C_0. R_l and C_l are the resistance and parasitic capacitance of the last link, and C_L is the load capacitance.

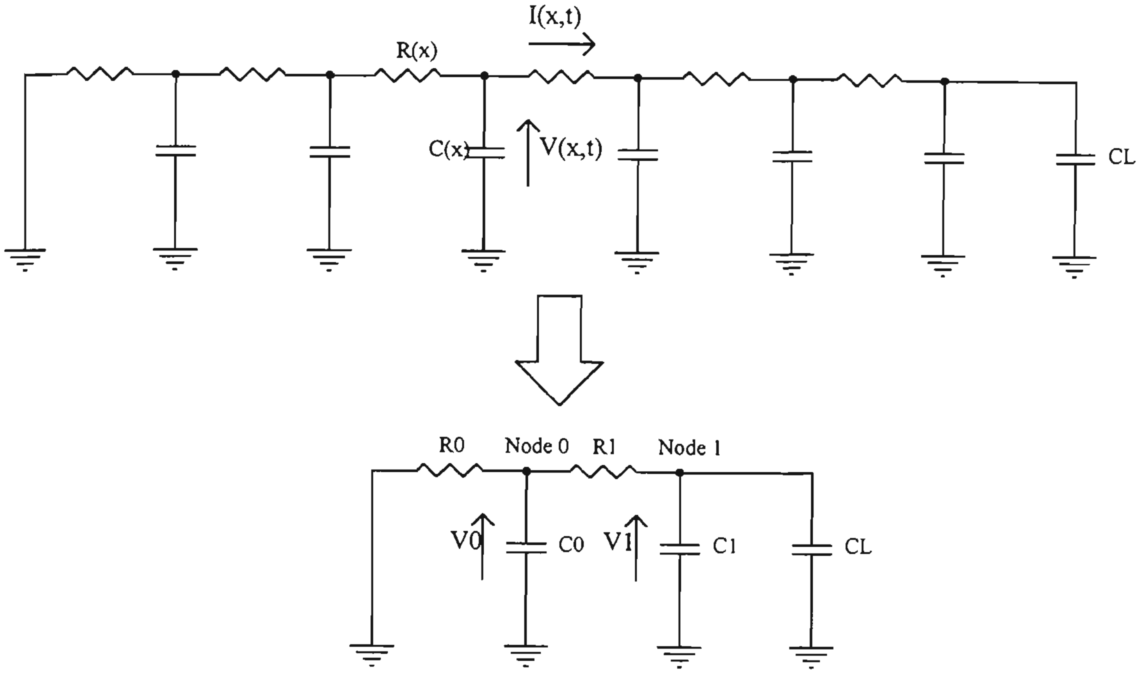


Figure 6.6 Equivalent circuit of a discharging domino chain.

Nodes 0 and 1 are originally charged to V_{dd}. The voltage on node 1 decays to $V_{dd}.e^{-1}$ = $0.36V_{dd}$ after time t_l, given that:

$$t_1 = R_0(C_0 + C_1 + C_L) + R_1(C_1 + C_L) \qquad \textbf{(6.0)}$$

When the size of a MESFET1 is increased by a fraction of Δk, in the equivalent circuit, C_l increases to $C_l(1 + \Delta k)$ and R_l decreases to $R_l/(1 + \Delta k)$. This changes the time t_l to:

$$t_1 = R_0(C_0 + C_1 + C_L) + R_1(C_1 + C_L) + R_0(C_1 - C_L.\frac{R_1}{R_0})\Delta k \qquad \textbf{(6.1)}$$

Then if C_L < $(R_0/R_l)C_l$, t_l decreases by decreasing size of E-MESFET1.

It can be concluded that it is advantageous to design a domino or multiple-output domino GaAs MESFET gates with large MESFETs, so that the loading of the output node is insignificant and the graded scaling technique is effective in the reduction of the delay time. This technique of scaling of MESFETs is particularly useful in very complex gate structures such as Carry Lookahead Generator in Carry Lookahead Adders.

6.2.2 Carry Lookahead Generator - Case Study One

6.2.2.1 Introduction

As the demand for higher performance VLSI processors with increased functionality grows, there is a continuing need to improve the performance, area efficiency and functionality of the arithmetic unit contained within them. Since high-speed arithmetic circuits predominantly use Carry Lookahead Adder (CLA) structures, one of the challenges in VLSI design is to structure multi-level CLA circuits without limiting the functional flexibility. Another more fundamental challenge is to explore circuits techniques which can exploit the performance of the CLA structure and yet minimise the inherent complexity involved. In this section, the design and performance of a carry generating circuit for a CLA is presented. The Carry Lookahead Generator (CLG) circuit was implemented with GaAs MESFETs using domino and multiple-output domino techniques and their relative performances are discussed.

6.2.2.2 Adder Structure

Figure 6.7 shows the structure of an eight-bit Carry Lookahead Adder. It consists of two types of basic units. The first is a four-bit unit which produces the propagate and generate terms (p_i and g_i) from the data a_i and b_i as well as the sum output S_i. The second unit produces the four-bit group propagate and generate terms (P_i and G_i) and all the carry bits (C_1 to C_4). The basic idea behind Carry Lookahead addition is to produce the carry signals directly from the inputs. The linear growth of adder carry-delay with the size of the input word for an n-bit adder can be improved by calculating the carries to each in parallel. The carry, C_i, and sum, S_i, for the i^{th} stage can be expressed as:

$$C_i = g_i + p_i C_{i-1} \qquad \textbf{(6.2)}$$

where $g_i = a_i b_i$

and $p_i = a_i \oplus b_i$

$$\begin{aligned} S_i &= a_i \oplus b_i \oplus C_{i-1} \qquad \textbf{(6.3)} \\ &= p_i \oplus C_{i-1} \end{aligned}$$

The signal $\mathbf{p_i}$ indicates that a carry will propagate through bit position ***i***. The signal $\mathbf{g_i}$ indicates that a carry is generated directly from the bits at position ***i***. The carry signals can be produced from the $\mathbf{p_i}$'s and $\mathbf{g_i}$'s as follows:

$$C_1 = C_0 p_0 + g_0 \qquad (6.4)$$

$$C_2 = C_0 p_0 p_1 + g_0 p_1 + g_1 \qquad (6.5)$$

$$C_3 = C_0 p_0 p_1 p_2 + g_0 p_1 p_2 + g_1 p_2 + g_2 \qquad (6.6)$$

$$C_4 = C_0 p_0 p_1 p_2 p_3 + g_0 p_1 p_2 p_3 + g_1 p_2 p_3 + g_2 p_3 + g_3 \qquad (6.7)$$

The size and fan in of the gates needed to implement this Carry Lookahead scheme can clearly become very complex. As a result, the number of stages of Carry Lookahead is usually limited to four. The four-bit Carry Lookahead Generator module produces the carry signals above and two additional signals group propagate, **P$_4$** and group generate, **G$_4$**. The group propagate and group generate signals are defined as follows:

$$P_4 = p_0 p_1 p_2 p_3 \qquad (6.8)$$

and $$G_4 = g_0 p_1 p_2 p_3 + g_1 p_2 p_3 + g_2 p_3 + g_3 \qquad (6.9)$$

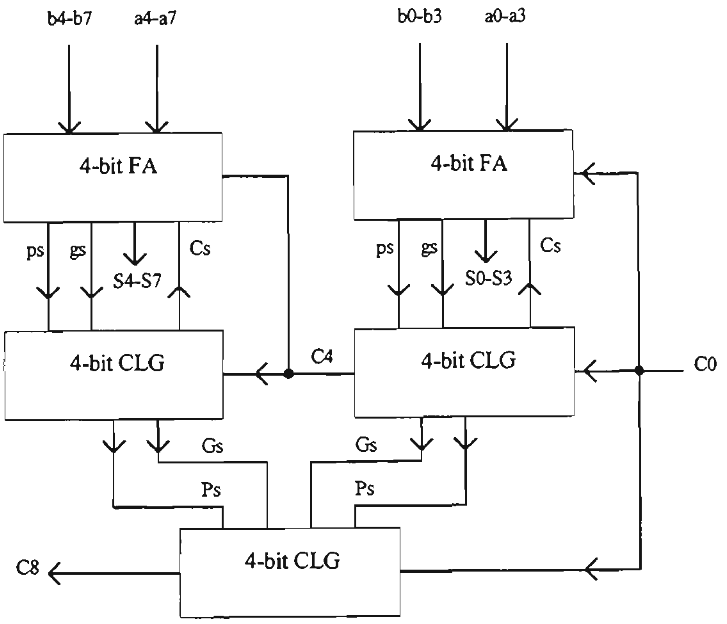


Figure 6.7 An eight-bit Carry Lookahead Adder structure.

6.2.2.3 Domino Implementation of the Carry Lookahead Generator

The carry signals, C_1 to C_4, of the Carry Lookahead Generator were implemented using dynamic domino logic as shown in Figure 6.8. The structure includes a logic tree and a static inverter for each output. As subsequent logic blocks are fed through this buffer, transistors in subsequent logic blocks will be turned off during the precharge phase. The output of the buffer is normally at logic low and during the evaluation phase it is conditionally charged to logic high.

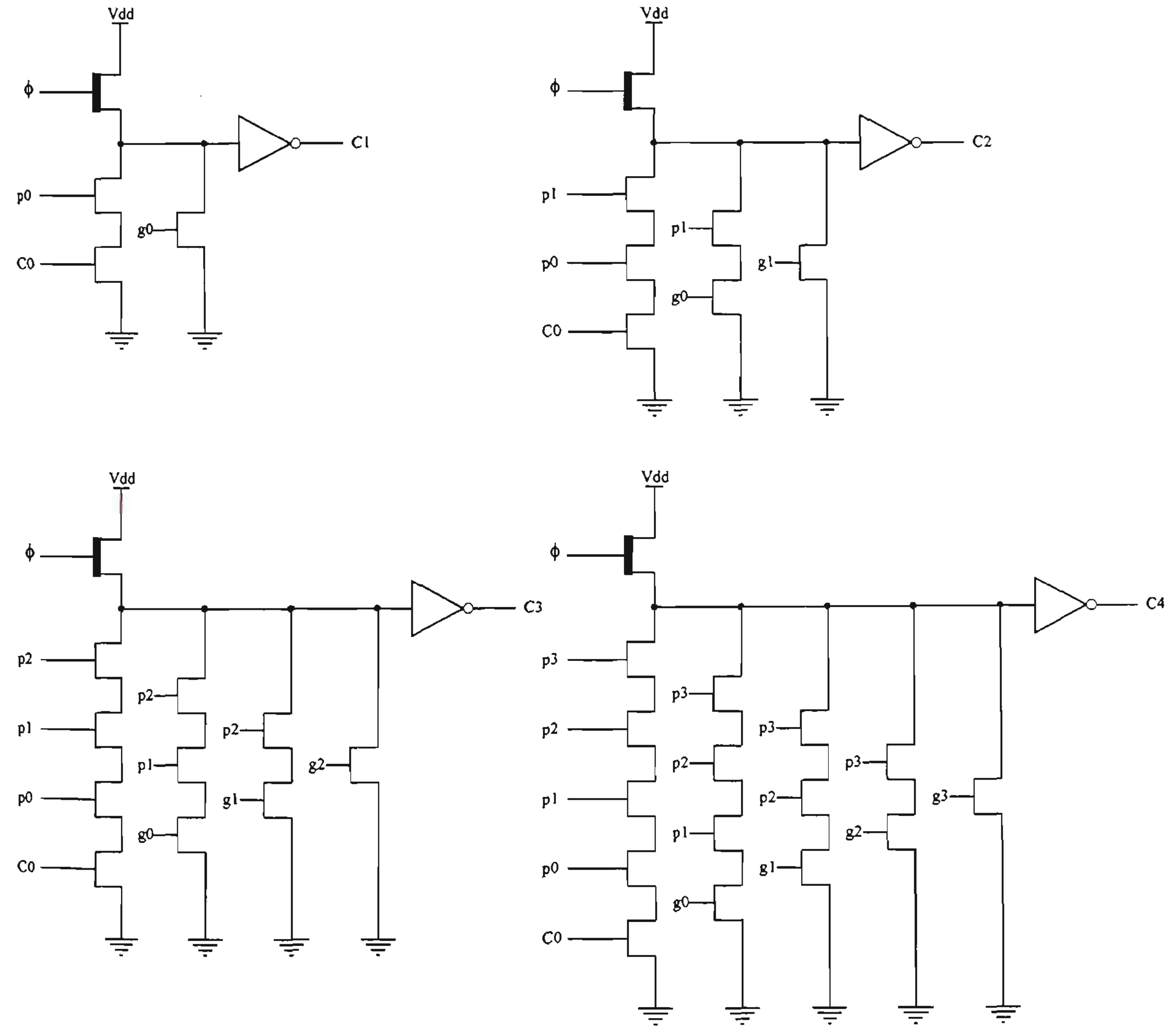


Figure 6.8 Domino implementation of carry signals of CLG.

Some limitations are evident from this structure. Firstly, only non-inverting outputs are possible and secondly, in common with all dynamic logic, charge distribution can be a problem. To overcome this problem additional precharge devices are added to the internal nodes of the logic tree so that these nodes are also charged during precharge phase, thus overcoming charge distribution problem. The structure is shown in Figure 6.9.

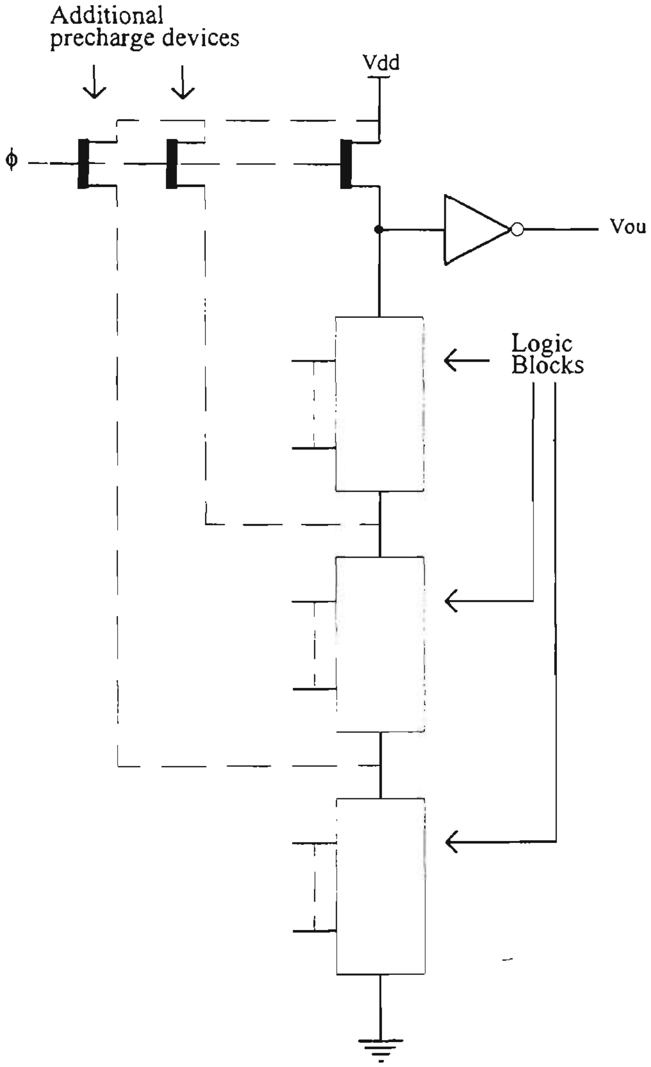


Figure 6.9 Domino chain with precharge devices.

6.2.2.4 Multiple-Output Domino Implementation of the Carry Lookahead Generator

The carry expressions have to be transformed to a form to enable it to be implemented using multiple-output domino technique. C_4 can be expressed as:

$$C_4 = ((((C_0 p_0 + g_0) p_1 + g_1) p_2 + g_2) p_3 + g_3) \qquad \textbf{(6.10)}$$

It can be readily seen that the first bracket defines C_1, the second bracket defines C_2, the third bracket defines C_3 and the fourth bracket defines $C_{4.}$ It is also important to note that C_1 is a sub-function of C_2, C_1 and C_2 are the sub-functions of C_3 and C_1, C_2 and C_3 are the sub-functions of $C_{4.}$ Since the overall saving in device count is due to a reduction of replication of the sub-functions, the actual advantage of this technique over domino logic is directly dependent on the degree of recurrence of the logic functions being realised. For the carry generating circuit, the expression for C_4 is highly recurrent and is most suitable for multiple-output domino implementation. The intermediate outputs for C_1, C_2 and C_3 are obtained by adding precharge devices and static inverters at the corresponding intermediate nodes of the logic tree. Figure 6.10 shows the carry generating circuit implemented in multiple-output domino technique.

6.2.2.5 Layout and Performance

The four-bit Carry Lookahead Generator was designed using standard domino and multiple-output domino techniques and implemented using ISD VLSI design suite with gate lengths of 0.8 micron. The layout methodology had significant influence upon the performance of the circuit. Positioning of power and ground busses have significant influence upon the performance of two circuits. For example, fast transitions on signal bus could bring about significant noise on the power bus. Thus, both the design methodology and layout will have to address the influence of coupling between busses on performance. The power and ground busses were placed adjacent to one another so as to reduce their self inductance, and hence their susceptibility to current transients.

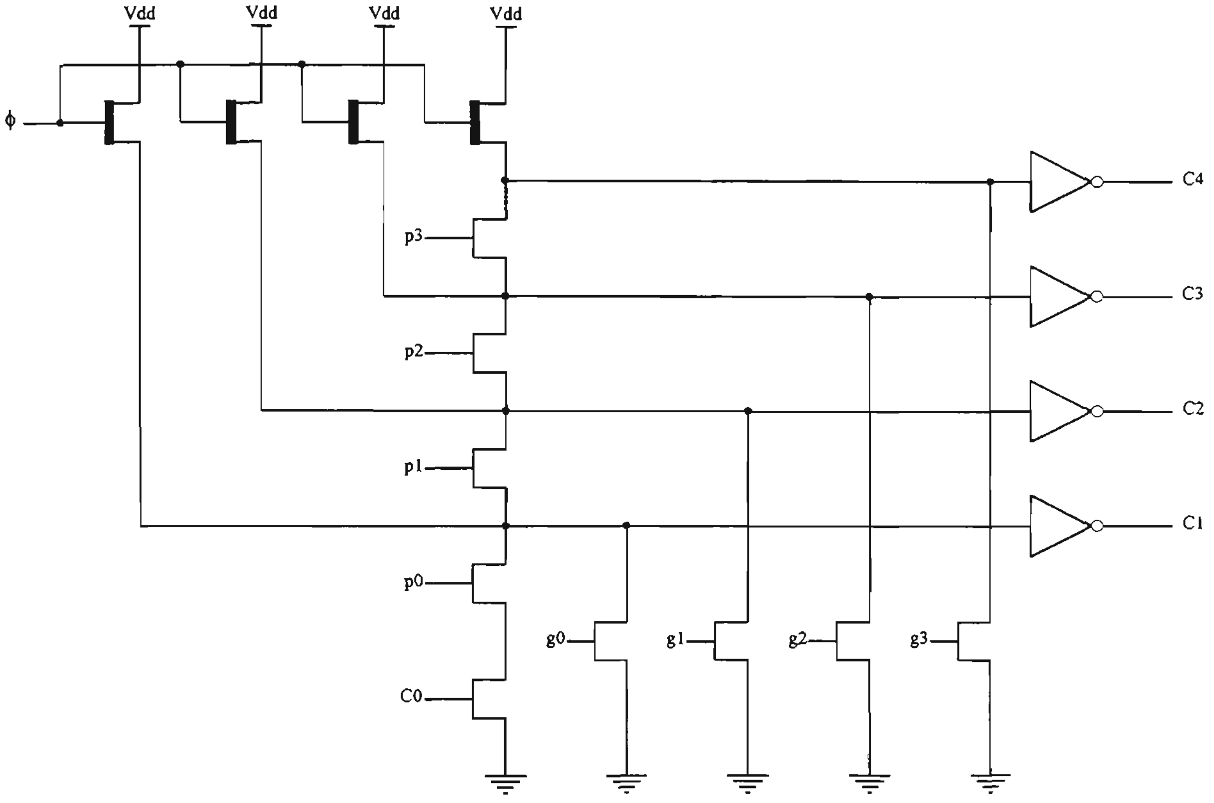


Figure 6.10 CLG circuit implemented in multiple-output domino technique.

The above circuits have been analysed and evaluated using GaAs net extractor and HSPICE circuit simulation tools. The simulation results indicate a power dissipation of 9.444 milliwatts for a standard domino implementation and 6.044 milliwatts for multiple output domino circuit. The decrease in power dissipation is directly attributed to decrease in the number of devices needed to implement the CLG in multiple-output domino technique. The average propagation delay for circuit implemented using domino technique is 0.1 nanosec whereas for the circuit implemented using multiple output domino technique is 0.13 nanosec. The most remarkable achievement using multiple-output domino technique is the reduction in the number of devices required to implement the CLG. This technique only requires 21 devices to implement four-bit, CLG whereas 46 devices are required for domino implementation of the same circuit. The HSPICE results for the CLG using the two design techniques are summarised in Table 6.2.

The simulation results for the four-bit, CLG using domino and multiple-output domino techniques are shown in Figures 6.11 and Figure 6.12 respectively. VIN1, VIN2, VIN3, VIN4 and VIN5 represent C_0, C_1, C_2, C_3 and C_4 respectively. The power waveforms illustrates the power dissipated by the four-bit, CLG implemented using the two techniques.

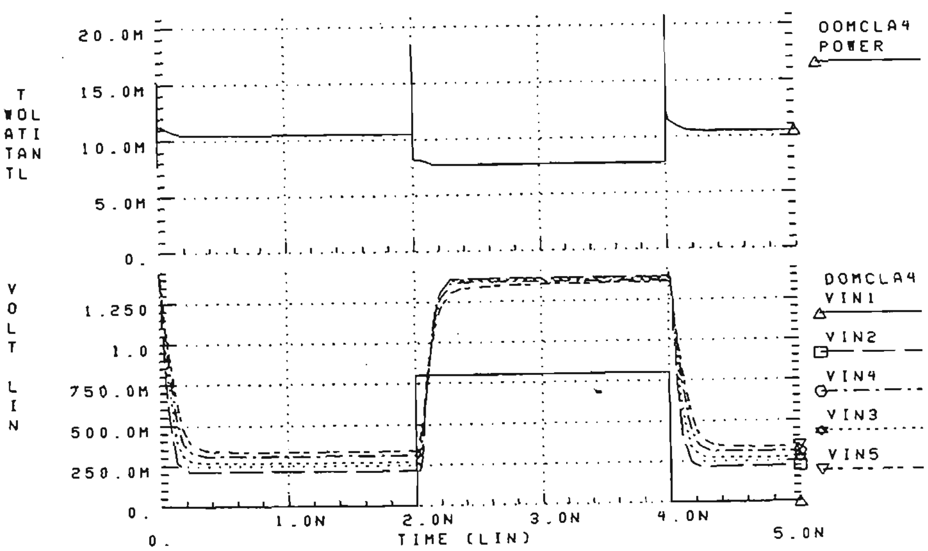


Figure 6.11 Performance of a 4-bit CLG implemented in domino technique.

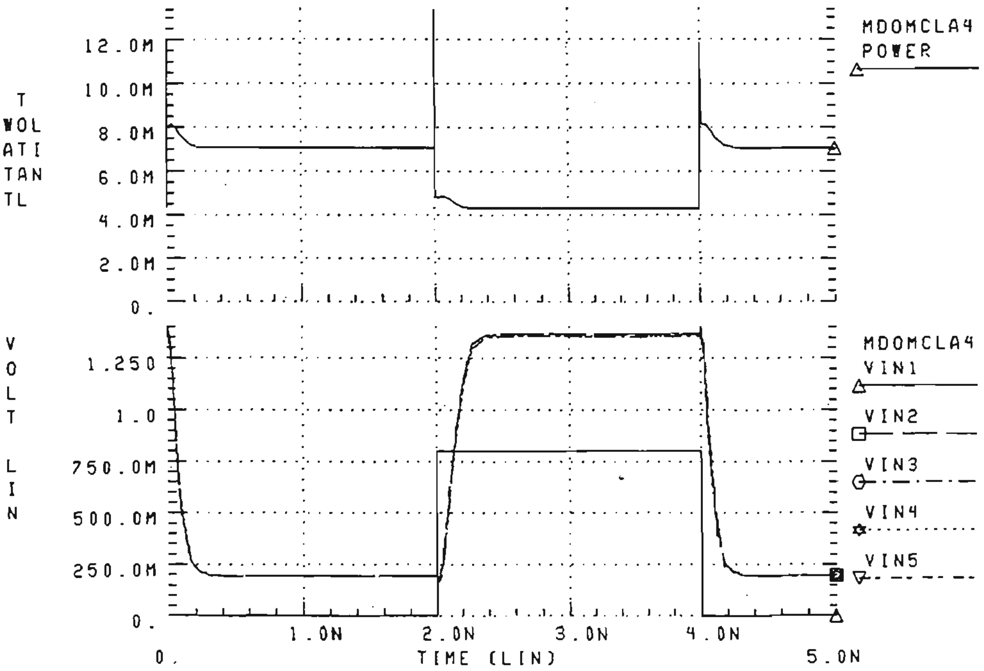


Figure 6.12 Performance of a 4-bit CLG implemented in multiple-output domino technique.

6.2.3 Conclusions - Part I

The principle behind multiple-output domino technique is to utilise the sub-functions available in the logic tree of the domino gates. Multiple outputs are available by adding precharge devices at the corresponding intermediate nodes in the logic tree. Since nodes, internal to the logic tree, are being precharged for functional purposes, multiple-output domino logic is considerably less susceptive to charge sharing than domino logic. Because the saving in the circuit area is mainly due to a reduction of replication of sub-circuits, the actual advantage of this design technique over domino logic design technique is directly dependent upon the number of recurrence in a logic function being realised.

Table 6.2 Performance comparison for four-bit Carry Lookahead Generator using domino and multiple-output domino techniques

Description	Domino Technique	Multiple-Output Domino technique
Number of devices	46	21
E-MESFET	38	13
D-MESFET	8	8
Gate length	0.8 micron	0.8 micron
Propagation delay		
C_1	0.1006 nsec	0.1336 nsec
C_2	0.1012 nsec	0.1338 nsec
C_3	0.1021 nsec	0.1366 nsec
C_4	0.1029 nsec	0.1398 nsec
Rise time		
C_1	0.1298 nsec	0.1779 nsec
C_2	0.1382 nsec	0.1958 nsec
C_3	0.1592 nsec	0.1972 nsec
C_4	0.2171 nsec	0.1924 nsec
Fall Time		
C_1	0.0807 nsec	0.1032 nsec
C_2	0.1172 nsec	0.1040 nsec
C_3	0.1618 nsec	0.1019 nsec
C_4	0.2174 nsec	0.0941 nsec
Power dissipation	9.444 mW	6.044 mW

The improvement in performance is due to a reduction of load capacitance for a given logic stage. This results from less overall device count and less parasitic wiring capacitance as a consequence of a smaller overall layout. This also leads to lower power consumption. The performance of multiple-output domino is further improved by graded scaling of the MESFETs in the logic tree.

The performance advantage of this design technique over dynamic domino technique has been demonstrated via the implementation of a four-bit CLG for a Carry Lookahead Adder. The multiple-output domino technique demonstrates increased circuit performance, reduced circuit area and power dissipation when compared with the domino technique. This is due to the reduction in the parasitic capacitance and output loading. The most remarkable achievement using this technique is the reduction in the number of devices required to implement the CLG.

Part II Static Design Technique

6.3 Merged Logic Design Technique

Static VLSI circuits are usually designed using one of the normally-off techniques described in Chapter 4, namely, DCFL, SDCFL or SFFL techniques. DCFL design technique is simplest and fastest of the static logic classes, but it suffers from several shortcomings. The most noticeable being the degradation of logic voltage swing with increasing fan out and very low noise margin (100 mV) [115]. This is due to the output voltage being limited by the barrier height of the MESFETs' Schottky diode at the input of the next DCFL stage (650 mV). Other limitations include the sensitivity of the gate delay to fan in, fan out and load capacitance, and the small temperature stability margin of the basic gate [106].

SDCFL design technique, as the name implies, consists of a DCFL stage and a source-follower buffer. The voltage levels at the input and the output are DCFL compatible. In contrast, the SFFL design approach precedes the DCFL stage with a source follower as a buffer at the input.

The Merged logic approach[1] to circuit design combines direct coupled MESFET logic (DCFL) with source follower DCFL (SDCFL) and source follower MESFET logic (SFFL) so that the advantages of each logic class are exploited and circuit performance

[1] This work was carried out in collaboration with the researchers at the Centre for GaAs VLSI Technology.

is achieved which is superior to that obtained from different design approaches. In the Merged logic static design approach, shown in Figure 6.13, DCFL is predominantly used to achieve higher packing density and improved circuit performance [116]. SDCFL technique is used to drive large capacitive loads and realise the And-Or-Invert (A-O-I) functions while SFFL is used to implement large fan out. In this way significant performance improvement can be achieved. The performance of different logic classes have been evaluated in terms of noise margin, power dissipation, fan in, fan out and average transition times and are summarised in Table 6.3.

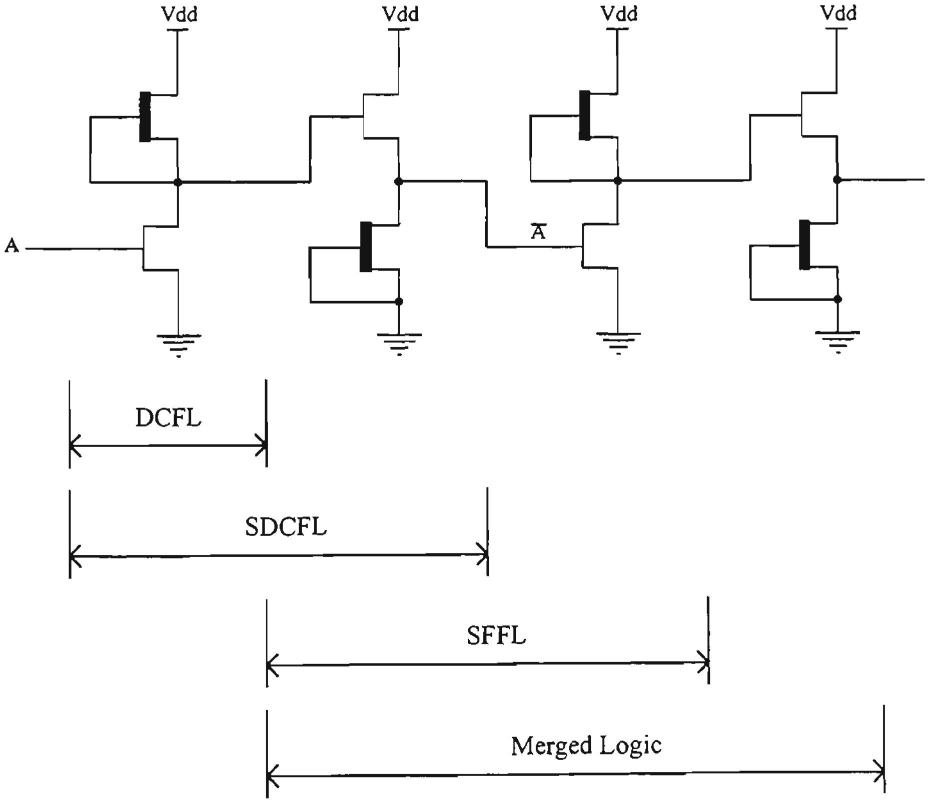


Figure 6.13 Merged Logic Design Approach.

It is evident from the results that with increasing fan out the performance of DCFL circuit is degraded. This is due to the reduced ability of the D-MESFET to drive the E-MESFET of the fan out load.

Table 6.3 Performance of optimal DCFL, SDCFL and SFFL inverters

Description	Logic Classes		
	DCFL	SDCFL	SFFL
Power (μWatts)			
Fan out = 1	200	590	650
Fan out = 3	220	600	660
Noise Margin (milliVolts)			
Fan out = 1	100	200	350
Fan out = 3	80	150	300
V_{HIGH} (milliVolts)			
Fan out = 1	650	700	750
Fan out = 3	600	650	610
V_{LOW} (milliVolts)			
Fan out = 1	100	20	100
Fan out = 3	120	100	100
t_{phl} (picosec)			
Fan out = 1	70	90	80
Fan out = 3	150	160	120
t_{plh} (picosec)			
Fan out = 1	30	70	80
Fan out = 3	70	170	110

V_{HIGH} and V_{LOW} are the output high and low voltages respectively, and t_{phl} and t_{plh} are the propagation delays high-to-low and low-to-high respectively.

The fan in capability of the DCFL is restricted by the drain to source leakage current of the E-MESFET, which when multiplied by the fan in, reduces V_{HIGH}. The SDCFL demonstrates its ability to drive capacitive load significantly faster than DCFL as highlighted in Figure 6.14. The fan out of SDCFL is limited by the ability of the D MESFET of the source follower to discharge the gate capacitance of the following stages, which can be significant. The SFFL class of logic has the ability to drive large fan out. Figure 6.15 shows the fan out performance of SFFL inverter. SDCFL and SFFL circuits dissipates more power than the DCFL circuit. This is because of the larger number of devices required to implement these circuits.

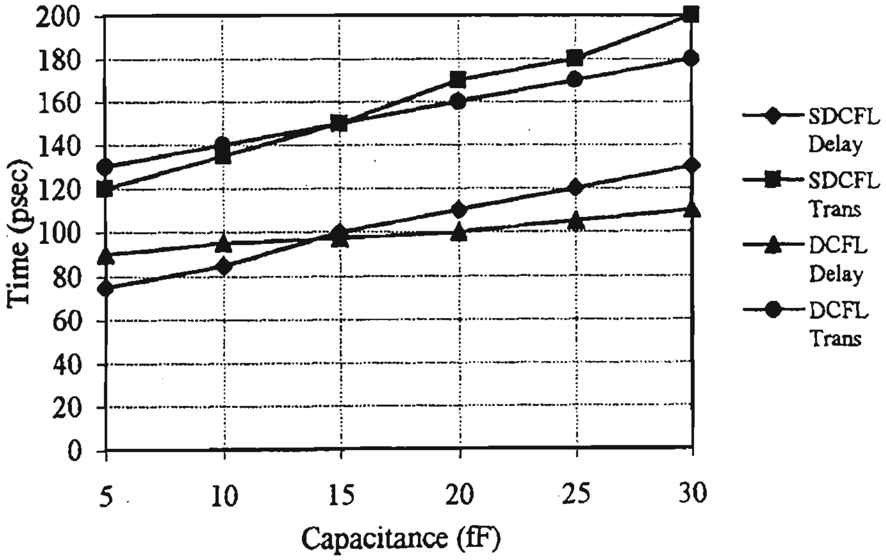


Figure 6.14 Capacitive load performance of SDCFL inverter.

The Merged logic approach to circuit design is the natural progression from comparative studies of DCFL, SDCFL and SFFL circuits. This approach involves identifying critical parts of the circuit where SDCFL and SFFL techniques can be used to improve circuit performance, such as using SDCFL stage to drive large capacitive loads and SFFL stage to implement large fan out.

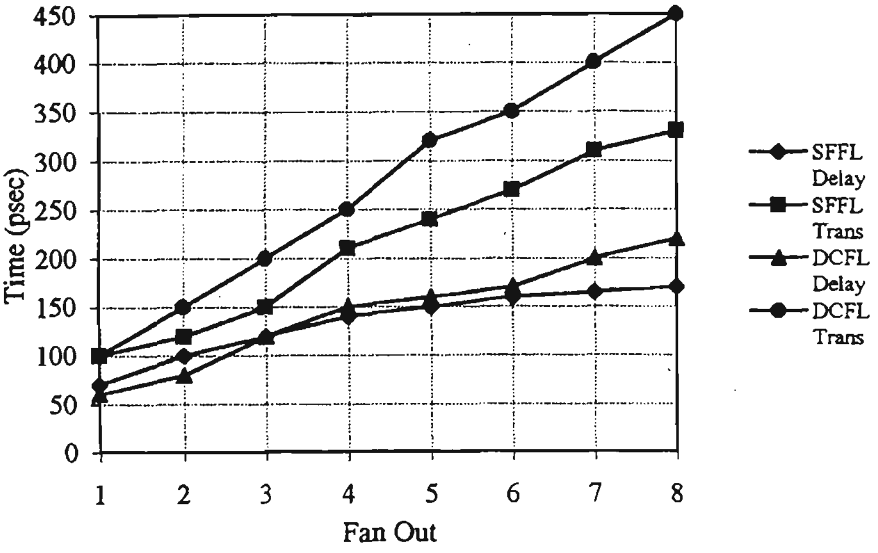


Figure 6.15 Fan out performance of SFFL inverter.

6.3.1 Power Series Evaluator - Case Study Two[2]

6.3.1.1 Introduction

In real time signal processing, there often exists a need for a very fast signal evaluators. A power series evaluator is an example of a type of processing element (PE) that performs a reasonably complex function. Although the architecture decided for the implementation of this particular power series evaluator is by no means the only approach, however, it works reliably and with minimum chip area. An important aspect of the design methodology is the need for both top-down and bottom-up approaches. Top-down design approach is necessary to allow the behavioural description to be realised correctly and the bottom-up design approach is needed to ensure that the

[2] This work was carried out in collaboration with the researchers at the Centre for GaAs VLSI Technology.

design algorithm chosen to implement the processing element is such that it can be readily mapped into GaAs, and furthermore, is consistent with the accepted design principles and limitations of the technology.

Merged logic design approach was chosen for the implementation of the power series evaluator. The choice is based upon the favourable properties of this design technique, namely, high noise margins, good temperature stability and good fan in and fan out capabilities.

6.3.1.2 Behavioural Model

The general representation of an ***n*** order polynomial is given by:

$$y(x) = a_n x^n + a_{n-1} x^{n-1} + \ldots + a_1 x + a_0 \qquad \textbf{(6.11)}$$

To evaluate this polynomial it is necessary to transform it into a bit-serial form so that it can be mapped into GaAs technology. The general form of a polynomial can be rewritten as [115]:

$$y(x) = ((..(a_n x + a_{n-1})x + a_{n-2})..)..)x + a_0 \qquad \textbf{(6.12)}$$

To evaluate points on the curve, it is necessary to perform ***n*** multiplications and ***n*** additions. Implementing multiplication algorithm consumes a large amount of substrate area and thus leads to excessive power dissipation and high fabrication costs. However, by examining the polynomial, it is possible to transform it into a form in which the only operation necessary for the evaluation of any point on the curve is found by the application of a recursive addition process. The decomposition of a polynomial into a recursive structure can be expressed in the Taylor's series form as:

$$y(x_0+h)=y(x_0)+hy'(x_0)+(\frac{h^2}{2!})y''(x_0)+\ldots+(\frac{h^n}{n!})y^n(x_0) \qquad \textbf{(6.13)}$$

where x_0 is a value of x for which the derivatives $y',y'',\ldots y^n$ exist, and $h=(x-x_0)$

Equation 6.13 can be rewritten as:

$$y(x_0+h)=y(x_0)+d_1(x_0) \qquad \textbf{(6.14)}$$

where $$d_1(x_0)=hy'(x_0)+(\frac{h^2}{2!})y''(x_0)+\ldots+(\frac{h^n}{n!})y^n(x_0) \qquad \textbf{(6.15)}$$

The polynomial is reduced to a recursive set options by iteration of this process as:

$$d_1(x_0+h)=d_1(x_0)+hd_1'(x_0)+(\frac{h^2}{2!})d_1''(x_0)+\ldots+(\frac{h^n}{n!})d_1^n(x_0) \qquad \textbf{(6.16)}$$

$$d_1(x_0+h)=d_1(x_0)+d_2(x_0) \qquad \textbf{(6.17)}$$

where $$d_2(x_0)=hd_1'(x_0)+(\frac{h^2}{2!})d_1''(x_0)+\ldots+(\frac{h^n}{n!})d_1^n(x_0) \qquad \textbf{(6.18)}$$

The process can be continued until the first derivative is zero. The polynomial can be rewritten in the new form, as:

$$y(x_{i+1})=y(x_i)+d_1(x_i) \qquad \textbf{(6.19)}$$

$$d_1(x_{i+1}) = d_1(x_i) + d_2(x_i) \qquad (6.20)$$

$$d_2(x_{i+1}) = d_2(x_i) + d_3(x_i) \qquad (6.21)$$

$$\cdot$$

$$d_{n-1}(x_{i+1}) = d_{n-1}(x_i) + d_n(x_i) \qquad (6.22)$$

$$d_n(x_{i+1}) = d_n(x_i) \qquad (6.23)$$

where $x_{i+1} = x_i + h$

From the transformed expression it can be seen that the processing element can calculate any point on the curve from the initial starting point y(x$_i$), using the step size, h, with application of a recursive addition process on the individual bits of both the initial point and a set of previously calculated coefficients, d$_1$, d$_2$, ... , d$_n$. Figure 6.16 shows the logical architecture in the mapping process.

The required functional blocks to realise the algorithm are simply adders and registers. The adders perform the calculations and the registers initially store the coefficients, and then store intermediate values as each block is clocked during the execution cycle.

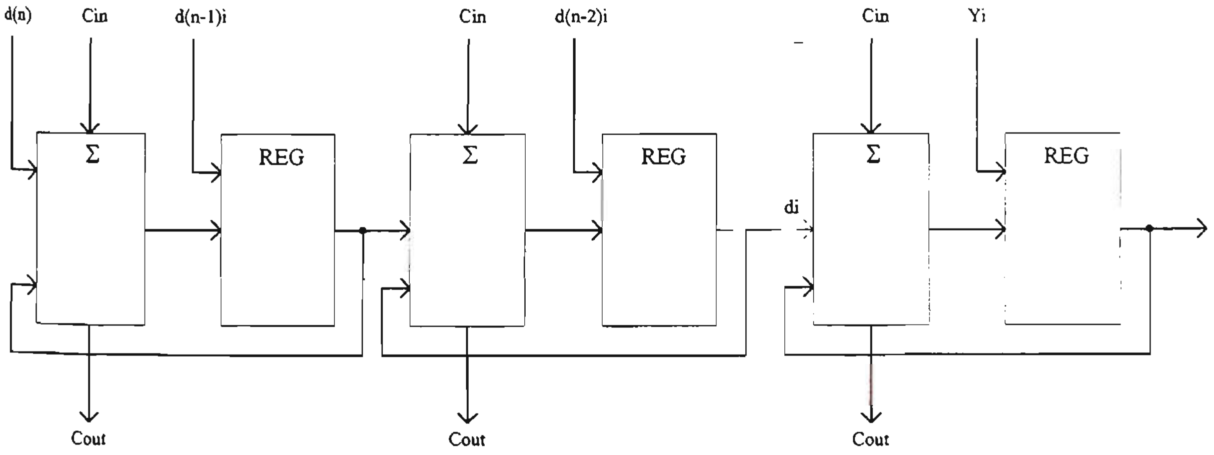


Figure 6.16 Block diagram of a bit-serial power series evaluator [115].

6.3.1.3 Physical Description

A single PE cell is shown in Figure 6.17. It consists of an adder, a register and two-to-one multiplexer connected in such a way so that the input to the register is selectable between the A input to the adder, and the S output of the adder. A single PE cell can be cascaded horizontally to increase the order of the polynomial, **n**, and cascaded vertically and pipelined to increase the bit size. The initial starting point coefficient are loaded into the system and stored in the registers. This is achieved by the inclusion of a two-to-one multiplexer, so that when coefficients are being loaded into the system, the adders are by-passed and no execution takes place. With the addition of this requirement the system has two modes of operation, namely, Load and Execute. Depending on the state of the control input, L_d, either

(a) the system passes constant values through the register (register input equals A, the input of the adder), i.e loading the data coefficients, or

(b) the system executes an evaluation cycle and produces a result (register input equals S, the output of the adder).

The Q output of the register is connected to the B input of the adder, to realise the feedback path and hence the recursive property of the cell.

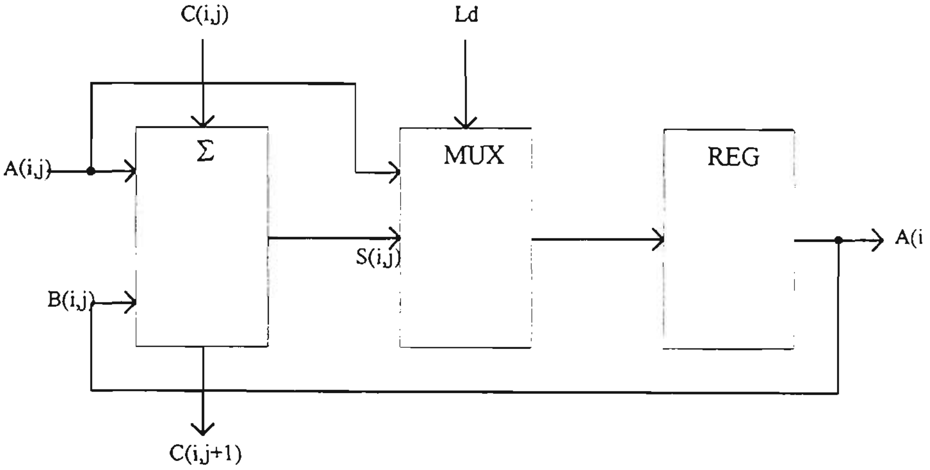


Figure 6.17 Processing element cell structure.

6.3.1.4 Adder

Addition is the most common arithmetic operation performed by any digital signal processing system. Since the class of logic that has been decided upon for the implementation of the circuit is the Merged GaAs logic, it is necessary to transform the expressions for sum and carry into a form which contains only OR and NOR gates. The following expressions describe the sum and carry for the adder:

$$Sum = \overline{\overline{(A+B+\overline{C})}+\overline{(A+\overline{B}+C)}+\overline{(\overline{A}+B+C)}+\overline{(\overline{A}+\overline{B}+\overline{C})}} \qquad \textbf{(6.24)}$$

$$Carry = \overline{\overline{(\overline{A}+\overline{B})}+\overline{(\overline{A}+\overline{C})}+\overline{(\overline{B}+\overline{C})}} \qquad \textbf{(6.25)}$$

Figures 6.18 shows the logical representation of the single-bit adder cell. Appendix F presents the design of a single-bit adder cell.

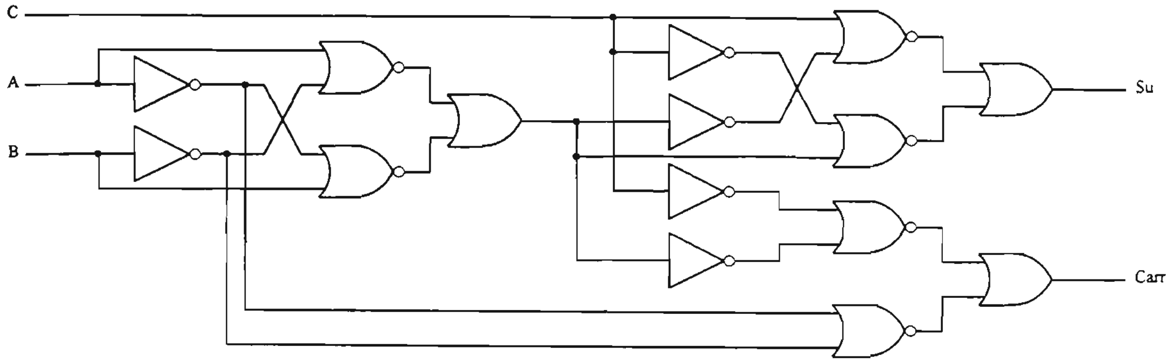


Figure 6.18 Logical representation of a single-bit adder cell.

6.3.1.5 Edge-Triggered Register

Edge-triggered registers are designed so that they only change their states based on input conditions at either the rising or the falling edge of the clock. The rising of the clock triggers a positive edge-triggered register and the trailing edge of the clock triggers the negative edge triggered register. Any change in the input values after the occurrence of the triggering edge will not bring about a state transition of these registers until the next triggering edge.

The register structure chosen for the processing element is, by necessity, an edge-triggered device. The data at the inputs would be changing while the data at the output is still needed for the next cell to the right. Therefore, transparent latches cannot realise this property without placing severe constraints on the clocking strategy. Figure 6.19 shows the negative edge-triggered register built out of six cross-coupled NOR gates. This structure is suitable for the implementation of the register by the GaAs Merged logic design technique. As can be seen from the timing diagram in Figure 6.20, after the trailing edge of the clock pulse, either W or Z becomes one. Note that the total time required for the output transition to occur is three gate delays after the trailing edge of the clock.

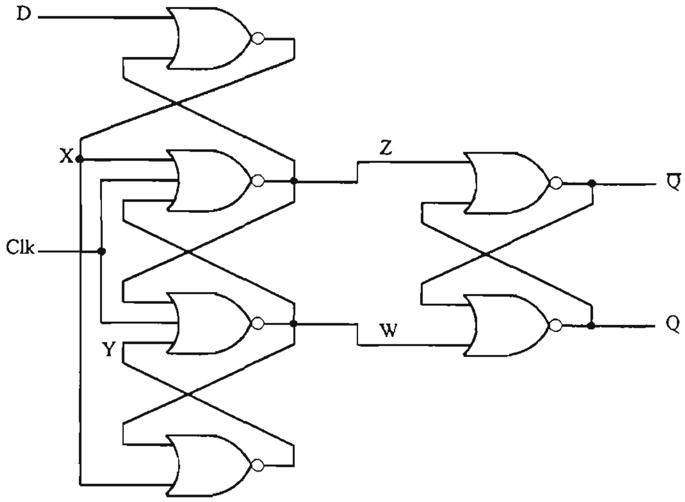


Figure 6.19 Negative-edge triggered register cell.

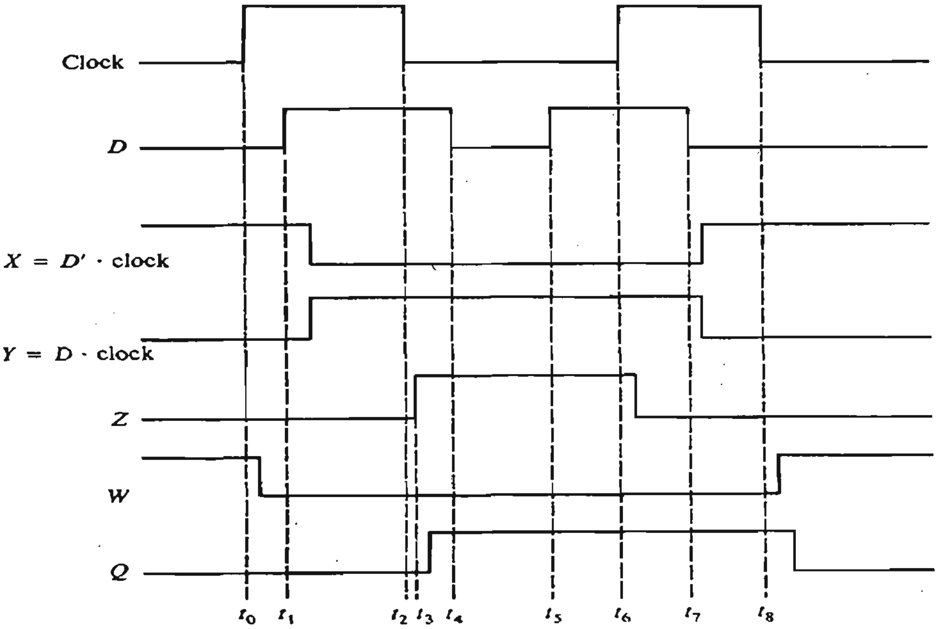


Figure 6.20 Timing diagram for the negative edge-triggered register cell.

6.3.1.6 Multiplexer

Multiplexing is the process of channelling information from one of several sources to a single destination. A multiplexer (selector) is thus a switch connecting one of its several inputs to the output. A set of **n** control inputs are needed to select one of the 2^n inputs. A two input multiplexer is shown in Figure 6.21.

The operation of the multiplexer can be described by the following expression:

$$Output = \overline{(\overline{L_d} + \overline{I_1})} + \overline{(L_d + \overline{I_2})} \qquad \textbf{(6.26)}$$

Each of the inputs I_1 and I_2 and the output in the multiplexer circuit is a single line. If the application requires that the data lines to be multiplexed have more than one bit each, the circuit shown in Figure 6.22 must be repeatedly duplicated, one per each bit of the data.

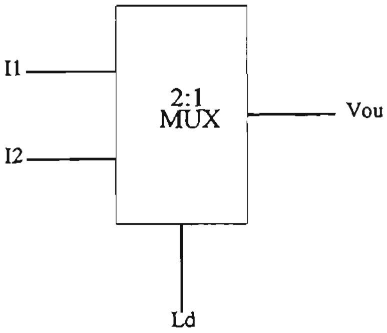


Figure 6.21 Two-to-one multiplexer.

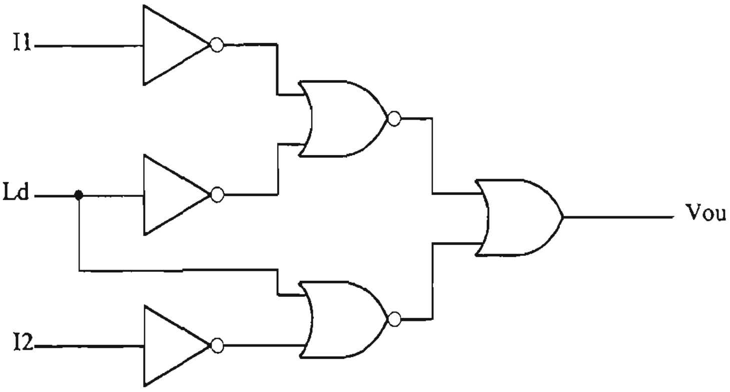


Figure 6.22 Logical representation of a 2-to-1 multiplexer.

6.3.1.7 VLSI Layout

Each single-bit power series evaluator cell, containing an adder, register and multiplexer, was designed using Merged GaAs logic design technique. The cell was implemented using Integrated Silicon Design VLSI design suite. The individual cells were designed using the ring notation approach [106]. The flow plan for the implementation of the single-bit evaluator is shown in Figure 6.23. It encompasses all the necessary design criteria, including placement of the input and output signals so the cell can be assembled with minimum length routing paths between cells. The logical representation of the cell is shown in Figure 6.24.

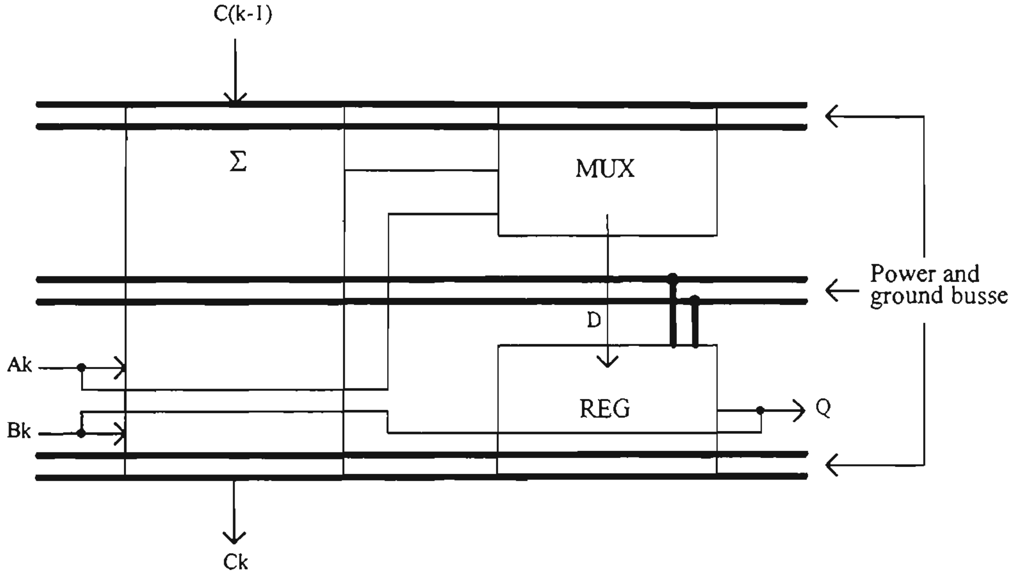


Figure 6.23 Floor plan of the power series evaluator cell.

The placement of power and ground busses adjacent to each other reduces their self inductance, and hence their susceptibility to current transients. From the results of coplanar strip line and coplanar waveguide models, the inductance of the power busses is reduced by a factor of two to three when the supply rails are placed in the proximity of one another [106].

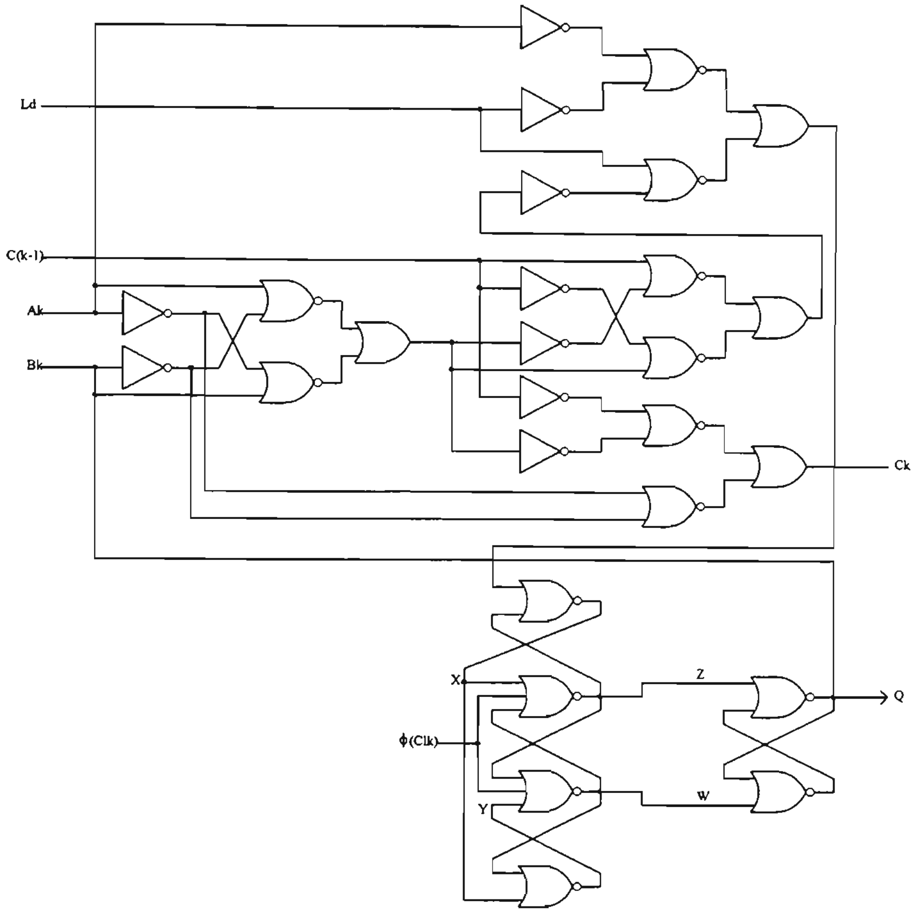


Figure 6.24 Logical representation of power series evaluator cell.

In the layout, the adder occupied seven rows of gates, register occupied four rows and the multiplexer occupied two rows with a total of 127 GaAs MESFET depletion and enhancement type devices. In the layout of the power series evaluator cell arrangement, shown in Figure 6.25, the clock, inputs and outputs, and the control signals are separated from the ground and power supply rails. This is due the high level of crosstalk and capacitive effects which introduce noise into the supply rails when there are high speed switching transients on signal lines in the proximity of the supply rails.

6.3.1.8 Simulation and Performance

The individual functional cells were analysed and evaluated using GaAs Net Extractor and HSPICE circuit simulation tools. The simulations results are summarised in Table 6.4.

The HSPICE simulation results obtained using HSPLOT for adder, register and two-to-one multiplexer are presented in Appendix F. From the results it can be seen that this design approach gives large logic level swings resulting in excellent noise margins. This design approach also allows large fan out.

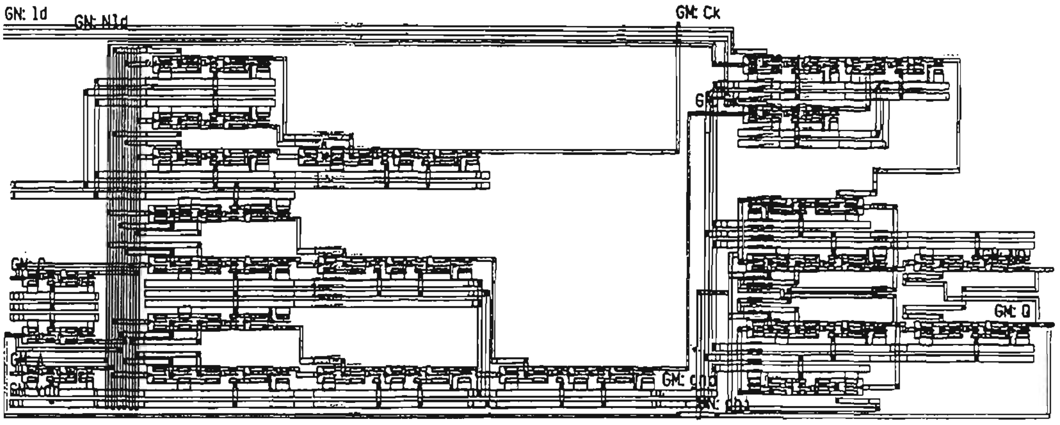


Figure 6.25 VLSI layout of a power series evaluator cell.

The performance of a single power series evaluator cell is summarised in Table 6.5 and the simulation results are presented in Figure 6.26, where VIN1, VIN2, VIN4, VIN5, VIN7 and VIN8 represent the data input A, multiplexer (ld) control, clock, Q, Sum and Carry outputs respectively. The propagation delay for each cell in the horizontal manner is 1.48 nanoseconds. In the vertical direction it is necessary to examine the propagation delay of the carry signal. Since during each evaluation cycle the data is moved from one cell to its intermediate right neighbour, the horizontal delay is independent of the polynomial order whereas the vertical delay depends upon the entire bit-depth of the array. The carry signal must propagate through the entire bit-depth of the array and allow the adder output data to settle in the most significant bit

Table 6.4 Performance of adder, register and multiplexer

Description	Adder	Register	Multiplexer
No. of Devices	80	32	15
E-MESFET	48	20	9
D-MESFET	32	12	6
Gate Length	0.8 micron	0.8 micron	0.8 micron
Propagation delay			
Sum	0.8787 nanosec		
Carry	0.5635 nanosec		
Q		0.4227 nanosec	
Out			0.1808 nanosec
Rise Time			
Sum	0.3114 nanosec		
Carry	0.3117 nanosec		
Q		0.2106 nanosec	
Out			0.1495 nanosec
Fall Time			
Sum	0.1113 nanosec		
Carry	0.1315 nanosec		
Q		0.2162 nanosec	
Out			0.1366 nanosec
Power Dissipation	12.19 milliWatts	5.362 milliWatts	2.229 milliWatts
Noise Margin	0.37 Volts	0.35 Volts	0.35 Volts
Fan out	3	3	3

Table 6.5 Performance of a single bit power series evaluator

Description	Power Series Evaluator
No. of Devices	127
E-MESFET	77
D-MESFET	50
Gate Length	0.8 micron
Propagation delay	
Q (load)	0.6035 nanosec
Q (execute)	1.4822 nanosec
Carry	0.5635 nanosec
Rise Time	
Q	0.2482 nanosec
Carry	0.3357 nanosec
Fall Time	
Q	0.5291 nanosec
Carry	0.2011 nanosec
Power Dissipation	17.71 milliWatts
Fan-out	3
Noise Margin	0.36 Volts
Max. Clock Freq.	1.8 GHz.

(MSB) cell before the MSB cell can be clocked. From the results the carry delay for single cell is 0.5635 nanosec. Therefore, the MSB can only be clocked after ***(n-1)*** times this delay plus the horizontal delay of the cell for a ***n***-bit deep array. As the bit depth increases the horizontal delay contributes relatively less to the overall delay. For large ***n***, this figure can be high resulting in very slow clocking speed.

One possible solution to overcome the time complexity of the array being proportional to the bit depth is to replace the ripple through carry adder with a Carry Lookahead Adder structure. This will greatly reduce the carry propagation delay thus improving the clocking frequency. The data load cycle will have considerably less delay since no carry signal is required and furthermore, the adder is bypassed resulting in very fast load cycle as compared with execution cycle. The maximum clock frequency of a single bit cell during the load cycle is 1.66 GHz and during the execution cycle is 676 MHz. The single bit power series evaluator cell dissipates 17.71 milliWatts of power. The circuit has a large voltage swing resulting in very good noise margin and also can drive large fan-out.

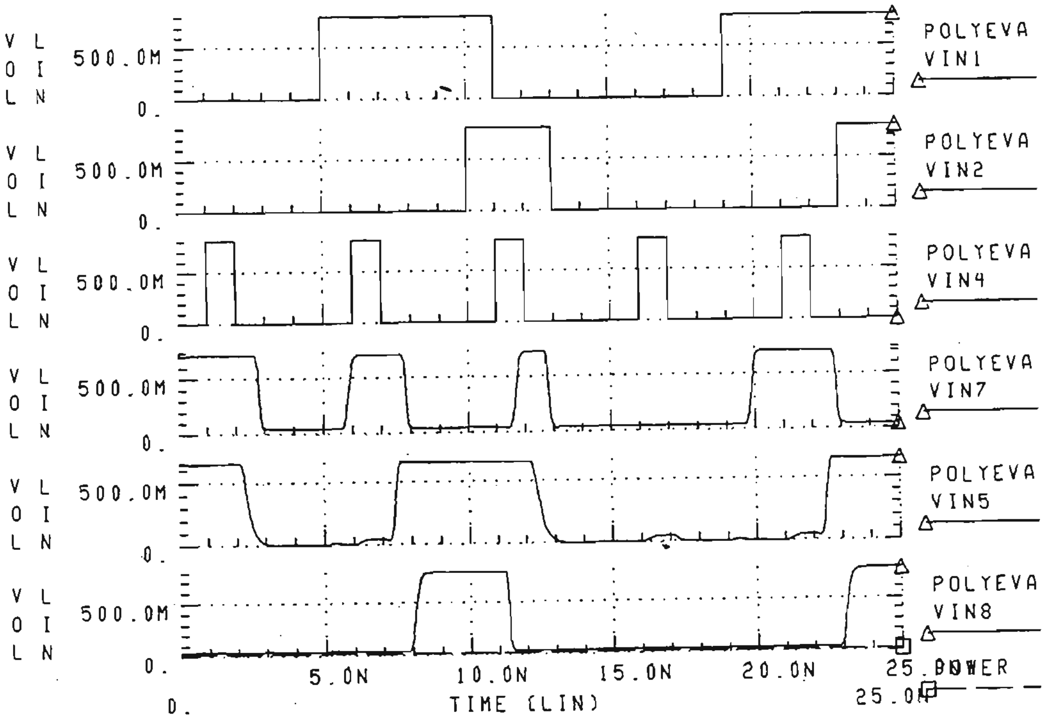


Figure 6.26 Simulation result for one-bit power series evaluator. VIN1, VIN2, VIN4, VIN5, VIN7 and VIN8 represent the data input A, multiplexer ld control, clock, Q, Sum and Carry outputs respectively.

6.3.2 Conclusions - Part II

The Merged logic approach to circuit design combines direct coupled MESFET logic (DCFL) with source follower DCFL (SDCFL) and source follower MESFET logic (SFFL) so that the advantages of each logic class are exploited and circuit performance is achieved which is superior to that obtained from different design approaches.

The Merged logic approach to circuit design is the natural progression from comparative studies of DCFL, SDCFL and SFFL circuits. This approach involves identifying critical parts of the circuit where SDCFL and SFFL techniques can be used to improve circuit performance.

The performance of Merged logic design approach is illustrated with the design and implementation of a power series evaluator chip. From the performance analysis it can be seen that this design approach demonstrates excellent performance with large logic swings resulting in excellent noise margins and large fan in and fan out capabilities.

Chapter Seven

Data Converters and Overcurrent Protection Relays

7.0 Chapter Overview

In this chapter the following topics are discussed:

(i) principles of analog-to-digital conversion, and

(ii) principles of overcurrent protection relay.

Part I Principles of Data Conversion

7.1 Introduction

Most physical signals are continuous in both time and amplitude. Transducers such as thermocouple produce continuous electrical signals (voltages or currents) that are analogous to physical variables. To process this analog signals using digital systems, the signals need to be converted so that they are discrete in time and amplitude. The interfacing between continuous, analog signals and discrete, digital signals require analog-to-digital conversion of the data.

Data converters are one of the largest sectors of linear integrated circuits. With information processing technology becoming digital to the greatest possible extent, analog-to-digital converters (ADC) and digital-to-analog converters (DAC) are the core of a data acquisition system, operating as a peripheral to a data processing computer.

Although much work has been performed on the design and implementation of silicon data converters [27 - 30], and many commercially available monolithic data conversion circuits exist, many system applications in the areas of instrumentation, signal processing and telecommunications require performance levels even higher than what is available today in silicon. GaAs data conversion circuits are aimed at addressing these applications with very high performance requirements.

7.2 Data Conversion Circuits

The design and implementation of an ADC is confined to linear circuit in which the digital signal is directly proportional to the amplitude of the analog signal. Nonlinear ADCs are special circuits, offering high signal-to-noise ratio at low signal levels, and are used primarily in telecommunication applications.

The data conversion process can be described by the following expression [73]:

$$V_a = V_{ref}(b_1.2^{-1} + b_2.2^{-2} + \ldots\ldots + b_{n-1}.2^{n-1} + b_n.2^n) \qquad \mathbf{(7.0)}$$

which can be applied to both analog-to-digital and digital-to-analog conversions. In the former case, the analog voltage V_a is converted into a n-bit binary number. V_{ref} is, in this case, the high logic level of the system.

For digital-to-analog conversion, the inputs b_1, b_2,....b_n is converted into an analog voltage by the scaling factor V_{ref}, which represents a reference voltage. The accuracy of V_{ref} is crucial in obtaining the required resolution for the conversion. According to equation 7.0, the conversion resolution is 1/2 LSB (least significant bit) resulting in a quantisation error of δV_a, where

$$\delta V_a = V_{ref}.2^{-(n+1)} \qquad \mathbf{(7.1)}$$

The sampling of V_a in analog-to-digital conversion introduces another error due to the time involved in performing the sampling. The error $\delta_t V_a$ is given by

$$\delta_t V_a = \int_0^{ta} {\delta V_a}\!\left/{\delta_t}\right. \, dt \qquad \mathbf{(7.2)}$$

where t_a is the sampling time of measurement.

The quantisation noise, computed using equation 7.2, can be used to define the signal-to-quantisation noise ratio (S/QN). The S/QN is given by:

$$\frac{S}{QN} = V_a . V_{ref}^{-1} . 2^{n+1} \qquad (7.3)$$

The above expression indicates that S/QN increases linearly with V_a, having its minimum value when $V_a = V_{ref} .2^{-n}$ or $\frac{S}{QN} = 2$.

The prime parameters characterising the performance of data converters are resolution, accuracy, and dynamic response.

7.3 Analog-to-Digital Converters

This section discusses the techniques and circuits used for analog-to-digital conversion. A variety of circuit organisations may be employed in the design of an ADC. Each architecture has particular performance characteristics in terms of speed, accuracy, and area. The major circuit architectures used in instrument and measurement environment are parallel (flash) ADC, successive-approximation ADC, charge redistribution ADC, tracking and dual slope ADC.

7.3.1 Parallel or Flash Analog-to-Digital Converter

The parallel or flash ADC organisation employs (2^n - 1) comparators for an n-bit ADC [108]. All the inputs are compared to a certain reference voltage, which is kept constant at each comparator. For a given input, the comparators below the input level will all give an output logic high and those above that level will give a complementary logic level. Following the comparators, the flash ADC employs an encoder to convert from a linear or thermometer code at the comparator outputs to a standard binary code. For some applications, a sample and hold circuit precedes the comparators. However, in many high speed circuits, the utilisation of sample and hold circuit may be difficult due to the high input capacitance of the comparators that it has to drive. Figure 7.1 illustrates a specific example of a three-bit flash ADC with quantisation level of $V_{ref}/8$.

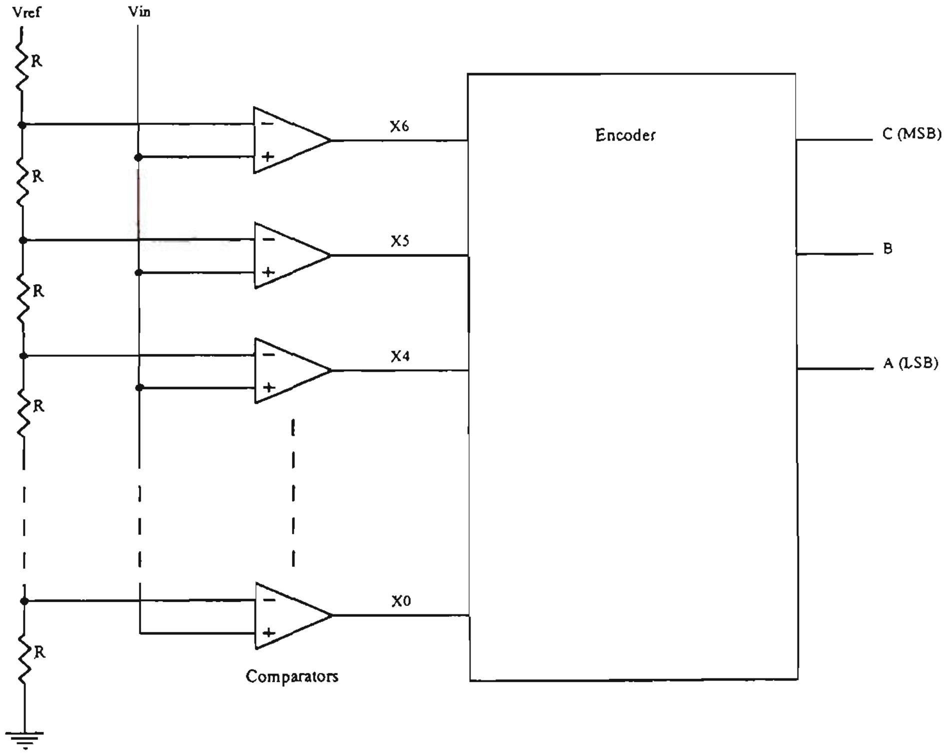


Figure 7.1 Block diagram of a three-bit flash ADC.

The flash ADC organisation is the fastest approach to analog-to-digital conversion, because the speed of the circuit is only limited by the response of the comparator and the propagation delay of the encoder. The comparator is the most critical circuit in the flash ADC, because its speed and accuracy determine the performance of the converter.

Conversion errors are due principally to comparator resolution and uncertainty (jitter) at the comparator outputs when both inputs are equal.

The converter with data size of more than eight-bits is very complex because of the large number of comparators [(2^n - 1) for a n-bit flash ADC)] and very complex encoding logic. In addition, 2^n precision resistors are needed at the input of the comparators.

7.3.2 Successive-Approximation Analog-to-Digital Converter

The successive-approximation analog-to-digital conversion technique [108, 118] is based on the functional block diagram in Figure 7.2. The comparator receives the buffered input signal and the output from the digital-to-analog converter (DAC). At the start of the conversion, all the bits of the successive approximation register (SAR) are set to zero except the maximum significant bit (MSB). Having the MSB set to one, the DAC provides a voltage output that represents half the digital range of the converter. Each approximation step takes place during a clock interval. The DAC converts the SAR contents to analog voltage V_d, which is compared against the input voltage V_a. The comparator output C is used to:

(i) retain the current bit value of one in the SAR if C is high, i.e. $V_a > V_d$, or

(ii) change the current bit value to zero if C is low.

At the start of next clock pulse, the next lower-order bit is set to one. The process of setting a bit to one and comparing V_d with V_a is carried out in sequence for all N-bits. At each step, a voltage increment (or decrement) of half the magnitude of the previous step results at the output of the DAC. Figure 7.3 shows the waveforms at the DAC output for a given value of V_a.

By starting the SAR at the midpoint, the circuit completes the conversion in exactly N-clock pulses regardless of the amplitude of the analog signal. This is an advantage in applications in which the time required for conversion must be a constant such as in uniform sampling.

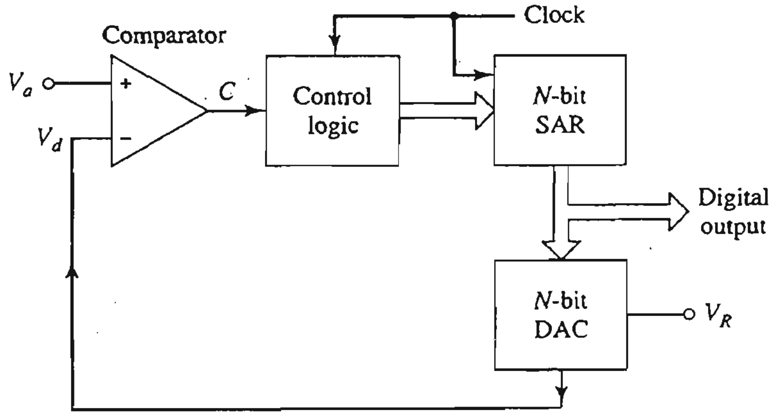


Figure 7.2 Successive approximation ADC.

The successive-approximation is the simplest analog-to-digital conversion organisation. However, since the output bits are determined sequentially, this configuration offers the slowest conversion time for a given technology. The accuracy of conversion is determined mainly by the accuracy of the DAC, and infact the best accuracy that can be achieved with this circuit cannot exceed the accuracy of the DAC.

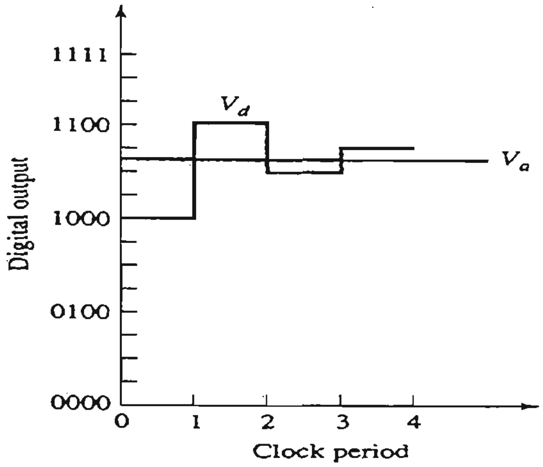


Figure 7.3 Waveforms at the output of a successive approximation ADC.

Another implementation of successive approximation ADC shown in Figure 7.4. It uses a string of resistors and an analog switching matrix. The control logic activates the appropriate switches and causes the binary fraction of V_R to be applied as V_d at each step. For a three-bit converter shown in Figure 7.4, the MSB is initially one and the two LSB's are zero, that is A = 1, and B = C = 0. This data combination closes switches S_{21}, S_{10}, and S_{00} in the path from (7/16).V_R to the inverting input of the comparator. If the analog input voltage V_a is above V_d = (7/16).V_R, the comparator output goes high. At the next step, the control logic applies an input of ABC = 110 to the switches. This results in V_d = (11/16).V_R. If the comparator output now goes low, the next approximation of the data is 101, which corresponds to V_d = (9/16).V_R. At the third and last step, the converted result is either 100 if (7/16).$V_R < V_a <$ (9/16).V_R, or 101 if (9/16).$V_R < V_a <$ (11/16).V_R. Bipolar analog signals are converted by connecting the resistor chain between +V_R and -V_R.

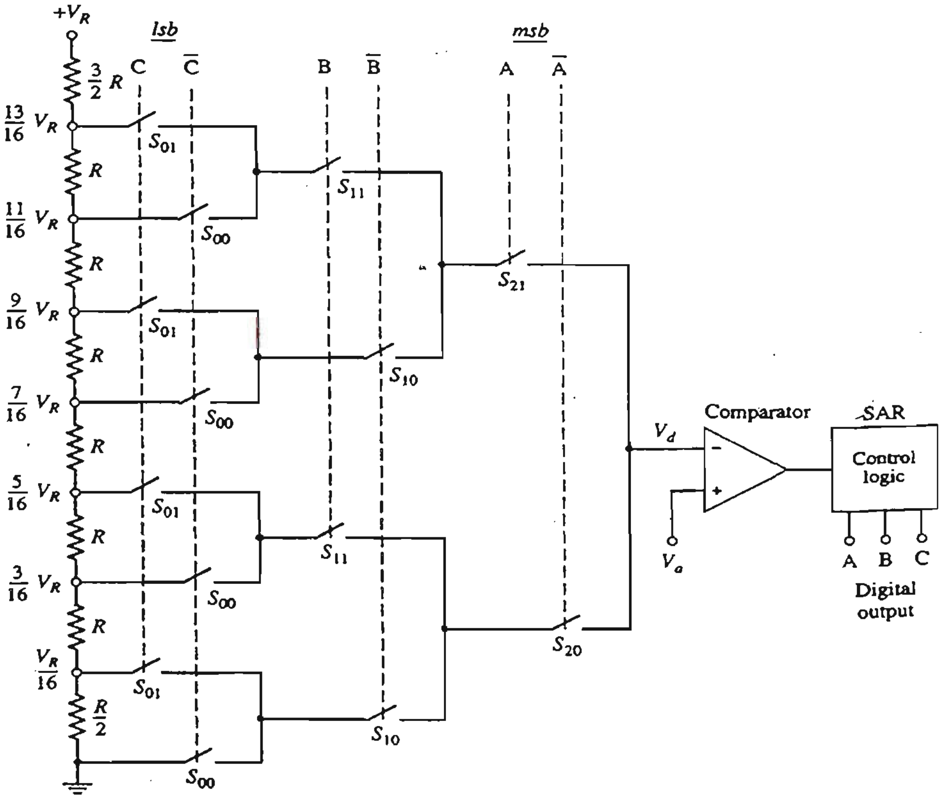


Figure 7.4 Modified successive approximation ADC [108].

For an N-bit converter, this technique requires [$2^{(N+1)}$ - 2] switches and 2^N resistors. Thus, this technique uses a large number of components as compared with Figure 7.2. The advantage, however, lies in the ability to implement all the elements of the converter in a single chip using GaAs technology.

7.3.3 Charge Redistribution Analog-to-Digital Converter

Charge redistribution ADC implements the successive approximation algorithm by using a bank of capacitors [108, 118]. Instead of a string of resistors, binary weighted capacitors redistribute the charge to obtain a voltage V_d proportional to the assumed digital data. Figure 7.5 shows the four-bit charge redistribution ADC. The circuit operates in three phases: sample, hold, and redistribute. During the sample phase (ϕ_s = 1), the switch at the upper plates of all capacitors is connected to ground, while the bottom plates are connected to the input signal V_i. In the hold phase (ϕ_h = 1), the bottom plates of the capacitors are connected to ground, while the ground connection at the top plates are removed. The voltage at the top plates of the capacitors is equal to:

$$V- = -V_a = -V_i\Big|_{(\text{sampled during } \phi_s)} \qquad (7.4)$$

relative to the bottom plates. The charge stored in the capacitor bank is given by:

$$Q = 2.V_a.C \qquad (7.5)$$

The redistribute phase (ϕ_r = 1), begins with digital value of 1000. In this phase the right most capacitor in the bank is connected to ground. The switches to the other capacitors connect to V_R or ground, depending on the bit value of one or zero. This phase takes N clock pulses during ϕ_r for a N-bit converter. The convergence of the digital value close to V_a is obtained by successively incrementing V- to zero. Figure 7.6 illustrates the waveforms for converting V_a in the range $(11/16).V_R > V_a > (10/16).V_R$. During the first clock in phase ϕ_r, the maximum significant bit capacitor is connected to V_R and all other capacitors are at ground. This gives a capacitive voltage divider with an external voltage V_R applied to two series capacitances of C each. Since the initial charge in the capacitor bank is $2.V_a.C$, the net voltage at the inverting input of comparator is equal to:

$$V- = \frac{V_R}{2} - V_a \qquad (7.6)$$

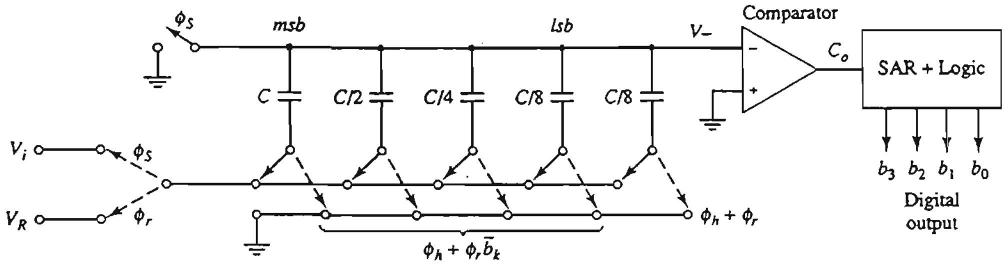


Figure 7.5 Charge redistribution ADC.

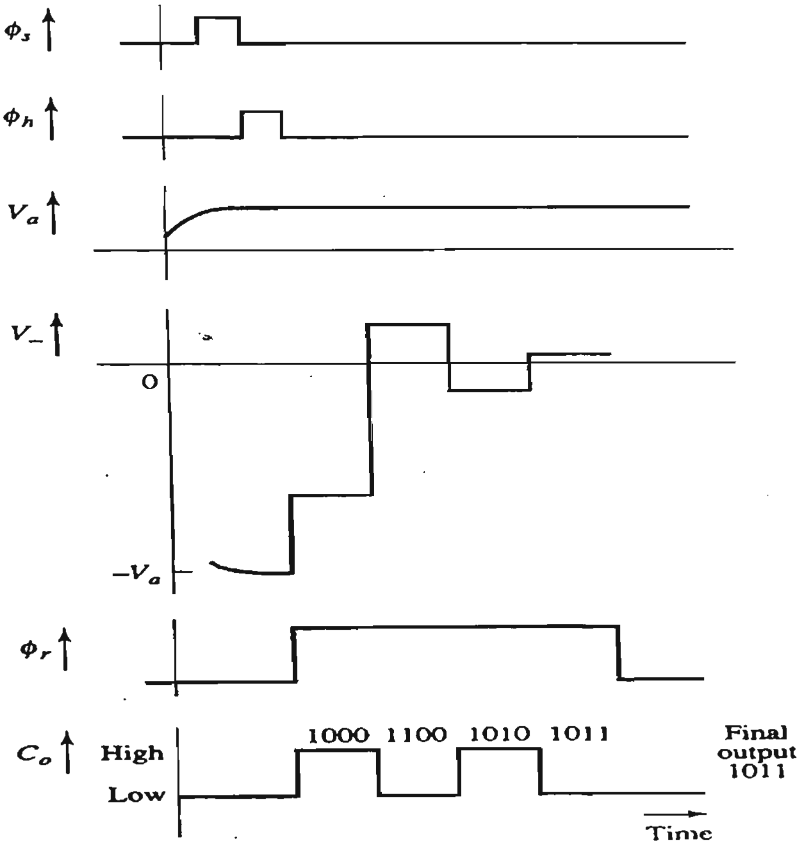


Figure 7.6 Waveforms for charge redistribution ADC.

With input $V_a > (V_R/2)$, the comparator output C_o goes to logic high. At the beginning of the next clock pulse, the control logic keeps the MSB at one, and digital value of 1100 is applied. At this value V- becomes $(3/4).V_R - V_a$, which is positive. This causes C_o to go to logic low; hence at the third clock pulse 1010 is tried. Now V- = $[(5/8).V_R - V_a] < 0$, which makes C_o to go high. Hence, the final value tried is 1011. At the end of the fourth clock, the digital output is 1011 or 1010, depending on whether C_0 is high or low.

7.3.4 Tracking and Dual Slope Analog-to-Digital Converters

Figure 7.7 shows a simpler alternative to successive approximation ADC, which uses a counter and a DAC [108]. The reference voltage V_R of the DAC is such that V_d at full scale (for the counter output of 11..11) is equal to the maximum input analog voltage, V_a, to be converted. Conversion begins by resetting the counter to zero at the arrival of a new sample of the analog voltage, V_a. With the DAC output $V_d < V_a$, the comparator output is at logic high. As the stair step voltage V_d increases due to increasing counter output, the comparator output switches to logic zero when V_d reaches V_a. The counter output now corresponds to the digital equivalent of V_a within half LSB. Conversion resolution is improved by increasing the number of bits on the counter and the DAC. The disadvantage of this scheme is that the DAC output always starts at zero before tracking V_a. Hence the conversion time is variable and depends on the amplitude of the analog signal V_a.

Conversion time can be speeded up by using UP/DOWN counter. Instead of resetting the counter at the beginning of each conversion, the comparator output is used to count up or down from the previous counter value. The counter output and the DAC voltage therefore track the input voltage V_a. Tracking ADCs with UP/DOWN counters are useful in low cost, low speed applications such as the measurements of slowly varying signals from temperature transducers and strain gauges.

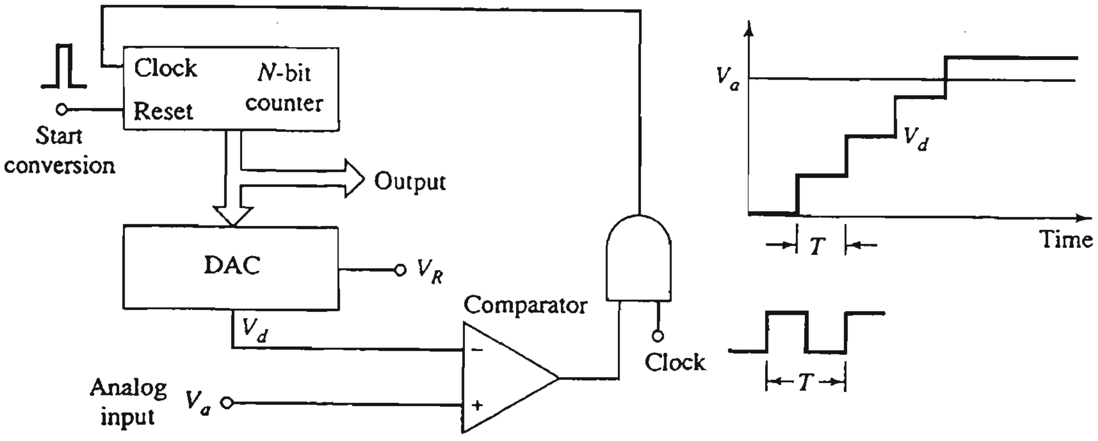


Figure 7.7 Counter ramp ADC.

Figure 7.8 shows the dual slope converter [108]. Instead of using a DAC in the feedback loop, this converter employs an integrator to integrate the analog voltage V_a over a fixed time interval. Charge accumulated in the integrator capacitor is discharged at a constant rate to zero. The ratio of the charging and discharging time intervals is proportional to the digital value of V_a.

Conversion in the circuit begins by discharging the capacitor C and connecting the SPDT switch at the input of the integrator to the analog input voltage V_a (> 0). As the capacitor charges, the N-bit counter is simultaneously enabled to increment from zero. Since the charging current derived from V_a is V_a/R, the output of the integrator ramps down with a slope of V_a/RC. Figure 7.9 illustrates the output waveform for the circuit [108]. With the reference (noninverting) voltage V+ at zero, the comparator output is at logic high for positive V_a. This causes the counter to increment. When the counter reaches the full count and resets to zero after 2^N clock pulses, the integrator input is switched to the reference voltage $V_R < 0$. Since V_R is negative, the accumulated charge in C is discharged at the rate of V_R/RC. The counter output is still high, so the counter continues to count from its reset state. When V- reaches zero, the comparator output switches to logic low disabling the counter. The output of the counter is now proportional to the digital value of the analog input signal, V_a.

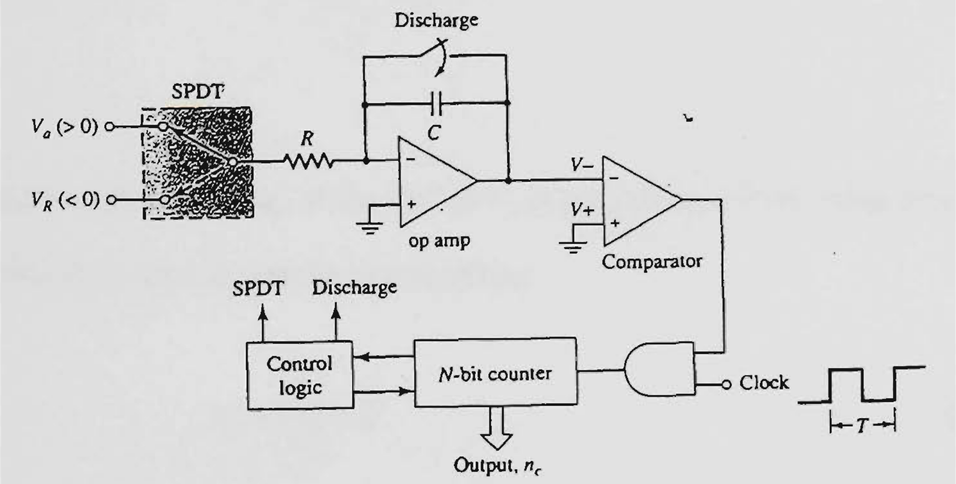


Figure 7.8 Dual slope ADC.

The charging time, T_1, for capacitor C is given by [108]:

$$T_1 = 2^N.T \tag{7.7}$$

where **T** is the period of the clock.

The output of the integrator, V-, reaches the peak value, V_P, at the end of T_1, given by:

$$V_p = (\frac{-V_a}{R.C}).T_1 \tag{7.8}$$

During T_2, C discharges from the initial value of V_p with a slope of (V_R/RC). The time interval T_2, when the comparator output switches from high to low, is given by:

$$(\frac{V_R}{R.C}).T_2 = (\frac{V_a}{R.C}).T_1$$

$$T_2 = (\frac{V_a}{V_R}).T_1 \qquad \textbf{(7.9)}$$

Since the counter output, $\mathbf{n_c}$, at the end of T_2 is proportional to the time intervals T_1 and T_2, the counter output $\mathbf{n_c}$ can be expressed as:

$$n_c = (\frac{V_a}{V_R}).2^N \qquad \textbf{(7.10)}$$

If $|V_R| = V_a|_{max}$, a counter output of $n_c = 2^N$ corresponds to the full-scale digital value of $V_a = V_a|_{max}$, and $n_c < 2^N$ is proportional to $V_a < V_a|_{max}$, within the least significant count.

The resolution of this converter can be improved by increasing the size of the counter. Although the converter features a variable conversion time, it has other advantages. From equation 7.11 it can be seen that the conversion is independent of the tolerances of both R and C. Only the clock must be stable with time for repeatability of the converted data. Due to inherent low pass filtering in integration, high frequency noise at the input is eliminated. In addition, if $T_1 = 2^N.T$ is chosen as a multiple of the power line period, the effects of low frequency power supply noise is minimised. To take advantage of the latter, however, a long integration time must be allowed. For this reason, dual slope converters are usually used for converting slowly varying or noisy signals. High accuracy digital voltmeters are built using dual slope converters.

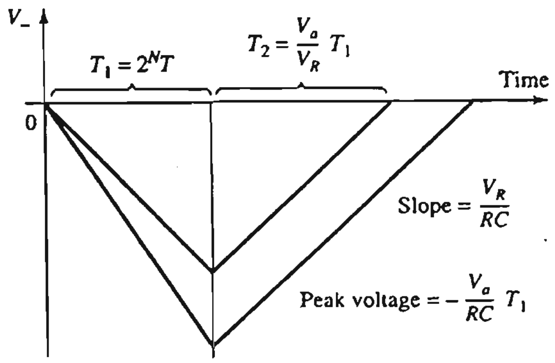

V_-
$T_1 = 2^N T$
$T_2 = \frac{V_a}{V_R} T_1$
Time
0
Slope = $\frac{V_R}{RC}$
Peak voltage = $-\frac{V_a}{RC} T_1$

Figure 7.9 Integrator output waveforms.

7.3.5 Conclusions - Part I

The voltage comparator is the basic analog-to-digital interface device. Its output is at logic high or low, depending on the relative voltages at its inverting and noninverting inputs. By nature, a comparator quantises an analog voltage as being above or below a reference voltage. Hence, a comparator is a one-bit ADC. Paralleling many comparators, each with a different reference voltage, and encoding the digital outputs of the comparators, a n-bit analog-to-digital conversion is obtained. Such an ADC, called a flash or parallel ADC, is very fast with only the propagation delay of the comparators and the encoding logic. However, a large number of comparators ((2^n - 1) comparators for an n-bit flash ADC) are required.

For ADCs requiring long time intervals, analog signal must be sampled and held constant during conversion. A sample and hold circuit uses a capacitor to charge to the analog voltage at the time of sampling. With low leakage capacitors and buffered circuitry, this charge can be held virtually constant during the conversion interval. Successive approximation ADCs use **n** step digital approximation to obtain a n-bit binary data. A DAC in a feedback loop converts the digital data and a comparator controls the approximation. This ADC takes n clock periods to complete a conversion. A variation on the successive approximation algorithm uses a switch matrix or a capacitor bank in place of a DAC.

Several other methods of analog-to-digital conversion use a counter for slowly varying signals. In the counter ramp method, a counter is activated at the beginning of a new analog voltage sample V_a. A DAC converts the counter output and applies the converted voltage, V_d, to the comparator. When V_d equals V_a, the counter is disabled. The conversion time depends on the amplitude of the analog voltage. An UP/DOWN counter is used to track the input voltage and reduce the conversion time.

A dual slope ADC uses a capacitor to integrate the analog voltage over a fixed time period. The capacitor is discharged at a constant rate, using a reference voltage, and a counter is run simultaneously. The output of the counter at the end of the discharge interval is proportional to the analog voltage.

Of all the structures for ADC discussed, the parallel or flash ADC organisation is the fastest approach to analog-to-digital conversion because the speed of the circuit is limited only by the response of the comparator and the propagation delay of the encoder. For this reason the implementation of the data acquisition chip will be based on the parallel or flash ADC.

Part II Principles of Overcurrent Protection

7.4 Introduction

The overcurrent protective devices isolate the section of the power system affected by a fault so that the remaining system can continue to operate normally. The approach to this protection mechanism is to identify a fault current, which must clearly distinguishable from the load current, so that the overcurrent protective device can respond to this current quickly and disconnect the affected circuit rapidly. Time-overcurrent devices have inverse time-current characteristics to clear faults with coordinated minimum time delays. With this type of characteristic, the greater the fault current the shorter the trip time.

The following sections describe the fundamentals of inverse time current relaying, related to transmission line protection.

7.5 Overcurrent Characteristics and Protection Practices

Overcurrent protection, which was developed some seventy years ago, is still the cheapest and simplest form of protection widely used in the power industry. It operates on the principle, that, once the predetermined fault current level is reached the relay will operate in a predetermined time and manner. Generally, classification of these relays are in terms of their time characteristic, for example, instantaneous, inverse time, very inverse time, extremely inverse time, very steep time and fixed or definite time [110]. The time-current relation for an overcurrent relay is given by:

$$T = \frac{K.t_m}{I^n - 1} \qquad \textbf{(7.11)}$$

where T is the theoretical operating time of the relay

K is the design constant

t_m is the time multiplier setting

n is an index characterising the algebraic function

I is the relay current in multiple of tap setting.

The derivation of the above expression is presented in Appendix G.

Figure 7.10 gives the range of typical operating time characteristics, including mathematical formulas applicable for the digital relay implementation, of the various types of inverse overcurrent relays.

Definite Time $T = K$ (K is a constant) **(7.12)**

Standard Time $$T = \frac{0.14}{I^{0.02} - 1} \qquad \textbf{(7.13)}$$

Very Inverse Time $$T = \frac{13.5}{I - 1} \qquad \textbf{(7.14)}$$

Extremely Inverse Time $$T = \frac{80}{I^2 - 1} \qquad \textbf{(7.15)}$$

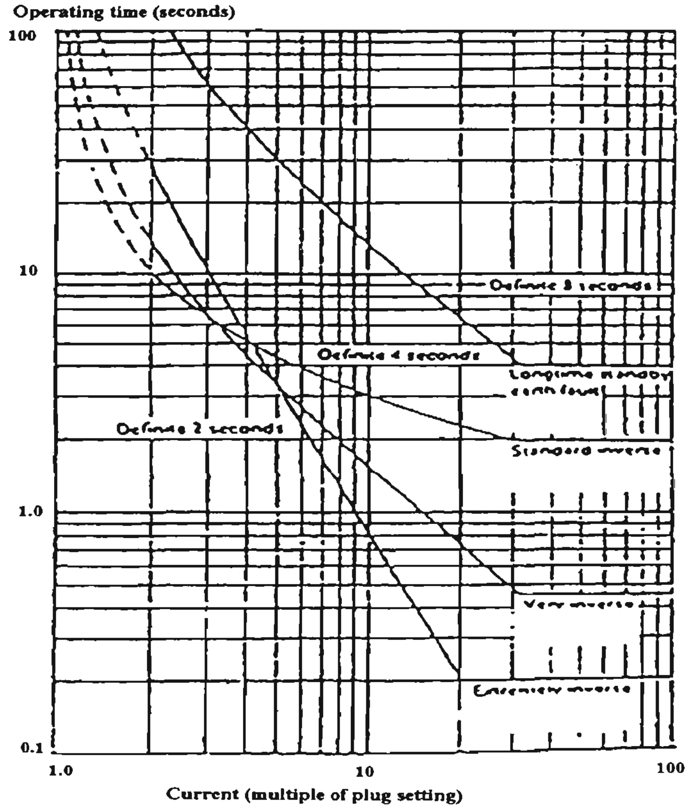


Figure 7.10 Time-current characteristics of inverse overcurrent relays.

7.5.1 Instantaneous Characteristic

The overcurrent relays having this type of characteristic operate with very small time lag once the system current exceeds the pick-up current of the relay. The time of operation does not change for variation in the system current above the pick-up current level. In order to achieve the selectivity of operation among a number of such relays, the pick-up current of each relay is set at a different level. In the power system, the relay connected nearer to the source has a higher plug setting. Thus, for a radial feeder, a fault in a succeeding section, having a lower current level will operate only the relay connected to that section. However, this type of selectivity can only be achieved if the source impedance is either comparable or less than the line impedance. The instantaneous overcurrent relay has a further disadvantage, an overreaching tendency, due to the offset current wave. In particular, for systems with high X/R ratio it becomes imperative to increase the time of operation to avoid overreach.

7.5.2 Definite Time-Current characteristic

In a radial feeder without any tapped connection, it is difficult to achieve a proper selectivity between two faults, with one occurring just before a section finishes and the other occurring just after the next section begins. The variation of fault current under such conditions is so small that sometimes it is impossible to set different pick-up currents for the relays connected to the respective sections. Under such conditions and for conditions where instantaneous relays fail, sometime definite time-current characteristic relays are used. These relays operate after a fixed interval of time after a fault current exceeds the pick-up current level. In a radial feeder this time interval setting gradually increases in steps for the relays connected to sections nearer to the source. Figure 7.11 illustrates the definite time-current principle. The time-current characteristic of such a relay can be expressed as:

$$I^0.T = K \tag{7.16}$$

where K is a constant.

The main disadvantage of the definite time relay lies in the fact that the most serious fault occurring in section one is cleared after the longest time lag. Therefore, for a long feeder with a large number of protection zones, the use of definite time-current relay may become a problem because of its very slow action near the source.

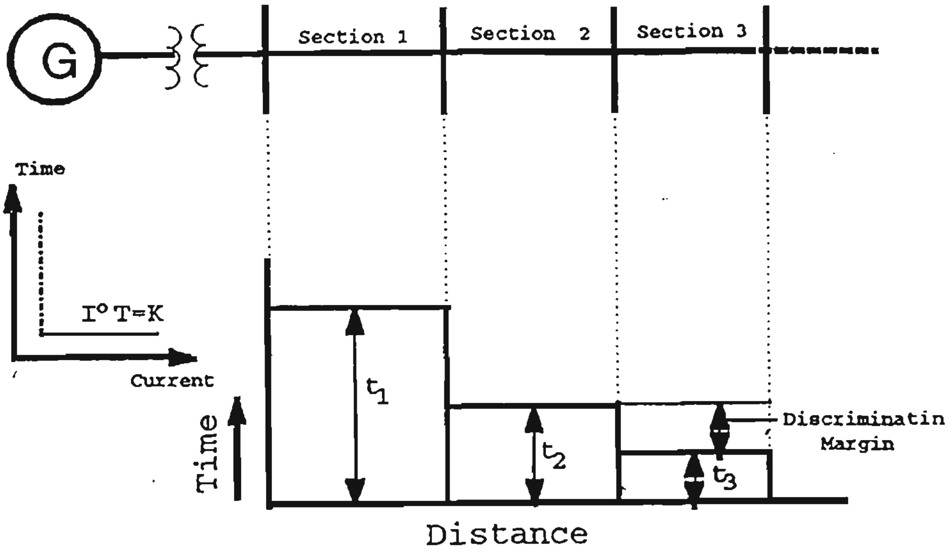


Figure 7.11 Definite time-current relaying technique.

7.5.3 Inverse Time-Current Characteristic

Normally the fault current at the far end of the protected section is considerably less than to that at the source end. The inverse time-current relay, with low operating time for a large current, will clear a source-end fault quickly. Contrarily, its high operating time for small fault current will allow a large time lag in clearing a far end fault. Figure 7.12 illustrates a inverse time-current characteristic and its application in power system protection.

It can be readily seen from Figure 7.12(b) that the fault occurring at the beginning of the protected zone is cleared faster than the fault occurring at the end of the protected zone. The relays connected to its preceding zone will respond to these faults at still a slower

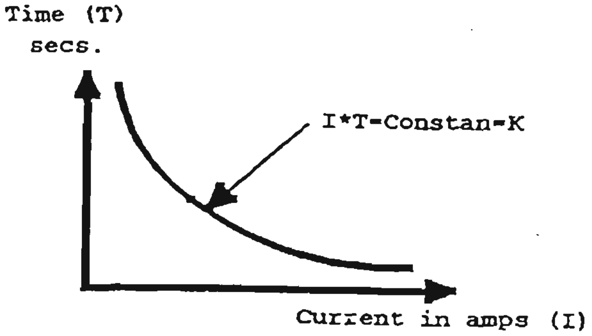


Figure 7.12(a) Inverse time-current characteristic.

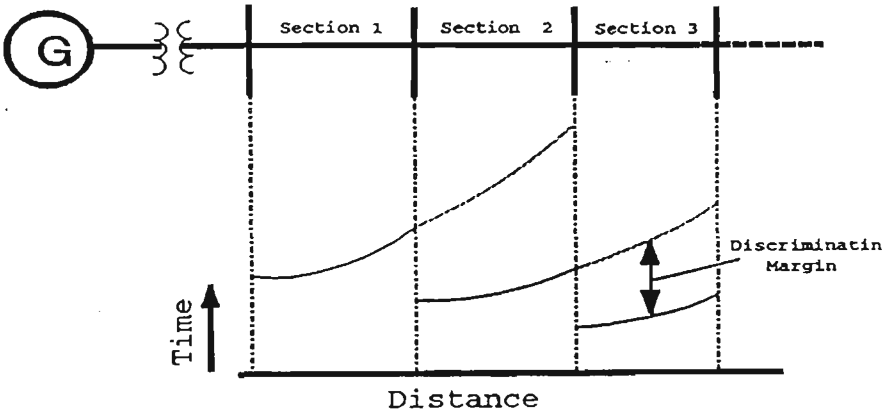


Figure 7.12(b) Power system protection using inverse time-current relays.

rate. This relay can act as back-up for the relay connected to the succeeding zone. The inverse-time, overcurrent relay generally provides good selectivity, but for the following reasons its selectivity may be affected. Firstly, if the source impedance of the system is very high compared with the protected line impedance, then the change in the fault current levels at the beginning and at the end of the protected zone is not considerable. Thus, the change in time of operation, (their ratio being inversely proportional to the fault current ratio, is given by $Z_S/(Z_S + Z_L)$, where Z_S is the source impedance and Z_L is the line impedance), becomes very small. Secondly, a change in generating capacity also changes the value of the source impedance. In particular, a sharp fall in the generating capacity increases the value of the source impedance and thus increases the operating time of the relay.

7.5.4 Inverse Definite Minimum Time Characteristic

The operating time of a inverse time-current relay becomes indeterminate for very high fault current leading to poor selectivity. Overcoming this problem, requires the adjusting of the characteristic to have a definite minimum time of operation for plug setting multiplier (PSM), higher than twenty. Thus the actual relay characteristic becomes a inverse characteristic below this value of PSM and a straight line characteristic above this value. In an actual relay, the operating time is further adjustable to discriminate even the minimum operating times of the relays connected to different sections of the feeder. This adjustment, known as time setting, is generally in steps of ten percent (10%) of the maximum operation time of a particular plug setting. Calibration of the steps is in terms of the time setting multiplier (TSM), which is defined as:

$$TSM = \frac{Actual\ operating time\ of\ the\ relay}{Calibrated\ opertaing\ time\ of\ a particularPSM}$$

The standard inverse definite minimum time (IDMT), characteristics are generally shown by a family of logarithmic curves as in Figure 7.13. The time-current relationship for a dependent overcurrent relay can be expressed as:

$$T = \frac{K.t_m}{I^n - 1} \qquad (7.17)$$

For standard IDMT relay, the recommended time-current relationship is given by:

$$T = {}^{0.14}\!\big/_{(I^{0.02} - 1)}.$$

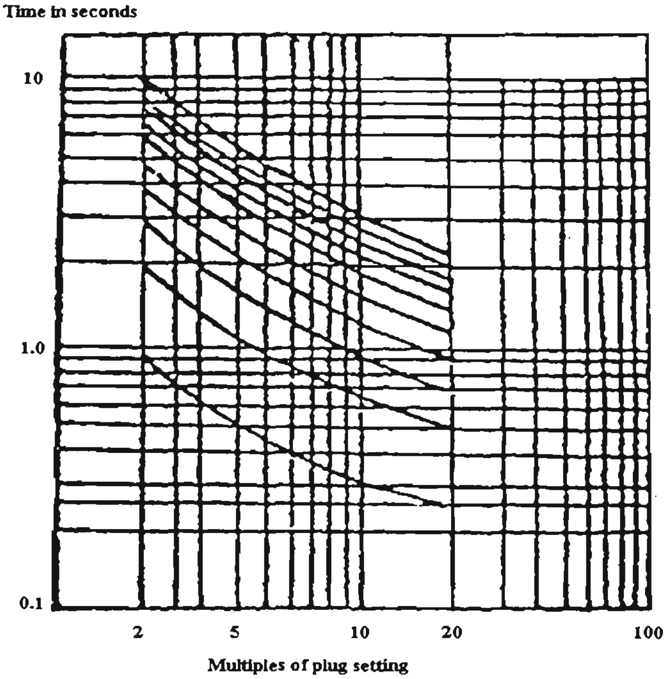


Figure 7.13 Standard IDMT characteristics.

7.5.5 Extremely Inverse Characteristic

Often there is a need to protect electrical equipment against overheating. An overcurrent relay, with its characteristic described by $I^2T = K$ (an extremely inverse characteristic) will provide such protection. The standard form of extremely inverse characteristic is $T = 80/(I^2 - 1)$. The extremely inverse characteristic for a fuses is described by $I^{3.5}T = K$. Protecting rectifier transformers, a highly inverse characteristic of $I^8T = K$ is required. All these characteristics having a value of n > 2 are realised by suitable static relays and microprocessor based overcurrent relays.

7.5.6 Very Inverse Characteristic

Standard IDMT characteristic fails to achieve good selectivity near the maximum current levels at different substations by overcurrent relays with same TSM. The difficulty arises in systems where the fault current rapidly decreases with increase in the protected length from the source. A plain inverse characteristic or its near equivalents are more suitable in such cases. In a very inverse time-current relays the value of ***n*** lies between 1.02 and 2. The recommended standard for very inverse time-current characteristic is T = 13.5/(I -1).

Figure 7.14 compares the IDMT and very inverse time-current characteristics. The relays come with a number of tap/plug points, each of which represents the minimum current at which the relay starts to operate. A relay that has been set on a particular tap/plug will begin to operate at that setting plus/minus the manufacture's tolerance. In addition to the tap/plug setting, these relays also have a time multiplier setting. This setting provides different operating times for the same operating current level. Figure 7.15 shows a typical family of inverse type operating time characteristics for various time multiplier setting [110].

7.5.7 Hybrid Characteristic Overcurrent Protection

Due to increasing demand of electrical energy, power systems have become more complex, fault levels have increased and transmission margins have reduced [110].

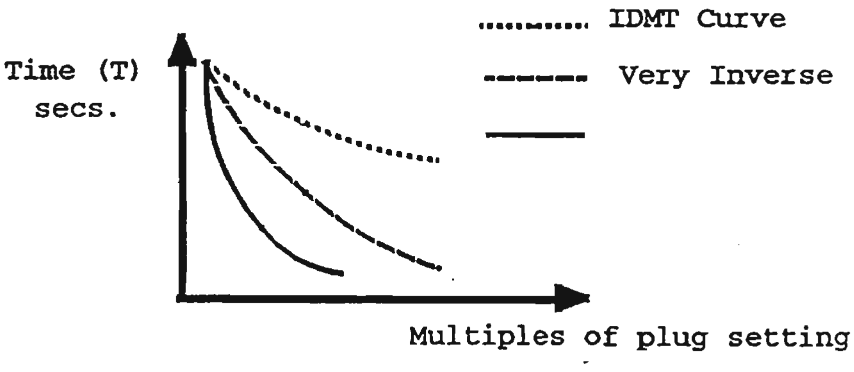


Figure 7.14 IDMT and very inverse time-current characteristics.

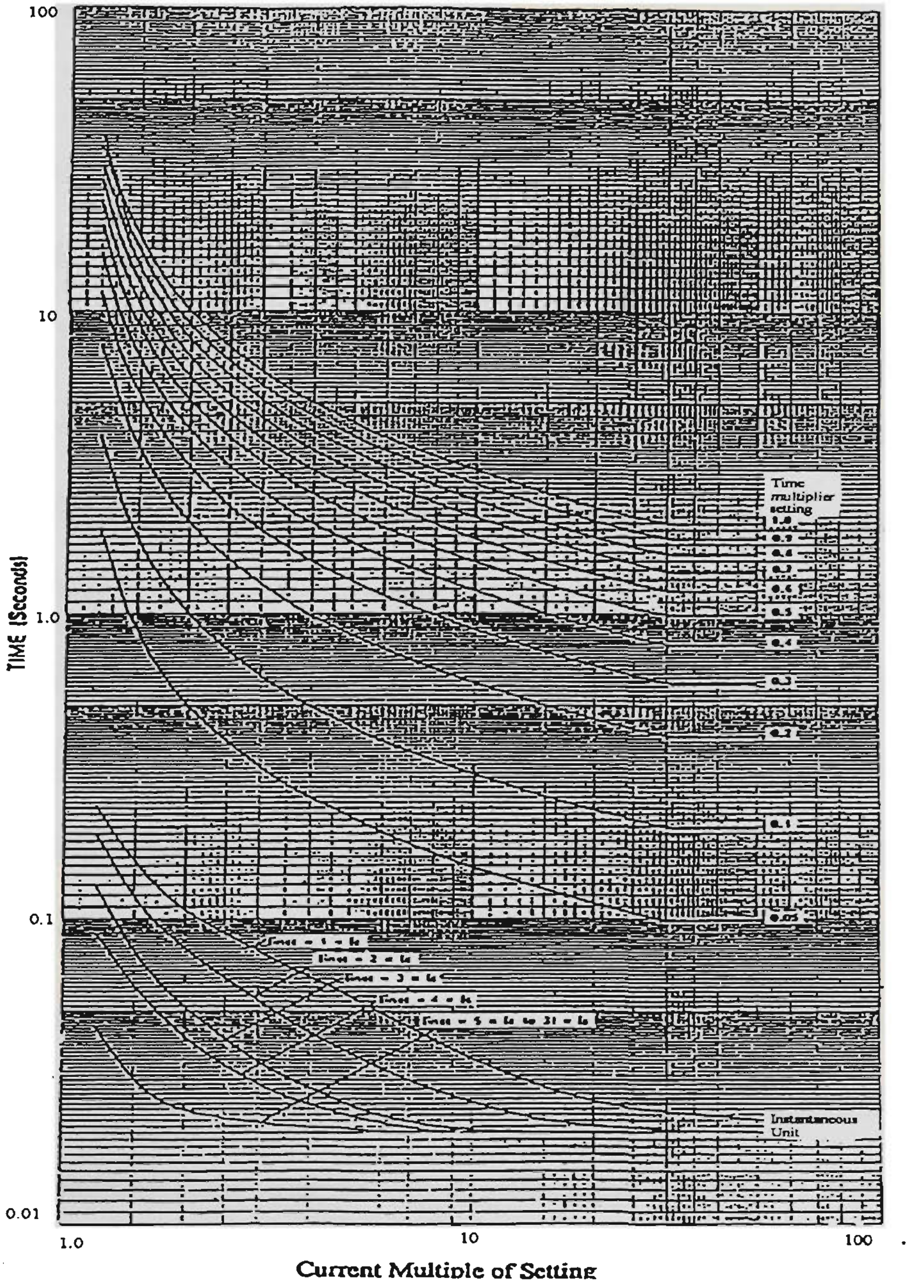


Figure 7.15 Inverse time characteristics for a various time multiplier setting.

These conditions demand that relays used to protect power systems be more reliable, accurate and fast compared to those used by the industry at the moment. Recent advances in microelectronics technology have made it possible to design digital relays to satisfy these requirements. A flexible multi-curve overcurrent protection relay provides significantly improved protection speed and sensitivity. Also, the incorporated use of definite and inverse time overcurrent characteristics provide the hybrid characteristics with no increase in cost or complexity to protection equipment [47].

Recently, the coordination of ground time overcurrent relay in transmission line protection application has been proposed [45, 111]. Fundamentally, the back-up relay pick up current must be adjusted so that each relay will operate for all faults in the immediately adjoining circuits and their time setting must be just long enough to permit the relay in the faulted circuit to operate first. This is implemented by using relays with similar time-current characteristics, such as definite time overcurrent relays. When the sensed current is above the threshold setting, they operate in a predetermined time regardless of the magnitude of the current. Conversely, inverse time relays have very long operating times and are often indeterminate at current magnitudes between 1 and 1.5 per unit of pick-up. To provide reasonable speed, such relays may need their pick-up setting at values lower than definite time relays. In order to improve the protection speed, sensitivity and security, a hybrid system incorporates characteristics of both definite and inverse time relay. Figure 7.16 illustrates the combined use of inverse and definite time characteristic curves.

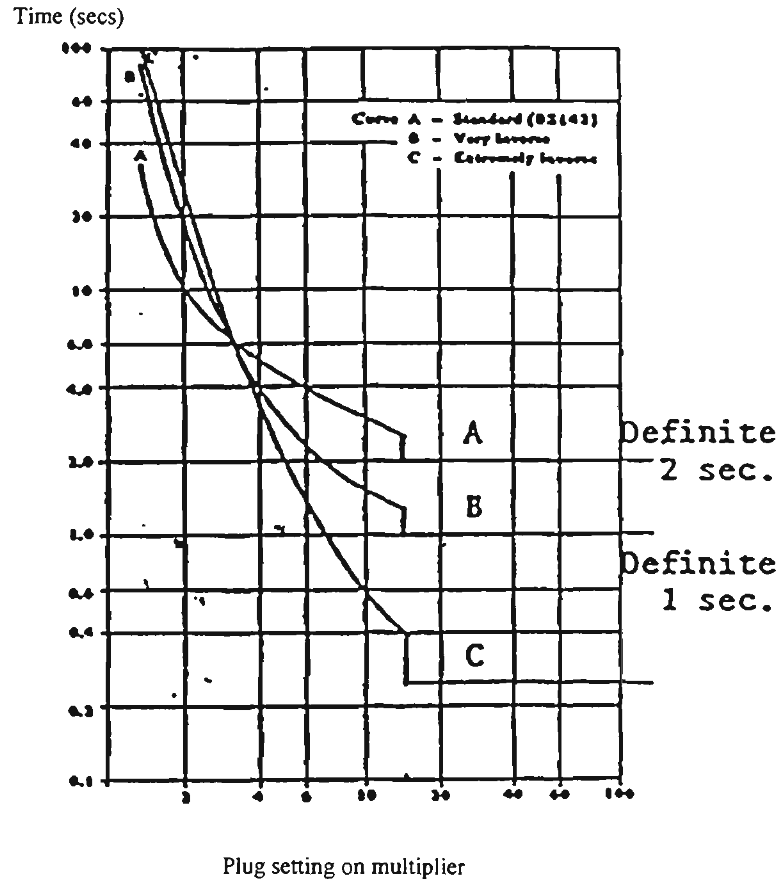


Figure 7.16 A combined use of inverse and definite time characteristic curves.

7.5.8 Conclusions - Part II

Overcurrent protection is the cheapest and simplest form of protection widely used in power industry. It operates on the principle, that, once the predetermined fault current level is reached the relay will operate in the predetermined time and manner. The principle of various overcurrent characteristics and the development of hybrid characteristic overcurrent protection scheme have been discussed. The combined use of multi-curves for definite and inverse time overcurrent characteristics have been used to significantly improve protection speed, sensitivity and security.

Chapter Eight

Multi-Channel Data Acquisition Integrated Circuit

Knowledge without practice makes but half an artist.

Proverb.

8.0 Chapter Overview

In this chapter, design, implementation and performance analysis of a high speed, low power, four-bit multi-channel data acquisition chip is presented.

8.1 Introduction

The computerised acquisition of analog quantities is becoming very important in today's automated world. Computer based data acquisition systems are capable of scanning several analog inputs in a particular sequence to monitor critical quantities and acquire data for on line use and future recall. Multi-channel data acquisition system usually consists of the following sub-systems:

(i) Transducers and signal conditioning circuits, which senses physical phenomena and provide electrical signals. Electrical signals generated by the transducers must be converted into a form that the data acquisition circuit can accept. Signal conditioning circuits can amplify low level signals, isolate and filter them for more accurate and safe measurements.

(ii) The data acquisition circuit, usually consists of analog-to-digital converter (ADC) and some sort of multiplexing circuit. Multiplexing is a common technique for measuring several inputs with a single ADC. The ADC samples one channel, switches to the next channel, samples it, switches to the next channel, and so on. Because the same ADC is sampling many channels instead of one, the effective rate of sampling each individual channel is inversely proportional to the number of channels sampled.

As speed is continuously increasing in electronic systems, especially in ADCs, data acquisition is becoming a real issue. To perform signal acquisition at sampling rates greater than 700 Megasamples per second (Ms/s), appropriate technology is necessary. For a very high speed operation in a semiconductor medium, three factors become significant, namely: carrier mobility, carrier saturation velocity and existence of semi-insulating substrate. The latter property allows mixed analog and digital circuits to be implemented on the same chip. GaAs technology mostly fulfils these requirements, and together with low power dissipation, provides a technology base for a new generation of analog and digital circuits.

The four-bit multi-channel data acquisition chip is based on very fast flash ADC with multiplexed inputs. The ADC is based on an algorithm that requires only $2^{(n - 1)}$ comparators instead of $(2^n - 1)$ comparators for a n-bit conversion. This approach, thus reduces the complexity of multi-bit flash ADC design. The design of the proposed ADC is module oriented, which enables multi-bit high resolution flash ADC to be developed by cascading a number of n-bit flash modules.

8.2 Analog-to-Digital Conversion for High Speed Data Acquisition System

Real-time data processing systems operating at Gigabit rate are primarily limited by the ADC performance. The fastest ADC available in practice is the flash ADC involving a conversion time equal to the propagation delays of the comparator and the encoding logic. However, the complexity of the circuit increases rapidly with the increase in the number of bits. An increase of one bit in the digital output nearly doubles the circuit complexity. For instance, when an eight-bit ADC needs 255 comparators for its realisation, a nine-bit ADC requires 511 comparators for its implementation. This increase in the complexity of the hardware discourages its feasibility of implementation for bigger number of bits. Some effort has been made to reduce the comparator count using pipelining technique [35, 36, 38]. This scheme generally requires DACs, amplifiers and other additional circuitry.

In this section, design and GaAs implementation of a four-bit flash ADC and a multi-channel data acquisition chip are described. The ADC requires only $2^{(n-1)}$ comparators instead of (2^n -1) comparators for a n-bit conversion and does not require complex hardware.

8.2.1 Flash Analog-to-Digital Converter Topology

The development of this technique can be explained with reference to a three-bit flash ADC shown in Figure 8.1 [117]. The outputs of the comparators and the corresponding digital outputs of the ADC are tabulated in Table 8.1. From the table it can be seen that the comparator which compares the analog input voltage with $V_{ref}/2$ generates the most significant bit of the converter. This comparator output, X_3, is chosen as a control signal. When X_3 is logic '0', the output of lower order comparators (X_2, X_1 and X_0) determine the final ADC outputs. Similarly, when X_3 is logic '1', only the higher order outputs of comparators (X_4, X_5, and X_6) determine the final outputs, because the lower order comparators outputs are all at logic '1'. Thus, either the three lower order comparator outputs or the three higher order comparator outputs determine the final ADC output, depending upon the output value of the $V_{ref}/2$ comparator. This implies that the comparator count can be halved, if, $V_{ref}/2$ comparator output is used to control a DPST switch. The two inputs of the switch or a multiplexer, connect to the corresponding reference voltages. Figure 8.2 shows the structure of such a scheme.

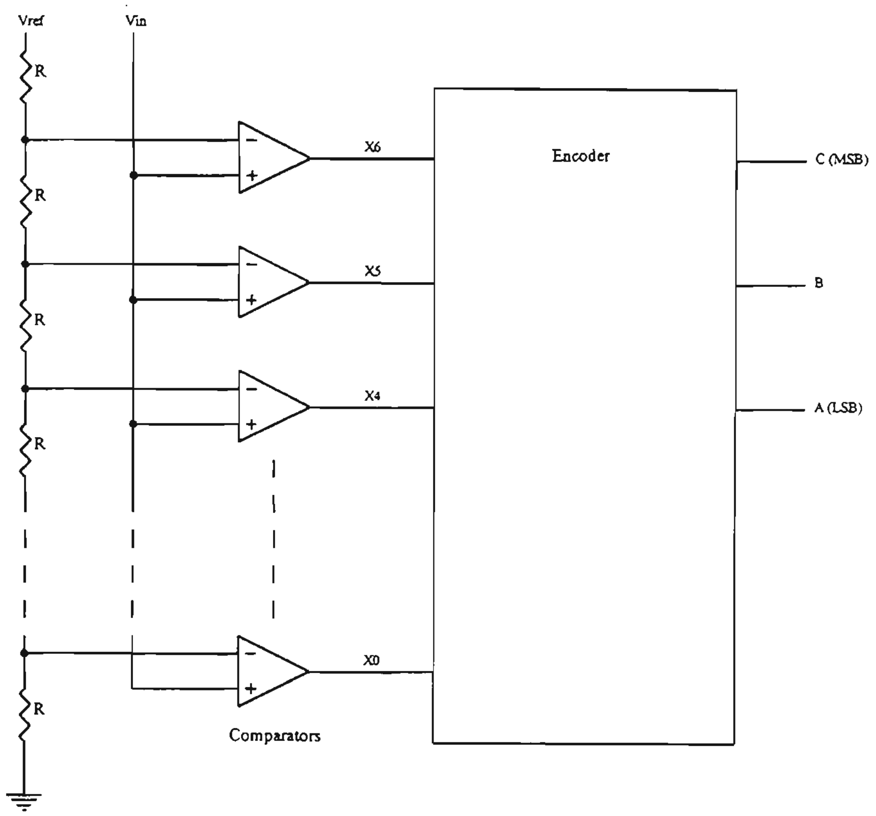


Figure 8.1 Three-bit flash ADC.

Table 8.1 Outputs for a three-bit flash ADC

X_6	X_5	X_4	X_3	X_2	X_1	X_0	C	B	A
0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	1	0	0	1
0	0	0	0	0	1	1	0	1	0
0	0	0	0	1	1	1	0	1	1
0	0	0	1	1	1	1	1	0	0
0	0	1	1	1	1	1	1	0	1
0	1	1	1	1	1	1	1	1	0
1	1	1	1	1	1	1	1	1	1

A suitable GaAs circuit topology can be used to produce the corresponding portions of reference voltages.

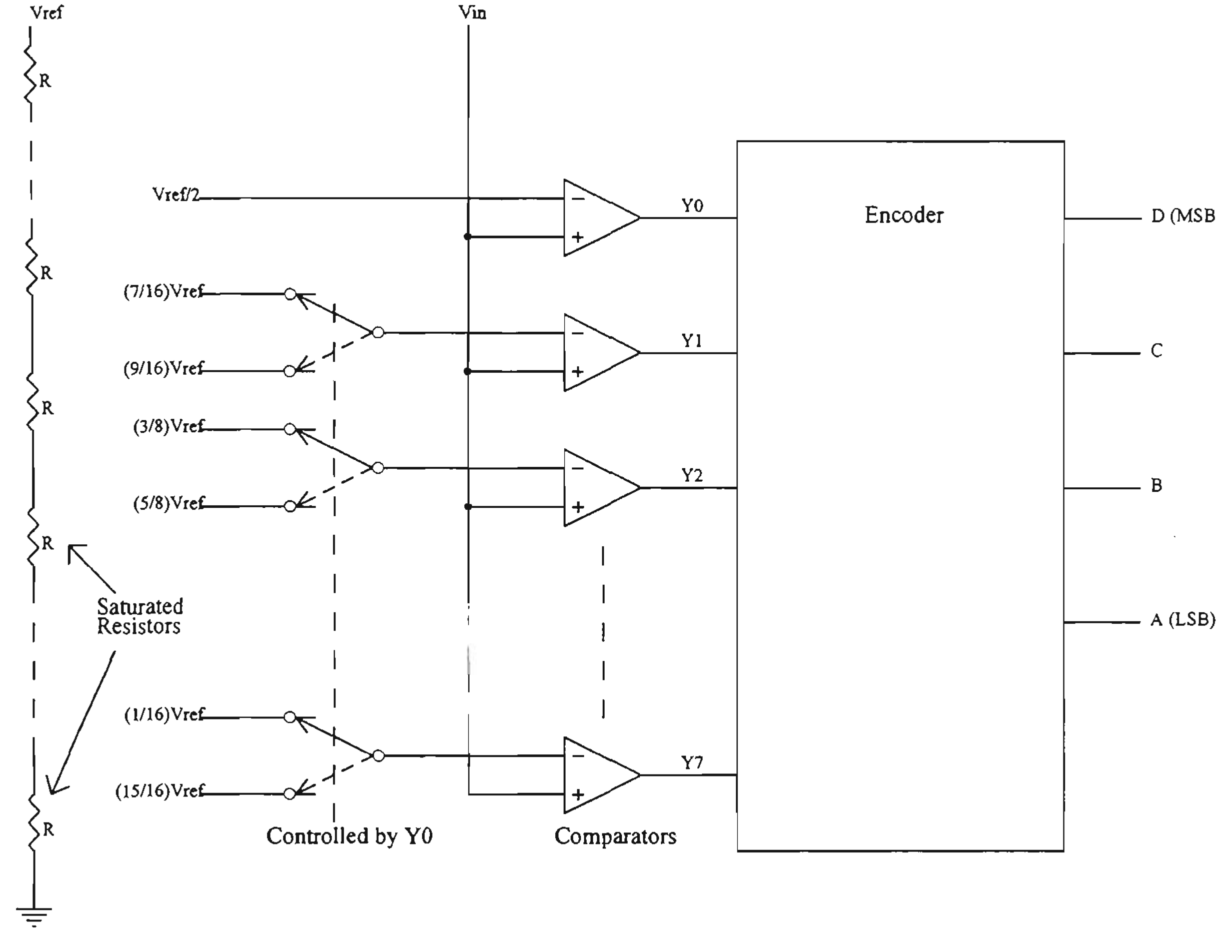


Figure 8.2 Four-bit flash ADC using the above technique.

8.2.2 Design of a Four-bit ADC using above Topology

The steps used in designing a four-bit flash ADC using the above topology are [117]:

(i) Start with $2^{(n-1)}$ comparators and label them in the ascending order as shown in Figure 8.2. Connect the noninverting inputs of all the comparators to the analog input voltage V_a. Set the inverting input of the comparator 'zero' to $V_{ref}/2$.

(ii) Use the output of this comparator to control the switches, which have their outputs connected to the inverting input of the other comparators. Connect the inputs of the switches to the appropriate portions of the reference voltages.

(iii) Encode the output of the comparators into appropriate binary values using the truth table of Table 8.2.

Table 8.2 Relationship between comparator outputs and ADC outputs

Y_0	Y_1	Y_2	Y_3	Y_4	Y_5	Y_6	Y_7	D	C	B	A
0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	1	0	0	0	1
0	0	0	0	0	0	1	1	0	0	1	0
0	0	0	0	0	1	1	1	0	0	1	1
0	0	0	0	1	1	1	1	0	1	0	0
0	0	0	1	1	1	1	1	0	1	0	1
0	0	1	1	1	1	1	1	0	1	1	0
0	1	1	1	1	1	1	1	0	1	1	1
1	0	0	0	0	0	0	0	1	0	0	0
1	1	0	0	0	0	0	0	1	0	0	1
1	1	1	0	0	0	0	0	1	0	1	0
1	1	1	1	0	0	0	0	1	0	1	1
1	1	1	1	1	0	0	0	1	1	0	0
1	1	1	1	1	1	0	0	1	1	0	1
1	1	1	1	1	1	1	0	1	1	1	0
1	1	1	1	1	1	1	1	1	1	1	1

8.3 Mixed Analog-Digital Design

Mixed analog-digital circuits are the largest growth area in microelectronics. Analog circuitry find wide use in systems applications such as telecommunications, consumer products, data acquisition systems, instrumentation and measurements which need an analog interface to an external environment to couple with digital signal processing systems. Many board-level mixed analog-digital systems have begun to migrate down towards single chip implementation, containing many different parts, both, analog and digital. That means that today's analog circuitry finds more use in mixed analog-digital systems than in stand alone analog circuits. In digital sections of these chips important parameters like noise are only a question of digital wordlength while the analog designers often deal with signals with near infinite levels of resolution.

The success of mixed analog-digital design relies strongly on appropriate design techniques for implementation of these circuits. The analog circuits for the multi-channel data acquisition chip have been implemented using Source Coupled GaAs MESFET logic and the digital circuits have been designed using E-D GaAs MESFET Merged logic.

8.3.1 Source Coupled GaAs MESFET logic

To realise high speed GaAs analog integrated circuits a suitable design technique should be chosen to meet the noise margin, power, speed and the interface requirements with the tolerance to fabrication process and temperature variations. The dispersion of device characteristics through out the chip and wafer is one of the biggest problem in realising integrated circuits in GaAs technology. It also is a very important consideration in comparator design. The threshold voltage of a GaAs MESFET is the difference of the Schottky barrier voltage and the pinch-off voltage. The latter being proportional to the square of the thickness of the active layer. This implies that the threshold is very sensitive to geometric variations. In SCFL circuitry the structure is such that only the relative variations of threshold voltages is important. Hence, the input level required for switching is only dependent on the difference between the threshold voltages of the MESFETs. In most cases the threshold voltage difference between neighbouring MESFETs on a chip is small.

The salient features of a SCFL circuit are as followers:

(i) If the FET's threshold voltage vary from wafer to wafer, the operating point and the output voltage can be adjusted by controlling the reference voltage.

(ii) Due to the source follower buffer, the SCFL circuits are capable of driving many gates.

(iii) Increase in fan in reduces the transition region in transfer characteristic and thus increases the transfer gain. The use of constant current source prevents variations in the output voltage swing and level.

(iv) High input sensitivity and versatility in applications.

SCFL technique seems to be the best choice in the MESFET process for a mix of GaAs digital and analog integrated circuits on the same chip, mainly because of its wide tolerance to threshold voltage range and its immunity to temperature variations. It also has an excellent fan out capability, a small input capacitance and a small discharging time permitting high speed operations.

8.4 Comparator

The comparator is the most critical circuit in a flash ADC, because its accuracy and speed determine the performance of the converter. The comparator speed has two parameters, namely, setup time and delay time. The sum of these parameters, called decision time, determines the time required by the comparator to determine a valid logic output level for a given difference in the magnitude of the inputs. The resolution of the comparator is also very important because it affects the resolution of the ADC. Two parameters determine the comparator resolution, namely, offset and hysteresis. Both of these parameters can be measured from the comparator transfer curve. Hysteresis and offset determine the smallest possible voltage difference which can be reliably sensed or resolved, and therefore the resolution that can be obtained from the ADC. Offset matching between comparators is a major design concern in configuring a flash ADC. The offset plus hysteresis between each comparator has to match to within one LSB in order to avoid errors like missing codes.

8.4.1 Comparator Implementation

A circuit diagram of a comparator using E-D GaAs MESFETs is shown in Figure 8.3. The circuit is based on a high gain cascade SCFL structure as a switching stage and a source follower level shifter for each output. When the input signal, V_{in}, is applied to MESFET1 of the differential amplifier, the voltage V_{in} is compared with the fixed reference voltage V_{ref} applied to MESFET2. Then either, MESFET1 or MESFET2 can switch on, (in the current mode) depending on whether V_{in} is higher or lower than the reference voltage V_{ref}. The characteristics of a comparator is characterised by the switching behaviour of differential pair. The drain current flow for the differential pair is given by:

$$I_{ds1} = \frac{I_0}{2} + \frac{\beta_1 (V_{in} - V_{ref})}{2} . \sqrt{\frac{2.I_0}{\beta_1} - (V_{in} - V_{ref})^2} \quad \textbf{(8.0)}$$

$$I_{ds2} = \frac{I_0}{2} + \frac{\beta_2 (V_{in} - V_{ref})}{2} . \sqrt{\frac{2.I_0}{\beta_2} - (V_{in} - V_{ref})^2} \quad \textbf{(8.1)}$$

where I_{ds1} and I_{ds2} are the drain currents for MESFET1 and MESFET2 respectively,

β_1 and β_2 are the HSPICE parameters dependent on the process and geometry of E-MESFET1 and E-MESFET2 respectively, and

I_0 is the current flow through the common source.

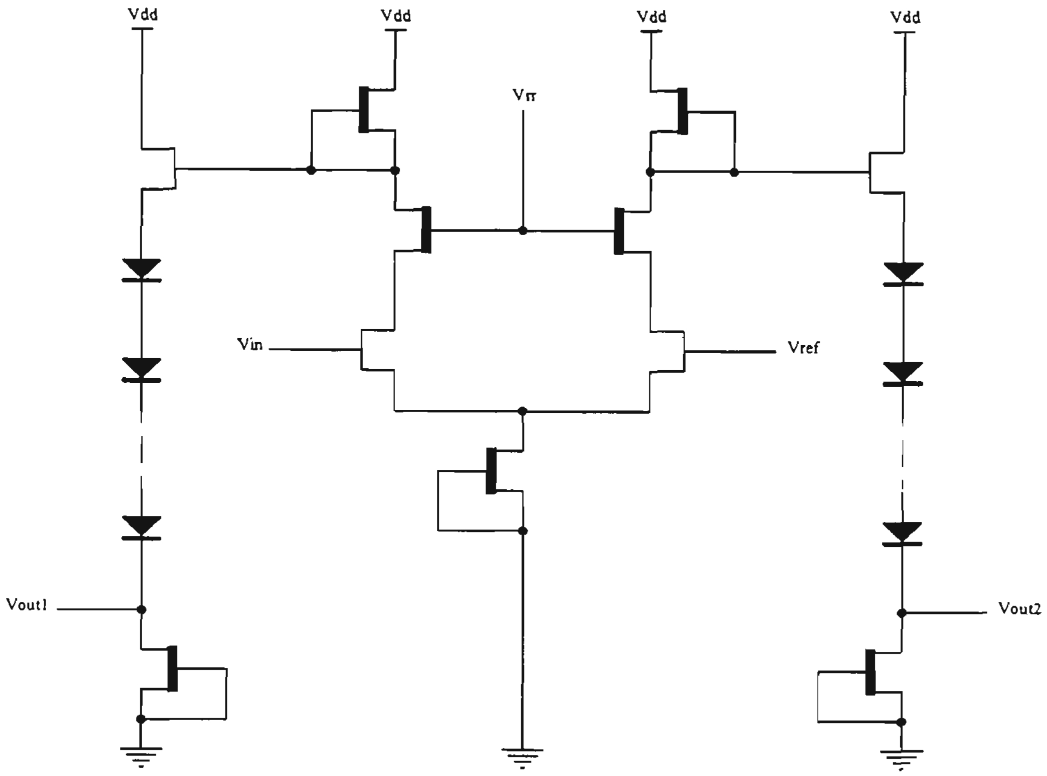


Figure 8.3 Comparator implementation.

From the switching characteristics described by the above expressions, it can be concluded that switching of the differential amplifier occurs independent of the device threshold voltage. As discussed in Chapter 4, this circuit has large voltage swing, is insensitive to threshold voltage variation, has excellent noise margin and relative large incremental gain. The circuit also exhibits an excellent symmetry in the two outputs, even though, the input is only single rail.

8.5 Encoder

The encoder translates the outputs of the comparators into a final binary outputs. Using the truth table of Table 8.2 the logic expressions for the four outputs (D, C, B, and A) can be expressed in terms of the comparator outputs as follows:

$$D = Y_0 \tag{8.2}$$

$$C = Y_4 \tag{8.3}$$

$$B = (Y_2 + Y_6).(Y_2 + \overline{Y_4}).(\overline{Y_4} + Y_6) \tag{8.4}$$

$$\begin{aligned} A = {} & (Y_5 + \overline{Y_6}).(Y_3 + \overline{Y_4}).(Y_1 + \overline{Y_2}).(Y_3 + \overline{Y_2}) \\ & (Y_5 + \overline{Y_4}).(Y_7 + \overline{Y_6}).(Y_1 + Y_2) \end{aligned} \tag{8.5}$$

where Y_0, ... Y_7 are the outputs of the eight comparators.

E-D GaAs MESFET Merged logic design technique was chosen for the implementation of the encoder. This design methodology combines DCFL with SDCFL and SFFL to exploit the advantages of each logic class and to achieve circuit performance which is superior to that obtained from the different individual design approaches. The Merged logic design technique, predominantly uses DCFL to achieve higher packing density and to improve circuit performance, SDCFL technique to provide drive for large capacitive loads and to realise the And-Or-Invert (A-O-I) functions, and, SFFL to implement large fan out. In this way, significant performance improvement can be achieved. Increasing fan out degrades the performance of DCFL circuit because of the reduced ability of the D-MESFET to drive the E-MESFET of the fan out load. The drain to source leakage current of the E-MESFET restricts the fan in capability of the DCFL. The logical circuit representation for the encoder, based on NOR/OR structure, is shown in Figure 8.4. Interfacing the analog circuits, operating at 12 volts supply, to the low voltage digital circuits operating at a supply voltage of 1.5 volts, required appropriate level shifting.

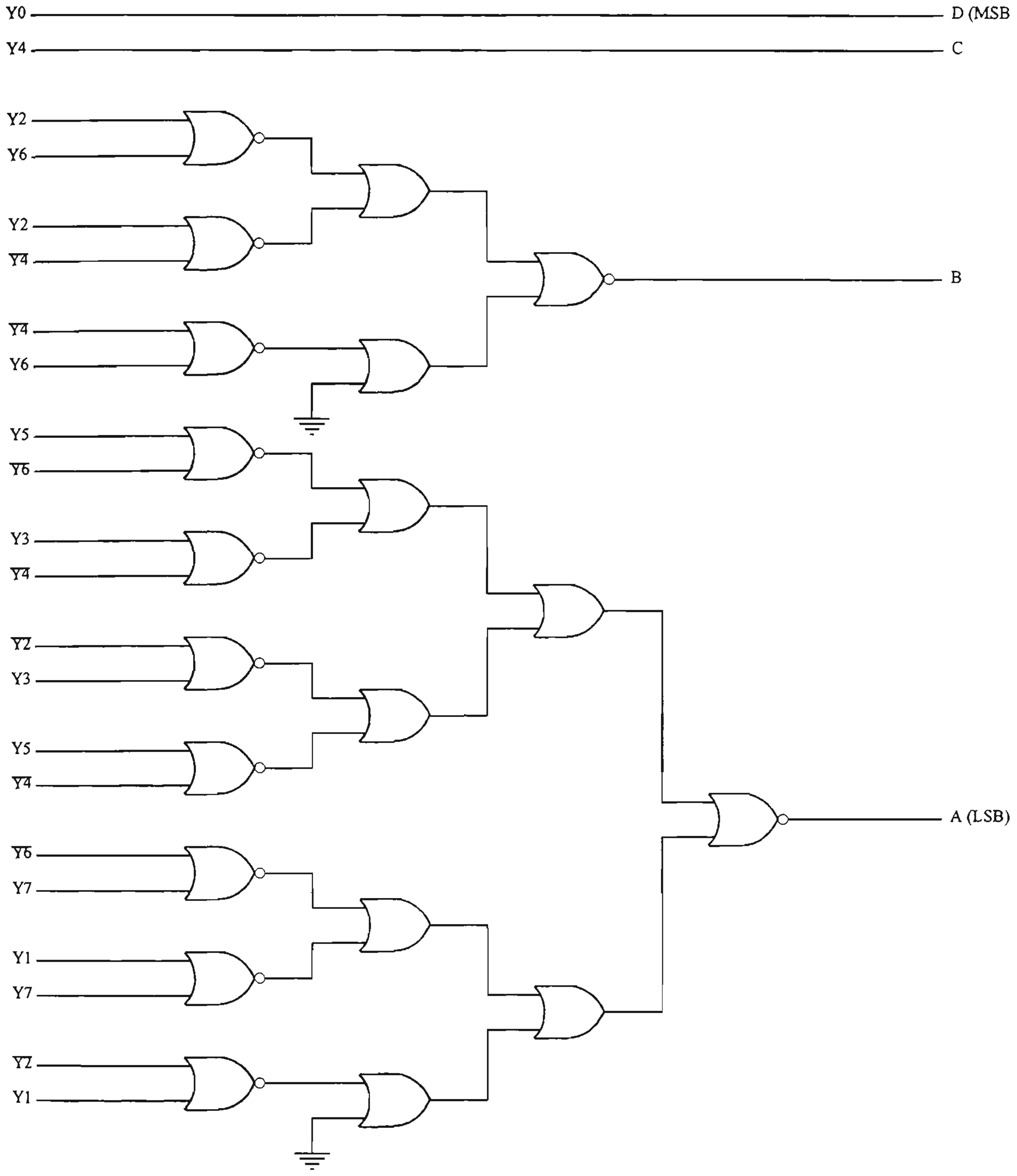


Figure 8.4 Logical representation of the encoder.

See Appendix H for the details of the encoder design.

8.6 Cascading Analog-to-Digital Converters

Multi-bit flash ADC can be designed by cascading a number of four-bit flash ADC modules, for example, a four-bit flash ADC by cascading two two-bit flash modules. In the cascaded implementation of two modules, two stages of comparison are made on the given analog input. For an analog input voltage, V_{in}, lying in the full scale range of 0 - V Volts, the first comparison is made for the three voltage levels at V/4, V/2, and 3V/4. The most significant two-bit digital outputs, D and C are determined, as in conventional flash ADC. As a carry-over operation, the next stage of comparison is made on the residue of the analog input voltage, V_{in}, from the analog equivalent of the most significant two-bits, producing the least significant two bits of the digital outputs, B and A. Before making this comparison, the residue voltage is amplified four times so as to use the same reference voltage levels for comparisons at the different stages. In general, an amplification factor of 2^n is needed for a n-bit flash module.

Figure 8.5 shows the structure of a four-bit flash module that can be cascaded to form a multi-bit flash ADC [38]. D, C, B, and A represent the digital outputs of the flash converter while V_a is its equivalent analog voltage. These bits (D, C, B, and A) control the switching of the reference voltages V/2, V/4, V/8, and V/16 respectively to the summing amplifier. The inverted analog input forms the fifth input of the summing amplifier. The gain factor of sixteen is used, thus the difference voltage, V_a, is defined by: $\{[V_{in}$ - {analog equivalent of (D, C, B, and A)}] x 16$\}$.

A sixteen-bit ADC can be realised using four cascaded four-bit modules as shown in Figure 8.6. The analog voltage of the first module serves as the analog input to the ADC. The combined digital outputs provided by the modules would form the overall digital output of the ADC. The front-end module gives the most significant bits while the tail-end module provides the least significant bits.

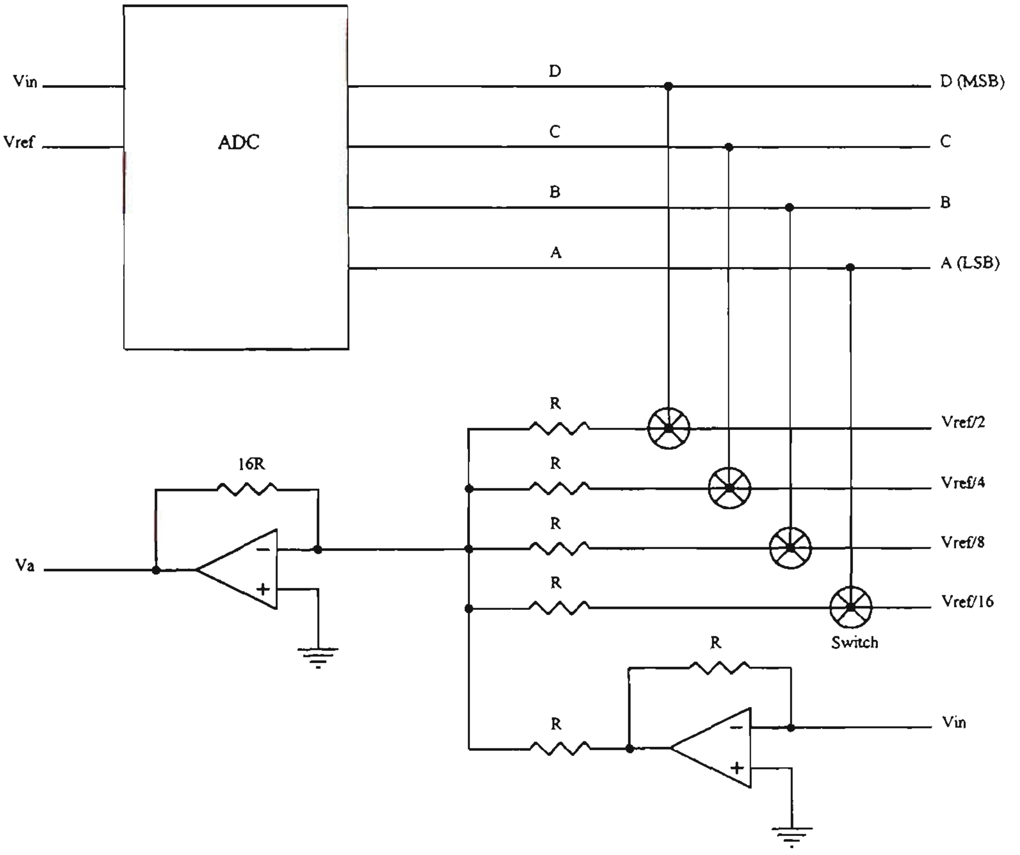


Figure 8.5 Four-bit flash ADC module.

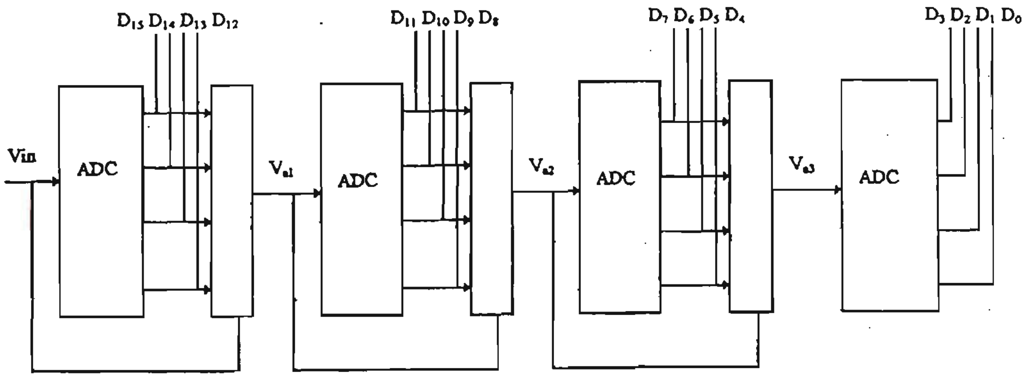


Figure 8.6 Cascading flash ADCs.

8.7 Analog-to-Digital Converter Layout and Performance

The component blocks of the four-bit flash ADC were implemented using E-D GaAs MESFETs with gate length of 0.8 micron. The comparators were designed using the Source Coupled GaAs MESFET logic and the encoder was designed using the E-D GaAs MESFET Merged logic design technique.

The layout methodology has significant influence upon the performance of the circuit. Communication paths between cells and positioning of power and ground busses have significant influence upon the performance of high speed VLSI systems. For example, fast transitions on signal bus could bring about significant noise on the power bus. Thus, both the design methodology and layout will have to address the influence of coupling between busses on performance.

The placement of power and ground busses adjacent to each other reduces their self inductance, and hence their susceptibility to current transients. From the results of coplanar strip line and coplanar waveguide models, the inductance of the power bus is reduced by a factor of two to three when they are placed in the proximity of one another [106]. The ring notation approach, discussed in Chapter 5, exploits this advantage and enables the designer to layout the skeleton of the circuit rapidly, paying particular attention to power and signal busses between adjacent circuitry.

Using the above design methodology and layout approach, the circuits were implemented using ISD VLSI design suite running on Sun workstation. The VLSI layouts for a comparator, encoder and the four-bit flash ADC are shown in Figures 8.7(a), (b), and (c).

The above circuits have been analysed and evaluated using GaAs net extractor and HSPICE circuit simulation tools. The simulation results indicated a power dissipation of 11.12 milliWatts with propagation delay of 0.31 nanosec for the four-bit encoder with a supply voltage of 1.5 Volts. The comparator, which operated from a supply voltage of 12 Volts dissipated 17.13 milliWatts with the hysteresis of 0.3 Volts. Table 8.3 details the results for the four-bit flash ADC and its components.

The sampled HSPICE simulation results for the four-bit flash ADC and the components are shown in Figure 8.8. Figure 8.8 (a) shows the simulation results for a comparator, where VIN1, VIN2, VIN3, and VIN4 represent the input voltage, vin, circuit reference voltage, vref, comparator true and complementary outputs, out1 and out2 respectively. The power waveform represents the power dissipated by the circuit. Figure 8.8 (b) shows the results for the encoder, where VIN1 and VIN2 represent the two LSBs (Z3 and Z4 respectively). The inputs to the encoder are represented by the waveforms of VIN3, VIN4, VIN5, VIN6, VIN7, and VIN8. The power waveform represents the power dissipated by the encoder circuit. Figure 8.8 (c) shows the simulation results for a four-bit ADC, where VIN1, VIN2, VIN3, VIN4, and VIN5 represent the input voltage, vin, and the outputs Z1, Z2, Z3, and Z4 respectively. The power waveform represents the power dissipated by the four-bit ADC.

Table 8.3 HSPICE simulation results

Description	Comparator	Encoder	4-bit Flash ADC
Number of Devices	31	85	333
E-MESFET	4	42	42
D-MESFET	7	33	89
Diodes	20	-	160
Gate Length	0.8 micron	0.8 micron	0.8 micron
Propagation Delay	0.36 nanosec	0.31 nanosec	-
Rise Time		0.21 nanosec	0.26 nanosec
Out1	0.36 nanosec	-	-
Out2	0.41 nanosec	-	-
Fall Time	-	0.17 nanosec	0.28 nanosec
Out1	0.32 nanosec	-	-
Out2	0.36 nanosec	-	-
Power Dissipation	17.13 milliWatts	11.12 milliWatts	120.6 milliWatts
Noise Margin	0.6 Volts	0.35 Volts	0.35 Volts
Hysteresis	-	-	0.3 Volts
Conversion Time	-	-	0.62 nanosec

where Out1 and Out2 are the two outputs of the comparator.

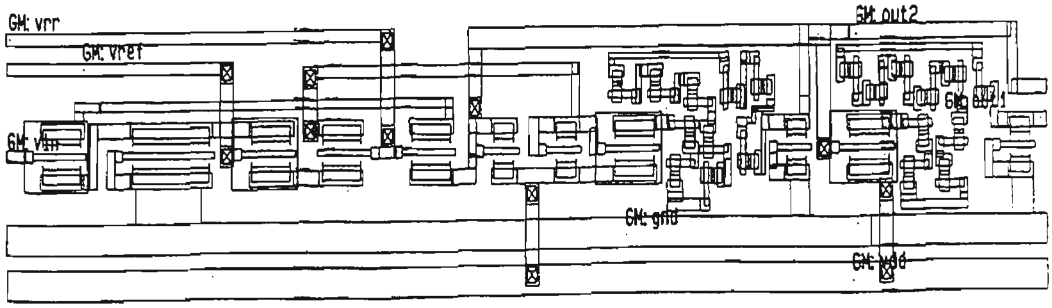


Figure 8.7 (a) Mask level layout of a comparator.

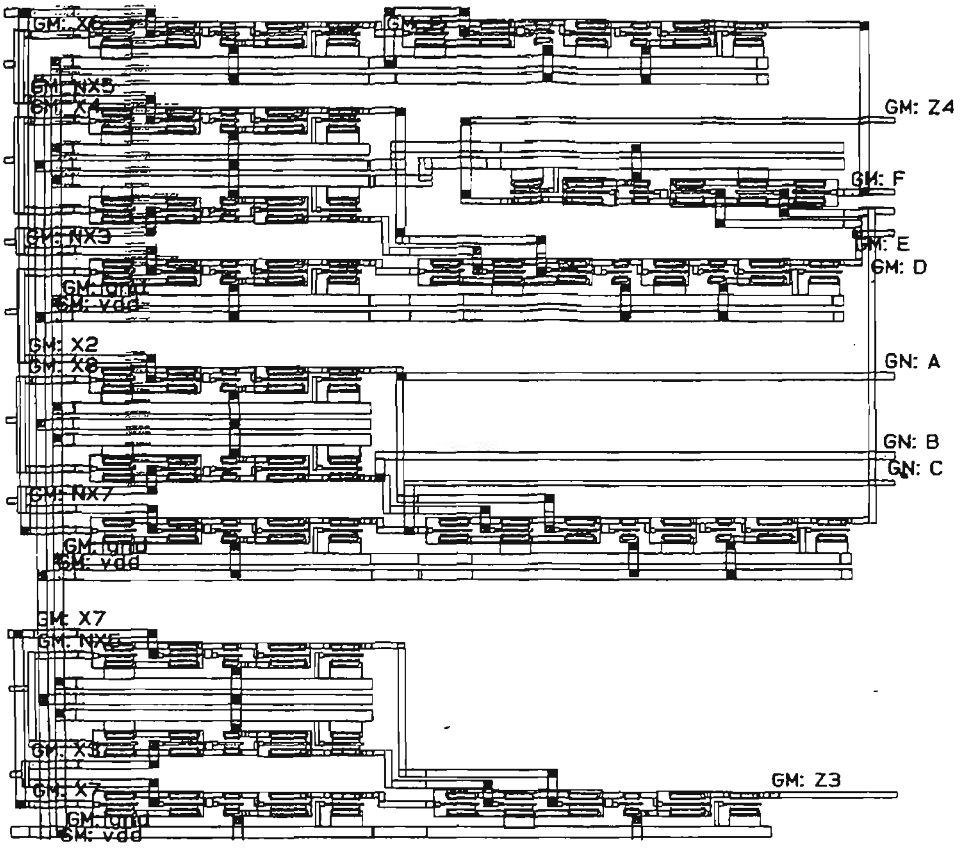


Figure 8.7 (b) Mask level layout of an encoder.

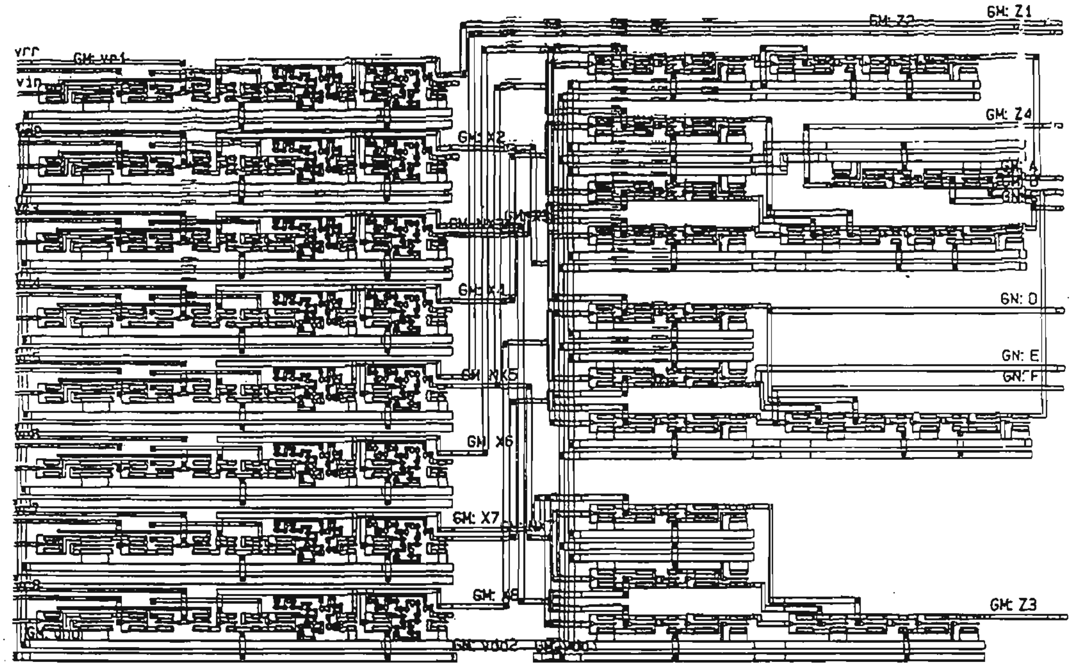


Figure 8.7(c) Mask level layout of a four-bit flash ADC.

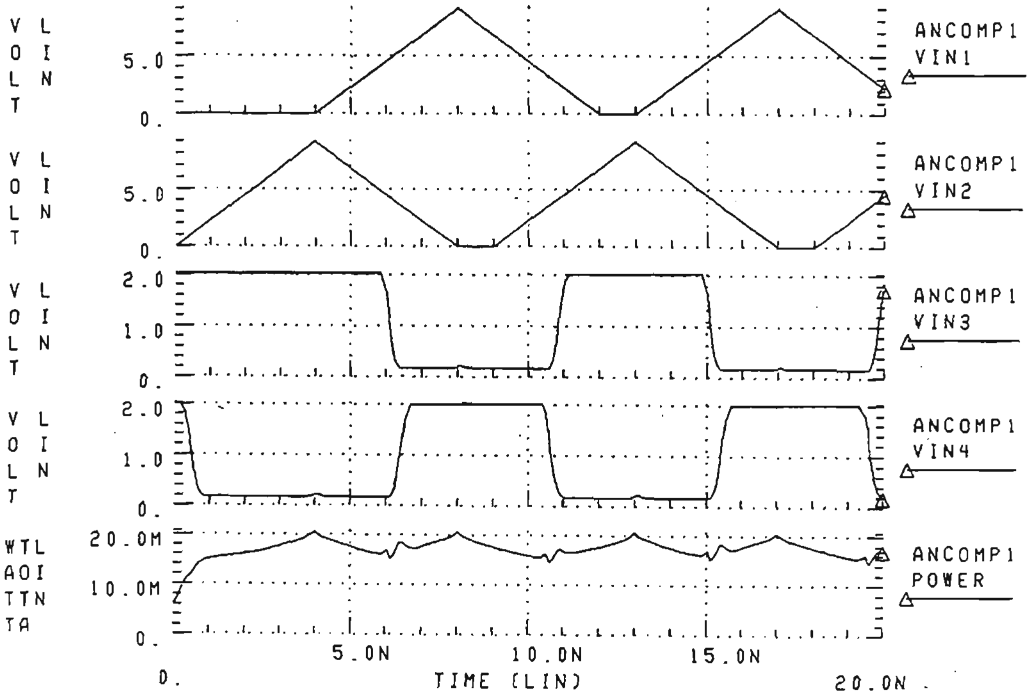


Figure 8.8 (a) HSPICE simulation for a comparator.
VIN1, VIN2, VIN3 and VIN4 represent vin, vref, true and complementary comparator outputs.

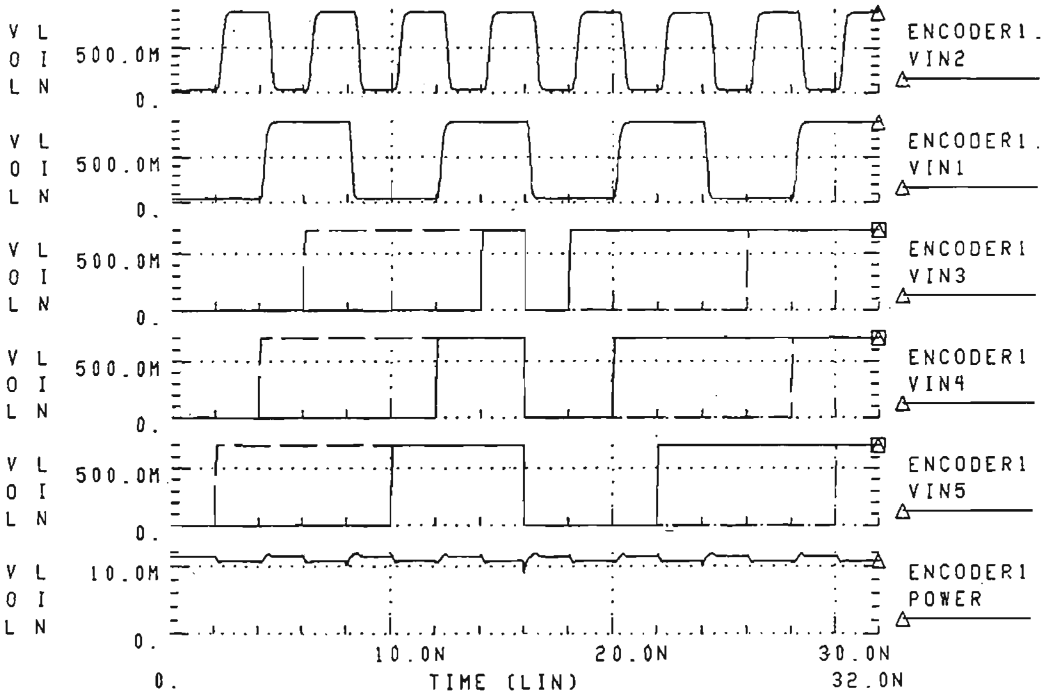


Figure 8.8 (b) HSPICE simulation for an encoder.
VIN1 and VIN2 represent the encoder outputs Z3 and Z4. VIN3 - VIN8 represent the encoder inputs.

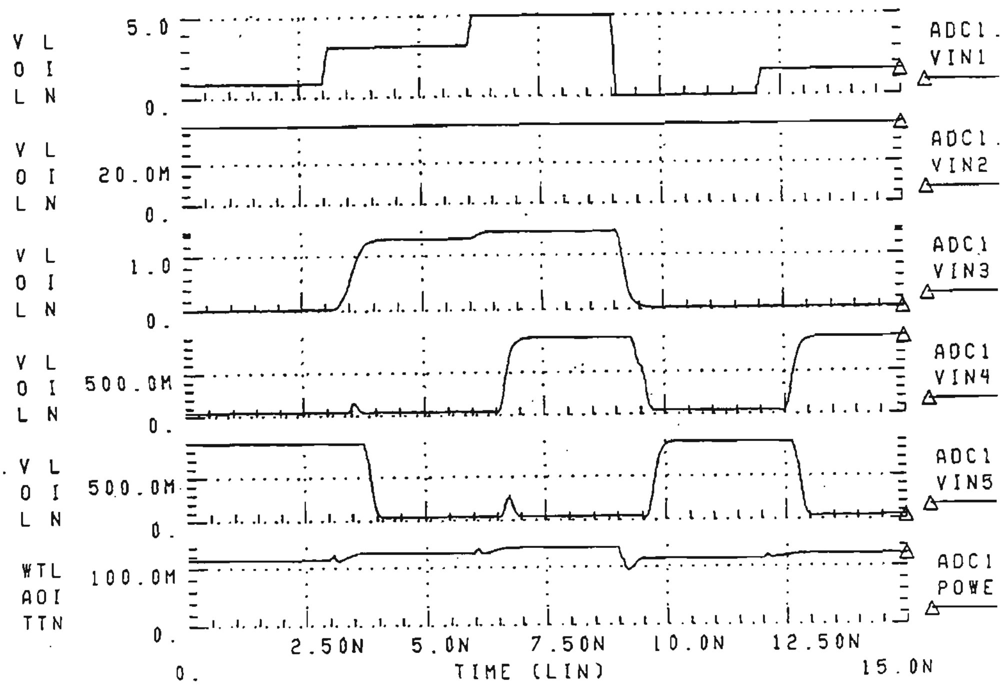


Figure 8.8 (c) HSPICE simulation for a four-bit flash ADC.
VIN1 - VIN5 represent the input voltage, vin, and the outputs Z1 - Z4 respectively.

8.8 VLSI Implementation of Four-Bit Multi-Channel Data Acquisition Chip

The four-bit multi-channel data acquisition chip, containing a analogue comparator, an encoder and multiplexer, was designed and implemented using Integrated Silicon VLSI design suite. To obtain low power, high speed, good noise margin and fan out, E-D GaAs Merged logic design technique was chosen for digital circuits. SCFL design technique was chosen for the design of the analog circuits on the same chip, mainly because of: its wide tolerance to threshold voltage variation, its immunity to temperature variations, its excellent fan out capability, its small input capacitance and a small discharging time (permitting high speed operations).

Figure 8.9 shows the floor plan for the four-bit multi channel data acquisition chip. It encompasses all the necessary design criteria, including placement of the input and output signals so that the cells can be assembled with minimum length routing paths between cells. Figure 8.10 shows the VLSI layout of the four-bit multi channel data acquisition chip.

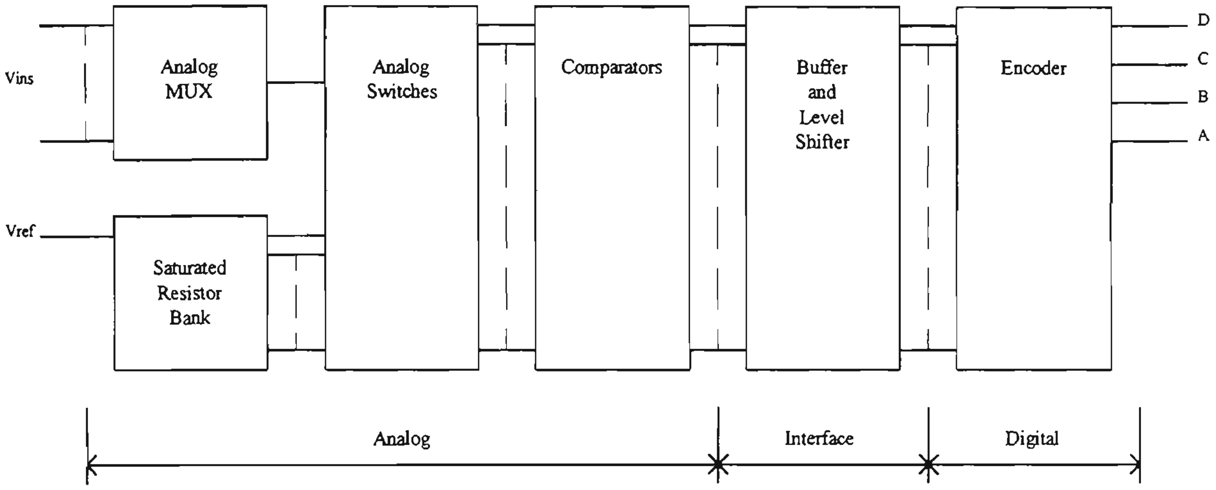


Figure 8.9 Floor plan for a four-bit multi-channel data acquisition chip.

8.9 Simulation and Performance

The four-bit multi-channel data acquisition chip was analysed and evaluated using GaAs net extractor and HSPICE circuit simulation tools. Table 8.4 details the results for the data acquisition chip.

Figure 8.11 shows the HSPICE simulation results, for different input conditions, where VIN1 represents the multiplexer control signal, VIN2, VIN3, VIN4, and VIN5 represent the four output bits of the data acquisition chip, and VIN6 represents the inputs to the two channels of the chip. From the results, it can be seen that this design technique gives large logic swings resulting in excellent noise margin. The total power dissipation for the chip is 185.6 milliWatts, indicating the suitability of this design technique in implementing VLSI circuits.

Table 8.4 Performance of the four-bit multi-channel data acquisition chip

Description	Data Acquisition Chip
Number of devices	397
E-MESFET	84
D-MESFET	138
Diodes	160
Saturated Resistors	15
Gate length	0.8 micron
Power dissipation	185.6 milliWatts
Noise margin	0.35 Volts
Conversion Time	0.85 nanosec

8.10 Conclusions

This chapter presents the design and implementation of a GaAs VLSI ultrafast multi-channel data acquisition chip. Appropriate design techniques and technology have been chosen for the design of this mixed analog-digital chip. SCFL technique is the best choice in the MESFET process for a mix of GaAs digital and analog integrated circuits on the same chip, mainly because of its tolerance to threshold voltage

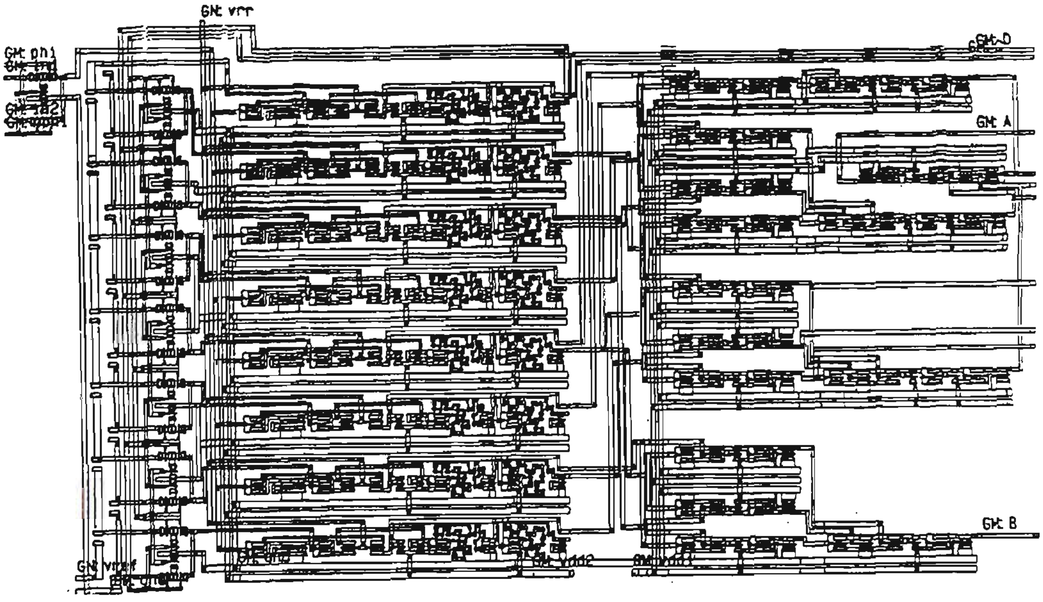


Figure 8.10 Mask level layout of a four-bit multi-channel data acquisition chip.

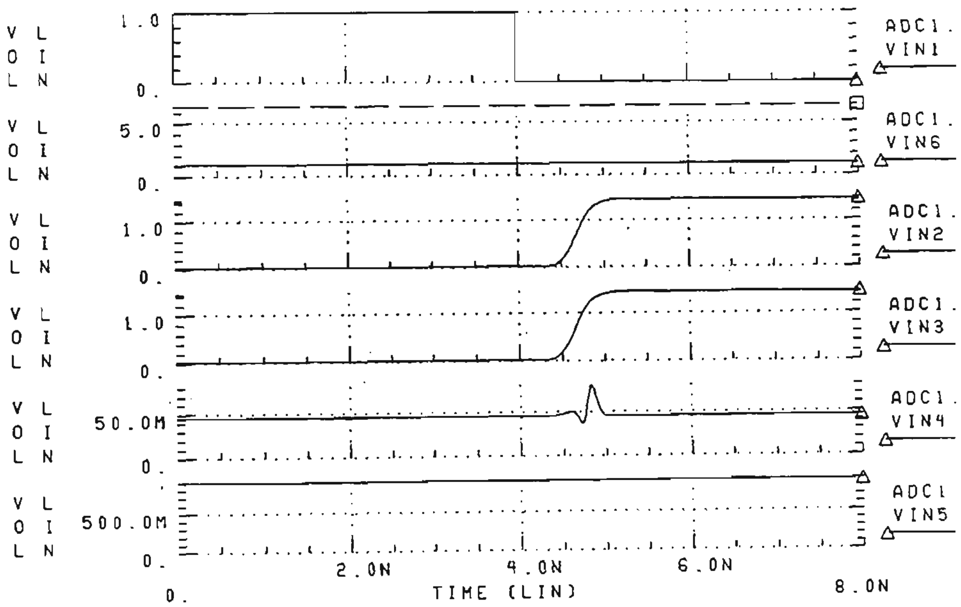


Figure 8.11 HSPICE simulation results for a data acquisition chip.
VIN1 - VIN5 represent the multiplexer control and the outputs of the data acquisition chip DCBA respectively. VIN6 represents the inputs to the chip.

range and its immunity to temperature variations. It also has an excellent fan out capability, a small input capacitance and a small discharging time permitting high speed operations. Digital components have been designed using E-D GaAs Merged logic design technique. This concept combined DCFL with SDCFL and SFFL so that the advantages of each logic class could be exploited. The circuit performance achieved using this technique was much superior to that obtained if the circuit had been implemented with any one of the logic class exclusively.

Design of a flash ADC as presented, required only $\mathbf{2^{(n-1)}}$ comparators to implement a n-bit flash ADC. The most significant bit of the comparator output formed the control signal for switches, which connected the appropriate reference voltages, depending on the input signal level, to the remaining comparators. This approach greatly reduced the complexity of the flash ADC. Depending upon the application, high resolution ADC could easily made by cascading four-bit flash ADC modules.

The multi-channel data acquisition chip needed 397 devices and dissipated 185.6 milliWatts of power. The conversion time was 0.85 nanosec with noise margin of 0.35 Volts. These results indicated the appropriateness of the design technology and techniques used for mixed analog-digital circuits on a single chip.

Chapter Nine

VLSI Implementation of an Eight-bit Multi-Function Multi-Protection Relay

If all the computer companies continue to buy all their logic devices from the merchants, the uniqueness of their computer products would disappear.

Peter R. Treiney.

9.0 Chapter Overview

This chapter describes the design, implementation and performance of an eight-bit multi-function multi-protection relay implemented using E-D GaAs MESFET Merged logic design technique.

9.1 Introduction

Modern power systems need to generate and supply high quality electric energy to the consumers. A growing demand for accurate, selective and reliable overcurrent relays have increased recently due to an increase in the complexity and capacity of power systems. Advancements in digital technology associated with power industry has had strong impact on the development of power system protection equipment and techniques.

Computer based digital relaying techniques have been well established in many aspects of power system protection [41, 42]. The availability of cheap and powerful microprocessors in recent years have led to their increasing use in power systems protection. Several types of microprocessors have been used to implement different type and level of relaying techniques. An eight-bit, microprocessor-based, overcurrent relay was developed [109], in which Intel 8085 microprocessor was used in the implementation of single input overcurrent relaying system. Further research using the same processor led to the development of a multiple overcurrent relay [42]. Recently a 32-bit relaying technique for power system protection was developed [47], in which a Motorola MC68020 microprocessor was used to provide a multi-function protection scheme with required speed, accuracy and reliability.

Recent developments in microelectronic technology, in particular the GaAs digital technology, has led to the application of VLSI GaAs ICs in high speed, low power relaying techniques for power system protection schemes.

9.2 Hybrid Characteristic Overcurrent Relay

The flow chart in Figure 9.1 characterises the operation of a hybrid overcurrent relaying system for power protection. For each overcurrent protection section, a look-up table stores the fault current values and the time-out delays based on time-current characteristics described by equations 7.13 - 7.16 in Read Only Memory. The relay monitors the magnitude of the incoming signal (phase and line currents and voltages) via data acquisition circuit (multiplexer, signal conditioning circuit and analog-to-digital converter) and compares this with the set value stored in memory as a look-up table. At this point in time the timer is loaded with an appropriate time-out value and waits for the controller to signal the start of time-out period. If the output of the comparator indicates that the monitored signal is greater than the set value, the controller starts the time out period. At the end of the time-out period, the controller checks if the monitored signal is still greater than the set value. If the monitored current is still greater than the set value, the controller generates the trigger pulse to enable the appropriate circuit breakers. The controller also communicates its status with the other relays. In the case where the monitored signal falls below the set value during the time-out period, the controller resets the timer with an appropriate time-out value and waits for the signal from the comparator to start the time-out period. The controller monitors all the signals in turn in a particular section under protection before monitoring the next section.

9.3 VLSI Design Technology

Silicon metal-oxide semiconductor has been the main medium for computer and system applications for a number of years and will continue to fill this role in the foreseeable future. However, silicon logic has speed limitations that are already becoming apparent in the state-of-art, fast, digital system design. Paralleling the developments in silicon technology, GaAs based technology has also produced some very interesting results.

Although the GaAs technology has been confronted with similar technological problems as did silicon technology in the 1970's, during the last few years considerable progress has been made in GaAs integrated circuitry and the fabrication technology has progressed to a point were a number of foundries are providing GaAs circuit fabrication.

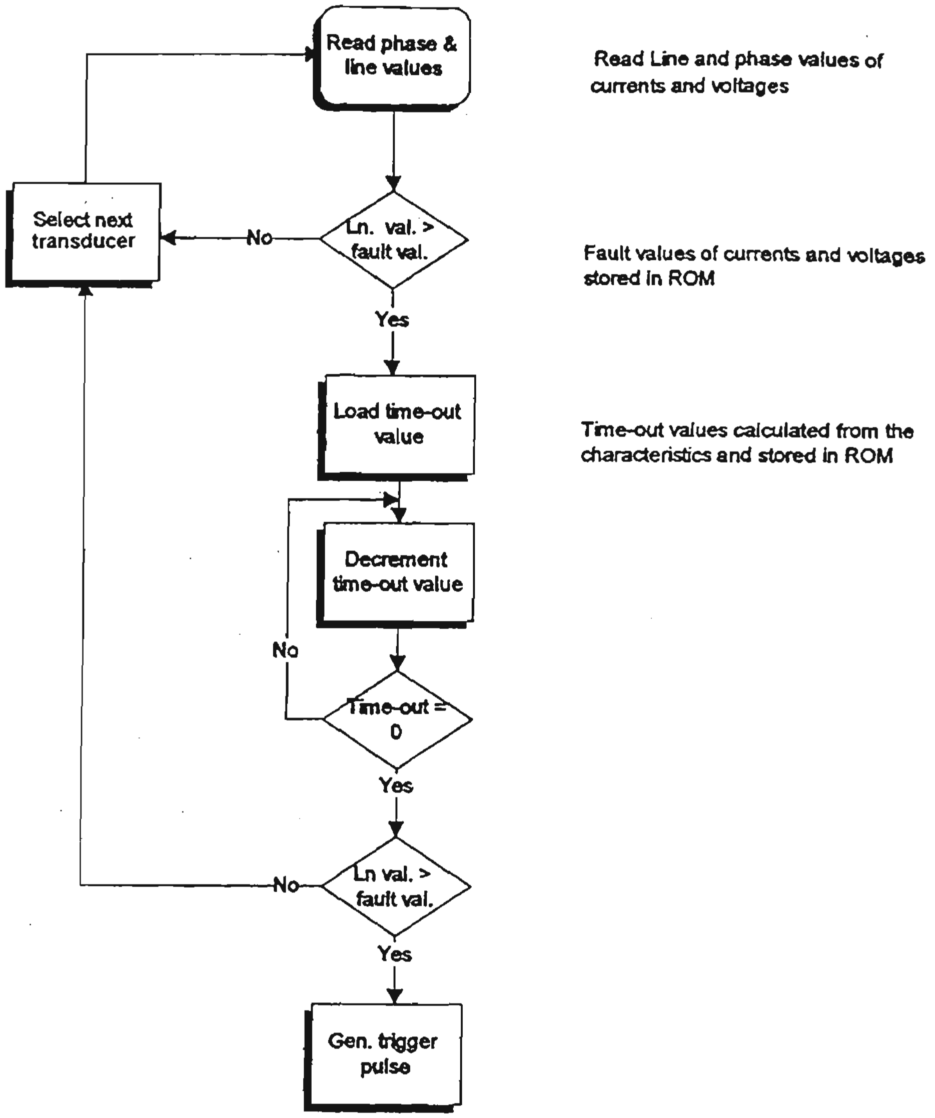


Figure 9.1 Flow chart for relay operation.

9.3.1 Choice of Technology

There is a need for high speed and low power digital ICs in many high performance military and commercial systems, including digital memories, digital signal processing and power system protection. Emerging silicon-based technologies, employing advanced processes, [49 - 51] have significantly improved the performance of silicon devices but the need for even higher speed continues. In a research and development environment, GaAs digital circuits have clearly outperformed silicon circuits in power-delay performance, as exemplified by a GaAs D-flip flop that worked at up to 5.1 GHz and dissipated only 1.9 milliWatts [6]. In addition to offering outstanding performance, the gate complexity of the GaAs digital IC is increasing. In recent years, the performance and yield of GaAs LSI circuits have increased dramatically due to improved material quality and advancing process technology.

The salient features of GaAs technology which makes it very attractive for high speed, low power applications such multi-function, multi-protection relay for power systems protection include:

(i) Electron mobility of six to seven times that of silicon, resulting in very fast electron transit times,

(ii) Large energy bandgap offers bulk semi-insulating substrate with resistivities in the order of 10^8 ohm-cm. This minimises parasitic capacitances and allows easy electrical isolation of multiple devices in a single substrate. This is an important property in designing mixed analog/digital circuits,

(iii) A wide operating temperature range is possible due to the larger bandgap. GaAs devices are tolerant to wide temperature variations over the range -200°C to +200°C,

(iv) Up to 70% reduction in power dissipation can be achieved over the fastest of the silicon technology logic such as Emitter Coupled Logic,

For a very high speed operation in a semiconductor medium, three factors become significant, namely: carrier mobility, carrier saturation velocity, existence of semi-insulating substrate. Gallium arsenide technology mostly fulfils these requirements, and together with low power dissipation, provides a technology base for a new generation of ICs.

9.4 Hardware Implementation of Multi-Function Multi-Protection Relay

Figure 9.2 shows the structure of an eight-bit multi-function, multi-protection relay. It consists of a magnitude comparator unit capable of comparing two eight-bit numbers

(A_7 - A_0 and B_7 - B_0), a programmable four-bit timer unit and a controller. The eight-bit magnitude comparator unit compares the incoming signals (phase and line currents and voltages) with the fault values of these signals, stored as look-up table in a memory, and generates a control signal if the magnitude of the incoming signal is greater than the fault value. A fully programmable four-bit timer unit incorporates features like asynchronous preset and reset, four-bit parallel load facilities, variable clock speed and four-bit parallel output.

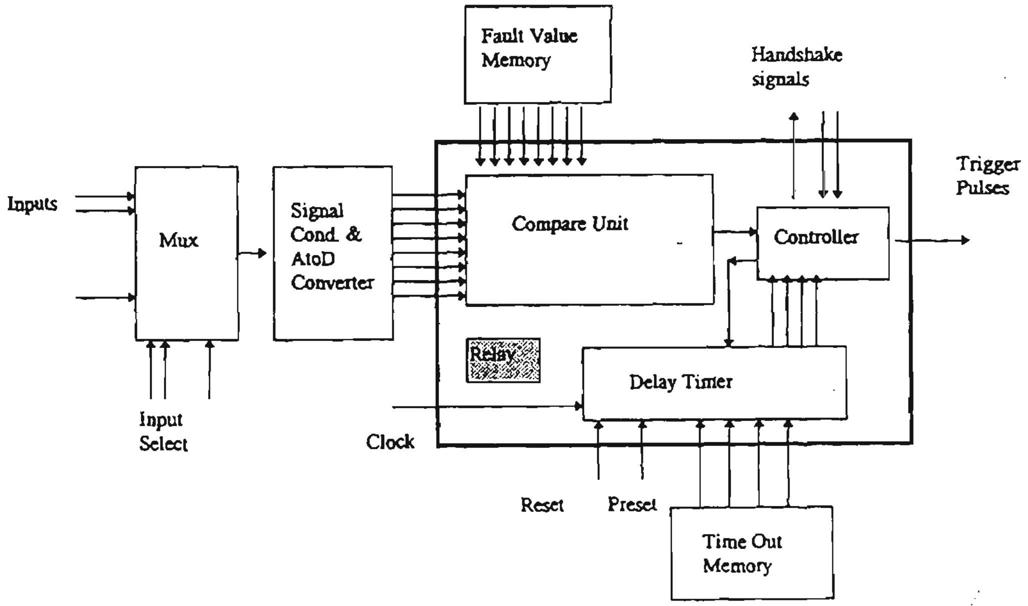


Figure 9.2 Multi-function multi-protection relay.

A look-up table, in a Read Only Memory, stores the time-out periods of the timer, based on definite and inverse time-current characteristics. Timer parallel load facilities are used to download these values into the timer. The controller unit monitors the comparator output and sends a signal to timer unit to either start time-out period or load the time-out value from the look-up table. At the end of time-out period if the magnitude of the incoming signal is still greater than the fault value, the controller generates the trigger pulse to operate appropriate circuit breakers. It also provides handshake signals for other relays in the protection scheme.

This structure gives the flexibility for the relay to be used as multi-function, multi-protection device. The cellular design of the basic unit enables cascading to give the flexibility to the basic units into a larger multi-bit (sixteen, thirty two, etc) multi-function multi-protection relay.

9.4.1 Eight-Bit Magnitude Comparator

This section describes the design, VLSI layout and performance for a cascadable comparator. Figure 9.3 shows an eight-bit comparator block diagram, using cellular structure of bit-slice comparator cells.

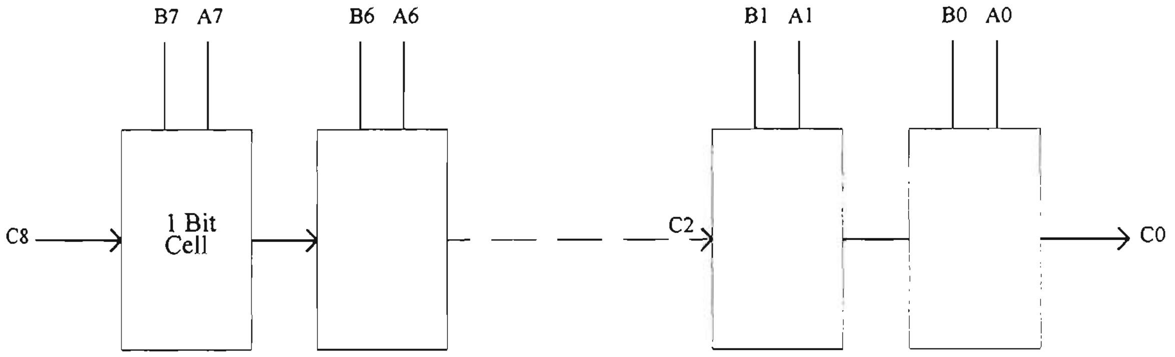


Figure 9.3 Eight-bit comparator functional diagram.

9.4.1.1 Behavioural Description

The block diagram and truth table for a binary one-bit comparator bit-slice is shown in Figure 9.4, where A_i and B_i are the two multi-bit numbers to be compared, C_{i+1} is the input from the output of the previous stage, and C_i is the output of the current stage. $C_i = 1$ for $A_i > B_i$ and $C_i = 0$ for $A_i = B_i$ and/or $A_i < B_i$.

C_{i+1}	A_i	B_i	C_i
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	0
1	X	X	1

"X" signifies don't care case.

Figure 9.4(a) Comparator cell truth table.

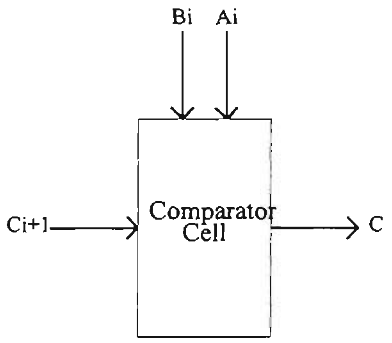


Figure 9.4(b) Bit-slice comparator cell.

The logical expression for the output signal in terms of the three input signals is expressed as follows:

$$\overline{C_i} = C_{i+1} + A_i.\overline{B_i} \qquad \textbf{(9.0)}$$

To make equation 9.0 implementable in E-D GaAs Merged logic, it needs to be transformed into the form:

$$C_i = \overline{(C_{i+1} + \overline{(\overline{A}_i + B_i)})} \tag{9.1}$$

Appendix I presents the detailed design procedure for the eight-bit magnitude comparator.

9.4.1.2 Structural Description

Direct implementation of expression 9.1 gives the logic circuit shown in Figure 9.5.

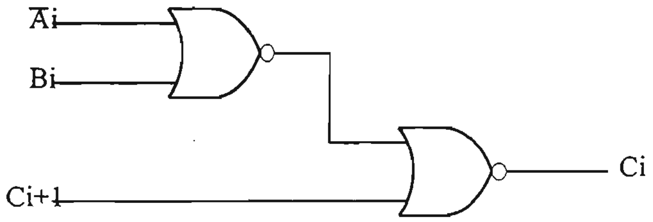


Figure 9.5 Logical representation of a comparator cell.

The critical delay in this circuit is the propagation delay through gates to the output. The gates in this path should be sized appropriately. The final sizing of transistors can only be determined after a series of simulations. Figure 9.6 depicts the transistor level implementation of the cell.

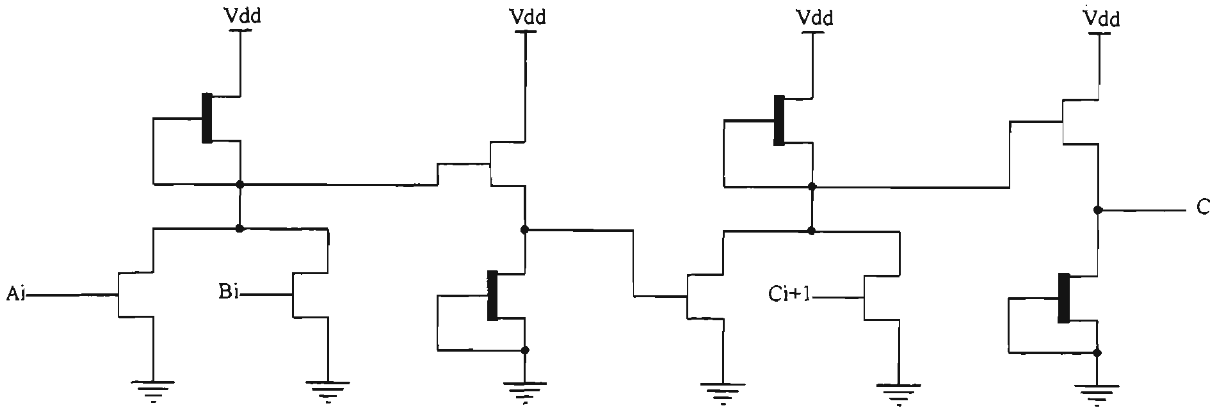


Figure 9.6 Transistor level implementation of a comparator cell.

The operation of the comparator circuit is as follows:

(i) The two binary numbers are compared by starting with the most significant bits. The output from this comparison is passed onto the next most-significant bit cell input. The output signal C_i remains 0 as long as the two bits being compared are either less than or equal to each other.

(ii) As soon as bit A_i is detected to be greater than bit B_i, the output C_i goes to 1.

(iii) All the remaining pairs of less significant bits then have no further affect on the subsequent and final output.

(iv) If all pairs of bits of the two numbers being compared are either equal or less, then the output C_i remains at zero.

9.4.1.3 Physical Description

The eight-bit comparator is realised by butting bit-slice comparator cells. One possibility would be to have both input bits on the same side of the cell with the output propagating at right angles to the input data path. Another possible layout would be to have the two input bits on opposite sides of the cell. The first approach was adopted in this case with each block being four-bits long horizontally. The second four-bit block was replicated vertically. The height of the comparator for each block remains constant while the width grows linearly with the number of bits. This implies that the width of each cell must be made as small as possible.

Figure 9.7 shows a possible floor plan for the eight-bit comparator. The inputs A_i and B_i come in at the top of each cell and C_i propagate horizontally. Power and ground rails also propagate horizontally in global terms. In a complex design, the number of leaf cells should be kept as small as possible, which implies that the complexity of the leaf cells should be as high as possible to gain maximum speed advantage of the GaAs technology. This will greatly simplify the global floor plan.

9.4.2 Four-Bit Timer

This section describes the design, VLSI layout and performance of a time-out synchronous timer. Figure 9.8 shows the block diagram of a four-bit synchronous timer using cellular structure of timer cells.

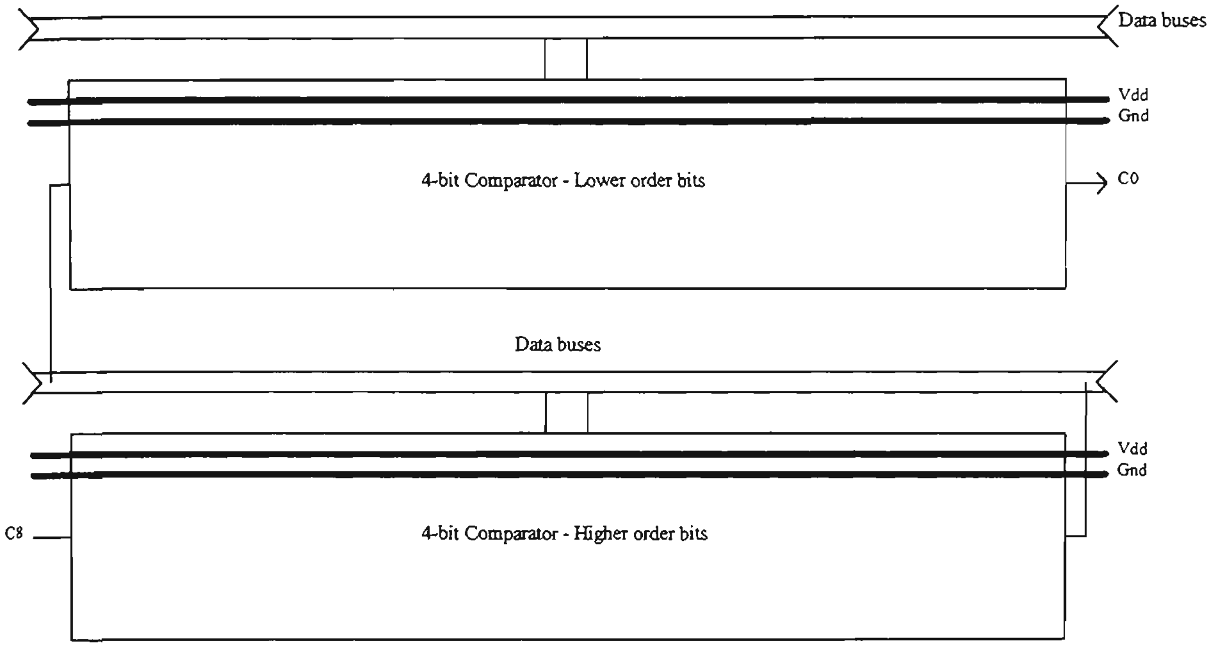

Data buses
Vdd
Gnd
4-bit Comparator - Lower order bits
CO
Data buses
Vdd
Gnd
C8
4-bit Comparator - Higher order bits

Figure 9.7 Floor plan for an eight-bit comparator.

The synchronous timer design minimises the state decoding error due to ripple propagation delay. Synchronous operation occurs by having all flip flops clocked simultaneously, changes in the outputs coincide with each other. However, even in this case decoding error can occur due to possible differences in propagation delay of the flip flops, unequal clock distribution, and unequal rise and fall times of the flip flop outputs. The decoding error in this case persists only as long as it takes for the flip flop to change state plus the maximum time difference in propagation time between flip flops. What is more important, however, in contrast to asynchronous designs, is that the decoding error interval does not depend on the number of flip-flops in the counter.

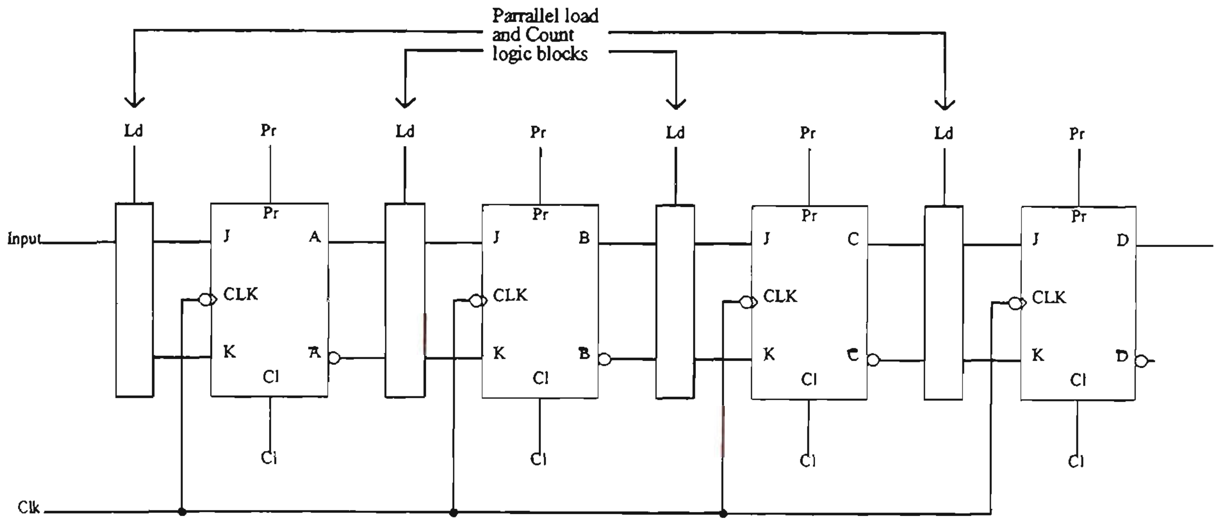


Figure 9.8 Four-bit time-out timer functional diagram.

9.4.2.1 Behavioural Description

The basic building block for a synchronous timer is a J-K flip flop. The flip flop configuration uses a single-phase clock and data input. The truth table and functional representation of a J-K flip flop is shown in Figure 9.9, where J and K are the synchronous inputs, P_r and C_l are the asynchronous preset and clear and Q and Q' are the true and complementary outputs.

The characteristic expression, Q_{n+1}, for J-K flip flop as a function of synchronous inputs, is:

$$Q_{n+1} = J \cdot \overline{Q_n} \oplus \overline{K} \cdot Q_n \qquad (9.2)$$

Figure 9.10 characterises the state graph of the four-bit timer, based on J-K flip flops. Figure 9.11 shows the corresponding state table with the flip flop inputs.

P_r	C_l	J	K	Q_n	Q_{n+1}
0	1	X	X	X	0
1	0	X	X	X	1
0	0	0	0	0	0
0	0	0	0	1	1
0	0	0	1	0	0
0	0	0	1	1	0
0	0	1	0	0	1
0	0	1	0	1	1
0	0	1	1	0	1
0	0	1	1	1	0

Q_n is the output state before the clock pulse and Q_{n+1} is the output immediately after the clock pulse. P_r = C_l = 1 is not allowed.

Figure 9.9(a) Truth table for J-K flip flop.

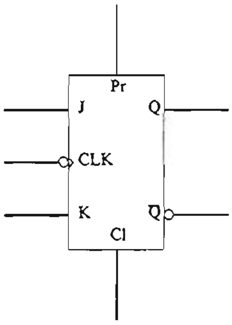


Figure 9.9(b) Functional block diagram for J-K flip flop.

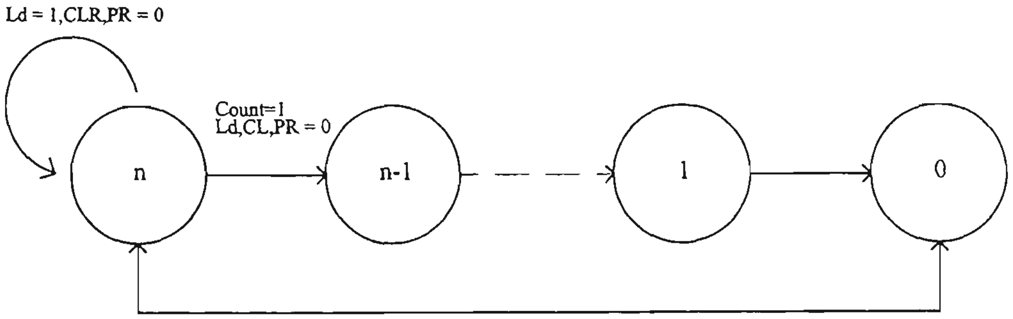


Figure 9.10 Four-bit timer state graph.

D	**C**	**B**	**A**	**D^+**	**C^+**	**B^+**	**A^+**	**J_D**	**K_D**	**J_C**	**K_C**	**J_B**	**K_B**	**J_A**	**K_A**
1	1	1	1	1	1	1	0	X	0	X	0	X	0	X	1
1	1	1	0	1	1	0	1	X	0	X	0	X	1	1	X
1	1	0	1	1	1	0	0	X	0	X	0	0	X	X	1
1	1	0	0	1	0	1	1	X	0	X	1	1	X	1	X
1	0	1	1	1	0	1	0	X	0	0	X	X	0	X	1
1	0	1	0	1	0	0	1	X	0	0	X	X	1	1	X
1	0	0	1	1	0	0	0	X	0	0	X	0	X	X	1
1	0	0	0	0	1	1	1	X	1	1	X	1	X	1	X
0	1	1	1	0	1	1	0	0	X	X	0	X	0	X	1
0	1	1	0	0	1	0	1	0	X	X	0	X	1	1	X
0	1	0	1	0	1	0	0	0	X	X	0	0	X	X	1
0	1	0	0	0	0	1	1	0	X	X	1	1	X	1	X
0	0	1	1	0	0	1	0	0	X	0	X	X	0	X	1
0	0	1	0	0	0	0	1	0	X	0	X	X	1	1	X
0	0	0	1	0	0	0	0	0	X	0	X	0	X	X	1
0	0	0	0	1	1	1	1	1	X	1	X	1	X	1	X

DCBA and $D^+C^+B^+A^+$ are the outputs of the timer immediately before and after the clock transition.

Figure 9.11 State table and input controls for a four-bit timer.

The flip flop input equations in terms of the present state outputs for the four flip flops are derived from the above state table and are described by the following expressions:

$$J_A = K_A = 1 \tag{9.4}$$

$$J_B = K_B = \overline{A} \tag{9.5}$$

$$J_C = K_C = \overline{B}.\overline{A} \tag{9.6}$$

$$J_D = K_D = \overline{C}.\overline{B}.\overline{A} \tag{9.7}$$

These expressions do not take into account the parallel load control. Parallel load is realised via a two-to-one multiplexer at the inputs of each flip flop.

9.4.2.2 Structural Description

The J-K flip flop with asynchronous preset and clear functions has been realised using NOR gates as shown in Figure 9.12. This structure was chosen because it was readily implementable in GaAs Technology. The outputs Q and $Q^{'}$ remain unchanged during the inactive interval of the clock. In addition the outputs remain unchanged during J = K = 0, regardless of the clock transition. When the clock is active the flip flop operates in a manner as described by the truth table in Figure 9.9(a).

The four-bit timer has been realised using J-K flip flops, multiplexers with NOR gate based control logic for the input. All the timer components were designed using E-D GaAs Merged logic design technique. Figure 9.13 shows the logical implementation of the one-bit timer cell.

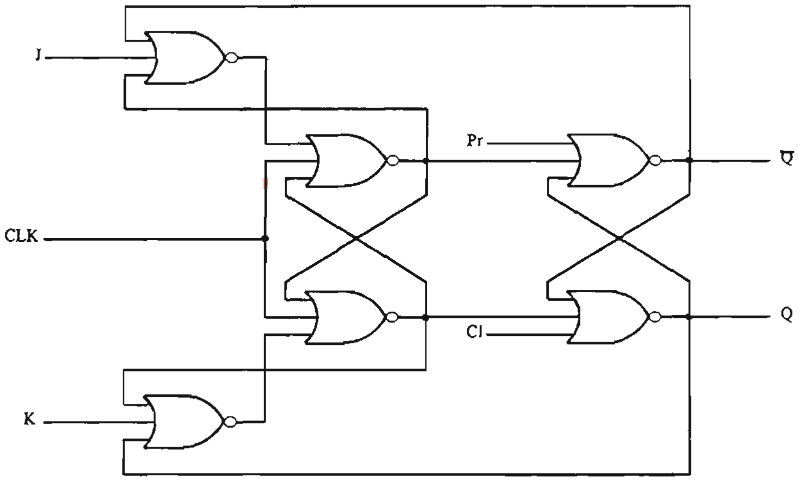


Figure 9.12 Logic representation of J-K flip flop.

The operation of the four-bit timer is described as follows:

A. Normal time-out mode

Flip flop A is in toggle mode and toggles between logic level one and zero on the falling edge of the clock pulse. The operation of flip flop depends upon the output of flip flop A only. Since A toggles at half the clock frequency, the output of flip flop B toggles at $f_{clock}/4$. Flip flop C depends upon the outputs of A and B, causing its output to change at $f_{clock}/8$. The operation of flip flop D depends upon the outputs of flip flops A, B and C, causing its output to change at $f_{clock}/16$. Thus the output monitored from the four flip flops, $DCBA_{LSB}$, gives a pure binary count. Since the input controls to each flip flop is from the complementary output of the previous stage, the outputs follow a countdown sequence. Thus the circuit allows the time-out period to be controlled anywhere between $1/f_{clock}$ to $16/f_{clock}$.

B. Parallel load mode

Setting the multiplexer control input to logic zero, causes the timer operates in a normal count down mode and for the multiplexer control input set to one, the timer operates in a parallel load mode. This enables the input data P_1 to P_4 to be loaded into the counter on the falling edge of the next clock pulse, regardless of the logic levels present at the other inputs. This function allows parallel loading of the counter.

C. Asynchronous controls

The preset and reset functions are asynchronous. A high level logic on reset input with preset set to logic low level, sets all four of the flip flop outputs low regardless of the logic levels present at the clock, load (multiplexer control input) or J K inputs. Similarly setting the preset input to logic high level with reset set to logic zero level, sets the outputs to logic high level, regardless of the logic levels present at the other inputs.

9.4.2.3 Physical Description

The four-bit time-out timer circuit was realised by butting single-bit timer cells with interleaving NOR based control logic between each cell. The timer control inputs (load, clock and asynchronous inputs) and parallel data inputs fed vertically into the cell with J-K inputs and outputs propagating horizontally. This floor plan allowed easier butting and reduced circuit height. The height of the timer remains constant with its width increasing linearly as the bit size increases. Figure 9.14 shows a floor plan for a four-bit timer.

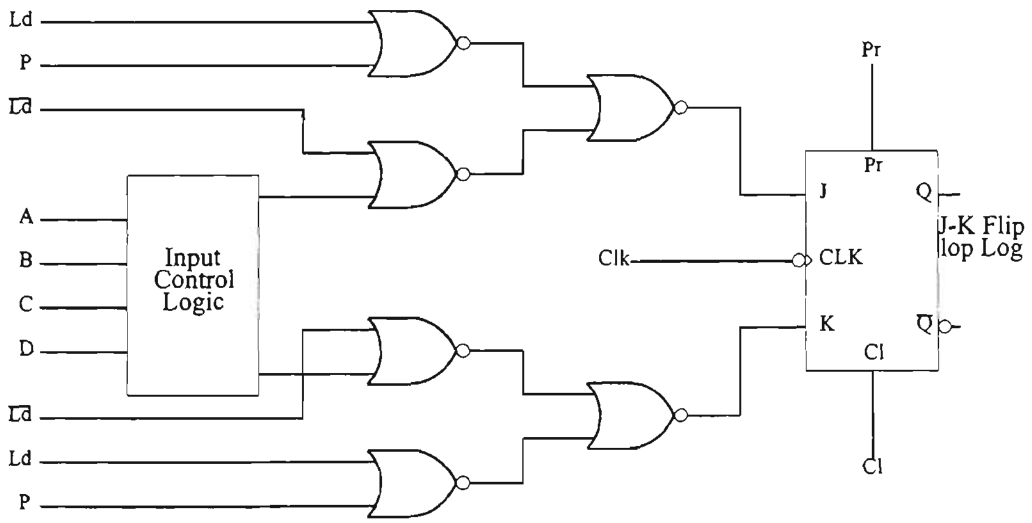


Figure 9.13 One-bit time-out timer.

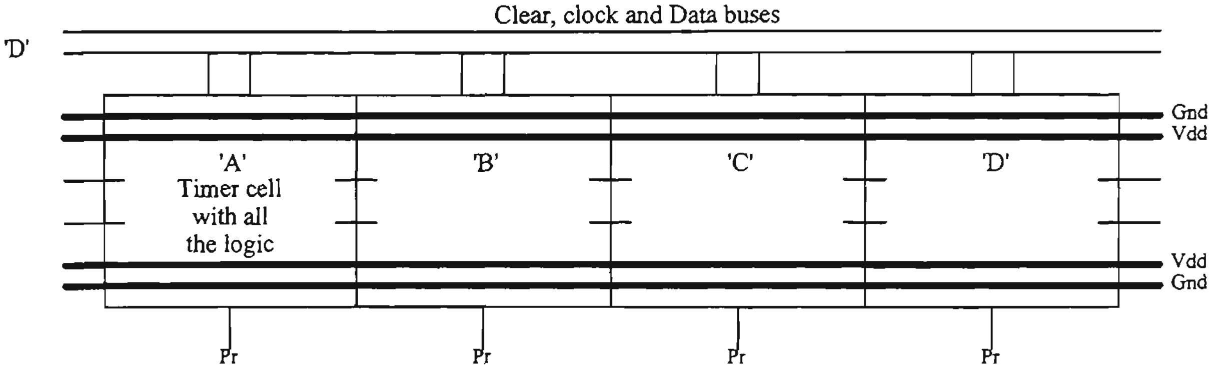


Figure 9.14 Four-bit timer floor plan.

Appendix J presents a detailed design procedure and performance for the timer.

9.4.3 VLSI Layout and Performance

The eight-bit comparator and the four-bit time-out timer were designed using GaAs MESFETs with gate length of 0.8 micron. The circuits were designed using Merged logic design technique. The layout methodology has significant influence upon the performance of the circuit. Communication paths between cells and positioning of power and ground busses have significant influence upon the performance of high speed VLSI systems. For example, fast transitions on signal bus could bring about significant noise on the power bus. Thus, both the design methodology and layout will have to address the influence of coupling between busses on performance.

The placement of power and ground busses adjacent to each other reduces their self inductance, and hence their susceptibility to current transients. From the results of coplanar strip line and coplanar waveguide models, placing of power buses in proximity of each other reduces the inductance of the power bus by a factor of two or more [106]. The ring notation approach, discussed in Chapter 5, exploits this advantage and enables the designer to layout the skeleton of the circuit rapidly, paying particular attention to power and signal busses between adjacent circuitry.

Using the above design methodology and layout approach, the eight-bit comparator and the four-bit timer circuits were implemented using ISD VLSI design suite. The VLSI layouts for an eight-bit comparator and the four-bit timer circuits are shown in Figures 9.15.

The above circuits have been analysed and evaluated using GaAs net extractor and HSPICE circuit simulation tools. The simulation results indicate a power dissipation of 18.48 milliWatts for an eight-bit comparator with worst case propagation delay of 1.586 nanosec. The four-bit timer circuit dissipated 31.02 milliWatts of power with propagation delays varying between 0.3232 nanosec to 0.4052 nanosec. The results for an eight-bit comparator and the four-bit timer are tabulated in Table 9.1. The HSPICE simulation waveforms for the circuits are shown in Figure 9.16. Figure 9.16 (a) shows the simulation results for an eight-bit comparator, where VIN1, VIN2 and VIN3 represent bit A5, Cin (input to the most significant stage) and cout (output of the list significant bit) respectively. The results indicate that when Cin is high, the inputs to the lower bit stages have no effect on the output. With Cin set to logic ‘0’, the output of the comparator is determined by A and B inputs. The power waveform indicates the power dissipated by the comparator circuit. Figure 9.16 (b) shows the simulation results for the four-bit timer circuit, where VIN1, VIN3, VIN4, VIN5 and VIN6 represent the clock pulse (phi), outputs A, B, C and D respectively. During the first 50 nanosecs, the parallel load is enabled and the timer is loaded with the time-out value of DCBA = 1111. At 50 nanosecs the count is enabled and the timer counts down to DCBA = 0000 with the time-out period of approximately 100 nanosecs. The power waveform indicates the power dissipated by the four-bit timer circuit.

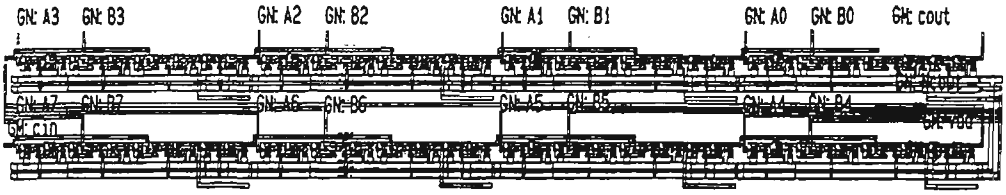


Figure 9.15(a) Mask level layout of an eight-bit comparator.

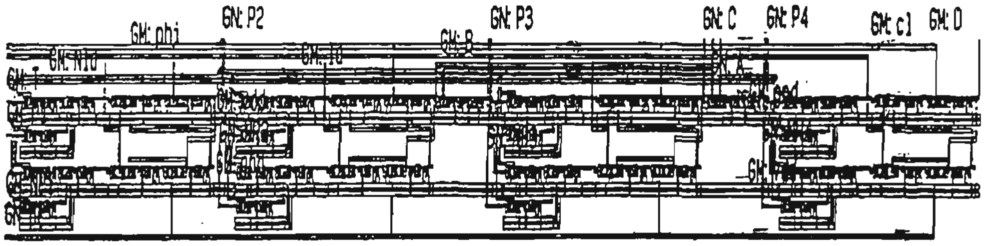


Figure 9.15(b) Mask level layout of a four-bit timer.

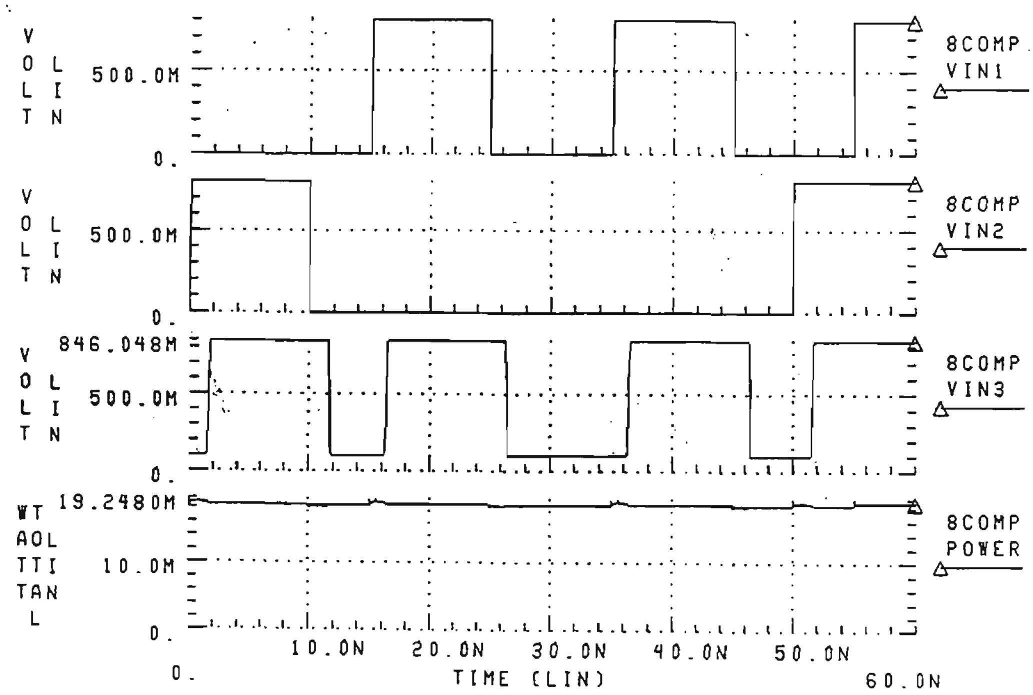


Figure 9.16(a) Simulation waveforms for an eight-bit comparator.

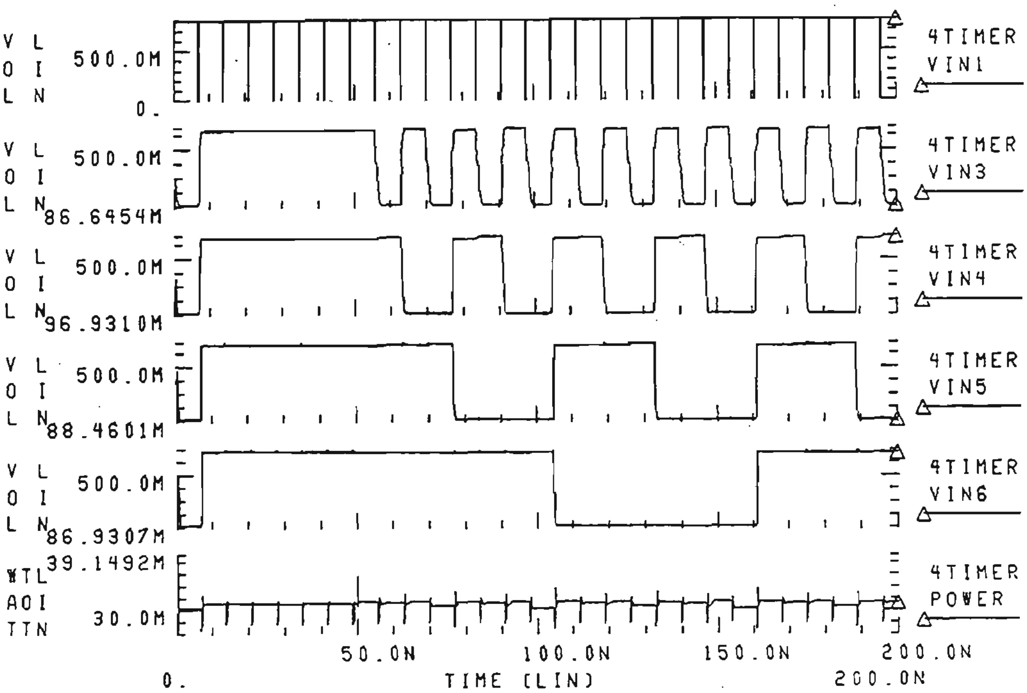


Figure 9.16(b) Simulation waveforms for a four-bit timer.

9.5 VLSI Implementation of a Multi-Function Multi-Protection Relay

An eight-bit multi-function multi-protection relay, containing an eight-bit comparator, a four-bit time-out timer and a controller, was designed and implemented using Integrated Silicon VLSI design suite. To obtain low power, high speed, good noise margin and large fan out E-D GaAs Merged logic design technique was chosen. Figure 9.17 shows the floor plan for the multi-function multi-protection relay. It encompasses all the necessary design criteria, including placement of the input and output signals so that the cells can be assembled with minimum length routing paths between cells. Figure 9.18 shows the VLSI layouts of the a eight-bit multi-function multi-protection relay.

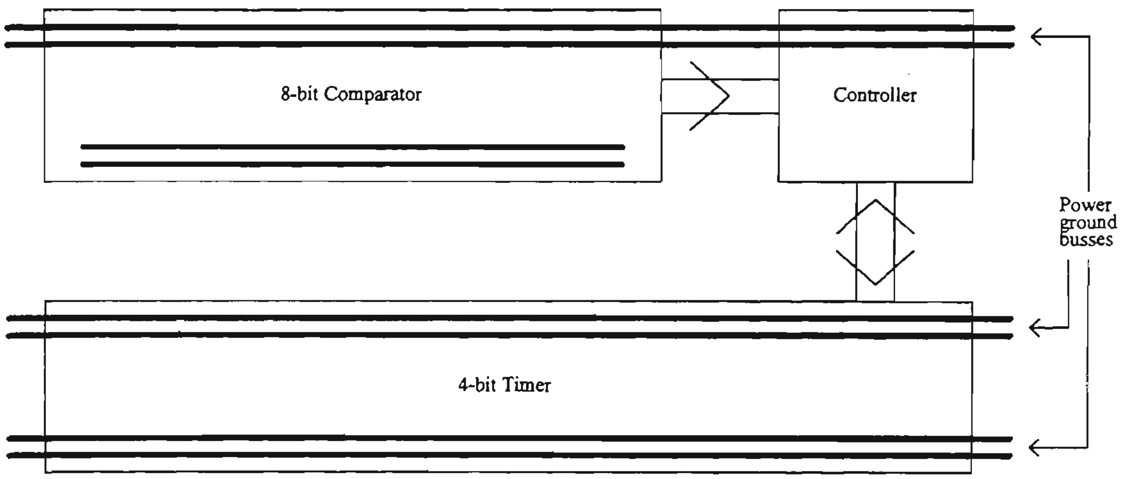


Figure 9.17 Floor plan for an eight-bit multi-function multi-protection relay.

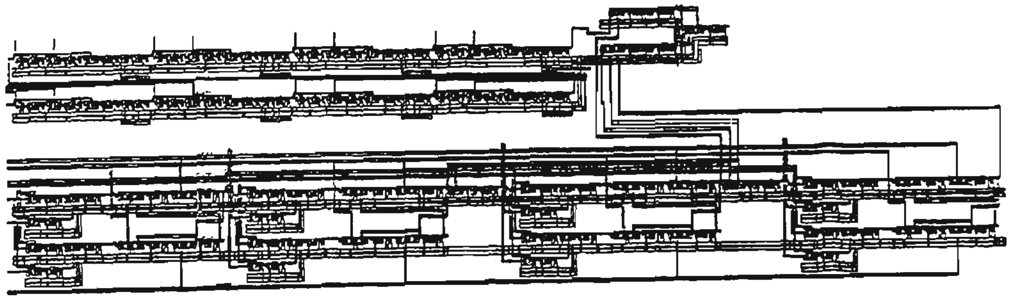


Figure 9.18 VLSI layout of an eight-bit multi-function multi-protection relay.

9.6 Simulation and Performance

An eight-bit multi-function multi-protection relay was analysed and evaluated using GaAs net extractor and HSPICE circuit simulation tools. The results are summarised in Table 9.2. Figure 9.19 shows the HSPICE simulation results, for an eight-bit multi-function multi-protection relay, where VIN3, VIN4, VIN5, VIN6, VIN7 and VIN8 represent relay output, comparator output, and the A, B, C, D outputs of the timer. The result shows that the relay loads the time-out number in the timer and waits for the controller to signal start of time-out period. This happens at 50 nanosecs, and the timer starts the time-out period. At the end of this period, with the controller

Table 9.1 Simulation results for an eight-bit comparator and the four-bit timer

Description	**Eight-bit Comparator**	**Four-bit timer**
Number of devices	144	231
E-MESFET	80	145
D-MESFET	64	86
Gate Length	0.8 micron	0.8 micron
Propagation Delay		
C_8 to C_0	1.586 nanosec	
Φ to A		0.4052 nanosec
Φ to B		0.3702 nanosec
Φ to C		0.3283 nanosec
Φ to D		0.3232 nanosec
Rise Time		
C_0	0.2473 nanosec	
A		0.9495 nanosec
B		0.3210 nanosec
C		0.2134 nanosec
D		0.2039 nanosec
Fall Time		
C_0	0.2215 nanosec	
A		1.136 nanosec
B		0.6844 nanosec
C		0.3701 nanosec
D		0.3645 nanosec
Power Dissipation	18.48 milliWatts	31.02 milliWatts
Noise Margin	0.30 Volts	0.30 Volts

indicating the input value still greater than the set value, an output pulse is generated, as indicated by VIN3. At 300 nanosecs the controller signals the input value less than the set value, resets the timer and waits for the signal from the comparator to start the time-out period. From the results it can also be seen that this design technique gives large logic swings resulting in excellent noise margins. The chip dissipates 49.73 milliWatts of power, indicating the suitability of this design technique in implementing VLSI circuits.

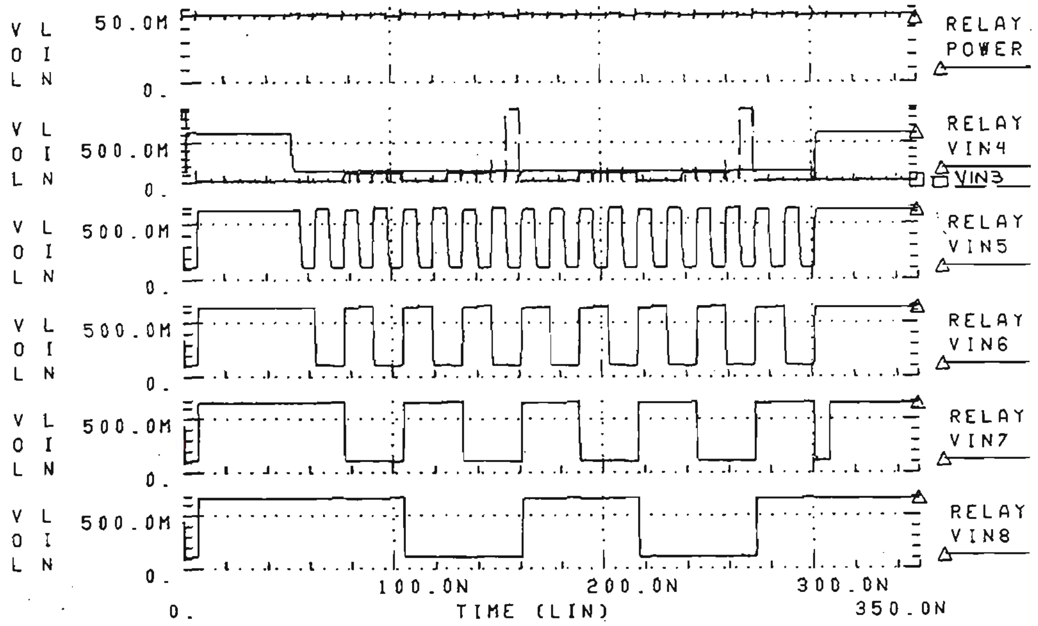


Figure 9.19 Simulation waveforms of the relay.
VIN3 represents the trigger pulse generated after each time out period of 150 ns and 265 ns.

Table 9.2 Performance of an eight-bit multi-function multi-protection relay

Description	Eight-bit relay
Number of devices	400
E-MESFET	240
D-MESFET	160
Gate length	0.8 micron
Power dissipation	49.73 milliWatts
Noise margin	0.30 Volts

9.7 Conclusions

The design and implementation of an eight-bit multi-function, multi-protection relay chip for power systems protection has been presented in this chapter. E-GaAs fabrication technology was chosen as a semiconductor medium because of its high electron mobility and existence of semi-insulating substrate properties. Merged logic design approach was used to design all the components of the relay. This approach to circuit design combines direct coupled MESFET logic (DCFL) with source follower DCFL (SDCFL) and source follower MESFET logic (SFFL) so that the advantages of each logic class are exploited and circuit performance is achieved which is superior to that obtained from different design approaches. In this technique, DCFL is predominantly used to achieve higher packing density and improved circuit performance. SDCFL design technique is used to drive large capacitive loads and realise the And-Or-Invert functions while SFFL design technique is used to implement large fan out.

The eight-bit relay chip was designed and implemented with 400 E-D GaAs MESFETs and dissipated 49.73 milliWatts of power. Results indicate a very high speed operation of the relay with respectable noise margin. The performance indicated the validation of the GaAs technology and Merged logic design technique to very fast integrated circuit design for power systems protection.

Chapter Ten

Conclusions

The reward of a thing well done is to have done it.

Proverb.

10.0 A Retrospective Overview of this Thesis

In this thesis, research has been conducted on the analysis of GaAs design techniques, the development of new static and dynamic design techniques in GaAs technology and design, implementation and performance analysis of a four-bit multi-channel data acquisition and an eight-bit multi-function multi-protection relay chips. The following stages of research are essential in the development of new GaAs MESFET design techniques to be used in the implementation of the above chips.

(i) Review of the VLSI circuit design technologies available and to determine the most suitable technology in the design of very high speed and low power integrated circuits.

(ii) Modelling the devices to be used in the given technology,

(iii) Having decided on the VLSI fabrication technology, review, design, analysis and evaluation of the currently available VLSI circuit design techniques and assessment on the suitability of these techniques for high speed low power VLSI circuit implementation,

(iv) Development, design, analysis and evaluation of design techniques for the implementation of high speed low power integrated circuits.

Technology review in Chapter 2 highlights that for very high speed operation in a semiconductor medium, three factors become significant, namely, carrier mobility, carrier saturation velocity, and existence of semi-insulating substrate. GaAs technology mostly fulfils the requirements, and together with low power dissipation provide a technology base for future VLSI circuits design.

Analysis of the currently available VLSI design techniques in GaAs technology reveals that though the normally-on static logic design techniques offer very high speed operation, they suffer from high power dissipation. Since the normally-on circuits are based on D-MESFETs, usually two power supplies are required for proper operation of these circuits. These make normally-on logic circuits unattractive for VLSI circuits design.

Normally-off static logic, on the other hand uses E-MESFETs for switching and also requires only single power supply. Although these techniques are being extensively used for VLSI circuit design, they suffer from a number of limitations such as low noise margins, sensitivity of the gate delay to fan in and fan out and load capacitance. TDFL dynamic circuit design techniques offered much smaller chip size per function resulting in much lower power dissipation but suffers from poor drive capability. Domino dynamic technique, on the other hand, has a very good drive capability.

One of the major problems in realising circuits in GaAs MESFET technology is caused by the dispersion of the device characteristics throughout the chip and wafer. The SCFL circuit design technique is such that only the relative variations of the threshold voltage is important. The evaluation of the design technique shows that SCFL circuit design technique is the best choice in the GaAs MESFET process for a mixed of digital and analog integrated circuits implementation on the same chip.

Two design techniques using GaAs MESFET technology have been developed to overcome some of the limitations of the normally-off static logic and the dynamic domino circuit design techniques. Merged logic design technique is developed using normally-off static logic and Multiple-output dynamic domino technique has been developed for dynamic circuits.

The Merged logic technique to circuit design combines direct coupled MESFET logic (DCFL) with source follower DCFL (SDCFL) and source follower MESFET logic (SFFL) so that the advantages of each logic class are exploited and circuit performance is achieved which is superior to that obtained from different design approaches. In the Merged logic static design technique, DCFL is predominantly used to achieve higher packing density and improved circuit performance. SDCFL technique is used to drive large capacitive loads and realise the And-Or-Invert functions while SFFL is used to implement large fan out. This technique involves identifying critical parts of the circuit where SDCFL and SFFL techniques can be used to improve circuit performance.

The performance of Merged logic design approach is illustrated with the design, implementation and performance analysis of a power series evaluator chip. From the performance analysis it can be seen that this design approach demonstrates excellent circuit performance.

The principle behind multiple-output domino technique is the utilisation of the sub-functions available in the logic tree of the domino gates. Multiple outputs are available by adding precharge devices at the corresponding intermediate nodes in the logic tree. Since the saving in the area is mainly due to a reduction of replication of sub-circuits, the actual advantage of this design technique over domino logic design technique is directly dependent upon the number of recurrence in a logic function being realised.

The performance advantage of this design technique over dynamic domino technique has been demonstrated via the implementation of a four-bit CLG for a Carry Lookahead Adder. The multiple-output domino technique demonstrates increased circuit performance, reduced circuit area and power dissipation when compared with the domino technique. This is due to the reduction in the parasitic capacitance and output loading. The most remarkable achievement using this technique is the reduction in the number of devices required to implement the CLG circuit. The performance of multiple-output domino is further improved by graded scaling of the domino chain.

Design, implementation and analysis of two VLSI chips are presented using the GaAs MESFET design techniques developed. Ultra fast four-bit multi-channel data acquisition chip was designed and implemented in E-D GaAs MESFET technology using 0.8 micron gate lengths. Appropriate design techniques and technology have been chosen for the design of this mixed analog-digital chip. SCFL technique was chosen in the design of a mix of digital and analog circuits on the same chip, mainly because of its wide tolerance to threshold voltage range and its immunity to temperature variations. It also has an excellent fan out capability, a small input capacitance and a small discharging time permitting high speed operations. Digital components were designed using GaAs Merged logic design technique.

Design of a flash ADC requires only $\mathbf{2^{(n-1)}}$ comparators to implement a n-bit flash ADC as compared with $(2^n - 1)$ comparators required for a classical n-bit flash ADC. This greatly reduces the complexity of the flash ADC. Depending upon the application, high resolution ADC can easily be cascaded using four-bit flash ADC modules.

The four-bit multi-channel data acquisition chip is implemented with 397 devices and dissipates 185.6 milliWatts of power. The conversion time is 0.85 nanosec with noise margin of 0.35 Volts. These results indicate the appropriateness of the design technology and techniques used for mixed analog-digital circuit design on a single chip.

An eight-bit multi-function multi-protection relay chip for power systems protection has been designed and implemented in GaAs technology using Merged logic circuit design technique. The relay chip is developed using eight-bit comparator, fully programmable four-bit time-out timer and a controller with necessary handshake logic. The eight-bit magnitude comparator unit compares the incoming signals (phase and line currents and voltages) with the set (normal) values of these signals, stored as look-up table in a memory, and generates a control signal if the magnitude of the incoming signal is greater than the set value. The time-out periods of the timer are stored as look-up table in a Read Only Memory based on definite and inverse time-current characteristics of the relay. This is downloaded into the timer using parallel load facilities. The controller unit monitors the comparator output and send a signal to timer unit to either start time-out period or load the time-out value. At the end of time-out period if the magnitude of the incoming signal is still greater than the set value, a trigger pulse is generated by the controller unit to operate appropriate circuit breakers. It also provides handshake signals for other relays in the synchronous protection scheme. This structure gives the flexibility for the relay to be used as multi-function, multi-protection device. A cellular design approach has been used to give the flexibility to the system to be easily cascaded into multi-bit (sixteen, thirty two, etc) multi-function multi-protection relay.

The eight-bit relay chip is implemented with 400 GaAs MESFETs and dissipates 49.73 milliWatts. The performance indicate the validation of the GaAs technology and

Merged logic design technique for the implementation of high speed low power integrated circuits.

The primary objective in the layout of GaAs circuits is optimum exploitation of the performance offered by the GaAs technology. This can be achieved only when the layout guarantees minimisation of parasitic capacitances. Full custom design approach has been used for all the design layout with the entire operation implemented on a single chip rather than on multiple chips. This allows to maximise on the advantages of the GaAs technology and reduce parasitic capacitances due to chip interconnections.

In conclusion, all the aims of this research have been successfully met.

10.1 Avenues to be Explored in Further Work

The only limits of our realisation of tomorrow will be our doubts of today.

Franklin D. Roosevelt

The studies reported in this thesis involve the development of new design techniques in GaAs technology using both static and dynamic approaches and design, implementation, simulation and analysis of a four-bit multi-channel data acquisition chip and an eight-bit multi-function multi-protection chip. The following aspects relating to the future research into VLSI circuits and systems design are suggested:

(i) Design and implementation of VLSI circuits using high electron mobility transistors (HEMTs) instead of MESFETs. Since HEMT devices belong to the E-MESFET family of technologies, they enjoy the inherent advantages and disadvantages of such technologies. For example, the variance of threshold voltage of about 10 millivolts must be obtained in HEMT VLSI circuits. The improvements in GaAs fabrication technologies and superior control offered by MBE is inherently capable of attaining this degree of uniformity. An important advantage of HEMT devices is that they achieve their high speed at lower logic voltage swings than E-MESFETs, which may result in dynamic power dissipation of one to two orders of magnitude lower. Although the small logic swing may compromise the circuit noise margin, low power is of great importance in VLSI circuit applications.

(ii) Design and implementation of VLSI circuits using hetrojunction bipolar transistors (HBTs). Performance of HBT devices ultimately projected to be in the 100 - 200 GHz range with gate delays in the range of 10 picosec. Furthermore, the high current drive capability of HBTs coupled with their threshold voltage insensitivities makes these devices the prime candidate for ultra high performance VLSI integrated circuits.

(iii) The multi-function multi-protection relay can be further improved by incorporation of multi-channel data acquisition and the memory circuits on the same chip. This will result in lower chip interconnection capacitance leading to higher speed, lower power dissipation and giving greater application flexibility.

(iv) Integration of sensors and signal conditioning circuits on multi-channel data acquisition chip will enable it to be used as micro-machine with digital signal available at the outputs. This will find major applications in remote sensoring.

Bibliography

[1] Suyama, K., Kusakawa, H., Okamura, S. and Fukuta, M., "An MSI GaAs integrated circuit: 4-bit arithmetic and logic unit", IEEE Journal on Solid-State Circuits, Vol. SC-17, No. 4, pp 653 - 657, 1982.

[2] Deming, R.N., Zucca, R., Vahrenkamp, R.P., Hou, L.D., Naused, B.A. and Gilbert, B.K., "A gallium arsenide configurable cell array using buffered fet logic", IEEE Journal of Solid-State Circuits, Vol. SC-19, No. 5, pp 728 - 738, 1984.

[3] Rocchi, M. and Gabillard, B., " GaAs digital dynamic IC's for applications up to 10 GHz", IEEE Journal of Solid-State Circuits, Vol. SC-18, No. 3, pp 369 - 376, 1984.

[4] Hirayama, M., Ino, M., Matsuoka, Y. and Suzuki, M., "A GaAs 4 kbit SRAM with direct coupled fet logic", IEEE Journal of Solid-State Circuits, Vol. SC-19, No. 5, pp 716 - 720, 1984.

[5] Osafune, K., Enoke, T., Yamasaki, K. and Ohwada, K., "GaAs ultra high frequency dividers with advanced SAINT fet's", IEEE Trans. on Electron Devices, Vol. ED-33, No. 12, pp 2059 - 2063, 1986.

[6] Singh, H.P., Sadler, R.A., Irvine, J.A. and Gorder, G.E., "GaAs low power integrated circuits for high speed digital signal processing", IEEE Trans. on Electron Devices, Vol. ED-36, No. 2, pp 240 - 249, 1989.

[7] Katsu, S., Nambu, S., Shimano, A. and Kano, G., " A GaAs monolithic frequency divider using source coupled fet logic", IEEE Electron Device Letter, Vol. EDL-3, No. 8, pp 197 - 199, 1982.

[8] Katsu, S., Nambu, S., Shimano, A. and Kano, G., "A source coupled fet logic - a new current mode approach to GaAs logics", IEEE Trans. on Electron Devices, Vol. ED-32, No. 6, pp 1114 - 1118, 1985.

[9] Idda, M., Takada, T. and Sudo, T., " Analysis of high speed GaAs source coupled fet logic circuits", IEEE Trans. on Microwave Theory and Techniques, Vol. MTT-32, No. 1, pp 5 - 10, 1984.

[10] Vu, T.T., Peczalski, A., Lee, K.W. and Conger, J., "The performance of source coupled fet logic circuits that use GaAs MESFET's", IEEE Journal of Solid-State Circuits, Vol. SC-23, No. 1, pp 267 - 279, 1988.

[11] Ohta, N. and Takada, T., "High speed GaAs SCFL monolithic integrated decision circuit for Gbit/s optical repeaters", Electronics Letter, Vol. 19, No. 23, pp 983 - 985, 1983.

[12] Shimizu, S. et al., "A 1 Ghz 50 mW GaAs dual modulars divider using source coupled fet logic", ISSCC Digest Technical Papers, pp 52 - 53, 1984.

[13] Vu, T.T. et al., "A gallium arsenide SDFL gate array with on-chip RAM", IEEE Journal of Solid-State Circuits, Vol. SC-19, No. 1, pp 10 - 22, 1984.

[14] Vu, T.T. et al., "Low power 2K cell SDFL gate array and DCFL circuits using GaAs self-aligned E/D MESFET's ", IEEE Journal of Solid-State Circuits, Vol. SC-23, No. 1, pp 224 - 236, 1988.

[15] Shur, M.S. et al., "Design and simulation of self-aligned modulation doped Al GaAs/GaAs IC's", ISSCC Digest Technical Papers, pp 264 - 265, 1985.

[16] Srivastava, A. and Dubey, M., "GaAs digital integrated circuits - a review from silicon point of view for designing ultra fast VLSI circuits", IEEE Journal of solid-State Circuits, Vol. 25, pp 1250 - 1254, 1990.

[17] Higashiska, N. et al., "GaAs DCFL 2.5 Gbps 16-bit multiplexer/demultiplexer LSI's", IEEE Journal of Solid-State Circuits, Vol. SC-29, No. 7, pp 808 - 814, 1994.

[18] Singh, H.P., Sadler, R.A., Tanis, W.J. and Schenberg, A.N., "GaAs prescalers and counters for fast settling frequency synthesisers", IEEE Journal of Solid-State Circuits, Vol. SC-25, No. 1, pp 239 - 245, 1990.

[19] Singh, H.P., Sadler, R.A., Geissberger, A.E. and Tanis, W.J., " High speed low power GaAs programmable counters for synthesiser applications", IEEE GaAs IC Symposium Technical Digest, pp 269 - 272, 1987.

[20] Pasternak, J.H. and Salama, C.A.T., "GaAs MESFET differential pass transistor logic", IEEE Journal of Solid-State Circuits, Vol. SC-26, pp 1309 - 1316, 1991.

[21] Hoe, D.H.K. and Salama, C.A.T., " GaAs trickle transistor dynamic logic", IEEE Journal of Solid-State Circuits, Vol. SC-26, pp 1441 - 1448, 1991.

[22] Yang, L., Chakhararapani, R. and Long, S.I., "A high speed dynamic domino circuit implemented with GaAs MESFET's", IEEE Journal of Solid-State Circuits, Vol. SC-22, No. 5, pp 874 - 879, 1987.

[23] Nary, K.R. and Long, S.I., "Dynamic latch for high speed GaAs domino circuits", Electronics Letter, Vol. 28, No. 1, pp 36 - 37, 1992.

[24] Krambeck, R.H., Lee, C.H. and Law, H.S., "High speed compact circuits with CMOS", IEEE Journal of Solid-State Circuits, Vol. SC-17, No. 3, pp 614 - 619, 1982.

[25] Lassen, P.S., Long, S.I. and Nary, K.R., "Ultra low power GaAs MESFET MSI circuits using two phase dynamic fet logic", IEEE Journal of Solid-State Circuits, Vol. SC-28, No. 10, pp 1038 - 1045, 1993.

[26] Nary, K.R. and Long, S.I., " GaAs two phase dynamic fet logic: a low power logic family for VLSI", IEEE Journal of Solid-State Circuits, Vol. SC-27, No. 10, pp 1364 - 1371, 1992.

[27] Corcoran, J., Poulton, K. and Hornak, T., "A 1 Ghz 6b adc system", ISSCC Digest Technical Paper, pp 102 - 103, 1987.

[28] Thomas, F. et al., "1 Ghz GaAs adc building blocks", IEEE Journal of Solid-State Circuits, Vol. SC-24, No. 2, pp 223 - 228, 1989.

[29] Ducourant, T. et al., "3 Ghz, 150 mW, 4 bit GaAs analog to digital converter", IEEE GaAs Symposium, pp 209 - 212, 1986.

[30] Ducourant, T., Meignant, D., Bertsch, P. and Wright, M., "A 5 bit, 2.2 Gs/s monolithic analog to digital converter with gigahertz bandwidth, and 6 bit a/d converter system", IEEE GaAs Symposium, pp 337 - 340, 1989.

[31] Naber, J.F., Singh, H.P., Sadler, R.A. and Milan, J.M., " A low power high speed 4-bit GaAs adc and 5-bit dac", IEEE GaAs Symposium, pp 333 - 336, 1989.

[32] Kleks, J. et al., "A 4-bit single chip analog to digital converter with 1.0 gigahertz analog input bandwidth", IEEE GaAs Symposium, pp 79 - 82, 1987.

[33] Hagelauer, R. et al., “A gigasample/s 5 bit adc with on-chip track & hold based on an industrial 1 μm GaAs MESFET E/D process”, IEEE GaAs Symposium, pp 365 - 368, 1991.

[34] Sauerer, J. et al., “System architecture and key components for an 8 bit/1GHz GaAs MESFET adc”, IEEE GaAs Symposium, pp 105 - 108, 1992.

[35] Doernberg, J. and Hodges, D.A., “A 10-bit 5 megasamples/sec CMOS 2-step flash adc”, Proceeding of IEEE Custom Integrated Circuits Conference, pp 18.6.1 - 18.6.4, 1988.

[36] Kerth, D.A., Sooch, N.S. and Swanson, E.J., “A 667 ns, 12 bit, two step flash adc”, Proceeding of IEEE Custom Integrated Circuits Conference, pp 18.5.1 - 18.5.3, 1988.

[37] Hagelauer, R. et al., “Investigations and measurements of the dynamic performance of high-speed adc’s”, IEEE Trans. on Instrumentations and Measurement, Vol. 41, No. 6, pp 829 - 833, 1992.

[38] Balsubramanian, K., “A flash adc with reduced complexity”, IEEE Trans. on Industrial Electronics, Vol. 42, No. 1, pp 106 - 108, 1995.

[39] Sachdev, M.S., “Microprocessor relays and protection systems”, IEEE tutorial course text, Publication No. 88EH0269-1-PWR, 1988.

[40] Kramer, C.A. and Elmore, W.A., "Flexible inverse overcurrent relaying using a microprocessor", IEEE Trans. on Power Delivery, Vol. 5, No. 2, pp 915 - 921, 1990.

[41] Sidhu, T.S., Wood, H.C. and Nagpal, M., "Design, implementation and testing of a microprocessor based high speed relay for detecting transformer winding faults", IEEE Trans. on Power Delivery, Vol. 7, No. 1, pp 108 - 117, 1992.

[42] Manzol, M.A., "Multiple overcurrent relays using a single microprocessor", IEEE Trans. on Industrial Electronics, Vol. 37, No. 4, pp 307 - 309, 1990.

[43] Harlow, J.H., "Applying a multifunction protection relay for the cogeneration industry", Beckwith Electric Company, Inc Largo, Florida. Topical Report, pp 153 - 158, 1991.

[44] Gillany, M.T., Makil, O.P. and Hope, G.S., "A digital protection technique for parallel transmission lines", IEEE Trans. on Power Delivery, Vol. 7, No. 1, pp 118 - 125, 1991.

[45] Yalla, V.V.S., "A digital multifunction protective relay", IEEE Trans. on Power Delivery, Vol. 7, No. 1, pp 193 - 201, 1992.

[46] Balasubramanian, K. and Oral, M., “Microprocessor based multi-function relay switching”, IEEE Trans. on Consumer Electronics, Vol. 38, No. 4, pp 878 - 883, 1983.

[47] Zayegh, A., Kalam, A. and Chen, J., “32-bit microprocessor based digital relaying techniques for overcurrent and differential protection”, Proc. of Int. AMSE Conf., AMSE Press, Vol. 3, pp 81 - 87, 1992.

[48] Woerlee, P.H. et al., “A low power 0.25 μm CMOS technology”, IEEE International Electron Devices Meeting, pp 31 - 34, 1992.

[49] Lee, Y.J., Garvin, H.L. and Slayman, C.W., “A high-speed high-density silicon 8 x 8-bit parallel multiplier”, IEEE Journal on Solid-State Circuits, Vol. SC-22, pp 35 - 40, 1987.

[50] Hunt, P.C. and Cooke, M.P., “Process HE: a highly advanced trench isolated bipolar technology for analogue and digital applications”, Proceeding IEEE Custom Integrated Circuits Conference, 22.2.1 - 22.2.4, 1988.

[51] Washio, K., Nakazato, K. and Nakamura, T., “2.7 ns 8 x 8-bit parallel multiplier using side wall base contact structure”, IEEE Journal on Solid-State Circuits, Vol. SC-22, pp 613 - 614, 1987.

[52] Nakayama, Y. et al., "A GaAs 16 x 16-bit parallel multiplier", IEEE Journal on Solid-State Circuits, Vol. SC-18, pp 599 - 603, 1984.

[53] Goel, A.K. and Kalia, A., "Comparison of NMOS, CMOS and GaAs technologies", Proceeding of IEEE Midwest Symposium on Circuits and Systems, pp 1238 - 1241, 1990.

[54] Brunvand, E., Michel, N. and Smith, K., "A comparison of self-timed design using FPGA, CMOS ans GaAs technologies", IEEE International Conference on Computer Design: VLSI in Computers and Processors, pp 76 - 80, 1992.

[55] Elrabaa, M. and Elmasry, M.I., " Multi-emitter BiCMOS cml circuits", IEEE Journal on Solid-State Circuits, Vol SC-24, pp 454 - 458, 1992.

[56] Chen, C.L., "Level shifted and voltage reduced 0.5 μm BiCMOS circuits", IEEE International Solid-States Conference, pp 236 - 237, 1990.

[57] Rofail, S.S, "low voltage, low power BiCMOS digital circuits", IEEE Journal of Solid-States Circuits, Vol. 29, No. 5, pp 572 - 579, 1994.

[58] Bellaaouar, A. and Touzene, H., "3.3 V BiCMOS current-mode logic circuits for high speed adders", IEEE Journal of Solid-States Circuits, Vol. 31, No. 8, pp 1165 - 1169, 1996.

[59] Kuraha, S. et al., “A 6 ns 1.5 V 4 Mb BiCMOS SRAM”, IEEE International Solid-States Conference, pp 144 - 145, 1996.

[60] Murabayashi, F. et al., “3.3V BiCMOS circuit techniques for a 120 Mhz RISC microprocessor”, IEEE Journal of Solid-States Circuits, Vol. 29, No. 3, pp 298 - 302, 1994.

[61] Liu, T.M. et al., “A half-micron super self-aligned BiCMOS technology for high speed applications”, IEEE International Electron Devices Meeting, pp 23 - 26, 1992.

[62] Suzuki, M. et al., “A 3.5-ns, 500-mW, 16-bit BiCMOS ECL RAM”, IEEE Journal of Solid-States Circuits, Vol. 24, No. 5, pp 1233 - 1237, 1989.

[63] Wanlass, F.M. and Sah, C.T., “Nanowatt logic using field effect MOS triodes”, IEEE Solid-States Conference Technical Digest, pp 32 - 35, 1963.

[64] Mukherjee, A., “Introduction to nMOS and CMOS VLSI systems design”, Prentice Hall, 1986.

[65] Ning, T.H. and Tang, D.D., “Bipolar trends”, IEEE Journal on Solid-State Circuits, Vol. SC-74, No. 12, pp 1669 - 1677, 1986.

[66] Kapoor, A.K. and Roulston, D.J., "Polysilicon emitter bipolar transistors", IEEE Press, 1989.

[67] Kobayashi, T., Nakayama, S., Miyake, M. and Okazaki, Y., "Nitrogen in-situ doped poly buffer LOCOs: simple and scalable isolation technology for deep-submicron silicon devices", IEEE International Electron Devices Meeting, pp 683 - 686, 1994.

[68] Ohzone, T., Iwata, H., Uraoka, Y. and Odanaka, S., "Two dimensional analysis of holt-carrier photoemission from LOCO- and trench-isolated MOSFETs", IEEE International Electron Devices Meeting, pp 527 - 530, 1992.

[69] Embabi, S.H.K., Bellaouar, A. and Elmasry, M.I., "Digital BiCMOS integrated circuit design", Kluwer Academic Publication, 1993.

[70] Yamaguchi, T. and Yuzuriha, T.H., "Process integration and device performance of a submicron BiCMOS with 16-GHZ f_t double poly-biploar devices", IEEE Trans. on Electron Devices, Vol. 36, No. 5, pp 890 - 896, 1989.

[71] Kua, J.B., Su, K.W. and Lou, J.H., "1.5V BiCMOS dynamic multiplier using Wallace tree reduction architecture", IEE Electronics Letter, Vol. 29, No. 24, pp 2097 - 2098, 1993.

[72] Robertson, D.H., “BiCMOS techniques for high speed, high resolution adcs”, IEEE International Symposium on Circuits and Systems, Vol. 6, pp 2695 - 2698, 1992.

[73] Chang, Y.C. and Francis, K., “GaAs high-speed devices”, John Wiley and Sons, Inc., 1994.

[74] Pucknell, D.A. and Eshraghian, K., “Basic VLSI design”, Third Edition, Prentice Hall, 1994.

[75] Kanopoulos, N., “Gallium arsenide integrated circuits”, Prentice Hall, 1989.

[76] Shah, D.M. et al., “Epitaxial lift-off GaAs HEMT’s”, IEEE Trans. on Electron Devices, Vol. 42, No. 11, pp 1877 - 1881, 1995.

[77] Yang, Y.F., Hsu, C.C. and Yang, E.S., “Integration of GalnP/GaAs hetrojunction bipolar transistors and high electron mobility transistors”, IEEE Electron Devices Letter, Vol. 17, No. 7, pp 363 - 365, 1996.

[78] Canfield, P.C. and Allostat, D.J., “A potential for p-well GaAs technology for precision integrated circuits”, IEEE Symposium on Circuits and Systems, pp 3065 - 3068, 1990.

[79] Shur, M.S., “Analytical model of GaAs fet’s”, IEEE Trans. on Electron Devices, Vol. ED-32, pp 70 - 72, 1985.

[80] Tuyl, R.V. and Liechti, C.A., “Gallium arsenide digital integrated circuits”, Airforce Avionics Laboratory, AFSC, WPAFB, Technical Report AFAL-TR-74 - 40, 1974.

[81] Pucel, R., Haus, H. and Statz, H., “Signal and noise properties of gallium arsenide microwave field-effect transistors”, Academic Press, pp 195 - 205, 1975.

[82] Krumm, C.F. et al., “Low noise field effect transistors”, Huges Research Labs., AFAL-TR-78-182, 1978.

[83] Curtice, W.R., “A MESFET model for use in the design of GaAs integrated circuits’, IEEE Trans. on Microwave Theory and Techniques, Vol. MTT-28, No. 5, pp 448 - 455, 1980.

[84] McCamant, A.J., McCormack, C.D. and Smith, D.H., “An improved GaAs MESFET model for SPICE”, IEEE Trans. on Microwave Theory and Techniques, Vol. MTT-38, pp 822 - 824, 1990.

[85] Sakurai, T. ans Newton, A.N., “A simple MOSFET model for circuit analysis”, IEEE Trans. on Electron Devices, Vol. 38, pp 887 - 893, 1991.

[86] De, V.K. and Meindl, J.D., " Three-region analytical models for MESFET's in low-voltage digital circuits", IEEE Journal of Solid-State Circuits, Vol. SC-26, No. 6, pp 850 - 857, 1991.

[87] De, V.K. and Meindl, J.D., "An analytical threshold voltage and subthreshold current model for short-channel MESFET's", IEEE Journal of Solid-State Circuits, Vol. SC-28, No. 2, pp 169 - 172, 1993.

[88] Chang, C.T.M. et al., "A subthreshold current model for GaAs Mesfet's", IEEE Electron Devices Letters, Vol. 8, No. 2, pp 69 - 72, 1987.

[89] Conger, J., Peczalski, A. and Shur, M.S., "Subthreshold current in GaAs MESFET's", IEEE Electron Devices Letters, Vol. 9, No. 3, pp 128 - 129, 1988.

[90] Helix, M.J. et al., "Improved logic gate with a push-pull output for GaAs digital ICs", Proceeding of International GaAs Symposium, pp 108 - 111, 1982.

[91] Beaumont-Smith, A. and Eshraghian, K., "Comparison of Gallium Arsenide MESFET process technologies", Technical Report GaAs 92-14, 1992.

[92] Lehovec, K. and Zuleeg, R., "Analysis of GaAs fet's for integrated logic", IEEE Trans. on Electron Devices, Vol. 27, No. 6, pp 1074 - 1090, 1986.

[93] Long, S.I. and Sundaram, M., "Noise margin limitations on gallium arsenide VLSI", IEEE Journal of Solid-State Circuits, Vol. 23, No. 4, pp 893 - 900, 1988.

[94] Huyn, C.H., Shur, M.S. and Peczalski, A., "Analysis of noise margin and speed of GaAs MESFET dcfl using UM-SPICE", IEEE Trans. on Electron Devices, Vol. 33, No. 10, pp 1421 - 1425, 1986.

[95] Haigh, D.G. and Toumazou, C., "GaAs MSI circuit design for communication systems", IEE Colloquium on Analogue VLSI, pp 5/1 - 11, 1990.

[96] Nakajima, S. et al., "Enhancement mode GaAs MESFET technology for low consumption power and low noise applications", IEEE MTT-S International Microwave Symposium Digest, pp 1443 1446, 1994.

[97] Bayruns, R. et al., "GaAs integrated circuits for consumer applications", IEEE International Electron Devices Meeting, pp 235 - 238, 1993.

[98] Cui, S., Burgess, N., Liebelt, M. and Eshraghian, K., "A GaAs IEEE floating point standard single precision multiplier", Proceeding of the IEEE Symposium on Computer Arithmetic, pp 91 - 97, 1995.

[99] Pretorius, J.A., Shubat, A.S. and Salama, C.A., "Analysis and design optimisation of domino CMOS logic with application to standard cells", IEEE Journal of Solid-State Circuits, Vol. 20, pp 523 - 530, 1985.

[100] Pretorius, J.A., Shubat, A.S. and Salama, C.A., "Latched domino CMOS logic", IEEE Journal of Solid-State Circuits, Vol. 21, pp 514 - 522, 1986.

[101] Dillinger, T.E., "VLSI Engineering", Prentice Hall, 1988.

[102] Schneider, T.K., Schwab, A.J. and Aylor, J.H., "A full custom VLSI design methodology using Mentor Graphics design software in a educational environments", Proceeding of IEEE International ASIC Conference, pp 305 - 308, 1993.

[103] Cheng, C.K., Hu, T.C. and Yao, S.Z., "The modular orientation of VLSI layout", IEEE International Symposium on Circuits and Systems", pp 1600 - 1603, 1990.

[104] Wilderotter, T.J. and Ott, D.E., " A designer's guide to VHDL synthesis", Kluwer Academic Publishers, 1994.

[105] Kission, P., Hong, D. and Jerraya, A.A., " Proceeding of European Design Automation Conference, pp 470 - 475, 1995.

[106] Eshraghian, K., “Design methodology and layout style for very high speed circuits and subsystems”, Technical Report, 1992.

[107] Mead, C. and Conway, L., “Introduction to VLSI systems”, Addison Wesley Publishing Company, 1980.

[108] Gopalan, K., “Introduction to digital microelectronic circuits”, IRWIN, 1996.

[109] Al-Nema, M.A., Bashi, S.M. and Ubaid, A.A., “Microprocessor based overcurrent relays”, IEEE Trans. on Industrial Electronics, Vol. IE-33, pp 49 - 51, 1986.

[110] Kalam, A. et al., “Power system protection”, Short Course Program, ESAA & VUT, 1992.

[111] Henville, C.F., “Combined use of definite and inverse time overcurrent elements assists in transmission line ground relay coordination”, IEEE Trans. on Power Delivery, Vol. 8, No. 3, 1993.

[112] Roth, G.H.Jr., “Fundamental of logic design”, West Publishing Co., Fourth Edition, 1995.

[113] Shur, M., “GaAs Devices and Circuits”, Plenum Press, 1987.

[114] Wing, O., “Gallium Arsenide Digital Circuits”, Kluwer Academic Publishers, 1991.

[115] Eshraghian, K., “Optomisation of High Speed VLSI Systems:Physical Mapping”, Technical Report, 1992.

[116] Eshraghian, K., “GaAs Design Methodology & Performance Estimates For Very High Speed Circuits Using Normally-Off Classes of Logic”, Microelectronics Conference, pp227 - 232, 1993.

[117] Ahmed, R.E., “New Design Technique For Two-Step Flash A/D Converter”, Electronics Letter, Vol. 26, No. 15, pp 1185 - 1186, 1990.

[118] Sedra, A.S. and Smith, K.C., “Microelectronic Circuits”, Third Edition, Saunders College Publishing, 1991.

Appendix A

GaAs MESFET Fabrication Process

A1.0 Introduction

Although there are various techniques that are currently used, high pressure Liquid Encapsulated Czochralski (LEC) growth of GaAs crystals is becoming a primary growth technique over several other methods that have emerged recently. The fabrication for GaAs MESFET is different from that of silicon MOSFET. However, for digital IC applications, Vitese Corporation has adopted the NMOS technology to fabricate their gate arrays. GigaBit Logic (now merged with TriQuint) has developed their standard cell based on SCFL structures.

The sequence of GaAs wafer preparation is very similar to that of silicon wafer preparation technique. The first step involves mechanically grinding the arsenide-boules to a precise diameter and incorporating orientation flats. This is followed by:

(i) wafering using a diamond saw

(ii) edge grinding

(iii) lapping

(iv) polishing

(v) wafer scrubbing.

A2.0 Depletion Mode Planar Process

The planar process for D-MESFET which entails the use of three or four inch LEC wafers is illustrated in Figure A1.1. Initially the GaAs substrate is coated with a first level of insulator, that is a thin layer of silicon nitride (Si_3N_4), which is sputted on the GaAs substrate. This film of insulator remains on the wafer throughout the processing steps that follow, allowing the annealing of GaAs at temperature of up to $900^o C$. The next step entails the formation of n^- type active layer. This is done using direct ion implantation into GaAs semi-insulating substrate. There are two main implantation steps, namely:

(i) a shallow high resistivity n^- layer for the formation of the channel layer, and

(ii) a deep low resistivity n^+ layer for the formation of source and drain.

The wafer is then coated with a interleaved dielectrics, SiO_2, using Chemical Vapour Deposited (CVD) process. This is followed by an anneal in a hydrogen ambient at a temperature of about $800-850^0 C$. This encapsulation phase is very important as it prevents out-diffusion of arsenic. The next step in the process is defining the MESFET gates, the ohmic contacts and the first level metal interconnects. Several points needs to be considered during this phase, namely:

(i) the metal must be carefully alloyed to ensure reliable low resistance contacts

(ii) the ohmic contacts between the metal interconnect and the source and drain are deposited by evaporation using E-beam technology. A thin layer of gold-germanium-nickel or gold-germanium-platinum is alloyed on the wafer

(iii) one of the most critical steps is the gate metallisation

(iv) Schottky gate, together with first level metallisation are formed by multilayer gold refractory thin films.

The metal contacts and interconnects are precisely registered with the plasma-etched insulator windows. The second level metallisation entails magnetron sputtered titanium/gold alloy, which is followed by filling the vias between first level and second level metal. The final step in the fabrication is the passivation, used to protect against contamination and moisture.

Since in D-MESFETs any regions of the source or drain channel that are not under the gate are strongly conducting, there is no need for precise alignments of the gate or gate recesses to avoid parasitic source drain resistances. However, in the planar process the position of the gate relative to the source and drain has significant influence upon the performance of the device.

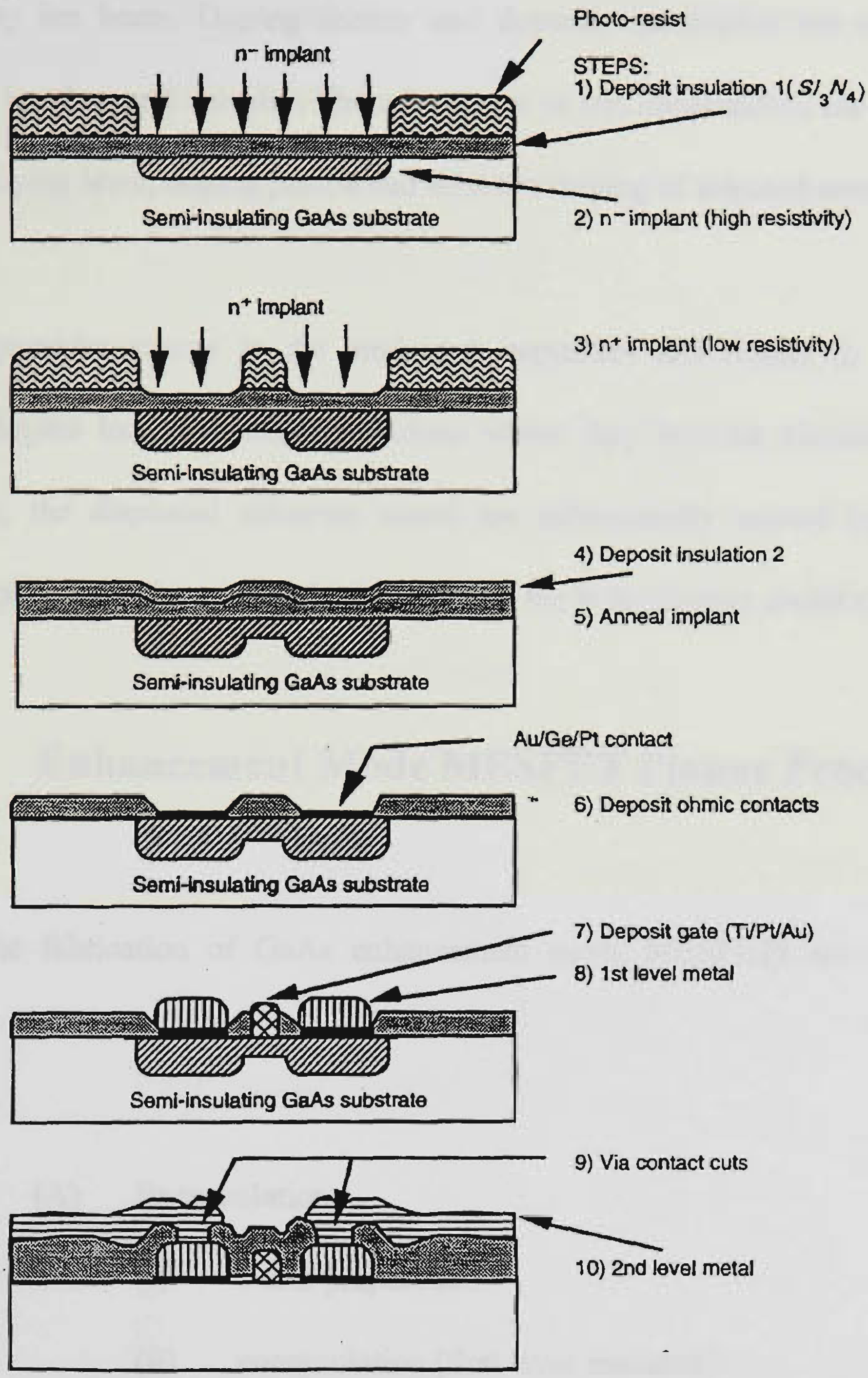


Photo-resist
n⁻ implant
STEPS:
1) Deposit insulation 1(S/3N4)
Semi-insulating GaAs substrate
2) n⁻ implant (high resistivity)
n⁺ implant
3) n⁺ implant (low resistivity)
Semi-insulating GaAs substrate
4) Deposit insulation 2
5) Anneal implant
Semi-insulating GaAs substrate
Au/Ge/Pt contact
6) Deposit ohmic contacts
Semi-insulating GaAs substrate
7) Deposit gate (Ti/Pt/Au)
8) 1st level metal
Semi-insulating GaAs substrate
9) Via contact cuts
10) 2nd level metal

Figure A1.1 GaAs D-MESFET planar fabrication process [74].

A2.1 Ion Implantation and Annealing

The ion implantation and subsequent annealing are very significant in this process. In ion implantation, doping is achieved by bombarding the semiconductor surface with high velocity ion beam. Doping density and dopants distribution are controlled by varying the ion flux and velocity. The advantages of ion implantation are independent control of doping level, doping profile and selective doping of selected areas.

Annealing provides energy to the implanted impurities and results in moving the interstitial dopant ions into lattice positions where they become electrically active. Furthermore, the displaced substrate atoms are subsequently moved back to their crystallographic lattice locations which then gives the high electron mobility.

A3.0 Enhancement Mode MESFET Planar Process

Steps for the fabrication of GaAs enhancement mode MESFETs are summarised below:

(A) Encapsulation

- (i) wafer preparation
- (ii) encapsulation (first layer insulator)
- (iii) alignment mark mask
- (iv) alignment mark metallisation and lift-off

(B) Ion implantation

- (i) first Si^+ implant (E-MESFET) mask
- (ii) channel implant

(iii) second first Si^+ implant (D-MESFET) mask

(iv) channel implant

(v) source and drain implant mask

(vi) n^+ implant and anneal

(C) Schottky junction and first level metal

(i) patterning ohmic contact mask

(ii) plasma etching contact windows

(iii) contact metallisation

(iv) contact definition and alloy

(v) H^+ implant

(vi) Schottky gate mask

(vii) plasma etch Schottky windows

(viii) metallisation and lift-off

(D) Second level metal

(i) dielectric (SiO_2 sputter)

(ii) via cut mask

(iii) metallisation and lift-off

(E) Scratch protection

(i) Si_3N_4 plasma deposition

(ii) pad/scribe street mask

(iii) plasma etch.

A4.0 Self-Aligned Gate E-D MESFET Process

An alternative approach in fabrication process technology for very high speed VLSI systems is the self-aligned gate (SAG) process. There are two methods for producing the self-aligned structure. These methods are normally referred as the gate-priority and ohmics-priority approaches. The first approach uses the temperature stable gate technique [73] in which the gate metal is first deposited and patterned which then acts as an implantation mask for the self-aligned n^+ contact layers.

The second approach involves more complex processing, relying on dielectric lift off using tri-level photoresist technique to define the placing of the gate metal at the controlled distance from the selectively implanted n^+ regions. Enhancement and depletion mode GaAs MESFETs have been fabricated using the self-aligned MESFET technology known as SAINT (self-aligned for n^+ layer technology). A typical process sequence for SAINT is illustrated in Figure A1.2. The main feature of the SAINT MESFET is that its n^+ layer is embedded between the source and the drain electrodes beside the gate channel region. Process steps for a self-aligned gate E-D GaAs MESFET are as follows:

(i) a n^- implantation for formation of E-MESFET

(ii) a second n^+ implantation for the formation of D-MESFET

(iii) formation of Schottky gates on the n-type GaAs layer

(iv) a third, n$^+$, implantation for the formation of source and drain

(v) an anneal cycle at $850^0 C$ to activate dopants

(vi) ohmic metallisation of the source and drain

(vii) interconnect metallisation.

In summary, the steps in this process entail defining the active areas that will eventually form E- and D-MESFETs, followed by two ion implantations, that is, lightly doped for E-MESFET and heavily doped for D-MESFET followed by the formation of gate metal.

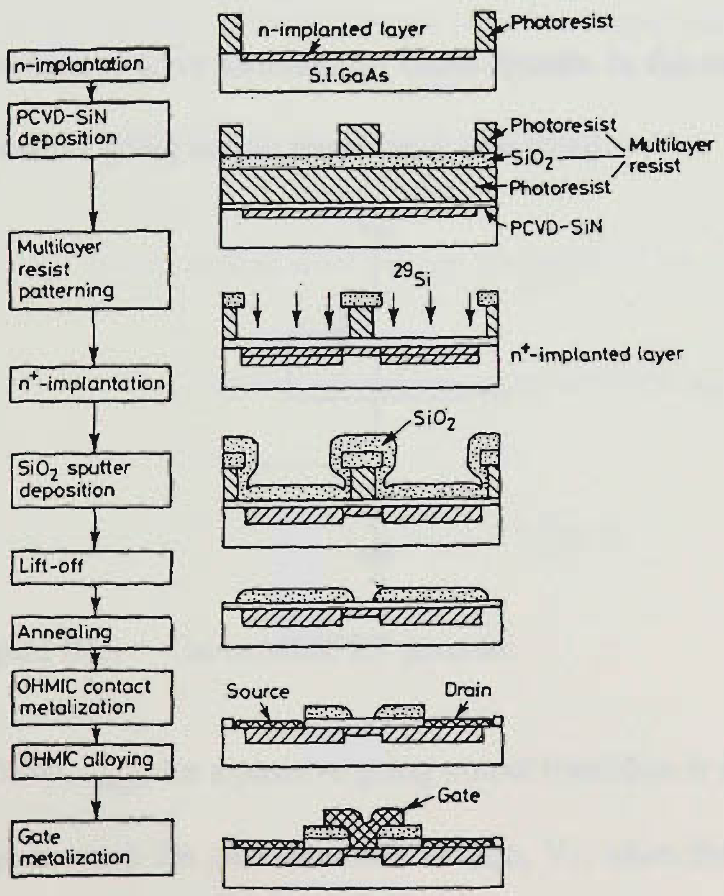


Figure A1.2 SAINT process flow [73].

Appendix B

Propagation Delay and Power Dissipation of GaAs MESFET Logic

B1.0 Propagation Delay - Enhancement Mode Logic Gates

The inverter structure, shown in Figure B1.1, is used as the basic building block for E-MESFET logic gates. Its operation is identical to an NMOS inverter and similar approximations are used to drive formulas for GaAs circuits. In this section propagation delay, $t_{pd(p)}$, of a positive going output transition is computed.

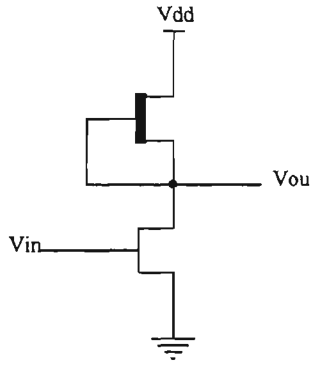


Figure B1.1 GaAs MESFET inverter.

The propagation delay, $t_{pd(p)}$, for a positive going output transition is defined as the time it takes the voltage to reach the gate threshold voltage, V_T, when the input is switched from the high logic level V_{HIGH} to a low logic level V_{LOW}. The computation of $t_{pd(p)}$ assumes that the output node is loaded with a constant capacitive load $C_{N.}$

During the transient, the E-MESFET is cut off while the D-MESFET is in its saturation region. This is because, in general, V_T is chosen so that,

$$V_T < V_{DD} - |V_{P(D)}| \qquad \textbf{(B1.0)}$$

where $V_{P(D)}$ is the pinch off voltage of the D-MESFET, and

V_{DD} is the positive supply voltage.

Considering that the gate-to-source voltage, V_{GS}, for D-MESFET is zero, the saturation current in the depletion device can be approximated as [75]:

$$I_{DS(D)} = K'_{(D)}.\frac{W_{(D)}}{L_{(D)}}.\left|V_{P(D)}\right|^2.(1+\lambda.V_{DS(D)}) \qquad \textbf{(B1.1)}$$

where $K'_{(D)}$ the process transconductance parameter for D-MESFET,

λ is the channel length modulation parameter, and

$V_{DS(D)}$ is the drain-to-source voltage for D-MESFET.

With $V_{DS(D)} = V_{DD} - V_{OUT}$, the above expression can be rewritten as:

$$I_{DS(D)} = K'_{(D)}.\frac{W_{(D)}}{L_{(D)}}.\left|V_{P(D)}\right|^2.(1+\lambda.V_{DD}-\lambda.V_{OUT}) \qquad \textbf{(B1.2)}$$

or

$$I_{DS(D)} = \frac{V_G - V_{OUT}}{R_G} \qquad \textbf{(B1.3)}$$

where

$$V_G = \frac{\lambda.V_{DD}+1}{\lambda} \qquad \textbf{(B1.4)}$$

and

$$R_G = \frac{1}{\left|V_{P(D)}\right|^2.K'_{(D)}.\frac{W_{(D)}}{L_{(D)}}.\lambda} \qquad \textbf{(B1.5)}$$

Expressions B1.3 through B1.5 imply that the D-MESFET can be represented by a voltage source V_G in series with a source resistance R_G. Assuming that the initial voltage is V_{LOW}, then the output voltage as a function of time can be written as:

$$V_{OUT} = V_{LOW} + (V_G - V_{LOW}).[1 - \exp(\frac{-t}{R_G.C_N})] \qquad \textbf{(B1.6)}$$

and therefore $V_{OUT} = V_T$ at time $t_{pd(p)}$ given by:

$$t_{pd(p)} = R_G.C_N.\ln\frac{V_G - V_{LOW}}{V_G - V_T} \qquad \textbf{(B1.7)}$$

For most cases it can be assumed that V_{LOW} is zero volts, and therefore

$$t_{pd(p)} = R_G.C_N.\ln\frac{V_G}{V_G - V_T} \qquad \textbf{(B1.8)}$$

The total effective load capacitance, C_N, of the output node is a result of the inherent device capacitances in a logic gate, the fan in and the fan out connected to the gate. Therefore, for a logic gate with fan in FI and fan out FO and by assuming one input is switched at a time, C_N can be expressed as:

$$C_N = (FI + 1).C_{GD(E)} + FI.C_{DS(E)} + C_{DS(D)}.C_{GD(D)} + FO.(C_{GS(E)} + 2C_{GD(E)}) \qquad \textbf{(B1.9)}$$

where C_{XX} are the interelectrode capacitances for E- and D-MESFETs and a factor of 2 has been included for the Miller effect. The above expression does not include the effect of stray capacitance which, in general, will be loading the circuit. The stray capacitance depends on the circuit geometry and the fabrication process.

The propagation delay $t_{pd(n)}$ for the negative going output transition is defined as the time required for the output voltage to switch from V_{HIGH} to a logic gate threshold, when the input is switched from V_{LOW} to V_{HIGH}. In this case also, a constant capacitive load C_N is assumed for the output node. The propagation delay $t_{pd(n)}$ is usually computed numerically through computer simulation.

An indirect way to determine the average propagation delay of a GaAs MESFET gate (i.e. $\frac{t_{pd(n)}+t_{pd(p)}}{2}$) is given by measuring the oscillation frequency of an odd number of inverters connected to form a ring oscillator. The average delay time, t_D, is given by:

$$t_D = \frac{t_{pd(n)}+t_{pd(p)}}{2} = \frac{1}{2.N_r.f_o} \qquad \textbf{(B1.10)}$$

where f_o is the oscillation frequency, and

N_r is the odd number of inverters forming a ring oscillator.

This expression, however, assumes that all the inverters have the same geometry and the interconnection between the stages contribute very little to the propagation delay. In a ring oscillator, all the inverters have fan in and fan out equal to one, which is rarely the case in a logic circuit. Therefore, the results obtained from expression B1.10 should be treated as relative indications of an upper bound that should be expected from a logic gate fabricated with a given process.

B2.0 Power Dissipation

The power dissipation of a GaAs MESFET inverter, shown in Figure B1.1, switching at frequency, *f*, has a static power P_{st} which is independent of *f* and a dynamic component P_d which is proportional to *f*. The static component of total power dissipation is described by the following expression [75]:

$$P_{st} = \frac{I_{DS}(V_{DD} - V_{LOW}).V_{DD}}{2} \qquad \textbf{(B1.11)}$$

This results from resistive heating of the switching device and the load during the periods when the switching device is ON, which is assumed to be half of the time. Additional static power is dissipated by current flowing through the gates of circuits connected to the output node in case $V_{DD} > V_{GM}$, where V_{GM}, is the forward gate bias at which the device gate junction becomes highly conductive. This power dissipation can be expressed as:

$$P'_{st} = \frac{I_{DS}(V_{DD} - V_{GM}).V_{DD}}{2} \qquad \textbf{(B1.12)}$$

The dynamic power dissipation results from the periodic charge and discharge of the output node capacitance, C_N, and is expressed as :

$$P_d = C_N.V_{OUT}^2.f \qquad \textbf{(B1.13)}$$

The total power dissipation for a GaAs MESFET inverter is thus expressed as:

$$P_{total} = P_{st} + P'_{st} + P_d \qquad \textbf{(B1.14)}$$

Appendix C

Analysis of Noise Margins of GaAs MESFET Logic

C1.0 Noise Margins

Noise margins of an inverter are a measure of its immunity against the possibility of producing a logical error (high instead of low, and vice versa) owing to impulsive noise injected at a node, to variation of the logical high and low levels over a chain of inverters or logic gates. They are best obtained by superimposing the transfer curves of two identical inverters with the input of one being the output of the other, as shown in Figure C1.1. Noise margins can be computed graphically from this transfer curve as:

$$\textbf{NML(noise margin low)} \quad = \quad V_{IL} - V_{OL} \qquad \textbf{(C1.0)}$$

$$\textbf{NMH(noise margin high)} \quad = \quad V_{OH} - V_{IH} \qquad \textbf{(C1.1)}$$

where V_{IL} is the input voltage low,

V_{IH} is the input voltage high,

$\mathbf{V_{OL}}$ is the output voltage low, and

$\mathbf{V_{OH}}$ is the output voltage high.

While the graphical solution gives us a qualitative description of the circuit performance, it does not serve as design guidelines that provide insights into design trade offs. An analytical formulas are needed to measure the noise margins performance.

Since the circuit is nonlinear, it is impossible to obtain closed form expressions for these measures. However, approximations can be made that will simplify the analysis to the extent that noise margins can be computed in terms of the device parameters.

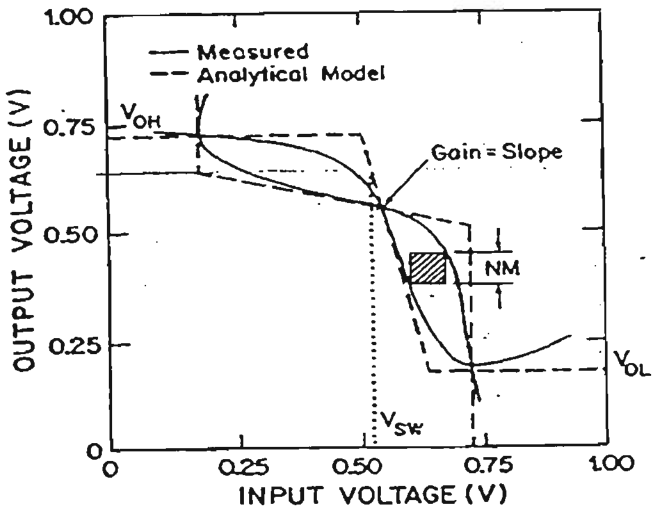


Figure C1.1 Transfer curves to calculate noise margins [94].

In this section, expressions for the low and high noise margins will be derived in terms of the device parameters. With reference to Figure C1.2, consider the case where $V_{in} = V_{OL}$. If V_{OL} is sufficiently low, V_{OH} will be high enough to cause gate current to flow in the second stage. Moreover, the drain current of the second stage will be substantial to cause the voltage drops across the series source and drain resistances to be significant. In a properly designed circuit, the output of the second stage must be at least as low as V_{OL} in order that the pair of inverters are self restoring. With reference to the equivalent circuit, shown in Figure C1.3, the circuit equations are defined as:

$$I_{d1} = I_{e1} + I_{D1} \qquad \textbf{C1.2)}$$

$$V_{OH} = V_{D1} + V_s \qquad \textbf{(C1.3)}$$

$$V_s = R_s(I_{D1} + I_{d2}) \qquad \textbf{(C1.4)}$$

$$I_{D1} = I_s[\exp(\frac{q.V_{D1}}{n.k.T}) - 1] \qquad \textbf{(C1.5)}$$

where I_s is the diode saturation current and n is the ideality constant.

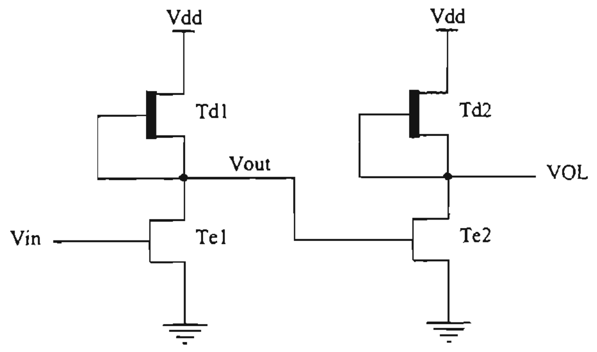


Figure C1.2 DCFL inverter structure for noise margin calculation.

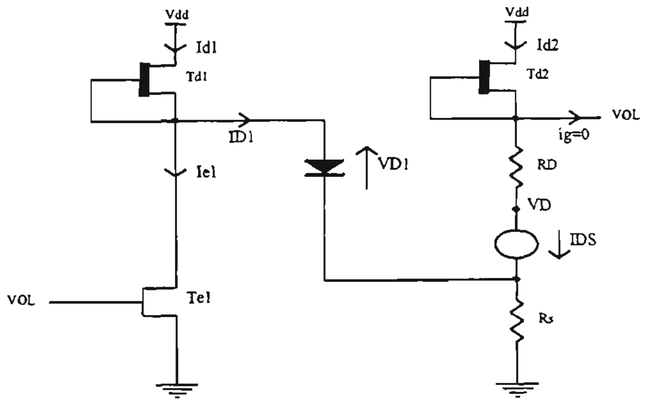


Figure C1.3 Equivalent circuit of the inverter circuit shown in Figure C1.2.

Combining the above expressions gives:

$$V_{OH} = (\frac{n.k.T}{q})\log(\frac{I_{d1} - I_{e1}}{I_s}) + R_s(I_{d1} - I_{e1} + I_{d2}) \qquad \textbf{(C1.6)}$$

From Figure C1.3 it can be seen that

$$I_{d2} = I_{e2} \qquad \textbf{(C1.7)}$$

and

$$V_s = R_s(I_{d1} - I_{e1} + I_{d2}) \qquad \textbf{(C1.8)}$$

Equations C1.6 - C1.8 constitute a set of three nonlinear equations and can be solved by Newton iteration.

The saturated value of the drain current, $I_{d2(sat)}$, is defined by [113]:

$$I_{d2(sat)} = \beta_{e2} \cdot \frac{(V_{OH} - V_s - V_{Te})^2}{1 + b_e(V_{OH} - V_s - V_{Te})} \cdot$$

$$\tanh \alpha_e(V_{OL} - V_s - R_D . I_{d2(sat)}).[1 + \lambda_e(V_{OL} - V_s - R_D . I_{d2(sat)}) \qquad \textbf{(C1.9)}$$

where β, α, λ and b are the GaAs MESFET HSPICE parameters, and V_T is the device threshold voltage. The subscript d and e signifies depletion and enhancement mode devices.

Since V_{OL} will be small, the last term can be approximated by unity and equation can be solved to give:

$$V_{OL} = V_s + R_D . I_{d2(sat)} +$$

$$\frac{1}{2\alpha_e}.\log \frac{\beta_{e2}.\frac{(V_{OH}-V_s-V_{Te})^2}{I_{d2(sat)}} + [1+b_e(V_{OH}-V_s-V_{Te})]}{\beta_{e2}.\frac{(V_{OH}-V_s-V_{Te})^2}{I_{d2(sat)}} - [1+b_e(V_{OH}-V_s-V_{Te})]} \qquad \textbf{(C1.10)}$$

The low level input voltage, V_{IL}, is defined as the input voltage such that if the input exceeds this value by a slight amount the output will drop to a value just low enough to cause the diode current, I_{D1}, to become zero. Similarly the input high voltage, V_{IH}, is defined as the largest input voltage for which there is no gate current in the enhancement transistor T_{e1} and its output voltage equals V_{OL}. The expressions for V_{IL} and V_{IH} are derived in a similar manner as V_{OL} and V_{OH}, and are expressed as [114]:

$$V_{IL} = V_{Te} + V_{ch}.\sqrt{1+\frac{V_{ch}^2.b_e^2}{4}+\frac{V_{ch}^2.b_e}{2}} \qquad \textbf{(C1.11)}$$

$$V_{IH} = V_{Te} + V_{cl}.\sqrt{1+\frac{V_{cl}^2.b_e^2}{4}+\frac{V_{cl}^2.b_e}{2}} \qquad \textbf{(C1.12)}$$

where $$V_{ch}^2 = \frac{I_{d1}}{\beta_{e1}(1+\lambda_e.V_{OH})\tanh\alpha_e.V_{OH}} \qquad \textbf{(C1.13)}$$

$$V_{cl}^2 = \frac{I_{d1}}{\beta_{e1}(1+\lambda_e.V_{OL})\tanh\alpha_e.V_{OL}} \qquad \textbf{(C1.14)}$$

Hence computed the values $V_{OH,}$ V_{OL}, V_{IL} and V_{IH}, the low and high noise margins can calculated using expressions C1.0 and C1.1 respectively.

Appendix D

SCFL Circuit - Analysis of SCFL circuit and Effect of Threshold Voltage Variation

D1.0 DC Characteristics

A SCFL inverter consists of a differential amplifier and source follower buffers as shown in Figure D1.1. The drain current, I_{dsi}, for the differential pair is given by [8]:

$$I_{dsi} = \beta_i . (V_{ini} - V_s - V_{ti})^2 \quad (i = 1,2) \qquad \textbf{(D1.0)}$$

where i represents GaAs MESFET$_i$

V_{ini} is the gate voltage

V_s is the common source voltage and

V_{ti} is the E-MESFET$_i$ threshold voltage.

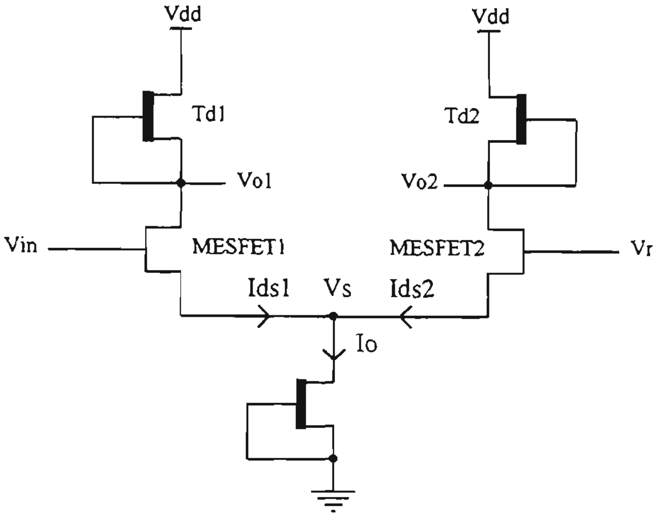


Figure D1.1 A SCFL inverter.

The current I_0 which flows through the common source, is given as a sum of the currents through E-MESFET1 and E-MESFET2 as:

$$I_0 = I_{ds1} + I_{ds2}$$
$$= \beta_1.(V_{in} - V_s - V_{t1})^2 + \beta_2.(V_{ref} - V_s - V_{t2})^2 \qquad \textbf{(D1.1)}$$

where I_{ds1} and I_{ds2} are the drain currents through E-MESFET1 and E-MESFET2 respectively, and

β_1 and β_2 are the HSPICE parameters dependent on process and geometry of E-MESFET1 and E-MESFET2 respectively.

Elimination of V_s from equations D1.0 and D1.1 yields:

$$I_{ds1} = \frac{a}{\beta_2} + \frac{b}{x^2} + c.x.\sqrt{(\beta_1 + \beta_2)I_0 - \beta_1.\beta_2.x^2} \qquad \textbf{(D1.2)}$$

and $$I_{ds2} = \frac{a}{\beta_1} + \frac{b}{x^2} + c.x.\sqrt{(\beta_1 + \beta_2)I_0 - \beta_1.\beta_2.x^2} \qquad \textbf{(D1.3)}$$

where $$x = (V_{in} - V_{ref}) + (V_{t1} - V_{t2})$$

$$a = \frac{\beta_1.\beta_2}{(\beta_1 + \beta_2)}$$

$$b = \frac{\beta_1.\beta_2}{(\beta_1 - \beta_2)}$$

$$c = \frac{2.\beta_1.\beta_2}{(\beta_1 + \beta_2)^2}$$

If E-MESFET1 and E-MESFET2 are symmetric, the following relationship becomes valid:

$$V_{t1} = V_{t2} \qquad \textbf{(D1.4)}$$

Thus expressions for I_{ds1} and I_{ds2} become

$$I_{ds1} = \frac{I_0}{2} + \frac{\beta_1}{2}(V_{in} - V_{ref}).\sqrt{\frac{2.I_0}{\beta_1} - (V_{in} - V_{ref})^2} \qquad \textbf{(D1.5)}$$

and

$$I_{ds2} = \frac{I_0}{2} + \frac{\beta_2}{2}(V_{in} - V_{ref}).\sqrt{\frac{2.I_0}{\beta_2} - (V_{in} - V_{ref})^2} \qquad \textbf{(D1.6)}$$

D2.0 Transition Frequency, f_T

A small signal equivalent circuit of a MESFET is shown in Figure D1.2. The hybrid parameter, h_{21} can be expressed as [9]:

$$h_{21} = \frac{g_m.j\omega.C_{gd}}{\omega^2.C_{gs}.R_i + j\omega(C_{gs} + C_{gd})} \qquad \textbf{(D1.7)}$$

where ω is the angular frequency

C_{gs} is the gate-to-source capacitance and

C_{gd} is the gate-to-drain capacitance.

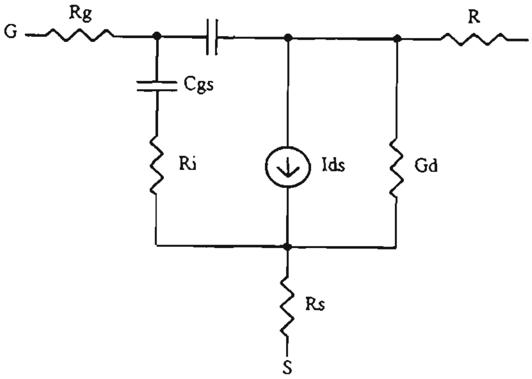


Figure D1.2 GaAs MESFET equivalent circuit for small signal analysis.

When $\omega^2 C_{gs} R_i$ is very much less than $\omega(C_{gs} + C_{gd})$ and g_m is very much greater than ωC_{gd} at low frequency, $|h_{21}|$ is obtained as follows:

$$|h_{21}| = \frac{g_m}{\omega(C_{gs} + C_{gd})} \qquad \textbf{(D1.8)}$$

When $|h_{21}| = 1$, f_T is expressed as:

$$f_T = \frac{g_m}{2\pi(C_{gs} + C_{gd})} \qquad \textbf{(D1.9)}$$

D3.0 Threshold Voltage variation in SCFL circuit

In this section the effects of threshold voltage variations of the enhancement GaAs MESFET on the circuit threshold voltage is analysed. For symmetrical SCFL circuit, at the cross over, $V_{o1} = V_{o2}$, so $V_{ds1} = V_{ds2}$ and $I_{ds1} = I_{ds2}$. Therefore

$$V_{gs1} - V_{t1} = V_{gs2} - V_{t2} \tag{D1.10}$$

or

$$V_{in} - V_s - V_{t1} = V_2 - V_s - V_{t2} \tag{D1.11}$$

In the case where $V_2 = V_{ref}$, the circuit threshold voltage V_{cir} is expressed as:

$$V_{cir} = V_{ref} + V_{t1} - V_{t2} \tag{D1.12}$$

and if $V_{in} + V_2 = V_{ref}$, then

$$2V_{cir} = V_{ref} + V_{t1} - V_{t2} \tag{D1.13}$$

In either case the circuit threshold voltage in independent of the device threshold voltage if $V_{t1} = V_{t2}$ and if the change in V_{t1} tracks the change in V_{t2}, a condition to be expected since the two E-MESFETs are likely to be adjacent to each other on a chip.

Appendix E

Gallium Arsenide MESFET Layout Methodology

E1.0 Lambda Based Layout Rule

The lambda based design rule was made popular by Mead and Conway [107] for silicon, and are based on single parameter, lambda (λ), which characterises the linear features as well as the resolution of the complete wafer implementation process. Table E1.0 and Figure E1.1 illustrate the lambda based rule set [74]. From Figure E1.1 it can be seen that the rule set is defined in terms of feature size, separation and overlaps.

Although diffusion, metal 1, and metal 2 can cross each other without interaction , in some processes metal 1 is not permitted to cross diffusion. There are two types of implant used to form the two different transistors. It is essential for gate metal (red) to

Table E1.1 Lambda based layout rule for GaAs MESFET

Layer	CIF Code	Rule Feature		Dimension - Lambda (λ)
Diffusion	GD	A1	width	5
		A2	spacing	5
		A3	to n^+	5
		A4	E-MESFET width	5
Depletion implant n^+	GI	B1	D-MESFET gate overlap	2
		B2	width	7
		B3	spacing	5
		B4	spacing to E-MESFET	2
Ohmic contact	GH	C1	contact width	5
		C2	spacing	5
		C3	cut overlap	2
Gate metal	GP	D1	gate metal extension	2
		D2	gate metal length	3
		D3	gate metal width	3
		D4	cut overlap	2
		D5	gate metal spacing	5
		D6	spacing to ohmic contact	3
Contact	GC	E1	cut size	4 x 4
		E2	cut spacing	4
		E3	spacing to via	4
Metal 1	GM	F1	width	4
		F2	spacing	5
		F3	cut overlap	2
		F4	via overlap	2
Via	GV	G1	via size	5 x 5

		G2	via spacing	5
Metal 2	GN	H1	width	5
		H2	spacing	5
		H3	overlap of via	2

completely cross the implant (green) region, otherwise the transistor that has been created will be shorted by a $\mathbf{n}^-$ path between source and drain. To ensure that this condition is satisfied, 2λ of gate metal extension is necessary. This is known as Schottky extension.

Orientation of GaAs MESFETs is an important consideration during layout. All MESFETs need to be positioned horizontally owing to the anisotropic nature of GaAs, which influences the threshold voltage of the device. There are several enhancements that may be added to the GaAs process, primarily to provide active load, capacitors, resistors and to increase routability of the circuit through a third metal layer.

The approach taken here has been to focus attention on the main features of a typical design rule that a VLSI designer must become familiar with.

E2.0 Layer Encoding and Layer Connectivity

The layer coding used for GaAs MESFET layout is presented in Figure E1.2. The coding has been complemented by monochrome encoding of the lines so that black and

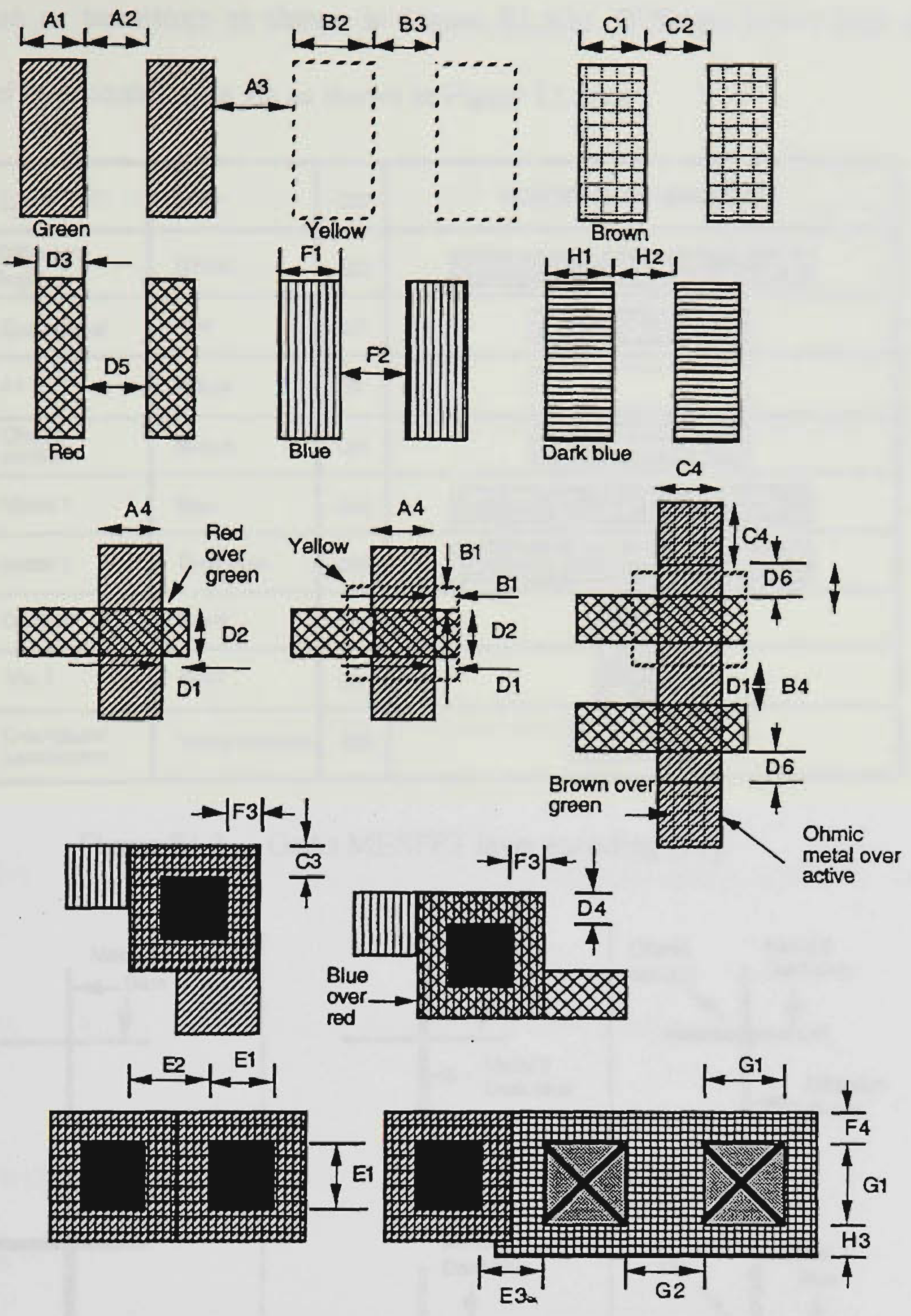
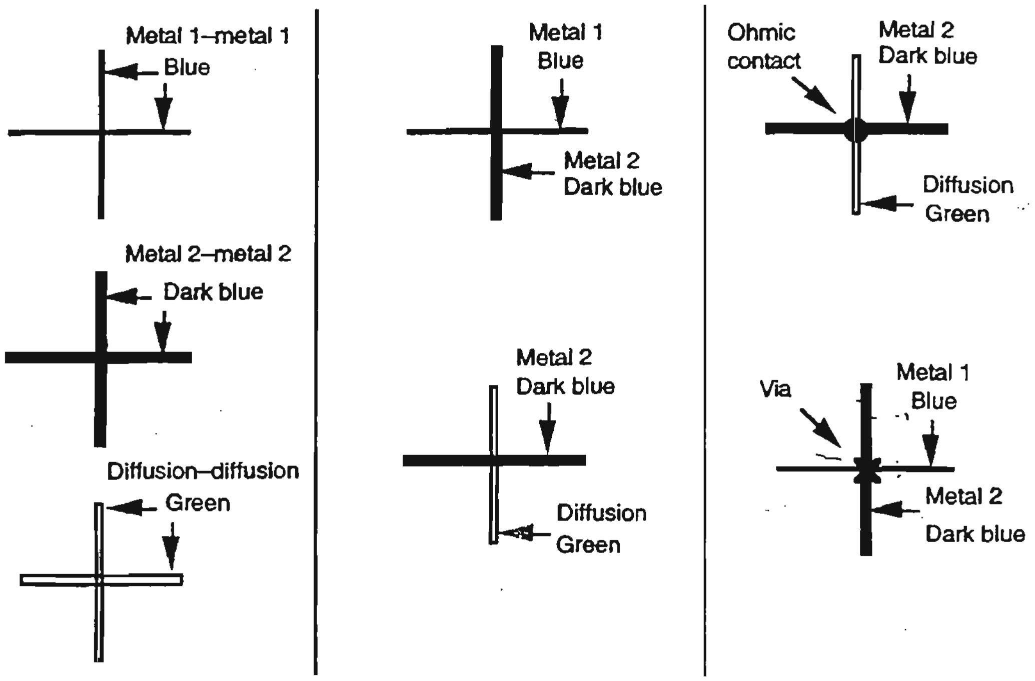


Figure E1.1 Lambda based rules for GaAs MESFET process.

white copies of circuit representation using ring notation do no loose the layer information. In GaAs MESFET layout, intersections on the same layer form interconnections as in Figure E1.3(a). Intersections on different layers do not form connection or transistors as shown in Figure E1.3(b). Different layers may also be connected by a contact or a via as shown in Figure E1.3(c).

Layer	Color	CIF	MONOCHROME ENCODING
Diffusion/ implant	Green	GD	▨
Gate-metal	Red	GP	▩
n+	Yellow	GI	⬚
Ohmic contact	Brown	GH	▦
Metal 1	Blue	GM	▥
Metal 2	Dark blue	GN	▤
Contact	Black	GC	■
Via 1	Gray	GV	⊠
Overglass/ passivation	White stipples	GG	▭

Figure E1.2 GaAs MESFET layer encoding [74].



(a) Same layer connection

(b) Different layers no connection

(c) Different Layers connection by contact

Figure E1.3 Layer connectivity [74].

E3.0 ISD GaAs VLSI Design Sequence

The design cycle usually followed using ISD VLSI Phase I software is illustrated in Figure E1.4. The Phase I suite consists of the following tools:

(i) **PLAN** a powerful mask level graphic full custom layout tool,

(ii) **SEE** a general purpose graphic display tool,

(iii) **CHECK** a fast corner based design rule checker,

(iv) **GAASNET** an accurate and efficient GaAs circuit extractor, and

(v) **ELEC** a versatile electrical rules checker,

together with three utility programs **P2C**, **C2P**, and **POINTS**.

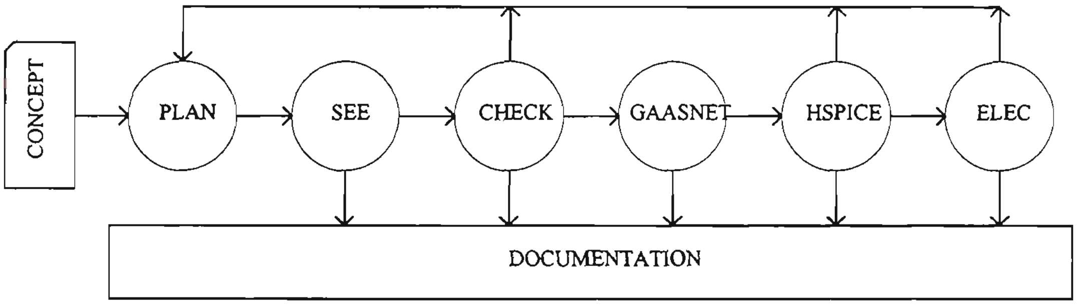


Figure E1.4 Phase I VLSI design cycle.

E3.1 PLAN

The tool PLAN is a menu driven, fixed grid, lambda based interactive graphic screen editing tool for Manhattan geometry VLSI design. The mask level layout of the circuit is designed and edited using the PLAN. The syntax for general PLAN command is:

```
plan [ -[options].......] [<filename>]
```

The available options in PLAN are:

v	version
u	brief user summary
i	turn off information message
t <name>	set technology
o <name>	set screen driver
r <number>	set replay mode

Typical PLAN graphic display is shown in Figure E1.5.

E3.2 SEE

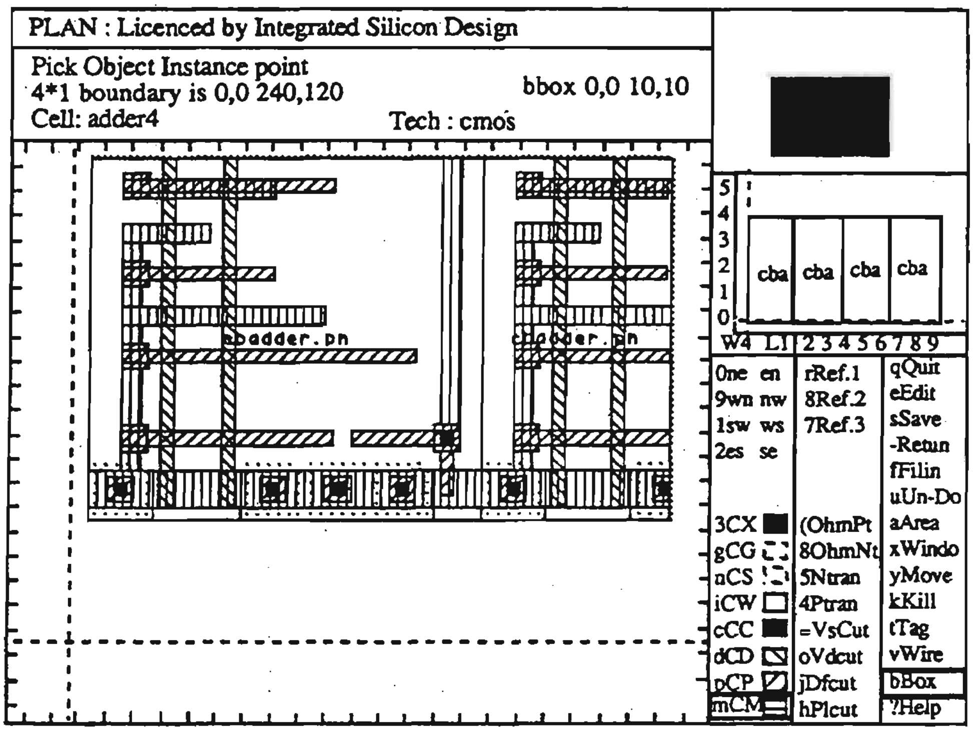
The tool SEE is a multimode VLSI circuit viewing aid designed to draw from a CIF circuit description a scaled representation of the circuit masks on a variety of screen. The syntax for the SEE command is:

```
see [ -[options].......] [<filename>]
```

The available options in SEE are:

d	choose default values
t <name>	set technology
u	brief user summary
o	hard copy device
v	print program identification

While in SEE there are a number of interactive keyboard commands available to enable the user to move about the design easily.



PLAN : Licenced by Integrated Silicon Design

Pick Object Instance point
4*1 boundary is 0,0 240,120 bbox 0,0 10,10
Cell: adder4 Tech : cmos

Figure E1.5 PLAN graphic display.

E3.3 Check

The tool check is a fast corner based VLSI circuit verification tool designed to detect geometrical design rule errors. The use of CHECK enables the designer to ensure that a design is fully compatible with the design rules of a particular fabrication process. The input required by CHECK is a CIF file describing the design. The output provided by the program is a design rule error file or a screen listing containing the list of errors found, a brief description of each, and a report of the location in lambda coordinates of the error. The syntax for the CHECK command is:

```
check [ -[options].......] [<filename>]
```

The available options in CHECK are:

c	lists the CIF file being parsed
f <name>	flatten geometry to a file
l <number>	sets lambda value
o <name>	sends check message to a file
r	lists design rules
t <name>	set technology type
s <tx ty>	set tile width and height
w <lx ly ux uy>	window a section of design to be checked
u	brief user summary
v	print program identification

E3.4 GAASNET

GAASNET is a VLSI circuit verification tool used to extract a net list description and other relevant design information from the circuit description file expressed in CIF. The syntax for the GAASNET command is:

```
gaasnet [ -[options].......] [<filename>]
```

The available options in GAASNET are:

c	lists the CIF file being parsed
f <format>	set output format to one of SPICE, PSPICE or HSPICE
R	select Raytheon MESFET model. The default is the Curtice MESFET model
z	select low frequency MESFET model

The circuit simulation is performed using HSPICE circuit simulation suite consisting of HSPICE, HSPLOT and the necessary Graphical Simulation Interface.

E3.5 ELEC

The tool ELEC is a VLSI circuit verification tool designed to operate on the netlist circuit description. ELEC is designed to give the user feedback on the electrical aspects of a design so that informed decisions can be made about the correctness or otherwise.

ELEC uses as its input the extracted circuit description generated by GAASNET. The syntax for the ELEC command is:

```
elec [ -[options].......] [<filename>]
```

The available options in ELEC are:

i	information listing
t <name>	set technology
v	print program identification
o <name>	write to ELEC warning file.

Appendix F

Adder Design and Performance of Components of Power Series Evaluator

F1.0 Adder Design

The functional representation of a full adder is shown in Figure F1.1. The operation of an adder is described by the truth table shown in Table F1.1 where A and B are the input bits to be added, C is the carry-in from the previous stage, S is the sum-out and C_{out} is the carry-out.

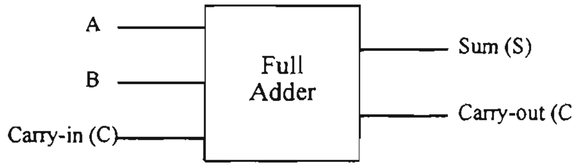


Figure F1.1 Full adder functional block diagram.

The boolean expressions for the two outputs S and C_{out} can be obtained using karnough mapping technique shown in Figure F1.2.

Table F1.1 Truth table for a full adder

Inputs			Outputs	
A	B	C	S	C_{out}
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

BA		00	01	11	10
C	0	0	1	0	1
	1	1	0	1	0

S (Sum)

BA		00	01	11	10
C	0	0	0	1	0
	1	0	1	1	1

C_{out} (Carry-out)

Figure F1.2 Karnough map for S (Sum) and C_{out} (Carry-out)

Sum and Carry-out are expressed as follows:

$$Sum = A'B'C + A'BC' + AB'C' + ABC \qquad \textbf{(F1.0)}$$

$$Carry\text{-}out = A'BC + AB'C + ABC' + ABC \qquad \textbf{(F1.1)}$$

Using De'Morgans theorem, expressions F1.0 and F1.1 can be expressed as:

$$Sum = \overline{\overline{(A+B+C')}+\overline{(A+B'+C)}+\overline{(A'+B+C)}+\overline{(A'+B'+C')}} \qquad \textbf{(F1.2)}$$

$$Carry\text{-}out = \overline{\overline{(A' + B')} + \overline{(A' + C')} + \overline{(B' + C')}} \qquad \textbf{(F1.3)}$$

F2.0 VLSI Mask Layout and Simulation of the components of Power Series Evaluator Cell

The VLSI layout and HSPICE simulation results for the adder, two-to-one multiplexer and the register are shown in Figures F1.3 - F1.8. The circuits were implemented using 0.8 micron E-D GaAs MESFET technology using ISD VLSI design suite.

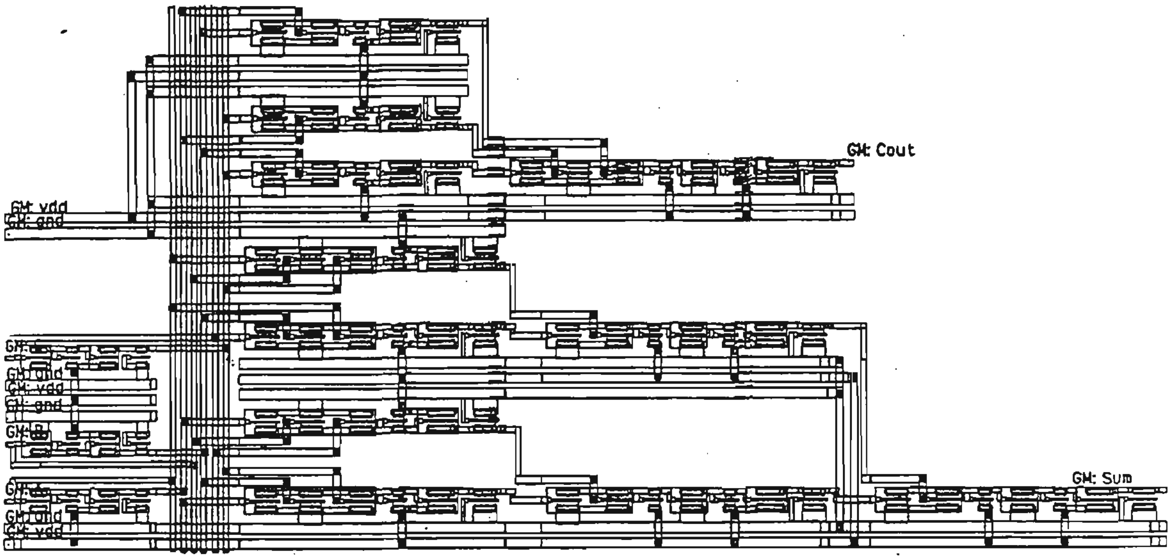


Figure F1.3 Mask layout of an adder.

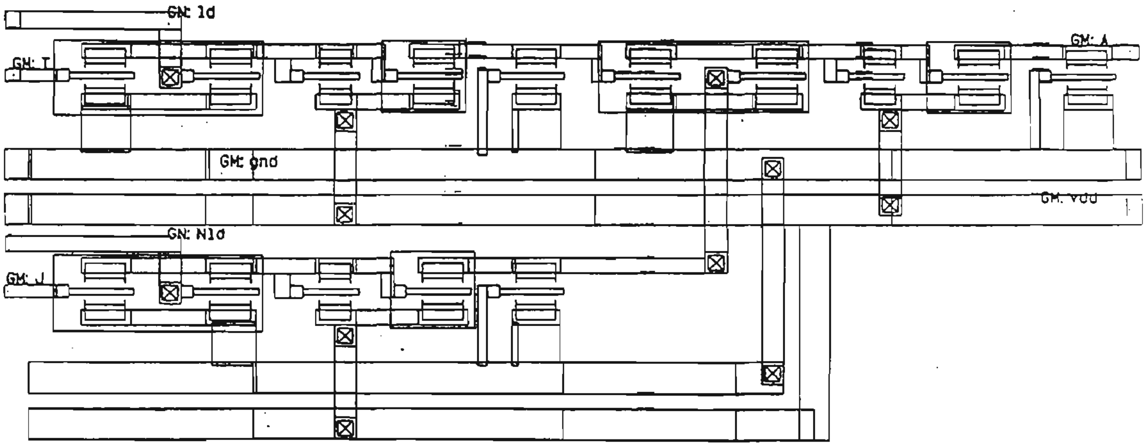


Figure F1.4 Mask layout of a two-to-one multiplexer.

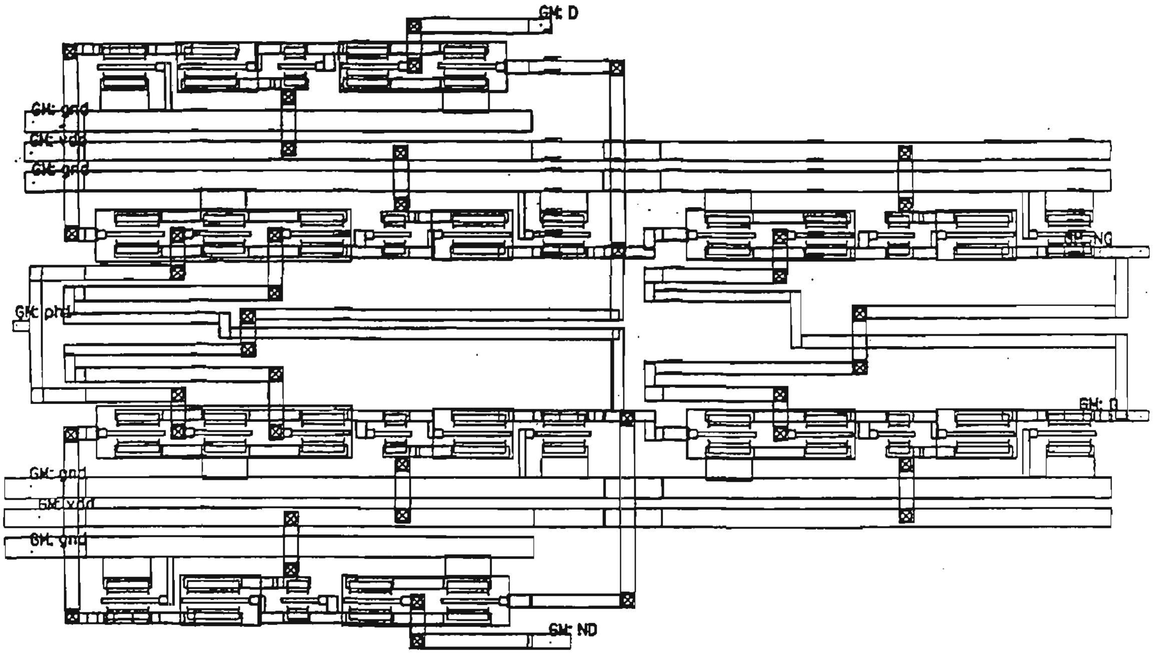


Figure F1.5 Mask layout of an one-bit register.

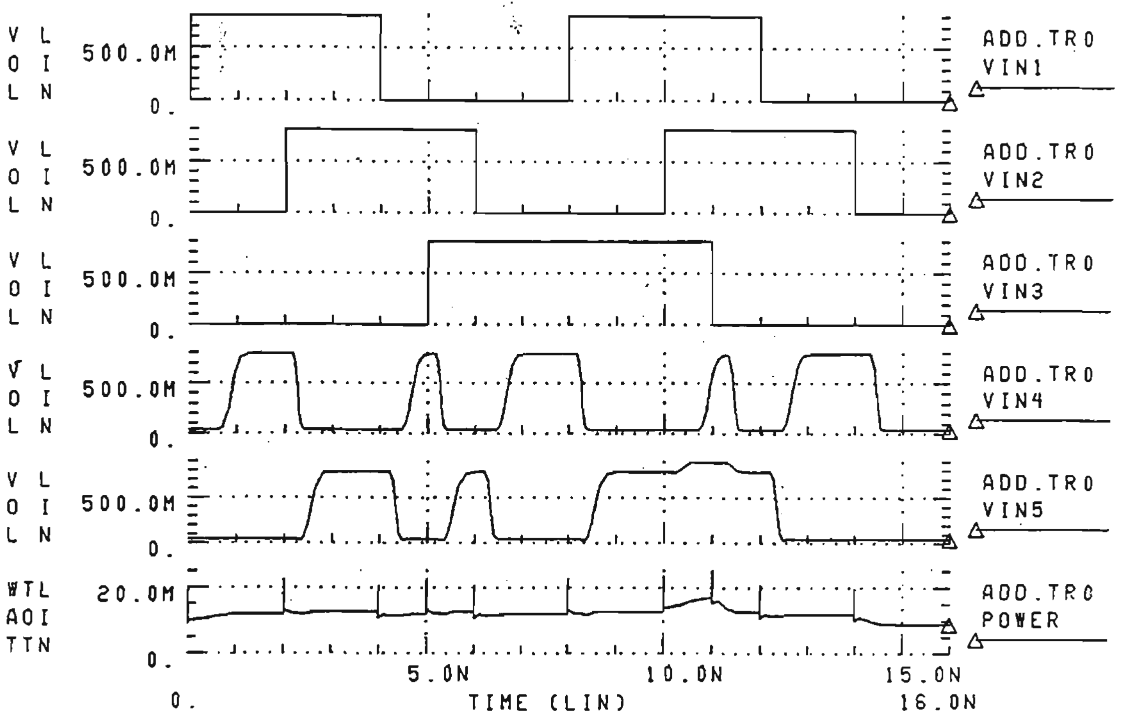


Figure F1.6 HSPICE simulation results for an adder.
VIN1 - VIN5 represent inputs A, B, C and outputs Sum and Carry out respectively.

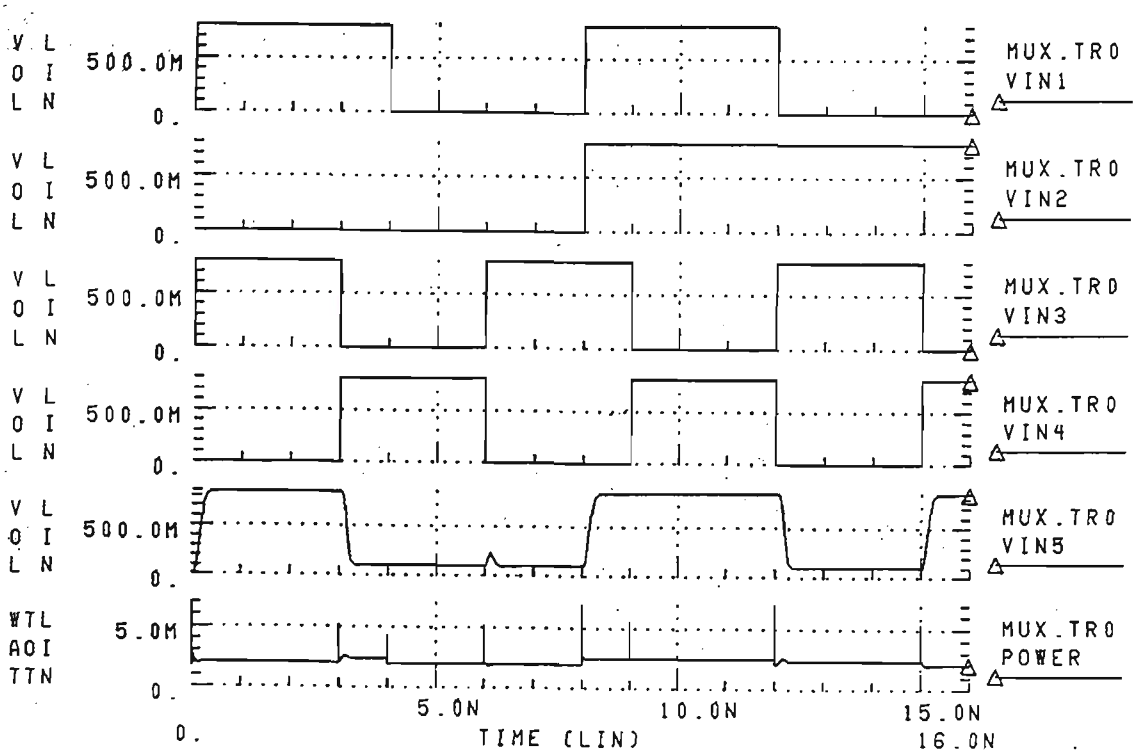


Figure F1.7 HSPICE simulation results for a two-to-one multiplexer. VIN1 and VIN2 represent the inputs J and T, VIN3 and VIN4 represent the true and complementary mux control and VIN5 represents the mux output.

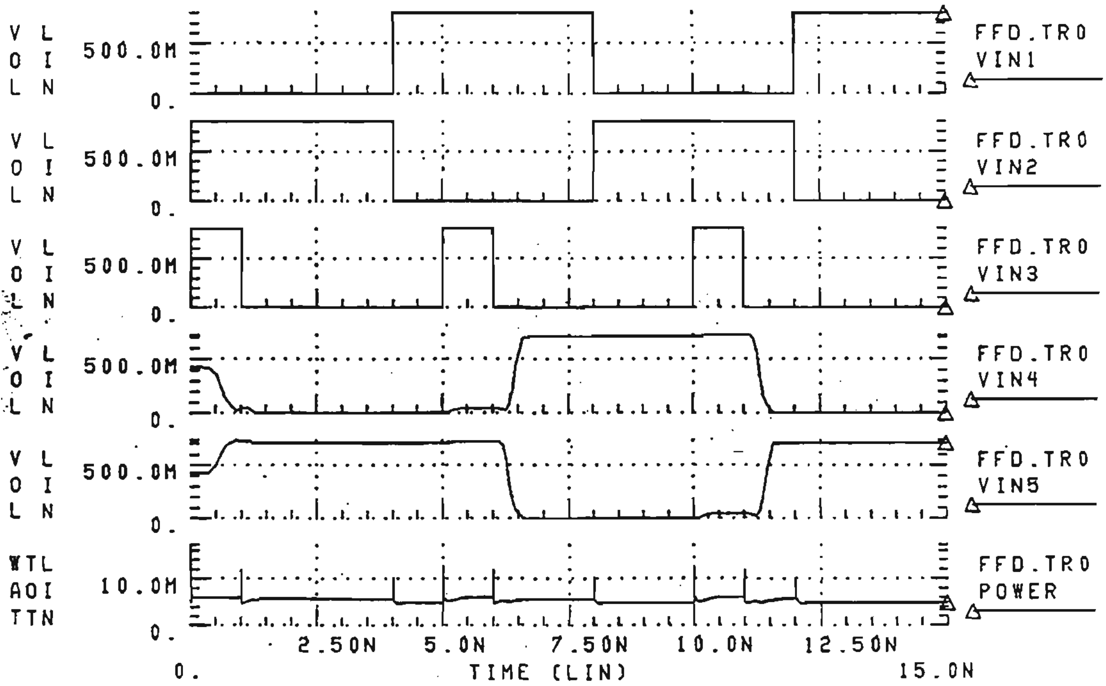


Figure F1.8 HSPICE simulation results for an one-bit register. VIN1 and VIN2 represent the flip flop true and complementary inputs respectively, VIN3 the clock (phi), VIN4 and VIN5 represent the flip flop true and complementary outputs respectively.

Appendix G

Inverse Time-Current Characteristics

An equation for inverse time-current characteristics can be derived from the following basic differential equation for input time delay as it applies to a induction relay [110]:

$$\tau_s(I^n - 1) = K_d \frac{d\theta}{dt} \qquad \textbf{(G1.0)}$$

where τ_s is the spring torque

I is the current in multiple of tap setting

n is an index characterising the algebraic function

K_d is the damping factor due to drag magnet

θ is the angular displacement and

$d\theta/dt$ is the angular velocity.

The small moment of inertia of the disc is neglected and the spring torque is represented by a constant because the effect of its gradient is compensated by an increase in torque caused by the shape of the disc. Integrating equation 1.0 given:

$$\theta = \int_0^{T_0} \frac{\tau_s(I^n - 1)}{K_d} dt \qquad \textbf{(G1.1)}$$

Dividing both sides of the equation G1.1 by θ gives the dynamic equation:

$$\int_0^{\mathrm{To}} \frac{\tau_s(I^n - 1)}{K_d.\theta} dt \;=\; \int_0^{\mathrm{To}} \frac{1}{t(I)} dt \;=\; \mathbf{1} \qquad \mathbf{(G1.2)}$$

Thus the inverse-time characteristic is given as:

$$T = t(I) = \frac{K.t_m}{(I^n - 1)} \qquad \mathbf{(G1.3)}$$

where T is the theoretical operating time of the relay

K is the design constant K_d, and

t_m is the time multiple setting.

Appendix H

Four-Bit Encoder

H1.0 Design Procedure

The encoder translates the outputs of the comparators into a final binary outputs. The inputs to the encoder is fed from the comparators. as shown. The following steps are used to develop the truth table for the encoder [117].

(i) Start with $2^{(n-1)}$ comparators and label them in the ascending order as shown in Figure 8.2. The non-inverting input of all the comparators are connected to the sampled analog input voltage. The inverting input of the comparator Y_0 (MSB comparator) is set to $V_{ref}/2$.

(ii) The output of this comparator, (Y_0), is used to control the switches, which have their outputs connected to the inverting input of the other comparators. The inputs of the switches are connected to the appropriate portions of the reference voltages. The output of the comparators are presented in Figure H1.1 for different values of input voltage, V_{in}.

Input Voltage	**X** 15	**X** 14	**X** 13	**X** 12	**X** 11	**X** 10	**X** 9	**X** 8	**X** 7	**X** 6	**X** 5	**X** 4	**X** 3	**X** 2	**X** 1
$V_{in} < V_{ref}/16$	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
$V_{ref}/16 < V_{in} \leq 2V_{ref}/16$	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
$2V_{ref}/16 < V_{in} \leq 3V_{ref}/16$	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1
$3V_{ref}/16 < V_{in} \leq 4V_{ref}/16$	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1
$4V_{ref}/16 < V_{in} \leq 5V_{ref}/16$	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1
$5V_{ref}/16 < V_{in} \leq 6V_{ref}/16$	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1
$6V_{ref}/16 < V_{in} \leq 7V_{ref}/16$	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1
$7V_{ref}/16 < V_{in} \leq 8V_{ref}/16$	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1
$8V_{ref}/16 < V_{in} \leq 9V_{ref}/16$	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
$9V_{ref}/16 < V_{in} \leq 10V_{ref}/16$	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1
$10V_{ref}/16 < V_{in} \leq 11V_{ref}/16$	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1
$11V_{ref}/16 < V_{in} \leq 12V_{ref}/16$	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1
$12V_{ref}/16 < V_{in} \leq 13V_{ref}/16$	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1
$13V_{ref}/16 < V_{in} \leq 14V_{ref}/16$	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1
$14V_{ref}/16 < V_{in} \leq 15V_{ref}/16$	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1
$V_{in} > 15V_{ref}/16$	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Figure H1.1 Outputs of the comparators for a four-bit flash ADC.

(iii) The output of the comparator is encoded into binary outputs using the truth table of Figure H1.1. The values of Y_is are computed using the following expressions:

$$Y_0 = MSB = X_M \qquad \textbf{(H1.0)}$$

$$Y_1 = X_{M-1}.\overline{X_M} + X_{M+1}.X_M \qquad \textbf{(H1.1)}$$

In general, for I = 1, 2, ...2^{n-1}

$$Y_i = X_{M-i}.\overline{X_M} + X_{M+i}.X_M \qquad \textbf{(H1.2)}$$

where MSB comparator output in a classical flash ADC is X_M and M = 2^{n-1}. Now the Y_is can be encoded to obtain the proper binary digits D, C, B, and A. The encoded outputs are presented in Figure H1.2.

Y_0	Y_1	Y_2	Y_3	Y_4	Y_5	Y_6	Y_7	D	C	B	A
0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	1	0	0	0	1
0	0	0	0	0	0	1	1	0	0	1	0
0	0	0	0	0	1	1	1	0	0	1	1
0	0	0	0	1	1	1	1	0	1	0	0
0	0	0	1	1	1	1	1	0	1	0	1
0	0	1	1	1	1	1	1	0	1	1	0
0	1	1	1	1	1	1	1	0	1	1	1
1	0	0	0	0	0	0	0	1	0	0	0
1	1	0	0	0	0	0	0	1	0	0	1
1	1	1	0	0	0	0	0	1	0	1	0
1	1	1	1	0	0	0	0	1	0	1	1
1	1	1	1	1	0	0	0	1	1	0	0
1	1	1	1	1	1	0	0	1	1	0	1
1	1	1	1	1	1	1	0	1	1	1	0
1	1	1	1	1	1	1	1	1	1	1	1

Figure H1.2 Relationship between comparator and encoder outputs for the proposed four-bit flash ADC.

The Karnough map method is an effective way to simplify switching functions which have a small number of variables. When the number of input variables is large, as is in this case, or if several functions must be simplified, karnough map method becomes very tedious and alternate approach to simplification of boolean functions is needed. The Quine-McCluskey method [112] is one such approach that provides a systematic simplification procedure for boolean functions with large number of input variables.

H1.1 The Quine-McClusky Method

The Quine-McClusky procedure reduces the minterm expansion (standard sum-of-products form) of a function to obtain a minimum sum of products. The procedure consists of two main steps:

(i) Eliminate as many literals as possible from each term by systematically applying the theorem $X.Y + X.\overline{Y} = X$. The resulting terms are called prime implicants.

(ii) Use the prime implicant chart to select a minimum set of prime implicants which, when ORed together, are equal to the function being simplified and which contain a minimum number of literals.

The objective of obtaining the set of prime implicants is achieved through the following steps:

(i) Express the function in expanded sum-of-products form or as a sum of minterms.

(ii) Represent each minterm by its minterm number in binary form. Note that variables must be ordered in accordance with weighting.

(iii) Make a table of terms, ordering them according to index (index is equal to the number of one's in the binary representation, eg. 0100, 0001, are of index 1, 1001, 0110, are of index 2, etc.).

(iv) By making groups, where ever possible across boundaries between terms which differ by 1 in index, form a second table of grouped terms ordered again by index and replacing grouped variables by a dash (-), (ie. where a zero and a 1 have been grouped). Terms will group when they differ in only one literal, eg. 001 will group with 101 to form -01, 100 groups with 110 to give 1-0, etc.

(v) Tick all terms which have to be grouped. Unticked terms must appear in the final prime implicant (PI) set.

(vi) Repeat the grouping exercise across the index boundaries with the constraint that dashes must also line up for grouping to be possible.

(vii) Continue the grouping procedure, forming subsequent tables until no further grouping is possible.

(viii) The terms in the final table together with all unticked terms in all previous tables constitute the PI set.

Having obtained the PI set the second objective of the procedure, namely choosing the optimum set of PI's is then achieved. One way of so doing is to use a PI chart. The Quine-McClusky procedure is illustrated by way of an example below.

H1.1.1 Example

Use the Quine-McClusky procedure to find the simplest realisation of the function T where:

$$T = \overline{X}.\overline{Y}.\overline{Z} + \overline{X}.Z + X.Y \qquad \textbf{(H1.3)}$$

The process is as follows:

(i) Express T in expanded SOP and binary forms:

$$T = \overline{X}.\overline{Y}.\overline{Z} + \overline{X}.\overline{Y}.Z + \overline{X}.Y.Z + X.Y.\overline{Z} + X.Y.Z \qquad \textbf{(H1.4)}$$

$$= \mathbf{000 \quad + \ 001 \quad + \ 011 \ + \ 110 \ + \ 111}$$

$$= \mathbf{\Sigma m(0, 1, 3, 6, 7)}$$

(ii) Set out tables (Table H1.1 and H1.2) according to index and carry out the grouping process.

Table H1.1 Quine-McClusky grouping process - first iteration

Index	**m**	**Terms**	
Zero	0	√	000
One	1	√	001
Two	3	√	011
	6	√	110
Three	7	√	111

Table H1.2 Quine-McClusky grouping process - second iteration

Index	**m**	**Terms**	
Zero	0,1	A	00-
One	1,3	B	0-1
Two	3,7	C	-11
	6,7	D	11-

No grouping is possible in table h1.2 because dashes do not line up across any boundary. Therefore identify all unticked terms A, B, C, and D to form PI set. The PI set for this example is thus:

$$T = A + B + C + D \qquad \textbf{(H1.5)}$$

(iii) The PI chart is set out as shown in Figure H1.3.

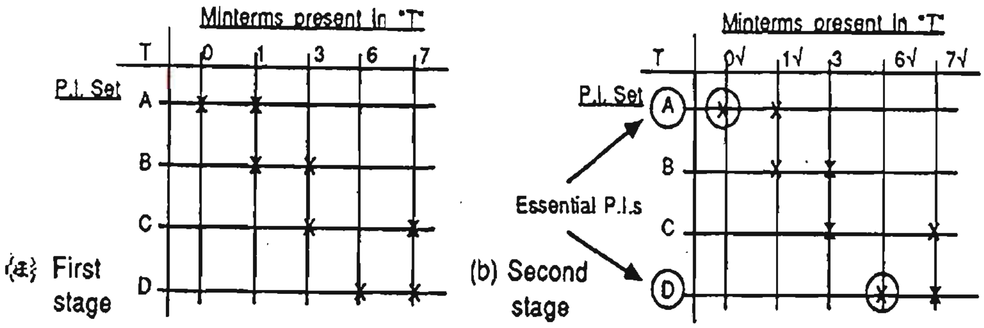


Figure H1.3 PI chart.

(iv) Circled PIs are the essential PIs since they cover minterms which are not covered by any other PI. The essential PIs must be present in any solution for T.

(v) Choose PIs as economically as possible to cover the remaining minterms. (In this case either PI B or C will do equally well since they are equal size groups).

(vi) Final solution as a set of PIs and algebraic form are:

$$T = A + D + B \text{ or } C \qquad \textbf{(H1.6)}$$

$$= \mathbf{00\text{-} + 11\text{-} + 0\text{-}1}$$

$$= \overline{X}.\overline{Y} + X.Y + \overline{X}.Z \qquad \textbf{(H1.7)}$$

The expressions for the four outputs (D, C, B, and A) were simplified using the Quine-McClusky procedure and are expressed in terms of the comparator outputs as follows:

$$D = Y_0 \qquad \textbf{(H1.8)}$$

$$C = Y_4 \qquad \textbf{(H1.9)}$$

$$B = (Y_2 + Y_6).(Y_2 + \overline{Y_4}).(\overline{Y_4} + Y_6) \qquad \textbf{(H1.10)}$$

$$A = (Y_5 + \overline{Y_6}).(Y_3 + \overline{Y_4}).(Y_1 + \overline{Y_2}).(\overline{Y_2} + Y_3).(\overline{Y_4} + Y_5).$$
$$(\overline{Y_6} + Y_7).(Y_1 + Y_7) \qquad \textbf{(H1.11)}$$

where $Y_{0,}$ .... Y_7 are the outputs of the eight comparators.

The OR/NOR based logical representation of the four-bit encoder is shown in Figure 8.4. Due to degradation of performance, the encoder circuit is limited to parallel branches in the input, ie., OR/NOR structure only. GaAs Merged logic design technique has been used to design the OR/NOR gates for the encoder.

Appendix I

Eight-bit Comparator

I1.0 Design Procedure

This section describes the design of a cascadable comparator cell using Merged GaAs MESFET logic. An eight-bit comparator was designed using cellular structure of cells. The general arrangement and the truth table for a binary one-bit comparator bit-slice is shown in Figure I1.1(a) and (b), where A_i and B_i are the two multi-bit numbers to be compared, C_{i+1} is the input from the output of the previous stage, and C_i is the output of the current stage. The behaviour of the cell is described as follows:

$\mathbf{C_i = 1}$ for $\mathbf{A_i > B_i}$, and

$\mathbf{C_i = 0}$ for $\mathbf{A_i = B_i}$ and/or $\mathbf{A_i < B_i}$.

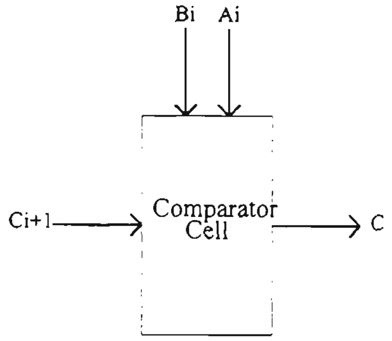


Figure I1.1(a) Bit-slice comparator cell.

C_{i+1}	A_i	B_i	C_i
0	0	0	1
0	0	1	1
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	0

Figure I1.1(b) Comparator cell truth table.

The output, C_i, in terms of the inputs are plotted on the karnough map as shown in Figure I1.2.

A_iB i C_{i+1}	00	01	11	10
0	1	1	1	0
1	0	0	0	0

Figure I1.2 Karnough for C_i.

The minimised logical expression for C$_i$ can be expressed as:

$$\overline{C_i} = C_{i+1} + A_i.\overline{B_i} \qquad \textbf{(I1.0)}$$

$$C_i = \overline{(C_{i+1} + A_i.\overline{B_i})}$$

$$C_i = \overline{C_{i+1}}.(\overline{A_i} + B_i)$$

$$C_i = \overline{C_{i+1} + \overline{(\overline{A_i} + B_i)}} \qquad \textbf{(I1.1)}$$

Expression for C$_i$ described by equation I1.1 can be implemented using NOR gates. The logical implementation of a single bit comparator cell is shown in Figure I1.3.

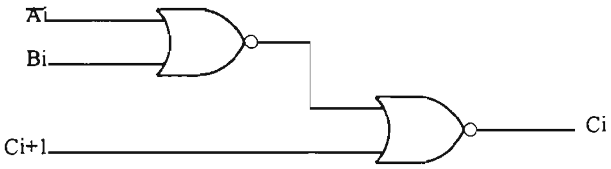


Figure I1.3 Logical representation of a comparator cell.

Appendix J

Design and Performance of a Four-Bit Time-Out Timer Using J-K Flip Flops

J1.0 Timer Design Procedure

The procedure used to design a four-bit time out timer is summarised as follows:

(i) Derive a state table from state graph or problem statement.

(ii) Plot the next state maps from the state table.

(iii) Plot the J-K input map for each flip flop.

(iv) Derive the J-K input expressions for each flip flop.

(v) Realise the circuit using J-K flip flops and additional logic.

Table J1.1(a) describes the next state output for a J-K flip flop as a function of the synchronous inputs and present state output. Using this, the required input conditions for J and K when Q and Q_{n+1} are given are derived. Thus if a change from Q = 0 to Q_{n+1} = 1 is required, either the flip flop can be set to 1 by using J = 1 and K = 0 or the state can be changed by using $J = K = 1$. In other words J must be 1, but K is a don't care. The J K input requirements are summarised in Table J1.1 (b).

Table J1.1 J K flip flop next state outputs

J	K	Q_n	Q_{n+1}
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

(a)

Q	Q_{n+1}	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

(b)

The state table for a four-bit time out timer is shown in Table J1.2 with columns added for the J and K flip flop inputs. The input columns are completed using the results in Table J1.1(b).

Table J1.2 State table and input controls for a four-bit timer

D	C	B	A	D^+	C^+	B^+	A^+	J_D	K_D	J_C	K_C	J_B	K_B	J_A	K_A
1	1	1	1	1	1	1	0	X	0	X	0	X	0	X	1
1	1	1	0	1	1	0	1	X	0	X	0	X	1	1	X
1	1	0	1	1	1	0	0	X	0	X	0	0	X	X	1
1	1	0	0	1	0	1	1	X	0	X	1	1	X	1	X
1	0	1	1	1	0	1	0	X	0	0	X	X	0	X	1
1	0	1	0	1	0	0	1	X	0	0	X	X	1	1	X
1	0	0	1	1	0	0	0	X	0	0	X	0	X	X	1
1	0	0	0	0	1	1	1	X	1	1	X	1	X	1	X
0	1	1	1	0	1	1	0	0	X	X	0	X	0	X	1
0	1	1	0	0	1	0	1	0	X	X	0	X	1	1	X
0	1	0	1	0	1	0	0	0	X	X	0	0	X	X	1
0	1	0	0	0	0	1	1	0	X	X	1	1	X	1	X
0	0	1	1	0	0	1	0	0	X	0	X	X	0	X	1
0	0	1	0	0	0	0	1	0	X	0	X	X	1	1	X
0	0	0	1	0	0	0	0	0	X	0	X	0	X	X	1
0	0	0	0	1	1	1	1	1	X	1	X	1	X	1	X

DCBA and $D^+C^+B^+A^+$ are the outputs of the timer immediately before and after the clock transition.

The J K maps of Figure J1.1 are obtained directly from Table J1.2. The J and K input expressions for each flip flop are derived using karnough maps of Figure J1.1.

BA DC	00	01	11	10
00	1	0	0	0
01	0	0	0	0
11	X	X	X	X
10	X	X	X	X

$$J_D = \overline{C}.\overline{B}.\overline{A}$$

BA DC	00	01	11	10
00	X	X	X	X
01	X	X	X	X
11	0	0	0	0
10	1	0	0	0

$$K_D = \overline{C}.\overline{B}.\overline{A}$$

BA	00	01	11	10
DC				
00	1	X	X	X
01	X	X	X	X
11	X	X	X	X
10	1	0	0	0

$$J_C = \overline{B}.\overline{A}$$

BA	00	01	11	10
DC				
00	X	X	X	X
01	1	0	0	0
11	1	0	0	0
10	X	X	X	X

$$K_C = \overline{B}.\overline{A}$$

BA	00	01	11	10
DC				
00	1	0	X	X
01	1	0	X	X
11	1	0	X	X
10	1	0	X	X

$$J_B = \overline{A}$$

BA	00	01	11	10
DC				
00	X	X	0	1
01	X	X	0	1
11	X	X	0	1
10	X	X	0	1

$$K_B = \overline{A}$$

BA	00	01	11	10
DC				
00	1	X	X	1
01	1	X	X	1
11	1	X	X	1
10	1	X	X	1

$$J_B = 1$$

BA	00	01	11	10
DC				
00	X	1	1	X
01	X	1	1	X
11	X	1	1	X
10	X	1	1	X

$$K_B = 1$$

Figure J1.1 Flip flop input maps.

The expressions for the inputs can be transformed into GaAs technology implementable form by using De Morgans theorems. The transformed expressions for the J K flip flop inputs are expressed as:

$$J_D = K_D = \overline{(C + B + A)} \qquad \textbf{(J1.0)}$$

$$J_C = K_C = \overline{(B + A)} \qquad \textbf{(J1.1)}$$

$$J_B = K_B = \overline{A} \qquad \textbf{(J1.2)}$$

$$J_A = K_A = 1 \qquad \textbf{(J1.3)}$$

The four-bit time out timer is implemented using J K flip flops and NOR based logic for the input controls. The clock input of the flip flops are connected together to give a synchronous operation. The logical circuit of an one-bit time out timer is shown in Figure 9.13.

Parallel load is facilitated by enabling a synchronous load signal which causes the parallel input data to be transferred to the output on the next clock pulse. The timer also has asynchronous preset and clear functions.

J2.0 Timer Performance

The performance of a one, two and three-bit time-out timer is shown in Figures J1.2 - J1.4.

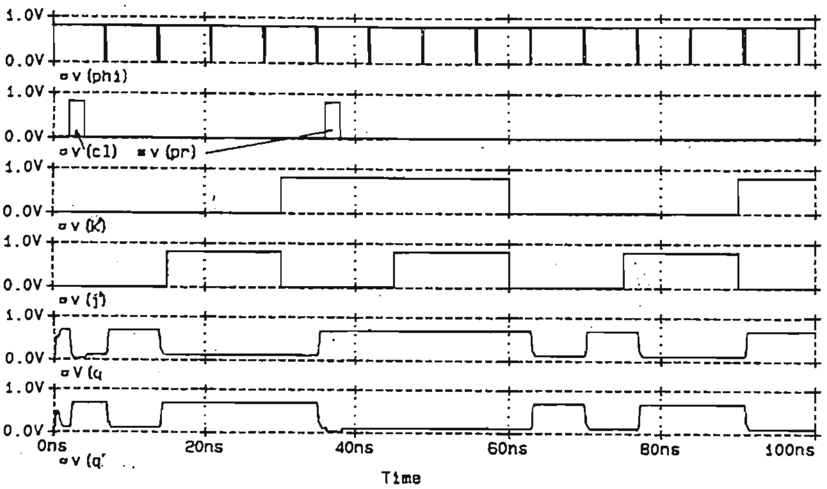


Figure J1.2 Performance of an one-bit timer.

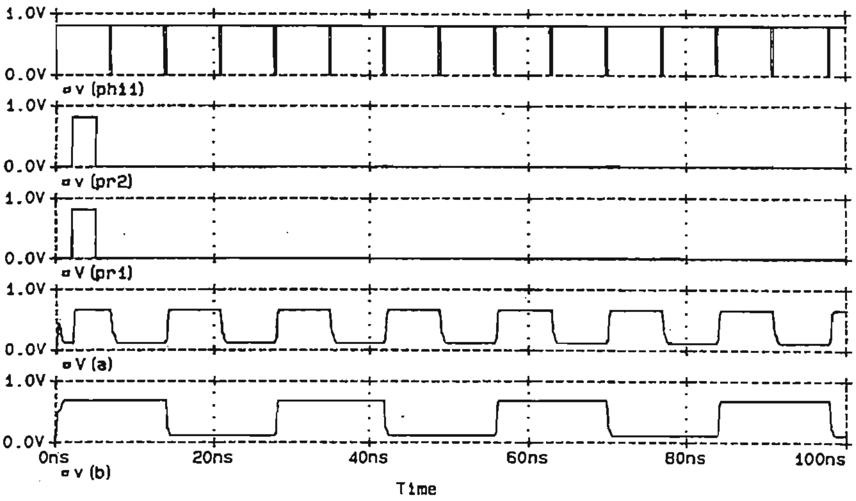


Figure J1.3 Performance of a two-bit timer.

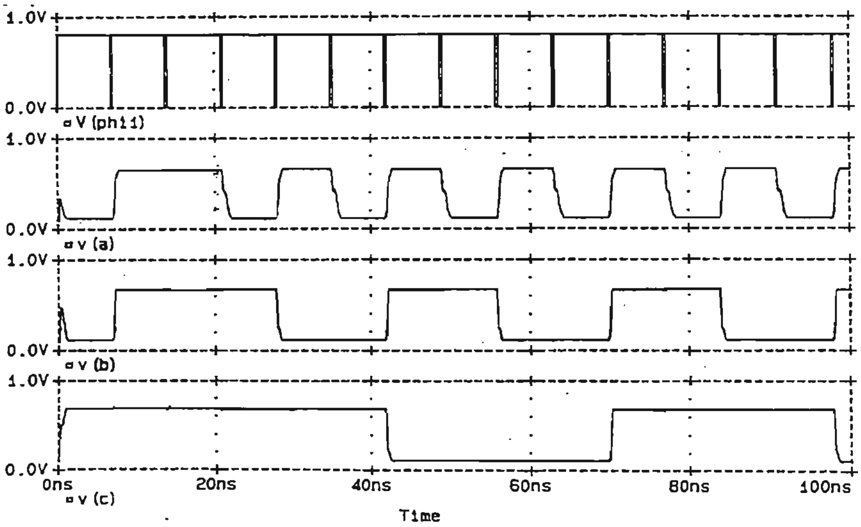


Figure J1.4 Performance of a three-bit timer.