cadence

Implementing Force Sense Connection

Product Version SPB16.6
October 15, 2013

Contents

Purpose

The use of separate Force (F) and Sense (S) connections (often referred to as a Kelvin connection) is quite a common requirement in the PCB design. These separate Force (F) and Sense (S) connections at the load removes any errors resulting from voltage drops in the force lead. Routing the Kelvin sense lines by separating lines for sensing signals (S) from lines delivering power to loads (F) prevents noise related problems in a closed loop system as it allows for more accurate measurement of the sense voltage.

The requirement is to implement this at the schematic to drive the PCB board so that both Force and Sense signals can be identified and constrained independently and still allowed to be physically shorted in layout.

Before you begin, download the Database from Cadence Online Support.
Click Here to Download.

Audience

Electrical Engineers and PCB Designers using Cadence Allegro tool set and implementing Kelvin connection using Force (F) and Sense (S) signals.

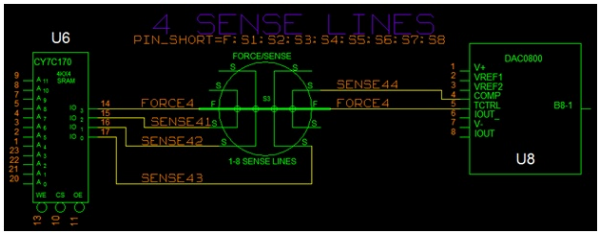
Flow Overview

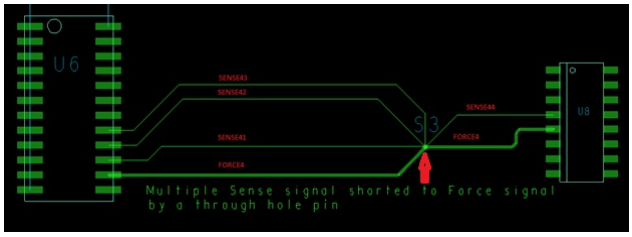
This flow is based on a special logical symbol, which is created and saved in a library.

The force sense library symbol(s) has shorting schemes defined within the symbol definition which allows the engineer to seamless define the nets to be force sense.

When placed in a schematic, will short at least two sense lines to a force line. During packaging, separate nets are generated and flow to the PCB. As shown in the image four sense lines are connected to a force line using the library symbol.

Inside PCB Editor, a Symbol gets placed, and defines the location of the short for force and sense signals.





To use this flow create a schematic symbol and footprint symbol as shown below.

DE HDL library requirements to define Force Sense symbols

Use the **PIN_SHORT** property on the logical symbol. The PIN_SHORT property uses the logical pin name list in the value. At the time of packaging, based on CPM directive (see page 10), the packager acknowledges the PIN_SHORT property value and creates NET_SHORT property with value containing the physical net names connected to the logical pin names.

This can be validated by reviewing the “pstxnet.dat” file for “NET_SHORT” property on the pin as shown in the example. This file is located in the “projectname/worklib/test/package” directory.

NET_NAME

'FORCE2'

'@TEST_LIB.TEST(SCH_1):FORCE2':

C_SIGNAL='@test_lib.test(sch_1):force2';

NODE_NAME S2 1

'@TEST_LIB.TEST(SCH_1):PAGE1_I13@TEST_LIB.FORCE_SENSE(CHIPS)':

'F':NET_SHORT='FORCE2:SENSE21:SENSE22',

CDS_PINID='F';

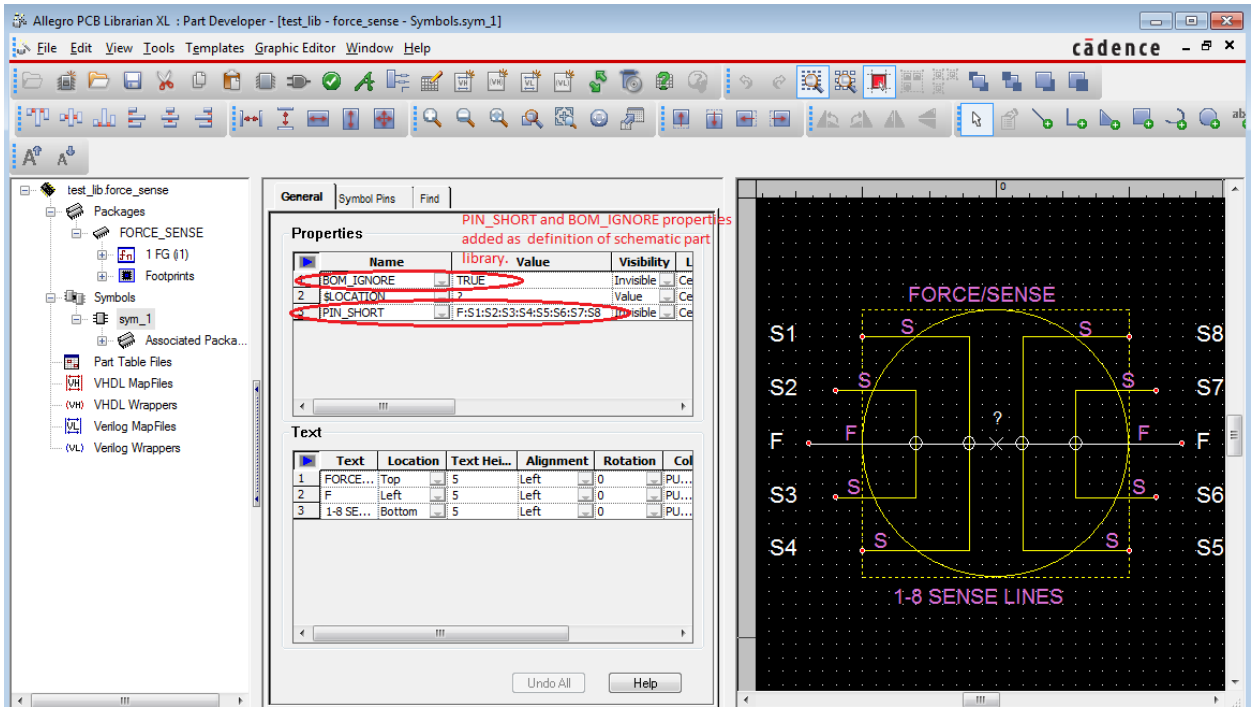
The symbol needs to be ignored from Bill of Material (BOM) utilizing the BOM_IGNORE = TRUE attribute and is associated to a footprint required to make the connection on board.

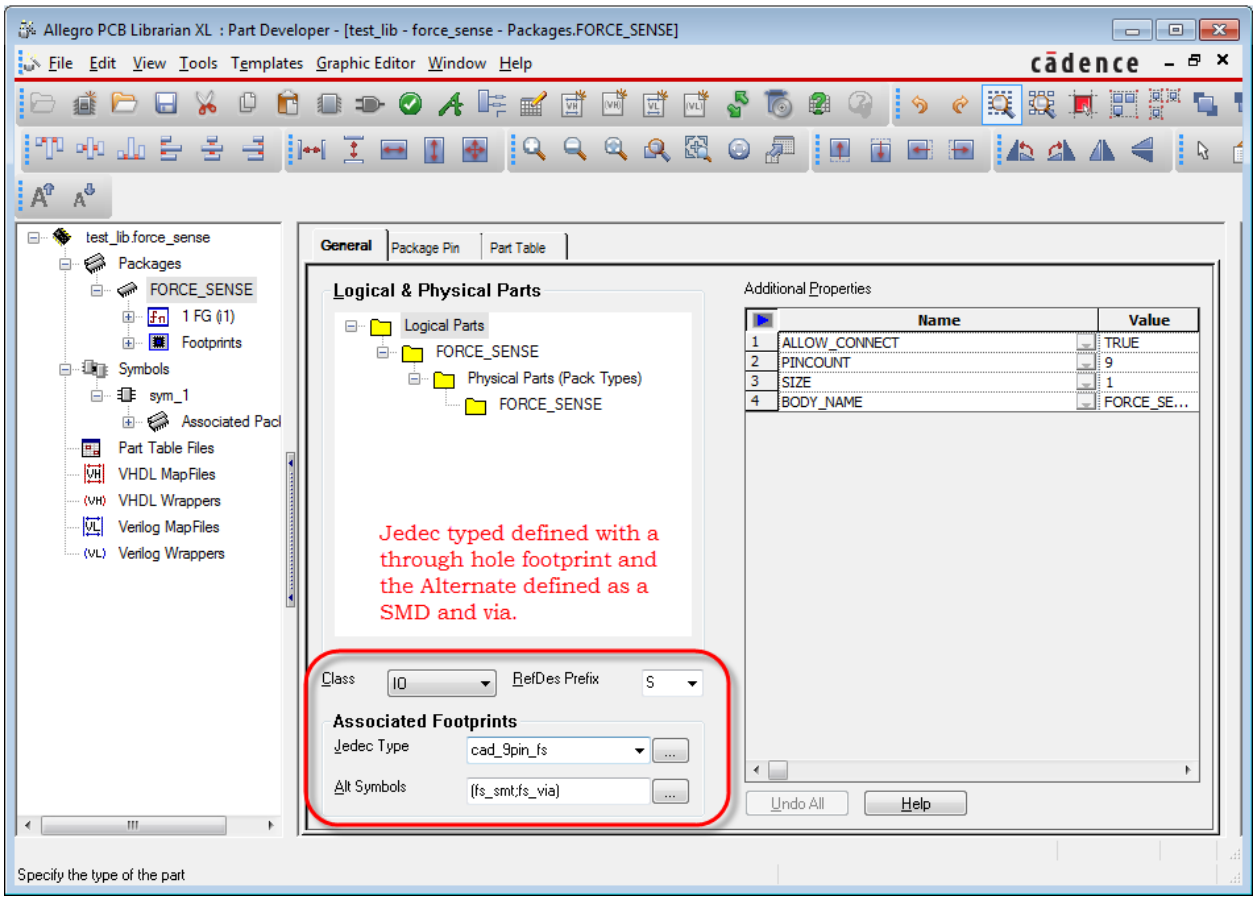
Example Schematic Symbol

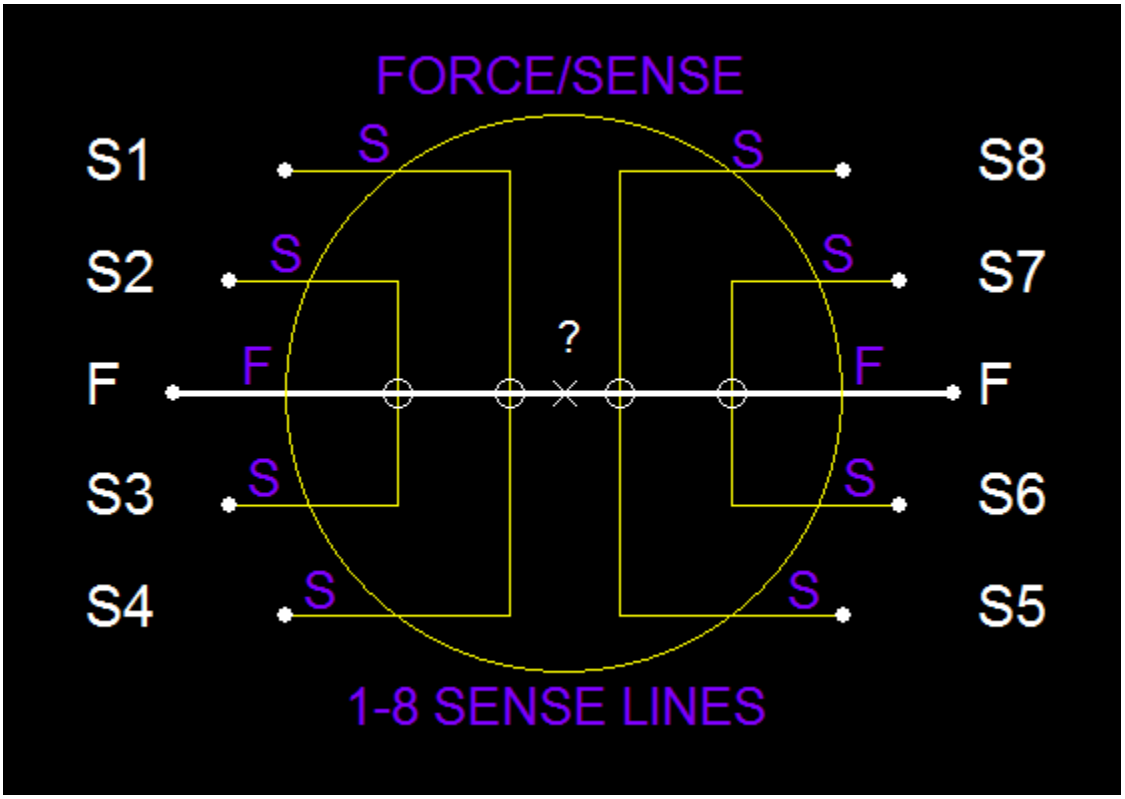
The Force-Sense symbol can connect one force line with one or multiple sense lines. In the example symbol provided, the Force & Sense symbol has been built to accommodate from 1 to 8 sense lines. PIN “F” is defined as pass-thru pin, so the total numbers of pins on the symbol are 9.

PIN_SHORT should be defined on symbol as–

PIN_SHORT=F:S1:S2:S3:S4:S5:S6:S7:S8


Allegro PCB Librarian XL : Part Developer - [test_lib - force_sense - Symbols.sym_1]
File Edit View Tools Templates Graphic Editor Window Help
cadence
test_lib.force_sense
Packages
FORCE_SENSE
1 FG (1)
Footprints
Symbols
sym_1
Associated Packa...
Part Table Files
VHDL MapFiles
VHDL Wrappers
Verilog MapFiles
Verilog Wrappers
General
Symbol Pins
Find
PIN_SHORT and BOM_IGNORE properties added as definition of schematic part library.
Properties
Name
Value
Visibility
BOM_IGNORE
TRUE
Invisible
$LOCATION
Value
PIN_SHORT
F:S1:S2:S3:S4:S5:S6:S7:S8
Invisible
Text
Text
Location
Text Hei...
Alignment
Rotation
FORCE...
Top
Left
1-8 SE...
Bottom
Undo All
Help
FORCE/SENSE
S1
S2
F
S3
S4
S8
S7
F
S6
S5
1-8 SENSE LINES


Allegro PCB Librarian XL : Part Developer - [test_lib - force_sense - Packages.FORCE_SENSE]
File Edit View Tools Templates Graphic Editor Window Help
cadence
test_lib.force_sense
Packages
FORCE_SENSE
1 FG (1)
Footprints
Symbols
sym_1
Associated Pacl
Part Table Files
VHDL MapFiles
VHDL Wrappers
Verilog MapFiles
Verilog Wrappers
General
Package Pin
Part Table
Logical & Physical Parts
Logical Parts
FORCE_SENSE
Physical Parts (Pack Types)
FORCE_SENSE
Jedec typed defined with a through hole footprint and the Alternate defined as a SMD and via.
Additional Properties
Name
Value
ALLOW_CONNECT
TRUE
PINCOUNT
9
SIZE
1
BODY_NAME
FORCE_SE...
Class
IO
RefDes Prefix
S
Associated Footprints
Jedec Type
cad_9pin_fs
Alt Symbols
(fs_smt;fs_via)
Undo All
Help
Specify the type of the part



Footprint Library

There are multiple ways to short the signals on the board. The most common methods are-

1. Shorting the signals on different layer or on same layer of board. This can be achieved by defining the footprint with Pin 1 defined as a through hole pin/pad combination, and a specified drill diameter. The remaining pins would be defined using a smaller diameter pad and a drill of zero. These would be positioned exactly on top of pin 1. Connections using this part could occur on any layer of the PCB. In the sample database a footprint “cad_9pin_fs” is defined for this.

2. Shorting the signals on a single layer, without a through hole part, can be achieved with a SMD pad. This can be achieved by defining the footprint with just the SMD pads for all the pins in the symbol. In the sample database a footprint “fs_smt” is defined for this. This could also be defined as an alternate symbol for the above defined footprint.

NOTE: If using an SMD pad is required on internal layers, the database needs to be set up with Embedded Layers. Setup>Embedded Layer Setup can be accessed to accomplish this. This would require a Miniaturization Option license.

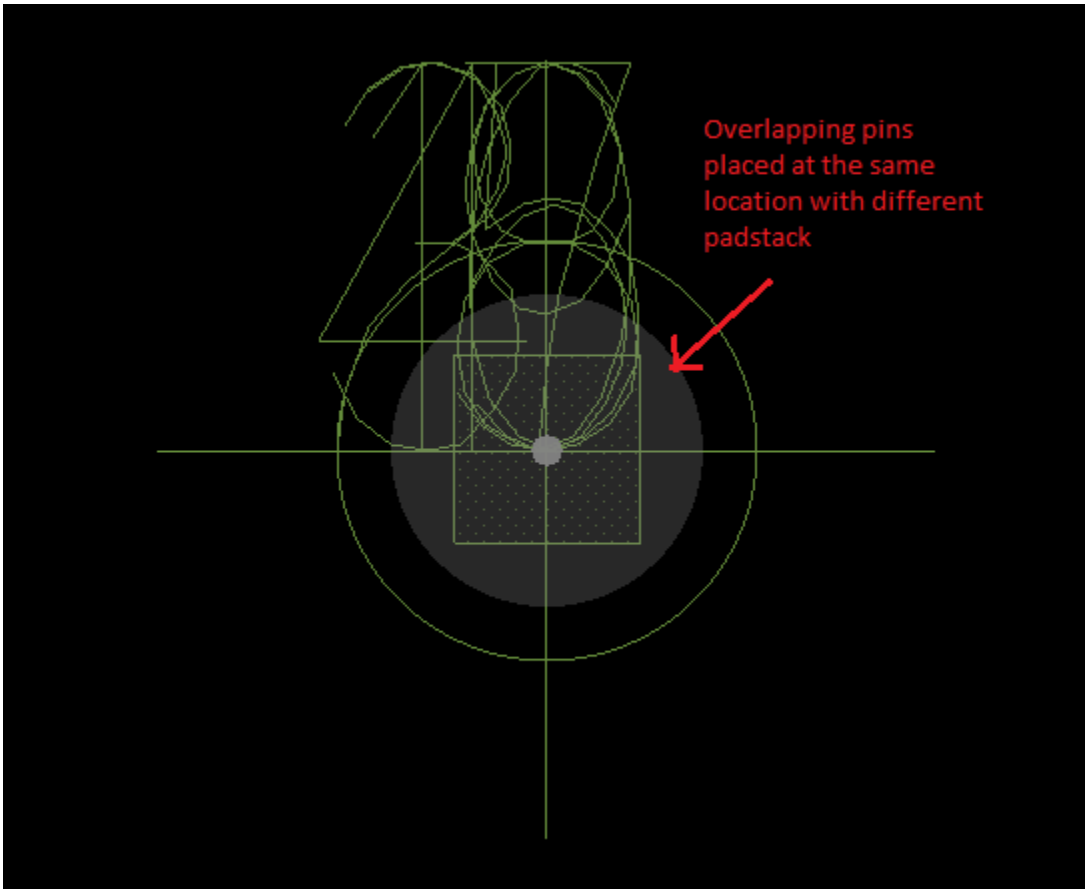
Example Footprint

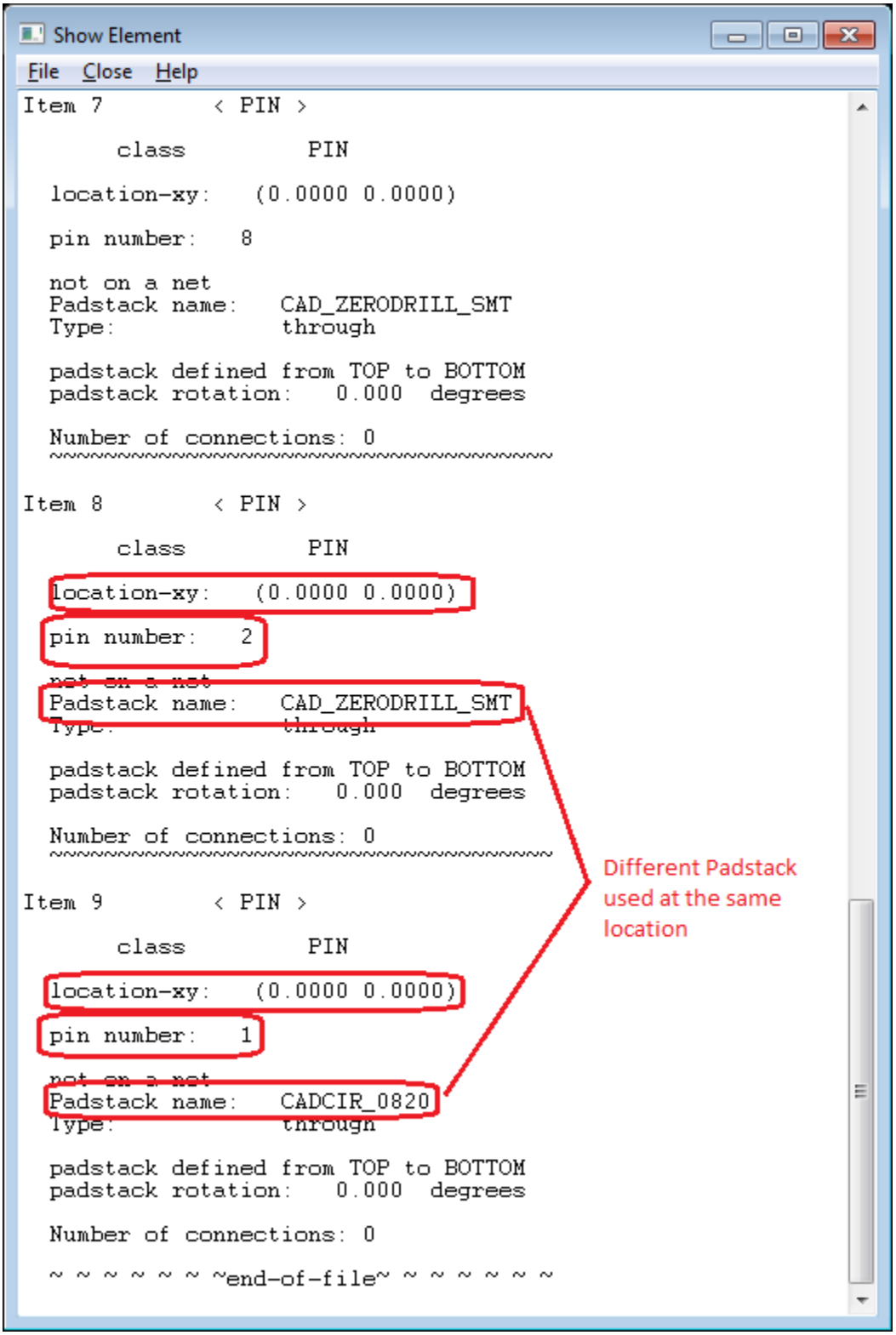
The above symbol for Force-Sense with eight sense and a force pin should be associated with a footprint with nine pins at the same location. The pins are defined with the padstack -

Pin 1: 20 mil pad and 8 mil drill hole

Pins 2 - 9: 2 mil pad and 0 mil drill hole

cad_9pin_fs.dra symbol image and pin definition.




Show Element
File Close Help
Item 7 < PIN >
class PIN
location-xy: (0.0000 0.0000)
pin number: 8
not on a net
Padstack name: CAD_ZERODRILL_SMT
Type: through
padstack defined from TOP to BOTTOM
padstack rotation: 0.000 degrees
Number of connections: 0
Item 8 < PIN >
class PIN
location-xy: (0.0000 0.0000)
pin number: 2
Padstack name: CAD_ZERODRILL_SMT
padstack defined from TOP to BOTTOM
padstack rotation: 0.000 degrees
Number of connections: 0
Item 9 < PIN >
class PIN
location-xy: (0.0000 0.0000)
pin number: 1
Padstack name: CADCIR_0820
Type: through
padstack defined from TOP to BOTTOM
padstack rotation: 0.000 degrees
Number of connections: 0
~ ~ ~ ~ ~ ~ ~end-of-file~ ~ ~ ~ ~ ~ ~
Different Padstack used at the same location

Front to Back Flow Environment Requirement

To transfer the NET_SHORT property to the netlist, and to board file based on the PIN_SHORT defined on the logical symbol, define the following in the project cpm file or in the site.cpm file in the packager section (“PKGXL”) as.

START_PKGXL

…

PROCESS_PIN_SHORT_PROP 'ON'

…

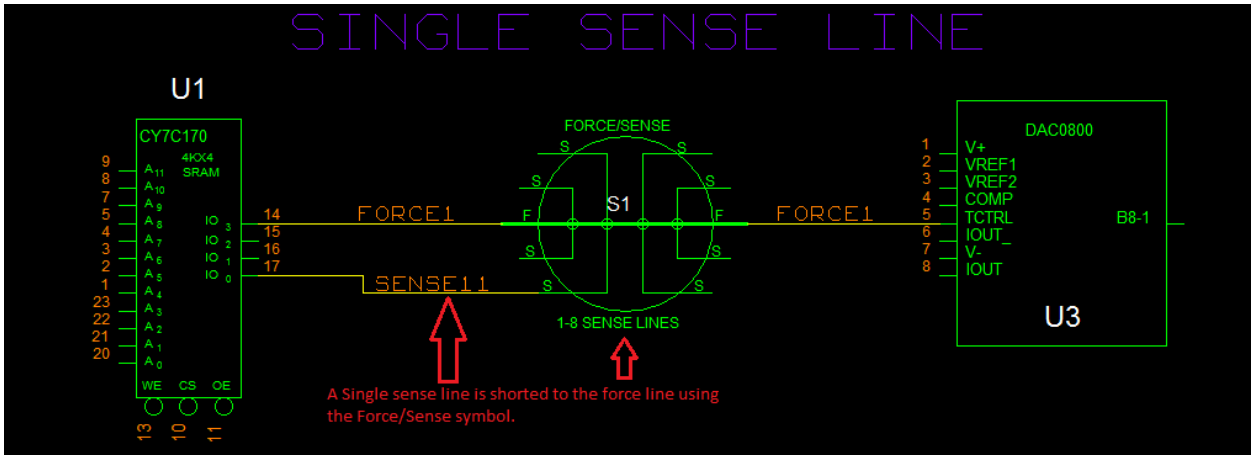
END_PKGXL

Schematic Capture

Once the logical symbol is defined, then the logical schematic can be created in Allegro Design Entry HDL (DE HDL).

Example Schematic

In this case one Force signal is shorted to one sense line using the Force/Sense symbol from the library.

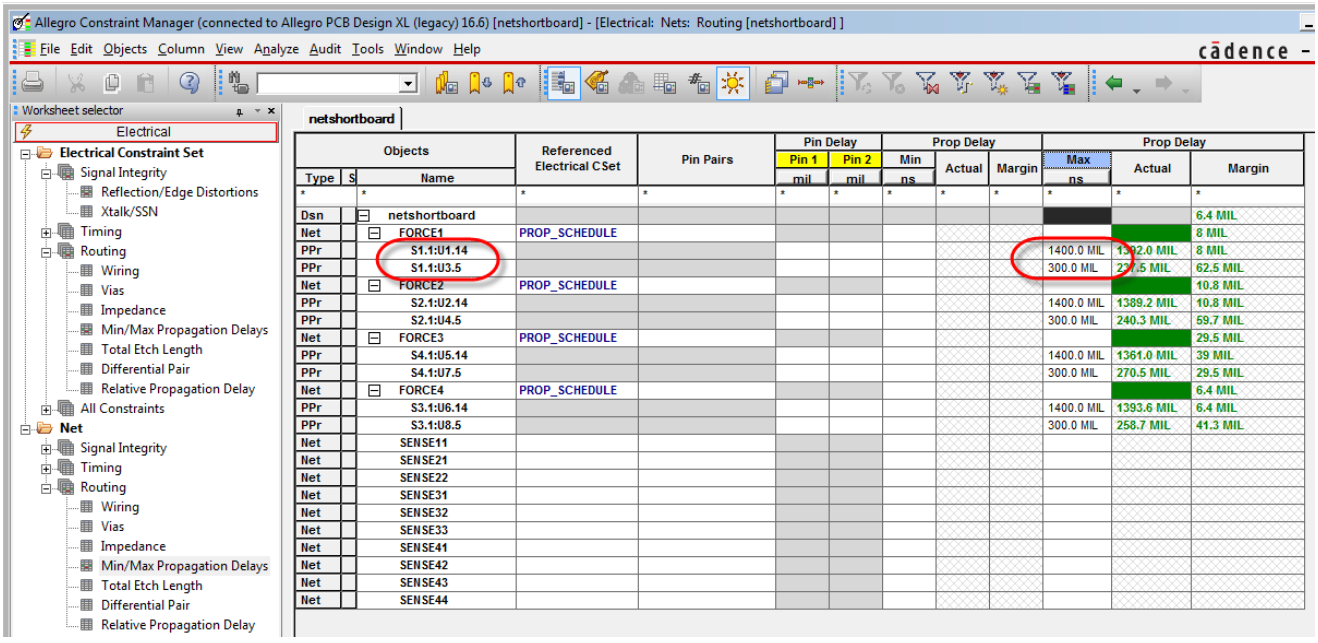


Constraint Assignment

The use of this flow, allows for individual net constraints to be assigned and used in the front to back flow. As an example, Net Schedule, Max Propagation Delay and trace width can be defined.

Max Propagation Delay

Pin Pairs can be created, then used to control location of short on FORCE.



Primary Width

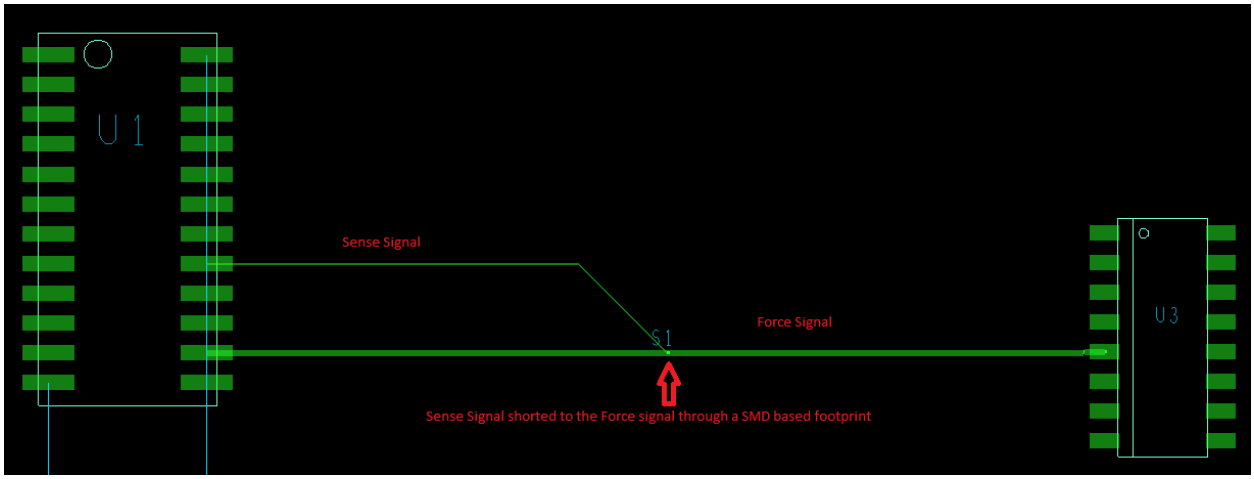
To control the width for FORCE and SENSE signals separately.

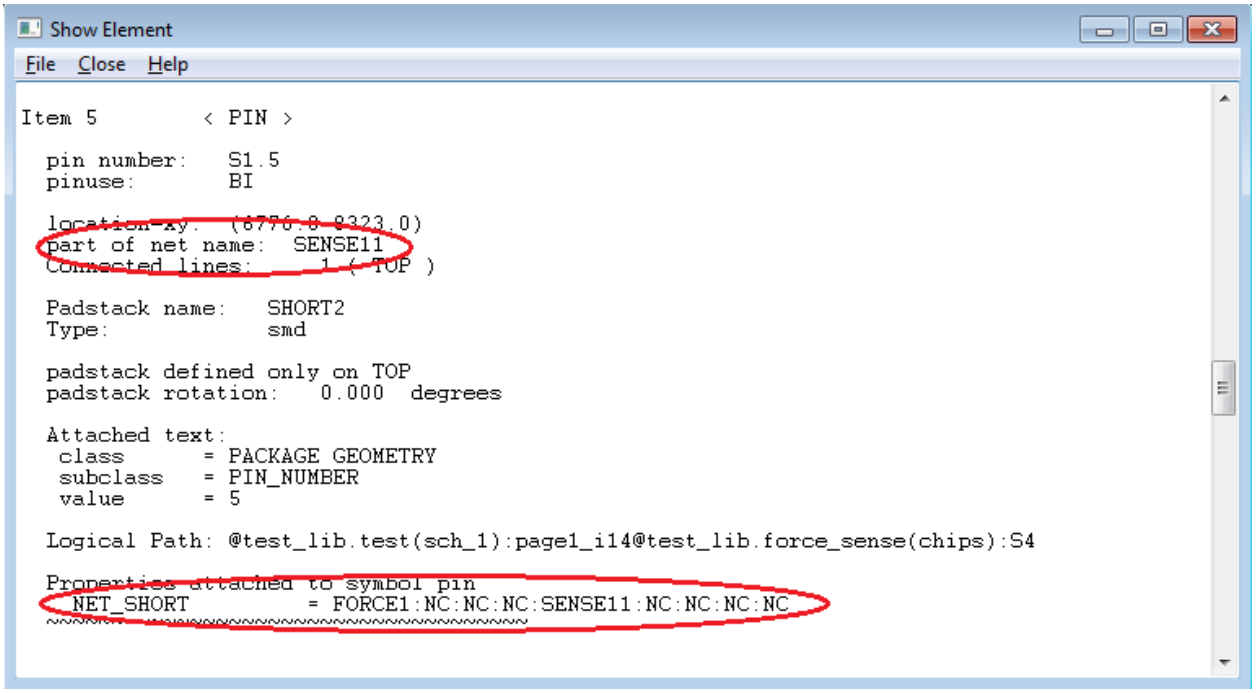
Type	Objects	c Phase		Min Line Spacing		
		Actual	Margin		Primary Gap	Primary Width
				mil	mil	mil
*	*	*	*	*	*	*
Dsn	test					
Net	FORCE1					12.0000
Net	FORCE2					12.0000
Net	FORCE3					12.0000
Net	FORCE4					12.0000
Net	FORCE5					12.0000
Net	SENSE11					
Net	SENSE21					
Net	SENSE22					

Also different constraints like line impedance, relative propagation can be used to meet the specific requirements.

Board Layout

Once the logic information is imported in the board, the NET_SHORT information is transferred to the pins of the footprint to which Force/Sense symbols is associated.





When interactively routing the F & S nets, it is best if you start from the Sense Pin and work from there, completing each net before moving to the next. There is an issue currently, where if you do not complete the interconnect and leave a dangling stub, when you select the next net to route, your stub gets truncated back into the Sense Pin.

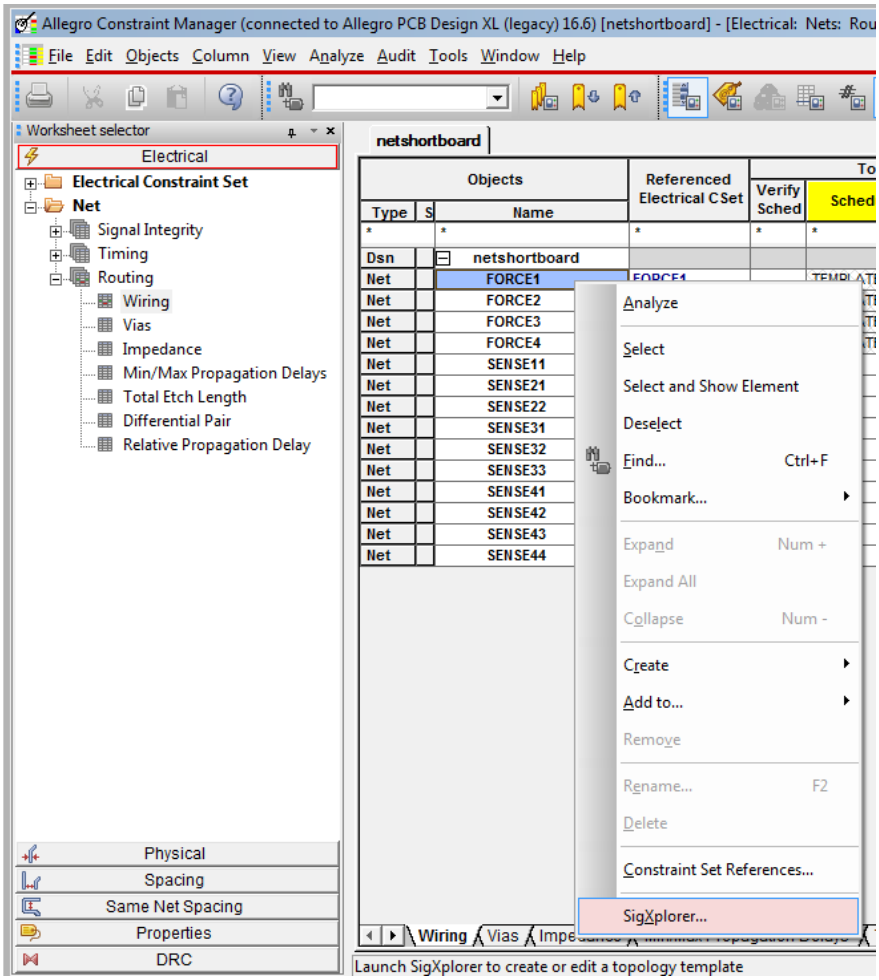
Once routed no DRC is generated for the short because of the NET_SHORT defined on the pin.

Allegro PCB Router

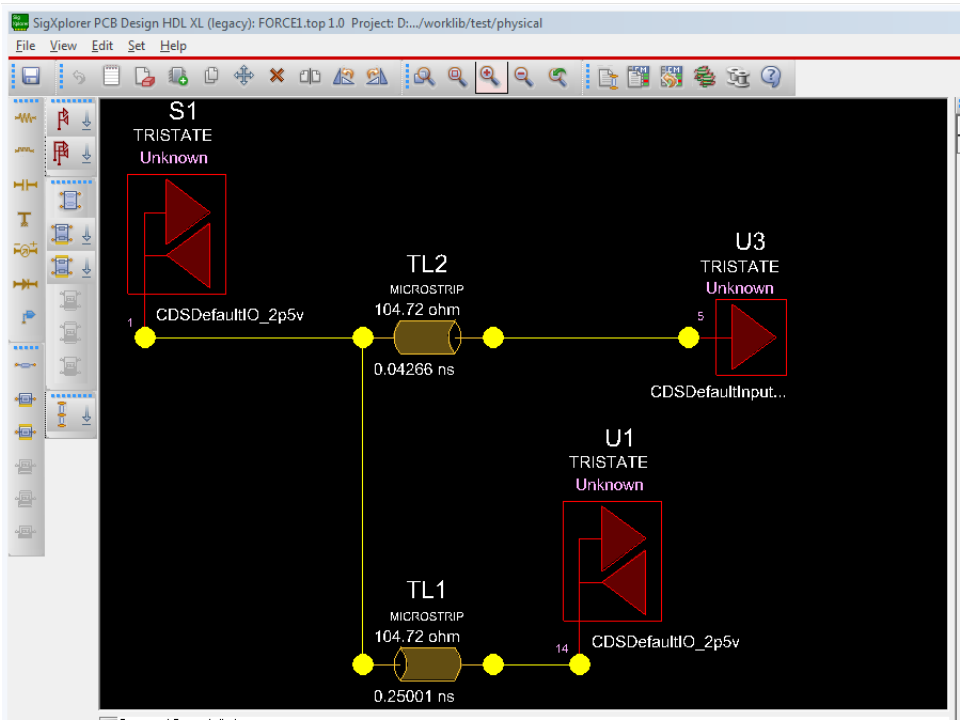
Allegro PCB Router has been enhanced to connect the Sense Pins that have the NET_SHORT property assigned.

Net Schedule

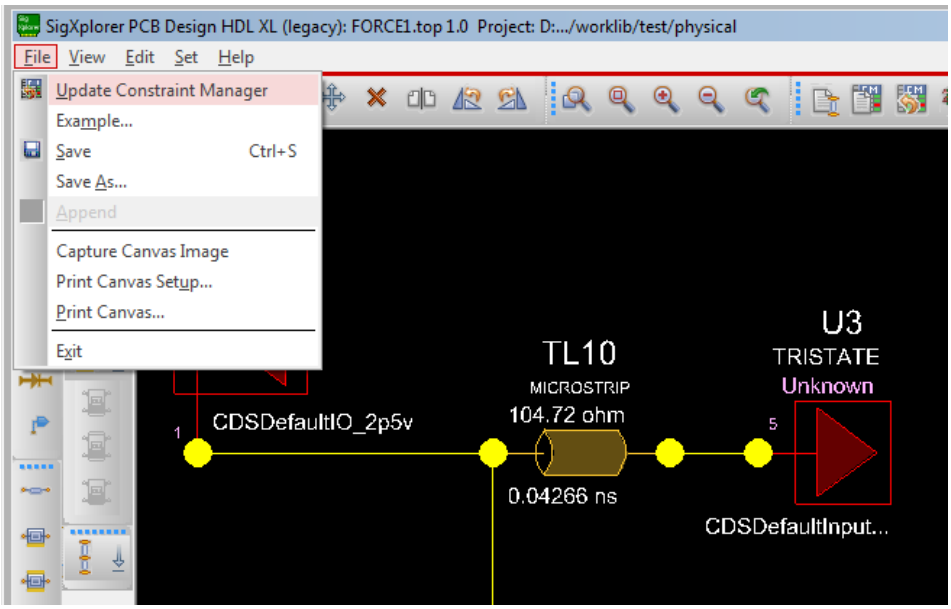
To ensure Allegro PCB Router connects in the expected manner, it is suggested to perform a Net Schedule on the Force net. If there are many such connections within your design, it is suggested to exact the net into SigXp:



Schedule the net on the SigXp canvas:



Then reapply in Allegro using Update Constraint Manager.



Apply the Referenced ECSet to the remaining Force nets within the Allegro PCB design.

If using Allegro PCB Router, when more than 2 or 3 Sense lines are required, it may be a good idea to schedule the nets on different layers of the design.

Identifying intentional short

Allegro PCB Editor reports the pins and x,y location with NET_SHORT property in the IPC356 netlist.

Example IPC-D-356 netlist

C **

C Nets shorted using NET_SHORT property

C **

C

C Object Location Property

C ----------

C PIN X+070780Y+054660
FORCE4:NC:NC:SENSE41:SENSE42:SENSE43:NC:SENSE44:NC

C PIN X+070780Y+054660
FORCE4:NC:NC:SENSE41:SENSE42:SENSE43:NC:SENSE44:NC

C PIN X+070780Y+054660
FORCE4:NC:NC:SENSE41:SENSE42:SENSE43:NC:SENSE44:NC

C PIN X+070780Y+054660
FORCE4:NC:NC:SENSE41:SENSE42:SENSE43:NC:SENSE44:NC

C PIN X+071280Y+067710
FORCE3:NC:NC:SENSE31:SENSE32:SENSE33:NC:NC:NC

Miscellaneous Notes

The use of this flow could potentially cause issues downstream in your manufacturing process. Currently there is no direct way to communicate shorted nets to validation software such as Valor. It would be up to the user to manage the data accordingly to those vendors.

It is recommended to create and use a standard and unique reference designator for the force and sense physical symbol, ex. SP_1 (Shorting Pin). This would aid in search, and report generation.

There is currently a CCR logged against Allegro PCB Router for the methodology used in this Rapid Adoption Kit. Ensure that you are using the latest SPB 16.6 Hotfix. At this update, there was no date assigned to the fix.

Software and License used

This Application Note and its associated database has been modified using Cadence SPB 16.6 release with Hotfix -15.

This feature was originally available in SPB 16.5 release. It was not implemented until later in the release stream. If you use this technique, use the latest SPB 16.5 hotfix available on the Cadence downloads site.

Various software and license used are-

Part Developer with PCB Librarian Expert license.

Allegro Design Entry HDL with Allegro Design Authoring license and High Speed option.

Allegro PCB Editor with Allegro PCB Designer license and High Speed option to define different Constraints.

Use the Miniaturization options, if using an SMD pad on internal layers for connection, as that layer needs to be defined as Embedded Layer.

Sample Database

Download the sample database attached to this application note. Use this database for the evaluation purpose.

Important Database Element

Force Sense Schematic symbol ***"force_sense"*** located in the folder - worklib\force_sense

Force Sense Footprint symbol (***"cad_9pin_fs.dra"*** and ***"fs_smt.dra")*** located in the folder - worklib\test\physical\symbols

Allegro Design Entry HDL project file - *"**force_sense.cpm**"*

Board file – *"**netshortboard.brd**"* located in the folder - worklib\test\physical

Summary

Using this methodology will reduce the time and effort required to design a board with force and sense connections. Also, nets can be individually constrained. Pin-Pairs can be defined in the schematic to control shorting location. It allows for quick search and navigation in a schematic for these types of signals. Additionally, custom reports can be extracted based on the reference designator to assist with downstream processes.

References

The following Allegro product documentation may be found in local Cadence SPB16.5 installation (CDSROOT) and also online at Cadence Online Support.

Allegro User Guide

($CDSROOT\doc\algromast\algromast.pdf)

Allegro Design Entry HDL User Guide

($CDSROOT\doc\concepthdl\concepthdl.pdf)

Allegro Platform Properties Reference Guide

($CDSROOT\doc\propref\propref.pdf)