TI Designs

Industrial Ethernet PHY Brick with Fiber-Optic

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Design Resources

TIDA-00224	Tool Folder Containing Design Files
TLK105L	Product Folder
TTPS75433	Product Folder

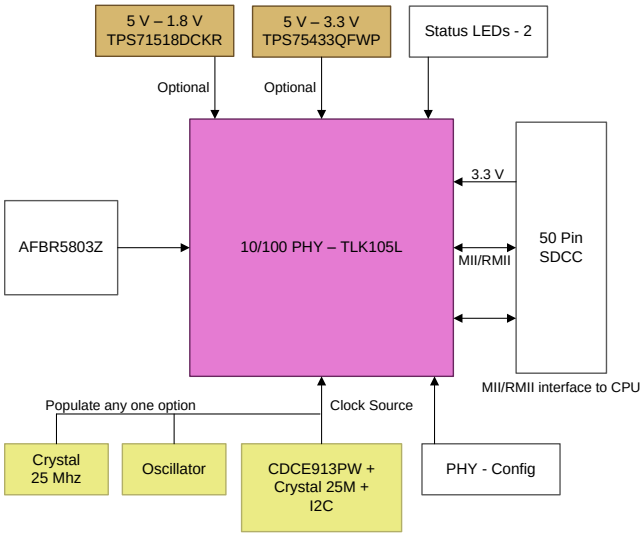
ASK Our Analog Experts
WEBENCH® Calculator Tools

Design Features

- Low Power Consumption <270 mW for EPHY, <850 mW for FO-Transceiver
- TLK105L Ethernet PHY Configured for MII Interface
- Programmable LED Support Link, Activity
- Avago AFBR5803Z. Fiber Transceiver Interface for Longer Distance and Better EMC Performance
- HBM ESD protection on RD± and TD±

Featured Applications

- Industrial Applications – Circuit Breakers, Protection Relays, Smart Meters (AMI)
- Substation Automation Products – RTU, Protection Relay, IEDs
- Power Quality Analyzer



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1 System Description

A simple and effective design makes Ethernet the most popular networking solution at the physical and data link levels of the Open Systems Interconnection (OSI) model. With high speed options and a variety of media types to choose from, Ethernet is efficient and flexible. In addition, the low cost of Ethernet hardware makes Ethernet an attractive option for industrial networking applications. The opportunity to use open protocols such as TCP/IP over Ethernet networks offers a high level of standardization and interoperability. The result has been an ongoing shift to the use of Ethernet for industrial control and automation applications. Ethernet is increasingly replacing proprietary communications.

1.1 Basic Fiber-Optic Communication System

Fiber-optics is a medium for carrying information from one point to another in the form of light. Unlike the copper form of transmission, fiber-optics is not electrical in nature. A basic fiber-optic system consists of a transmitting device that converts an electrical signal into a light signal, an optical fiber cable that carries the light, and a receiver that accepts the light signal and converts the light signal back into an electrical signal.

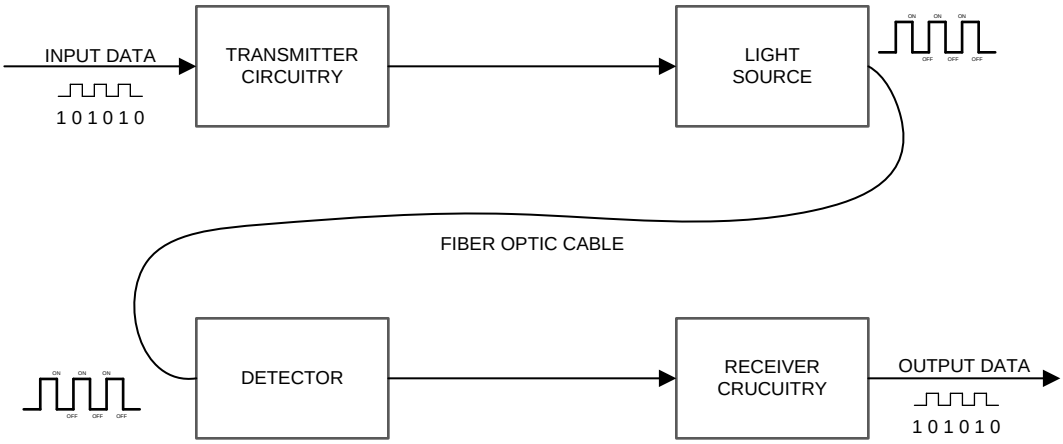

Figure 1. Basic Fiber-Optic Communication System

The complexity of a fiber-optic system can range from very simple (for example, a local area network) to extremely sophisticated and expensive (for example, long distance telephone or cable television trunking). For example, the system shown in Figure 1 can be built very inexpensively using a visible LED, plastic fiber, a silicon photodetector, and some simple electronic circuitry. The overall cost could be less than $20. On the other hand, a typical system used for long-distance, high-bandwidth telecommunication that employs wavelength-division multiplexing, erbium-doped fiber amplifiers, external modulation using DFB lasers with temperature compensation, fiber Bragg gratings, and high-speed infrared photodetectors could cost tens or even hundreds of thousands of dollars. The basic question is “how much information is to be sent and how far does it have to go?”

1.2 Types of Fiber

- Step-index multimode
- Step-index single mode
- Graded-index

1.2.1 Fiber-Optic Transceivers Overview

A fiber-optic transceiver is simply a transmitter-receiver pair. A transceiver is tasked with transmitting and receiving data (1's and 0's). A fiber-optic transceiver accomplishes this task by either turning the light source on or off. Transceivers fall under two categories: LED transceivers and laser transceivers. LEDs are generally more cost effective and extremely reliable. However, due to the nature of the technology, LEDs are limited to shorter link distances and slower speeds. Lasers are generally higher in power and emit a signal of better quality, resulting in longer-link distances. Lasers are used for applications requiring greater speeds.

1.2.2 Multimode Communication Links

Multimode communication links are generally the most common, due to the low cost of fiber cabling and transceivers. When forming a multimode link, one must use multimode transceivers as well as multimode cabling. Multimode fiber cable is generally specified as two numbers such as 62.5/125 µm or 50/125 µm. This specification implies a core size of 62.5 µm in diameter and a cladding size of 125 µm. 62.5/125 µm cabling is generally the most popular, followed by 50/125 µm. For historical reasons, 62.5/125 µm cabling has a large install base. However, 50/125 µm cabling is generally recommended for all new installations to allow for an upgrade path to gigabit (and beyond) speeds.

Multimode fiber cable is called multimode because the light used to transmit the data actually travels multiple paths within the fiber core. The fiber cable is designed with a core and cladding index difference to keep the majority of light energy within the fiber so that the light 'bounces' around. At the other end of the fiber, a data signal is composed of the light beams that took straight paths through the center of the core, as well as the light beams that 'bounced' around. This bouncing-around phenomenon is called modal dispersion. Modal dispersion is the primary characteristic that limits multimode fiber cable link distances.

The major benefits of multimode fiber are as follows.

- Multimode fiber is relatively easy to work with.
- Because of multimode fiber's larger core size, light is easily coupled to and from multimode fiber.
- Multimode fiber can be used with both lasers and LEDs as sources.
- Coupling losses are less than those of single-mode fiber.

The drawback of multimode fiber is that because many modes are allowed to propagate (a function of core diameter, wavelength, and numerical aperture), multimode fiber suffers from modal dispersion. The result of modal dispersion is bandwidth limitation, which translates into lower data rates.

1.2.3 Single-Mode Communication Links

Single-mode communication links are less common than multimode links, but single-mode communication links are quickly gaining ground when longer link distances (>3 km) are required. When constructing a single-mode link, the engineer must use single-mode transceivers with single-mode cabling. Single-mode fiber is also specified as two numbers such as 9/125 µm. The two numbers imply a core of just 9 µm, and a cladding 125 µm in diameter.

9/125 µm cabling is generally the most common, followed by 8/125 µm. Single-mode cabling is typically slightly more expensive that the multimode counterparts, but can reach distances up to 10 or 20 times farther. The whole idea behind a single-mode link path is that light carrying the data travels a single path. Light energy that strays away from the center path leaves the core and becomes trapped in the cladding due the properties of single-mode cabling. Because almost all the light received at the opposite end travels approximately the same path, modal dispersion (or timing jitter) is no longer a factor. The primary distance-limiting factor for single-mode links is signal power (or amplitude).

1.3 Transmission Windows

Optical fiber transmission uses wavelengths that are in the near-infrared portion of the spectrum. These wavelengths are just above the visible spectrum, and therefore undetectable to the unaided eye. Typical optical transmission wavelengths are 850 nm, 1310 nm, and 1550 nm. Both lasers and LEDs are used to transmit light through optical fiber. Lasers are usually used for 1310-nm or 1550-nm single-mode applications. LEDs are used for 850-nm or 1300-nm multimode applications. These ranges are the wavelength ranges that optical fiber transmission operates best.

1.3.1 Fiber-Optic Standards

Table 1. Fiber-Optic Standards

WAVELENGTH	MODE
850 nm	Multimode
1300 nm	Multimode
1310 nm	Single-mode
1550 nm	Single-mode

These wavelengths were chosen because they best match the transmission properties of available light sources with the transmission qualities of optical fiber.

1.3.2 Advantages of Fiber-Optic

- Galvanic isolated and robust communication interface
- Cabling distance is greater than UTP cable to meet demand of widely range (communicate over longer distances) and reduced communication failures
- Harsh environment capability: electromagnetic interference (EMI) immunity (insensitive to EMI), high temperature, high pressure, high voltage
- No grounding is required
- Intrinsically safe
- Small size and lightweight
- Integrated telemetry: fiber itself is a data link
- Wide bandwidth
- High sensitivity

1.3.3 Disadvantages of Fiber-Optic

- More challenge for cable installation
- Must use expensive fiber-optic cable and connectors
- Need for more expensive optical transmitters and receivers
- Cannot carry electricity to operate or power terminal devices

1.4 Ethernet Fiber-Optic

Copper-based Ethernet connections are limited to a data transmission distance of only 100 meters when using unshielded twisted pair (UTP) cable. By using fiber conversion solution, fiber-optic cabling can be used to extend data transmission over greater distances. An Ethernet with fiber can also be used where there is high level of EMI, which is a common phenomenon found in industrial plants. This interference can cause corruption of data over copper-based ethernet links. Data transmitted over fiber-optic cable, however, is completely immune to this type of noise.

Since fiber can transport more data over longer distances than copper cabling, increased distances provide the ability to reach more users and equipment. Fiber has complete immunity to electrical interference, and provides higher security than copper cabling because fiber has no electro-magnetic emission. These characteristics have made fiber an ideal medium for commercial, utility, government, and financial networks. Distances supported by fiber network infrastructure are limited mostly by the optical power, or brightness, supplied by the active hardware interface. Fiber distances can range from 300 meters to 140 kilometers, depending on the type of media converter, cable, wavelength, and data rate.

The use of Ethernet fiber-optics in LANs has increased due to the inherent advantages of fiber and high data rates can be maintained without electromagnetic (or radio-frequency) interference. Fiber offers higher voltage isolation, intrinsic safety, and elimination of ground loops in geographically-large installations.

This reference design platform demonstrates the advanced performance of the TLK10xL Ethernet PHY transceiver devices. The brick provides an IEEE 802.3u 100BASE-FX fiber Interface. This reference design operates from a single power supply (5 V with on-board regulator or 3.3 V). All other voltages required for the Ethernet PHY transceiver are generated internally within the device.

This Ethernet PHY brick reference design enables Texas Instruments' customers to quickly design and release to market systems using TI industrial Ethernet PHY transceiver devices. A 50-pin interface has been provided to interface with a 32-bit Cortex M4 processor-based controller board. The board has been designed in a small (2 inches x 3 inches) form factor, which makes it easy to fit into any of the present products.

2 Design Features

Table 2. Design Features

Ethernet PHY	The TLK105L Ethernet PHY features: • Industrial temperature rating: –40°C to 85°C • Configurable PHY addresses – resistor strapping • MII or RMII – resistor strapping options
Ethernet fiber-optic interface	1300 nm, multimode, Ethernet 100 base-FX
Power consumption	Single Supply: <275 mW, <850 mW for fiber-optic
Power supply	The device is designed for power-supply flexibility and can operate with a single 3.3-V power supply
Power input options	• 5 V from external 2-pin connector • 5-V DC input from MII and on-board regulator to generate 3.3 V • 3.3-V DC input from MII interface with no on-board regulator
MAC – controller interface	50-pin MII interface connector
Clock	25-MHz crystal with internal oscillator
Status LEDs	Two LEDs [(Link and activity with option to configure as Pull Up (PU) or Pull Down (PD)]
ESD	IEC61000-4-2 – Level 3 , Criteria B

3 Block Diagram

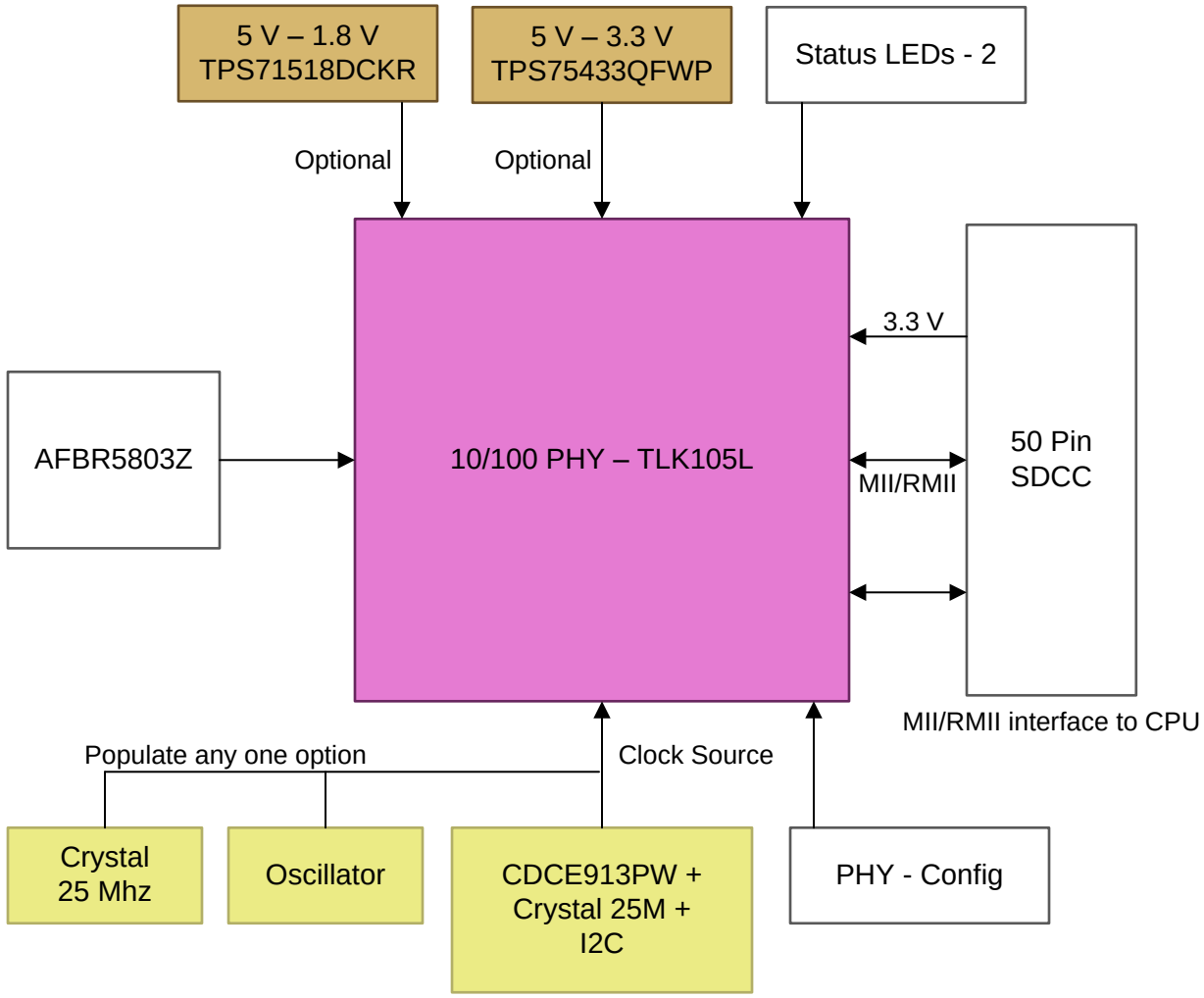

Figure 2. Block Diagram

4 Board Pictures

Figure 3. Board Picture –Top

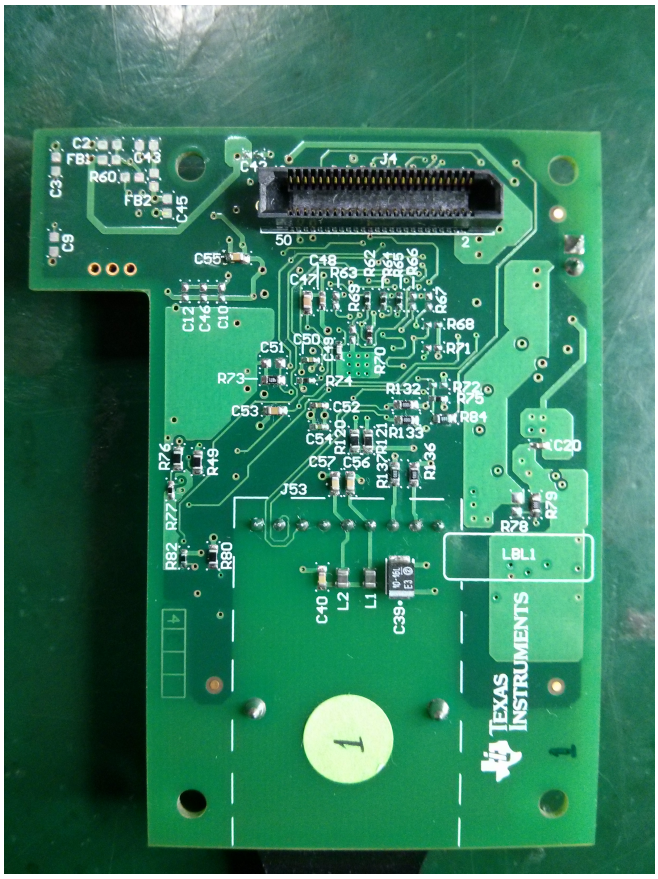

Figure 4. Board Picture – Bottom

5 Highlighted Products

For more information on each of these devices, see the respective product folders at www.ti.com.

5.1 Single Port 10/100 Mbs Ethernet Physical Layer Transceiver

The Ethernet PHY used in the reference design is TLK105L. The major features of the Ethernet PHY are described as follows.

5.1.1 MAC Data Interface (MII)

TLK105L is a single port 10/100 Mbs Ethernet physical layer transceiver. In this reference design, the Ethernet PHY brick is interfaced to the MAC through the MII interface.

5.1.2 Bootstrap Configuration

Provision is provided to configure the PHY through resistors. The details are provided in Section 6.

5.1.3 LED

An option for two LEDs has been provided.

- Activity
- Link

The LEDs can be configured as active pull-up or active pull-down.

5.1.4 Clock Circuit

For the MII interface, the clock source is a 25-MHz crystal with internal oscillator.

5.2 Ethernet - Fiber Transceiver - 100BASE-FX

The TLK10xL supports 100Base-FX signaling via an external optical transceiver. AFBR-5803Z/ FDDI, 100 Mb/s ATM, and Fast Ethernet Transceiver is used in this design.

5.3 MII (MAC) - Controller Interface

The interface to the controller is through a 50-pin high speed connector. The male connector is mounted on the controller board, and the female connector is on the Ethernet PHY brick board. The female connector has the MII interface signals and the power input (5-V DC or 3.3-V DC).

5.4 Power Supply

The Ethernet PHY operates on a single power supply. The Ethernet PHY brick board can be powered by:

- External 5 V
- 5 V from the controller board
- 3.3 V from the controller board

5.4.1 Filtering

The required filter capacitors have been provided in the reference design.

6 Circuit Design and Component Selection

6.1 Single Port 10/100 Mbs Ethernet Physical Layer Transceiver

6.1.1 MAC Data Interface (MII)

TLK105L is a single port 10/100 Mbs Ethernet physical layer transceiver which has the signals for the MII interface shown in Figure 5.

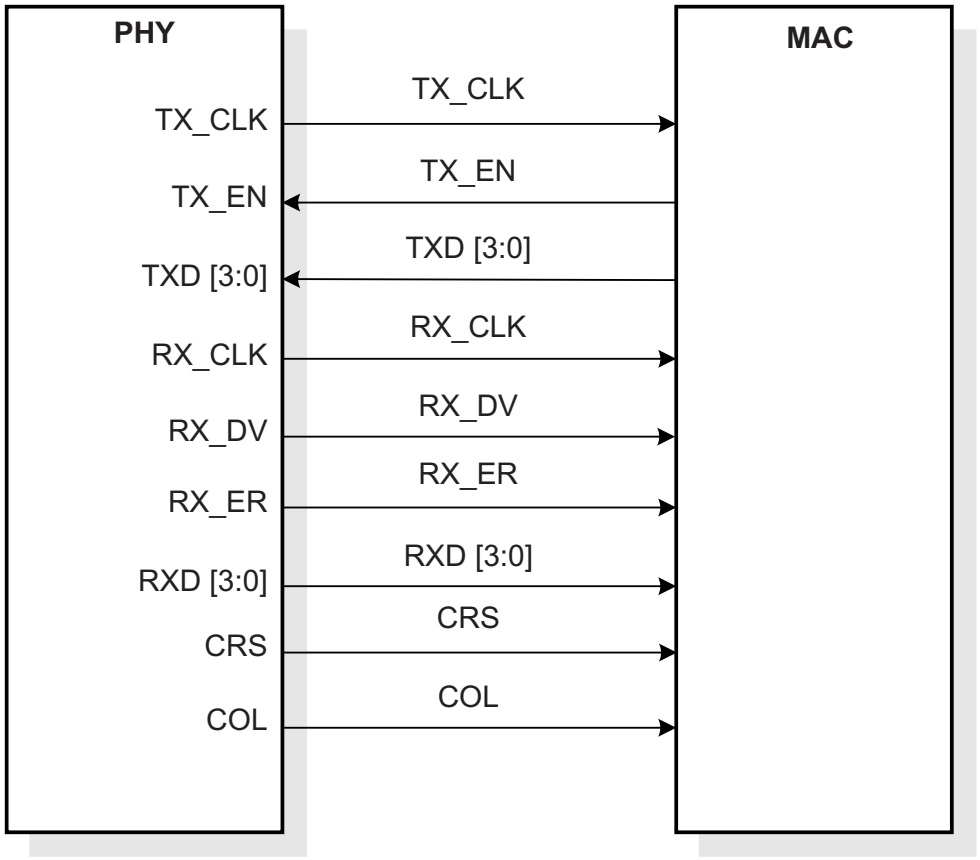

Figure 5. MII Signaling

The Media Independent Interface (MII) is a synchronous, 4-bit wide nibble data interface that connects the PHY to the CPU MAC in 100B-TX and 10B-T modes. The MII is fully compliant with IEEE802.3-2002 clause 22.

The MII signals are summarized as follows:

- Data signals TXD [3:0],RXD [3:0]
- Transmit and receive-valid signals TX_EN,RX_DV
- Line-status signals CRS (carrier sense)
- COL (LED_LINK)

Additionally, the MII interface includes the carrier sense signal CRS, as well as a collision detect signal COL. The CRS signal asserts to indicate the reception of data from the network or as a function of transmit data in half-duplex mode. The COL signal asserts as an indication of a collision, which can occur during half-duplex operation when both transmit and receive operations occur simultaneously.

6.1.2 Bootstrap Configuration

Bootstrap configuration is a convenient way to configure the TLK10xL device into specific modes of operation. Some of the functional pins are used as configuration inputs, as shown in Figure 6. The logic states of these pins are sampled during reset and are used to configure the TLK10xL device into specific modes of operation. Table 3 describes bootstrap configuration. A 2.2-kΩ resistor is used for pull-down or pull-up to change the default configuration. If the default option is desired, there is no need for external pull-up or pull-down resistors. Because these terminals may have alternate functions after reset is de-asserted, these terminals must not be connected directly to V_{CC} or GND.

Table 3. Bootstrap Configuration

<table>
<tr><th>TERMINAL</th><th>COMPONENTS OF THE BOARD</th><th>DESCRIPTION</th></tr>
<tr><td>PHYAD0 (COL)
PHYAD1 (RXD_0)
PHYAD2 (RXD_1)
PHYAD3 (RXD_2)
PHYAD4 (RXD_3)</td><td>R52, R53
R64,
R65,
R66,
R67</td><td>PHY Address [4:0]: The TLK10xL provides five PHY address terminals, the states of which are latched into an internal register at system hardware reset. The TLK10xL supports PHY Address values 0 (<00000>) through 31 (<11111>). PHYAD [4:1] terminals have weak internal pull-down resistors, and PHYAD [0] has a weak internal pull-up resistor, setting the default PHYAD if no external resistors are connected.</td></tr>
<tr><td>AN_0 (LED_LINK)</td><td>R46, R51</td><td>AN_0: FD-HD config. FD = pull-up.
The default wake-up is autonegotiation enable 100BT.
<table>
<tr><th>AN_0</th><th>Forced Mode</th></tr>
<tr><td>0</td><td>10Base-T, Half-duplex
100Base-TX, Half-duplex</td></tr>
<tr><td>1</td><td>10Base-T, Half- or full-duplex
100Base-TX, Half- or full-duplex</td></tr>
</table></td></tr>
<tr><td>LED_CFG (CRS)</td><td>R69</td><td>LED Configuration: This option selects the operation mode of the LED_LINK terminal (the default mode is Mode 1). All modes are also configurable via register access. See PHY Control Register (PHYCR), Address 0x0019.</td></tr>
<tr><td>AMDIX_EN (RX_ER)</td><td>R70</td><td>Auto-MDIX Enable: This option sets the Auto-MDIX mode. By default, it enables Auto-MDIX. An external pull-down resistor disables Auto-MDIX mode.</td></tr>
<tr><td>MII_MODE (RX_DV)</td><td>R63</td><td>MII Mode Select: This option selects the operating mode of the MAC data interface. This terminal has a weak internal pull-down, and it defaults to normal MII operation mode. An external pull-up causes the device to operate in RMII mode.</td></tr>
</table>

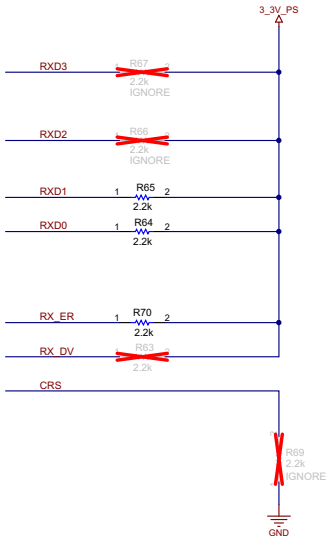

Figure 6. Configuration Pins

6.1.3 LED

The TLK10xL devices support the use of two LEDs. The LEDs can be configured for pull-up or pull-down using the resistors as shown in Figure 7.

Figure 7. LED

6.1.4 Clock Circuit [Clock In (XI) Requirements]

The TLK10xL supports an external CMOS-level oscillator source or an internal oscillator with an external crystal. The use of a 25-MHz, parallel, 20-pF load crystal is recommended if a crystal source is desired. Figure 8 shows a typical connection for a crystal resonator circuit. The load capacitor values will vary with the crystal vendors; check with the vendor for the recommended loads.

The oscillator circuit is designed to drive a parallel-resonance AT-cut crystal with a minimum drive level of 100 µW and a maximum of 500 µW. If a crystal is specified for a lower drive level, a current limiting resistor must be placed in series between XO and the crystal. As a starting point for evaluating an oscillator circuit, if the requirements for the crystal are not known, set the values for CL1 and CL2 at 33 pF, and set R1 at 0 Ω. Specifications for a 25-MHz crystal are listed in Table 4.

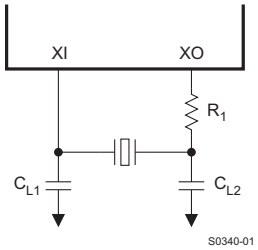

Figure 8. Crystal Oscillator Circuit

Table 4. 25-MHz Oscillator Specifications

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Frequency			25		MHz
Frequency tolerance	Operational temperature			±50	ppm
Frequency stability	1 year aging			±50	ppm
Rise / Fall time	10%–90%			8	nsec
Jitter (short term)	Cycle-to-cycle		50		psec
Jitter (long term)	Accumulative over 10 ms			1	nsec
Symmetry	Duty cycle	40%		60%	
Load capacitance			15	30	pF

6.2 Ethernet - Fiber Transceiver - 100BASE-FX

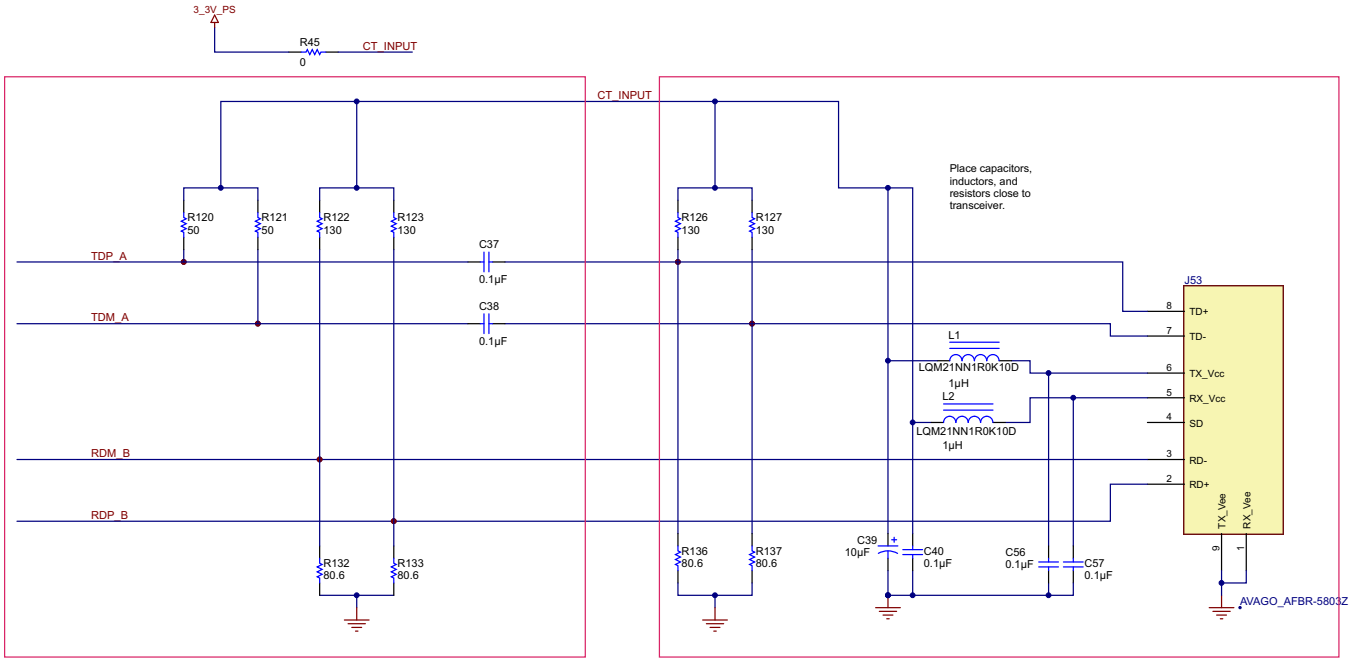

Figure 9. Ethernet - Fiber Transceiver - 100BASE-FX

6.2.1 Transmitter Sections

The transmitter section of the AFBR-5803Z utilizes 1300–nm surface-emitting, InGaAsP LEDs. These receiver sections are packaged in the optical subassembly portion of the transmitter section. These LED are driven by a custom silicon IC, which converts differential PECL logic signals, ECL referenced (shifted) to a 3.3-V supply, into an analog LED drive current.

6.2.2 Receiver Sections

The receiver sections of the AFBR-5803Z utilize InGaAsPIN photodiodes coupled to a custom silicon trans-impedance preamplifier IC. These are packaged in the optical subassembly portion of the receiver. These pin and preamplifier combinations are coupled to a custom-quantizer IC which provides the final pulse shaping for the logic output and the signal detect function. The data output is differential. The signal-detect output is single-ended. Both data and signal-detect outputs are PECL compatible, ECL referenced (shifted) to a 3.3-V or 5-V power supply.

In 100BASE-FX mode, the device-transmit pins connect to an industry standard fiber transceiver with PECL signaling through a capacitively-coupled circuit. In FX mode, on the TX path, the device bypasses the scrambler and the MLT3 encoder, enabling the transmission of serialized 5B4B-encoded, NRZI data at 125 MHz. On the RX path, the device bypasses the MLT3 decoder and the descrambler, enabling the reception of serialized 5B4B-encoded, NRZI data at 125 MHz. The only added functionality in the aspect of data transmission for 100BASE-FX (compared to 100BASE-TX) is the support of far-end fault detection and transmission.

6.2.3 Far-End Fault (FEF) Mechanism

Because 100BASE-FX does not support autonegotiation, a far-end fault facility is included in the design. The far-end fault facility allows detection and transmission of link failures. When no signal is being received as determined by the signal detect function, the device sends a far-end fault indication to the far-end peer.

The far-end fault indication detects repeating cycles. Each cycle consists of 84 ones followed by a single zero. The cycle pattern will not satisfy the 100BASE-FX carrier sense mechanism. However, the cycle pattern is easily detected as the fault indication. The cycle pattern will be transparent to devices that do not support far-end fault detection. The far-end fault detection process continuously monitors the receive-data stream for the far-end fault indication. When detected, the link monitor is forced to de-assert link status, causing the device to begin transmitting far-end fault signaling to the far-end peer.

6.3 MII(MAC) - Controller Interface

The Ethernet PHY has been interfaced and tested with the TM4C129XNCZAD 32-bit ARM® Cortex™-M4F MCU. The drivers required to interface TLK105L to the MCU are available.

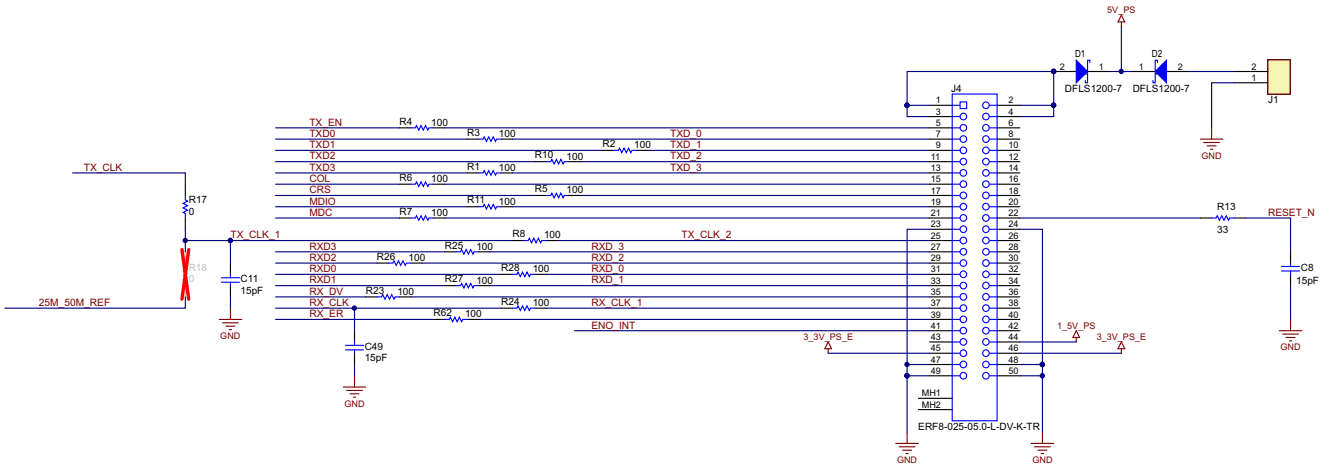

Figure 10. MII (MAC) - Controller Interface

6.4 Power Supply

The Ethernet PHY can be powered by a single 3.3-V supply.

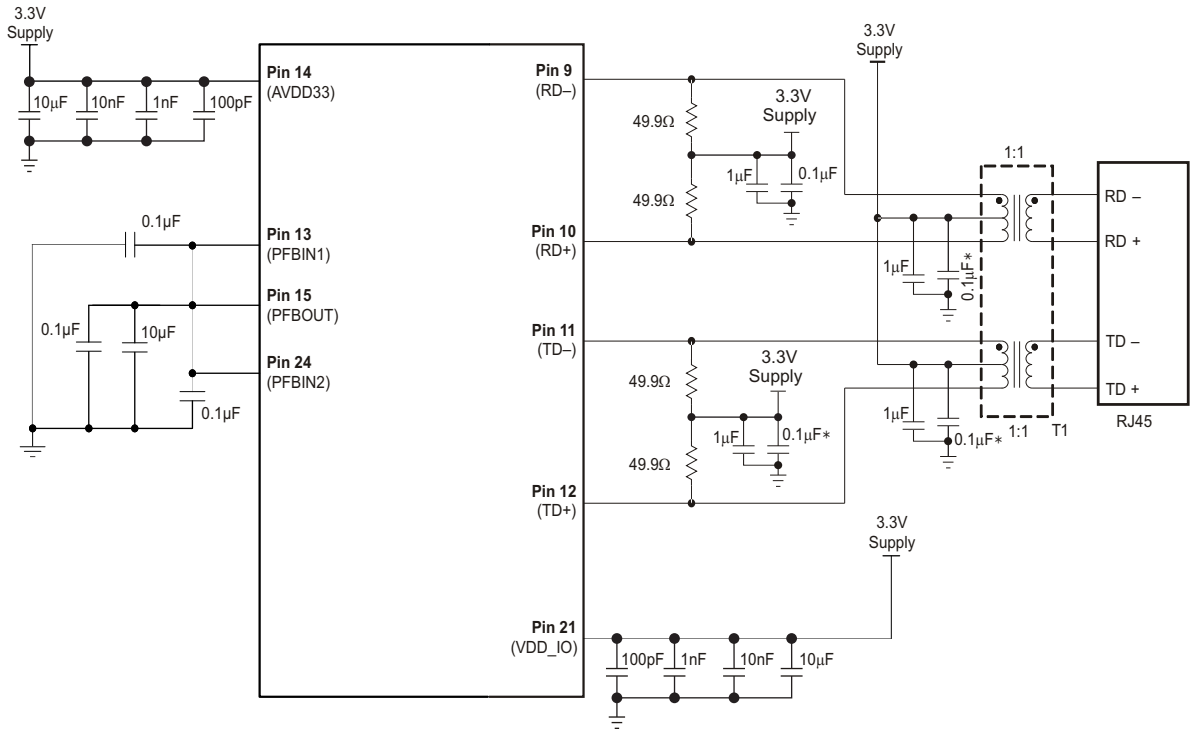

Figure 11. Power Connections for Single Supply Operation

The Ethernet PHY brick board can be powered by either of the following two methods as shown in Figure 12 and Figure 13.

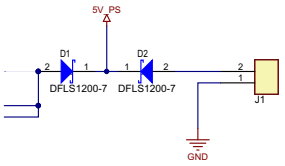

Figure 12. Powered By External 5 V or 5 V from the Controller Board

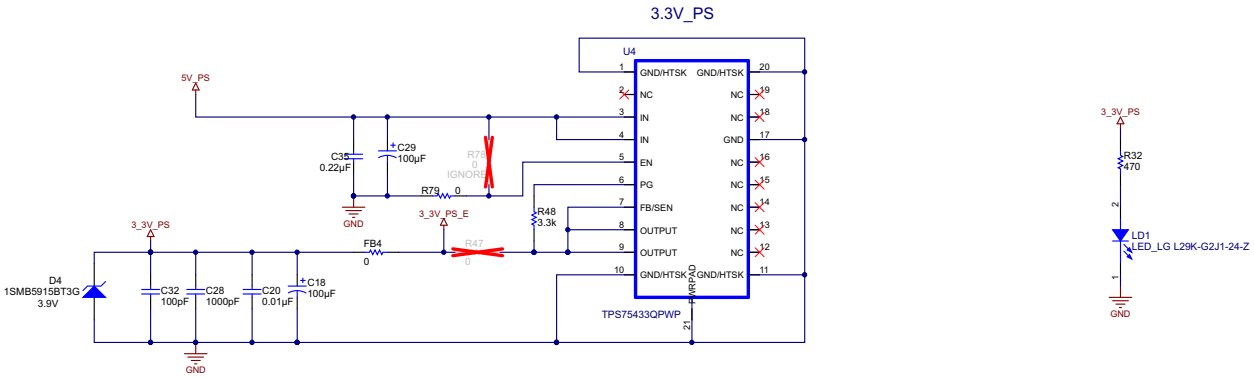

Figure 13. Powered By 3.3 V from the Controller Board

6.4.1 Filtering

Bypass the power rails with the following low-impedance surface mount capacitors: 10 µF, 10 nF, 1 nF, and 100 pF. To reduce EMI, place the capacitors as close as possible to the component's V_{DD} supply pins, preferably between the supply pins and the vias connecting to the power plane. In some systems, it may be desirable to add 0-Ω resistors in series with supply pins, as the resistor pads provide flexibility by adding an EMI bead when the design needs to meet system–level certification and testing requirements.

PCBs should have at least one solid ground plane and one solid V_{DD} plane to provide a low impedance power source to the component. This also provides a low impedance return path for non-differential digital MII and clock signals. Place a 10.0-µF capacitor near the PHY component for local bulk bypassing between the V_{DD} and ground planes. The rise time of the V_{DD} should typically be 500 µs.

Table 5. Power Consumption at 3.3 V

PARAMETERS	POWER (MAX)
Ethernet PHY – single supply	270 mW
Fiber-optic – transmit	600 mW
Fiber-optic – receive	250 mW
Total	1220 mW

6.5 4.5 Fiber-Optic Cords Ideal for Ethernet Applications

Figure 14. Fiber-Optic Cords

Fiber-optic patch cords are ideal for high data-rate systems including FDDI, multimedia, Ethernet backbone, ATM, or any network that requires the transfer of large and time-consuming files.

Features

- Ideal for use in Ethernet applications
- High bandwidth supporting longer distances

Table 6. Major Specifications for Fiber-Optic Cords for Ideal Use in Ethernet Application

First connector	SC duplex
Second connector	SC duplex
Cable diameter	0.12" (3 mm)
Cable type	Buffered fiber
Fiber type	62.5/125
Length - overall	16.4' (5 m)
Type	Multimode, duplex

SC Connector

- The SC connector is a fiber-optic connector, with a push-pull latching mechanism which provides quick insertion and removal, while also ensuring a positive connection.
- The SC connector has been standardized as FOCIS 3 (Fiber Optic Connector Intermateability Standards) in EIA/TIA-604-03.

6.6 PCB Dimensions and Physical Layout

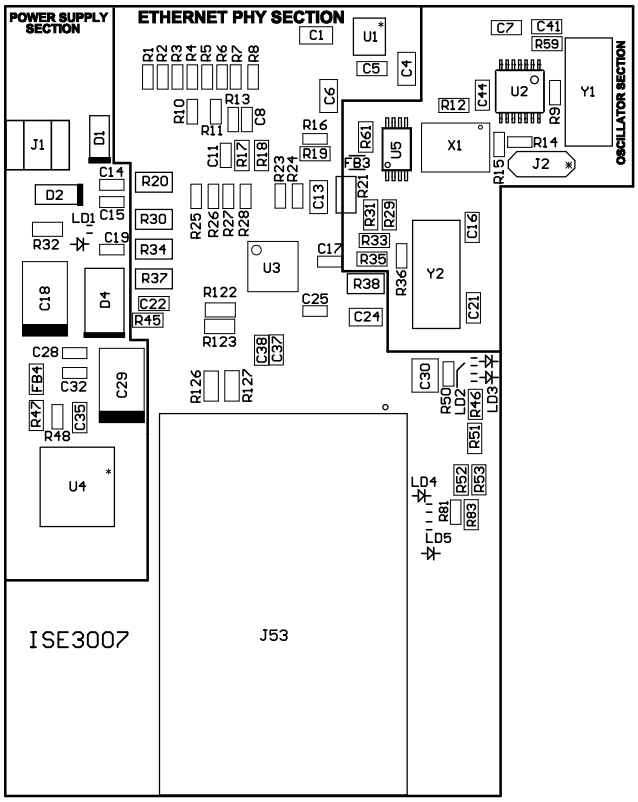

Figure 15. PCB Dimensions and Physical Layout

PCB Dimensions

Total dimensions - the current board is 3 inch × 2 inches. The board has provisions for the following:

- Power supply
- Ethernet PHY and associated components
- RMII interface

The size can be reduced based on the application.

PCB Physical Layout

- FR4 material
- Trace impedance - differential impedance 100 ohms, ±5%
- Uniform supply and ground plane
- Four layers
- Combination of through-hole and surface-mount technology

6.7 ESD Protection

The network or medium dependent interface (MDI) connection is via the transmit (TD+ and TD–) and receive (RD+ and RD–). Both transmit and receive are ESD protected. On-chip HBM, ESD protection on RD± and TD± of 16 kV is provided.

7 Software Description

Table 7. Software Description

FUNCTIONALITY	CONFIGURATION DESCRIPTION
Hardware reset	A hardware reset is accomplished by applying a low pulse (TTL level), with a duration of at least 1 µs, to /RESET. This pulse resets the device so that all registers are reinitialized to default values, and the hardware configuration values are re-latched into the device (similar to the power-up/reset operation). The time from the point when the reset pin is de-asserted to the point when the reset has concluded internally is approximately 200 µs.
External MII PHY initialization	Set the external PHY address (as per the boot strap configuration). All the read and write requests to the PHY use the configured external PHY address. Reset the PHY: 1. MII reset - Set the BMCR (0x00) register bit 15 to one. 2. Software/Digital reset – Set PHYRCR (0x1F) data register bit15 and bit14 to one. Issue a delay of 500 microseconds. Set the BMCR (0x00) register autonegotiation enable and autonegotiation restart by setting bit-12 and bit-8 to one. Poll the BMSR (0x01) register bit5 to check if autonegotiation is complete.
MII_MODE	The MII_MODE is selected by pin 26 (RX_DV). This pin has internal weak pull-down and defaults to MII mode. (External pull-up makes the PHY to operate in RMII mode).
PHY ID	PHY ID is decided by the pull-up registers (refer to the Bootstrap section of *Industrial Temp, Single Port 10/100Mbs Ethernet Physical Layer Transceiver*, TLK105L/6L Data Sheet SLLSEE3). Care has to be taken that the appropriate PHY id is used for appropriate hardware bootstrap configuration (per pull-up registers). This values of pins 29, 30 ,31 ,32, and 1 (PHYAD0/COL, PHYAD1/ RXD0, PHYAD2/ RXD1, PHYAD3/ RXD2, and PHYAD4/ RXD3) are latched into an internal register at hardware reset.
LED configuration	Pin 17 and pin 29 can be used for LED configuration either as pull-up or pull-down. Pin 17 indicates link status (fully lit) by default; activity is indicated by blinking the same LED. If the designer needs to use pin 29 for indicating LED status, MLEDCR has to be configured. Configuring MLEDCR provides an option to route the activity signal to pin 29 instead of pin 17. In order to route the activity signal to pin 29 instead of pin 17, the COL signal has to be disabled. For further details. refer the LED Interface section of *Industrial Temp, Single Port 10/100Mbs Ethernet Physical Layer Transceiver*, TLK105L/6L Data Sheet SLLSEE3.
Testing TLK105L	This design has been created with the assumption that the hardware is connected to one end of the Ethernet cable and the other end of the Ethernet cable is connected to the PC. TX clock and RX clock can be probed or measured (after the PHY is powered up and not in reset state). Initiate a ping request with an IP address that is within the PC's subnet. For example, 192.16.0.100 is the PC IP address and 255.255.255.0 is the subnet mask. Initiate a ping command, for example, ping 192.16.0.1 –t TX[0:3] and RX[0:3]. The ping result will show some data patterns. Ping will create traffic at every plug-in of the Ethernet cable. After some time, when a destination host unreachable message is seen, there may not be a further Ethernet message on the wire.

7.1 FO Register Configuration for TLK105L

Table 8. Fiber Mode Control Register, Address 0x00FD

BIT	NAME	DEFAULT	FUNCTION
15	FX FEF faulting status	RO, LH	Asserted when the FEF (far-end fault) detection mechanism detects FEF signaling from the far-end peer.
14	FX PECL signaling status	RO ,LH	Asserted if the FX receiver detects violation of the PECL signaling from the optic transceiver (such as glitches or invalid pulse width).
13	FX SD status	RO, LL	Indicates the Status of SD_IN signal in the fiber RX path. If SD_IN is de-asserted, SD_IN will be latched low. Upon read, the value of the bit will be updated with the current value.
12:10	RESERVED	011, RO	
9	Enable auto SD Indication	0, RW	When asserted, this bit enables auto detection of the SD_IN signal based on the optic transceiver output. This mode assumes that when SD_IN is low, the optic transceiver does not transmit valid PECL signaling. The Auto SD_IN feature can detect Valid PECL signaling, and once detected, Auto SD_IN assumes the SD_IN is asserted and establishes the FX link.
8:0	RESERVED	1 0110 0100, RO	

Table 9. Fiber Mode Control Register, Address 0x0102

BIT	NAME	DEFAULT	FUNCTION
15	Enable manual SD_IN Config	0, RW	Allows manual configuration of the SD_IN signal. Manual configuration of the SD_IN signal allows the MAC to control the start of an FX link, assuming the MAC is in 'PHY link partners connected' status. The actual control on the SD_IN is done using bit [14] in this register.
14	SD_IN manual Config	0, RW	SD_IN manual control: '1' - notifies the PHY SD_IN is on and '0' notifies the PHY the SD_IN is off. Manual configuration overrides all other SD_IN mechanisms.
13:0	RESERVED	00 0010 0000 0000, RO	Writes ignored, read as 0x200h.

7.2 Sample Code

```
EMACPHYWrite(EMAC0_BASE, ui8PHYAddr, EPHY_BMCR, EPHY_BMCR_SPEED);//Force 100Mbps using register
0x0000
ui16Val = EMACPHYRead(EMAC0_BASE, ui8PHYAddr, EPHY_BMSR);
       SysCtlDelay(100);
EMACPHYWrite(EMAC0_BASE, ui8PHYAddr, 0x0040, 0x2000);//set bit 13//force link
       SysCtlDelay(100);
EMACPHYWrite(EMAC0_BASE, ui8PHYAddr, EPHY_CFG2, 0x4000);//set bit 14 for PHY register 0x000A
       SysCtlDelay(100);
status = EMACPHYRead(EMAC0_BASE, ui8PHYAddr, EPHY_BMSR);//PHY register 0x0001
       SysCtlDelay(100);
// EMACPHYExtendedWrite(EMAC0_BASE, ui8PHYAddr, 0xFD, 0x0200);
status = EMACPHYExtendedRead(EMAC0_BASE, ui8PHYAddr, 0xFD);
       SysCtlDelay(10000);
```

8 Test Results

8.1 Functional Testing

Table 10. Functional Testing

Clock	25 MHz
V_{CC} (3 V–3.6 V)	3.31-V DC
Internal 1.55 V	1.55-V DC
MII interface	OK
Link and activity LED	OK

8.2 Communication Interface Testing (Computer to Device)

Media converter mode, shown in Figure 16, allows conversion of copper to fiber and conversion of fiber to copper at 100 Mbs. This configuration allows longer-run fiber to be used in situations where fiber support is not built into the end device. This configuration can also be combined with power over Ethernet on the copper side.

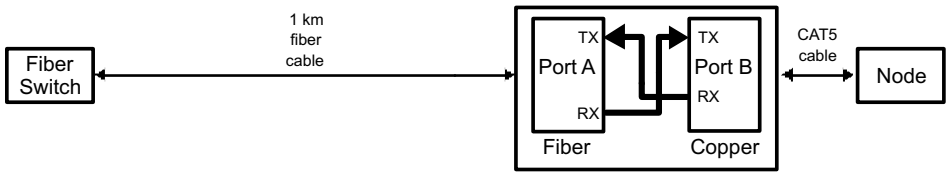

Figure 16. Media Converter Example

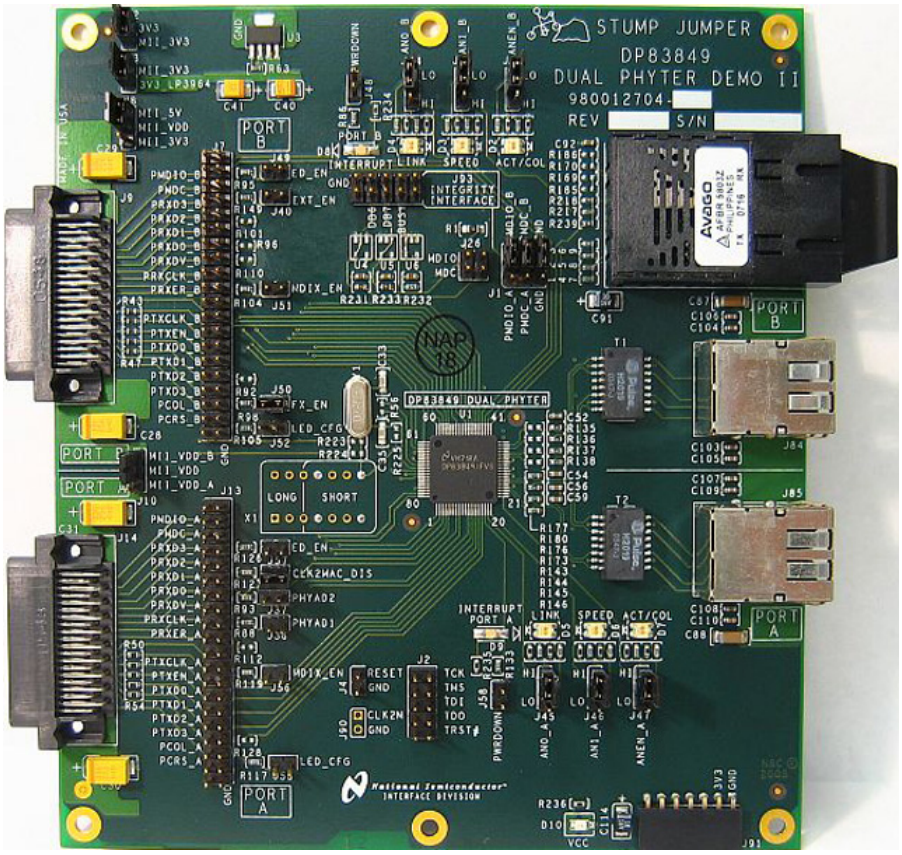

Figure 17. DP83849IVS-EVK with Copper and Fiber Options

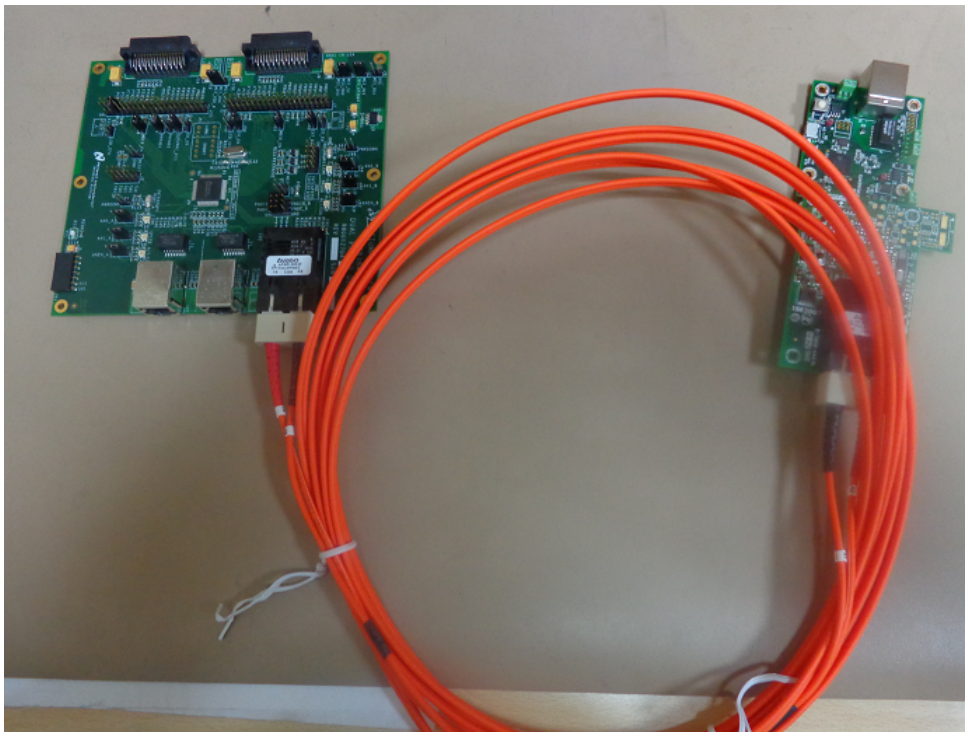

Figure 18. DP83849IVS-EVK Connected with FO-Brick

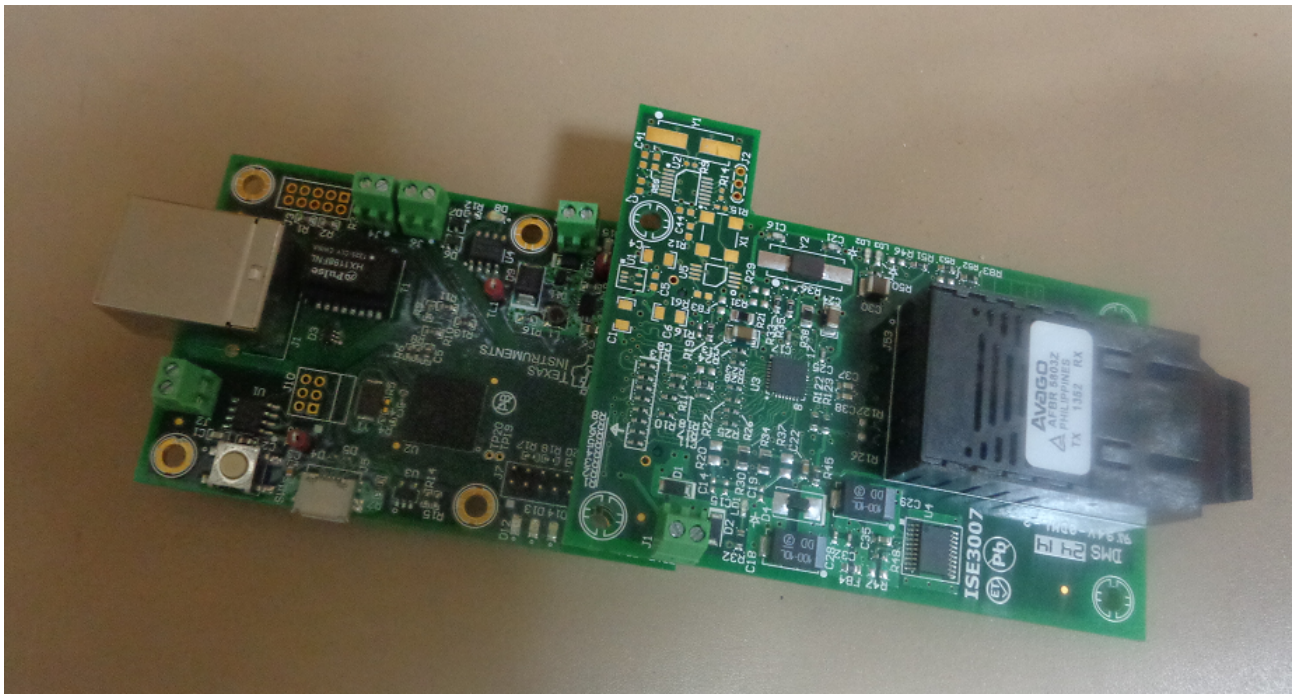

Figure 19. FO-Brick Connected to Tiva TM4C129XNCZAD (TIDA-00226)

8.2.1 Extender/Media Converter Implementation

The PHYTER dual incorporates two methods of configuring extender/media converter mode: via a simple strap option or register control. *The definitions of extender and media converter only differ in their physical (copper or fiber) interfaces; the port swapping is the same.* The optional use of RMII mode in conjunction with Extender/Media Converter mode allows flexibility in the system design.

8.2.2 Notes and Restrictions

Both ports must be operating at the same speed (100 MBPS). This can be accomplished using straps or port register controls. Both ports must be in full-duplex mode. Both ports must use a common-clock mode, either RMII mode (RBR:RMII_EN = 1) or single clock MII mode (RBR:SCMII_RX = 1 and RBR:SCMII_TX = 1) to ensure synchronous operation. If single clock MII mode is used and only one RX to TX path is enabled, RBR:SCMII_RX in the RX port and RBR:SCMII_TX in the TX port must be set to 1. Media Conversion is only supported in 100-Mb mode.

8.2.3 Strapped Extender or Media Converter Mode

The PHYTER dual provides a simple strap option to automatically configure both ports for extender or media converter mode, shown in Figure 20, with no device register configuration necessary. The RXD_2_B/EXTENDER_EN strap is used in conjunction with two autonegotiation straps (LED_ACTCOL/AN_EN, LED_SPD/AN1), the RMII mode strap (RX_DV/MII_MODE), and the fiber mode (COL/FX_EN) strap to allow many possible configurations.

If extender mode is strapped but RMII mode is not strapped, both ports will automatically be configured for single clock MII receive and transmit modes. *Note that in strapped extender/media converter mode, the RX MAC interfaces are still active, allowing easy monitoring of the data received on each port.*

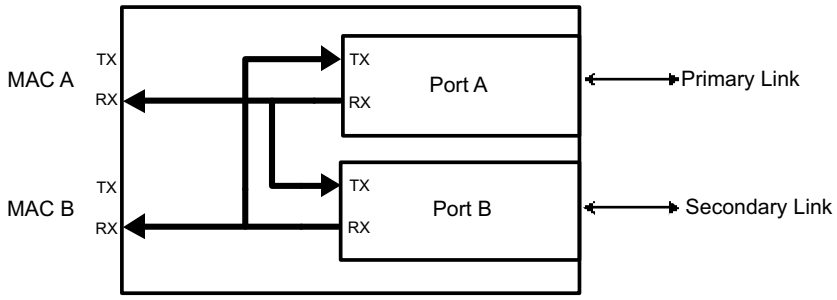

Figure 20. Extender/Media Converter (Strapped)

Several common configurations are shown in Table 11. Note that either single-clock MII or RMII can be configured independently from the flexible port mode. However, there is a requirement that both ports must be configured to the same common-clock mode.

Since the EXTENDER_EN strap forces full-duplex mode (including autonegotiation advertisement), the AN0 (duplex) strap is not shown. If the receive MII ports are to be monitored, energy-detect and power-down modes should be disabled.

Table 11. Common Strapped Extender/Media Converter Mode Configurations

MODE	AUTONEGOTIATION STRAPS				FIBER MODE STRAPS		NOTES
	AN_EN_A	AN1_A	AN_EN_B	AN1_B	FX_EN_A	FX_EN_B	
100-Mb copper extender	1	1	1	1	0	0	Advertise 10/100 Mb full-duplex
	0	1	0	1	0	0	Force 100-Mb full-duplex
100-Mb fiber extender	Do not care	Do not care	Do not care	Do not care	1	1	No autonegotiation
100-Mb copper extender	1	0	1	0	0	0	Advertise 10-Mb full-duplex
	0	0	0	0	0	0	Force 10-Mb full-duplex
100-Mb media converter	Do not care	Do not care	1	1	1	0	Port A is fiber, B is copper with autonegotiation
	1	1	Do not care	Do not care	0	1	Port A is copper with autonegotiation, B is fiber
	Do not care	Do not care	0	1	1	0	Port A is fiber, B is copper-forced
	0	1	Do not care	Do not care	0	1	Port A is copper-forced, B is fiber

Table 12. Jumper Tables

JUMPER	NAME	FUNCTION	SETTING
AUTONEGOTIATION			
J42	ANEN_B	Port B – enable/disable autonegotiation	Jumpered-low
J43	AN1_B	Port B – forced/advertised operation mode in autonegotiation	Jumpered-low
J44	AN0_B	Port B – forced/advertised operation mode in autonegotiation	Jumpered-high
J45	AN0_A	Port A – forced/advertised operation mode in autonegotiation	Jumpered-high
J46	AN1_A	Port A – forced/advertised operation mode in autonegotiation	Jumpered-high
J47	ANEN_A	Port A – enable/disable autonegotiation	Jumpered-high
FUNCTION			
J40	XTENDER_EN	Allow extender mode (For DP83849IVS/IFVS)	Jumpered
J41	CLK2MAC_DIS	Disable clock to MAC output	
J48	PWRDOWN_INT_B	Port B – allow power down and interrupt mode	
J49	ED_EN_B	Port B – enable energy detect mode	
J50	FX_EN_B	Port B – enable fiber mode (For DP83849IDVS/IFVS)	Jumpered
J51	MDIX_EN_B	Port B – enable/disable MDIX mode (default is enabling)	Jumpered-high
J52	LED_CFG_B	Port B – allow LEDs configuration. See *Industrial Temp, Single Port 10/100Mbs Ethernet Physical Layer Transceiver*, TLK105L/6L Data Sheet SLLSEE3.	
J55	LED_CFG_A	Port A – allow LEDs configuration. See *Industrial Temp, Single Port 10/100Mbs Ethernet Physical Layer Transceiver*, TLK105L/6L Data Sheet SLLSEE3.	
J56	MDIX_EN_A	Port A – enable/disable MDIX mode (default is enabling)	Jumpered-high
J57	ED_EN_A	Port A – enable energy detect mode	
J58	PWRDOWN_INT_A	Port A – allow power down and interrupt mode	
J13	PCOL_A		Jumpered
J92	3V3	Remove jumper and connect 3.3 V to power externally, use J13 ground pins	

8.2.4 Ping Test

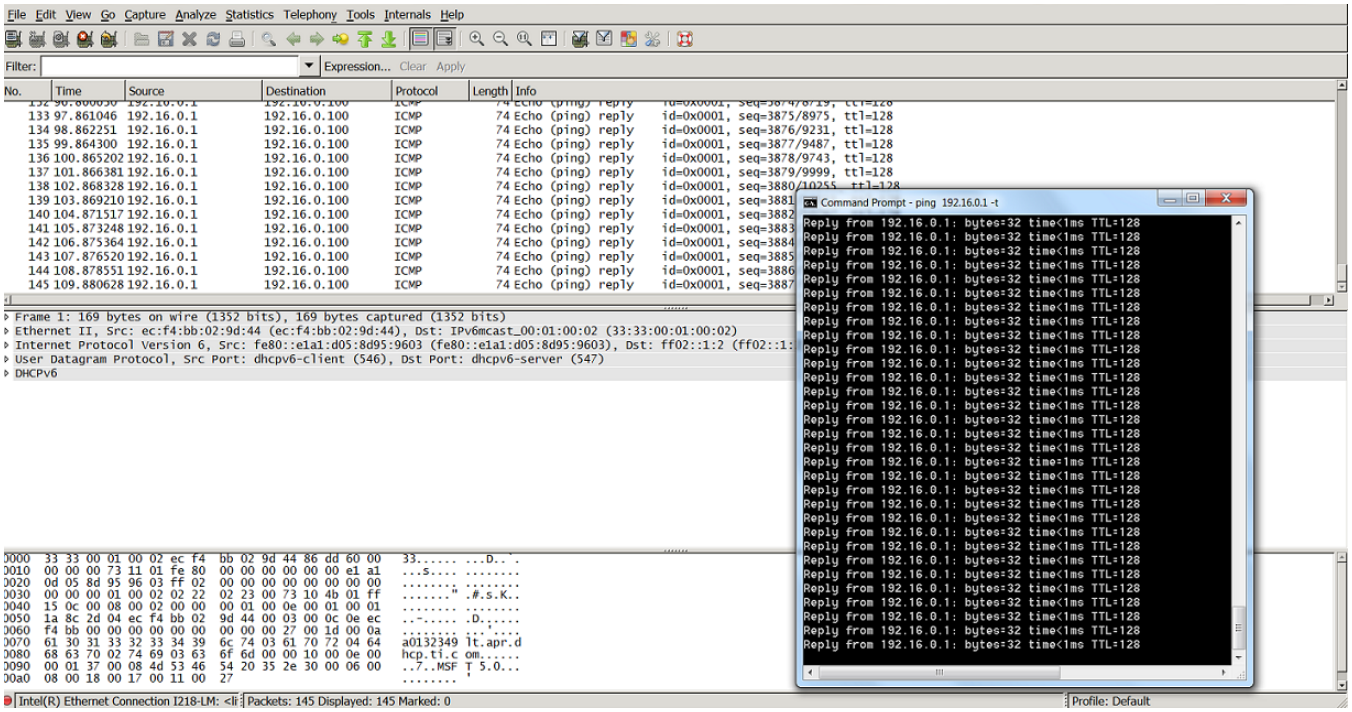

Figure 21. Ping Test

8.2.5 Webserver Interface

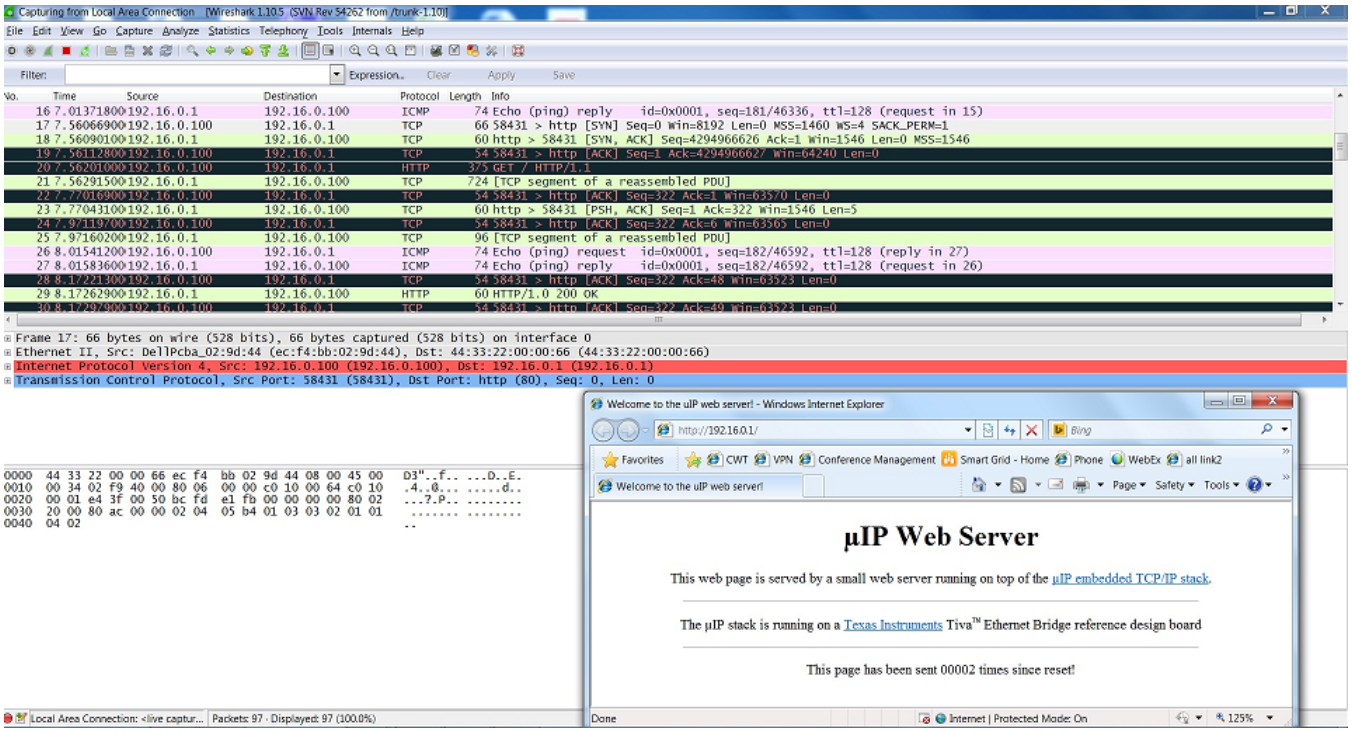

Figure 22. Webserver Interface

8.3 ESD

Table 13. ESD

DISCHARGE TYPE	LEVELS	CRITERIA	RESULTS
Contact	7 kV	Criteria B	Pass
Air discharge	10 kV	Criteria B	Pass

8.4 ESD, EMI, and EMC Recommendations and Design Guidelines

The following recommendations are provided to improve EMI performance:

- Series resistors on all MII signals
- Guard ring for crystal

There are two design cases in which immunity to ESD damage is important.

- The first case is during handling of the transceiver prior to mounting it on the circuit board. Use normal ESD handling precautions for ESD sensitive devices. These precautions include using grounded wrist straps, work benches, and floor mats in ESD controlled areas.
- The second case to consider is static discharges to the exterior of the equipment chassis containing the transceiver parts. To the extent that the duplex SC connector is exposed to the outside of the equipment chassis, the exterior may be subject to whatever ESD system-level test criteria that the equipment is intended to meet.
- Ensure the power supply tracks are >12 ml to carry the FO-Transceiver current.

9 Design Files

9.1 Schematics

To download the Schematics, see the design files at TIDA-00224.

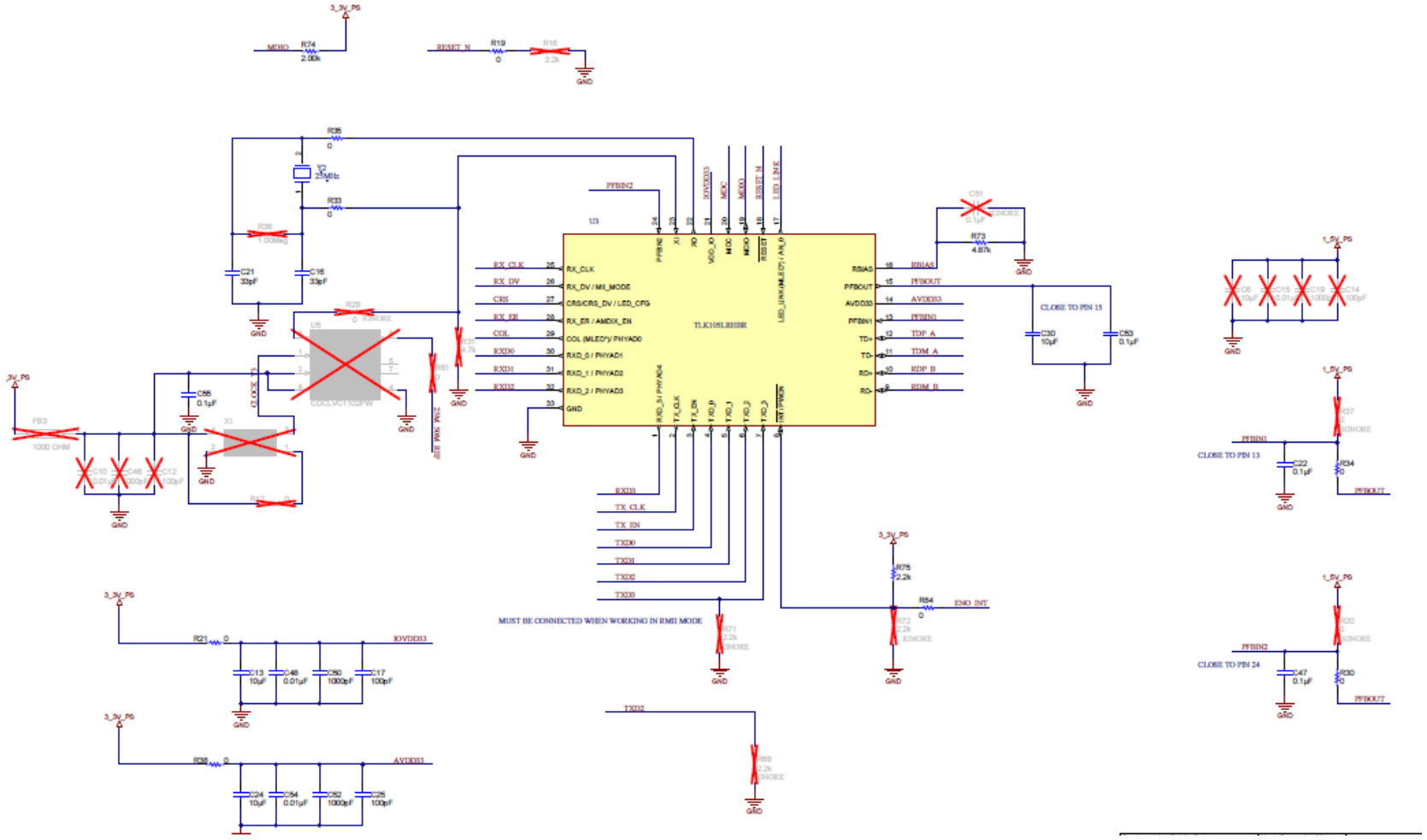

Figure 23. Schematics Page 3

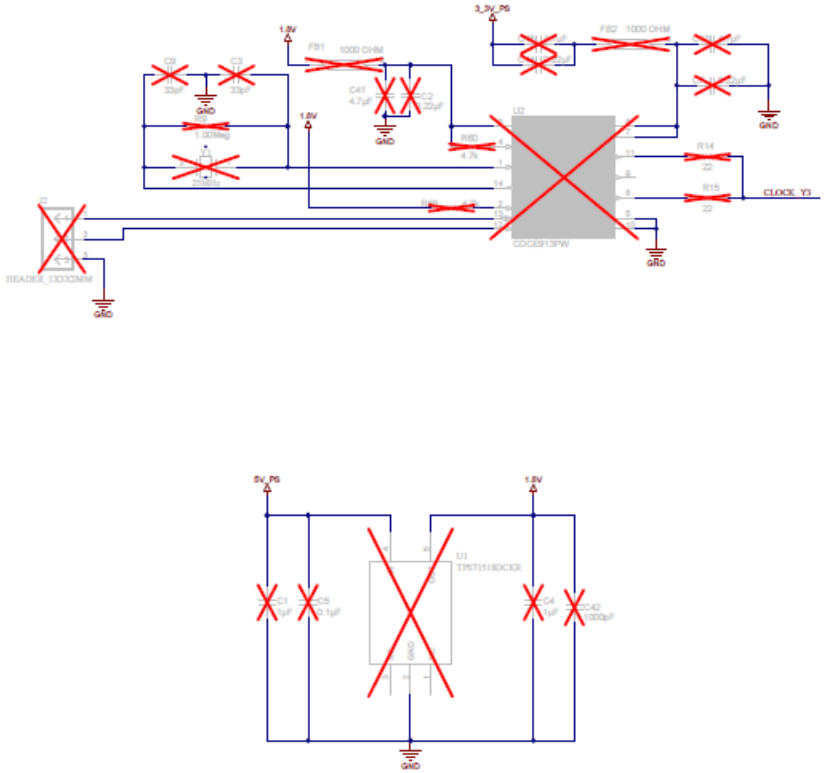

Figure 24. Schematics Page 4

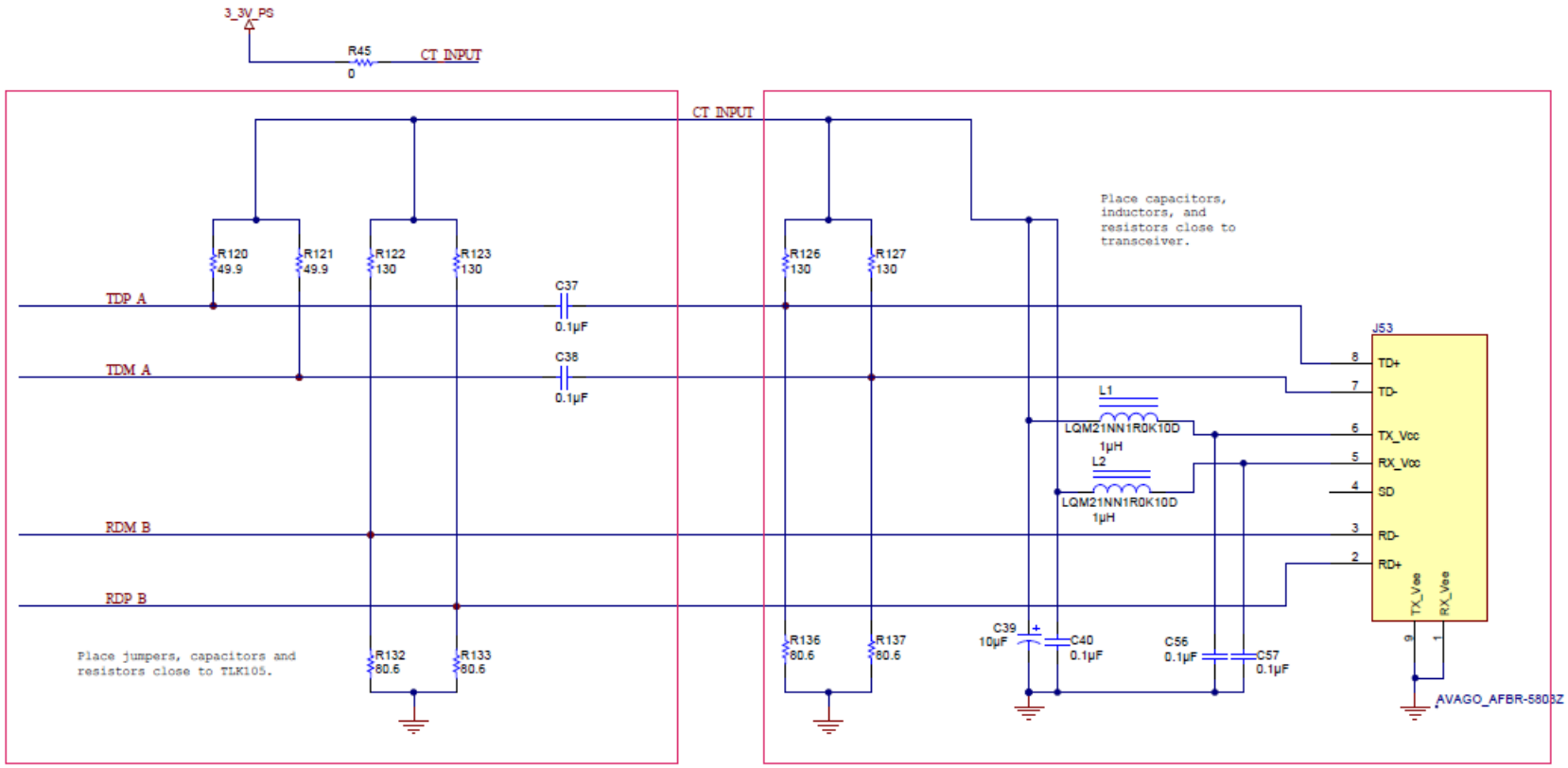

Figure 25. Schematics Page 5

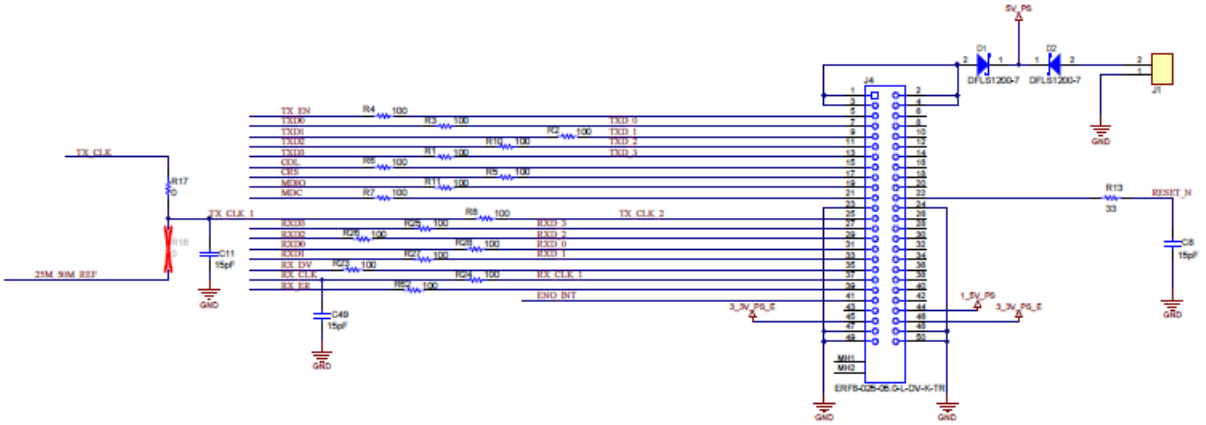

Figure 26. Schematics Page 6

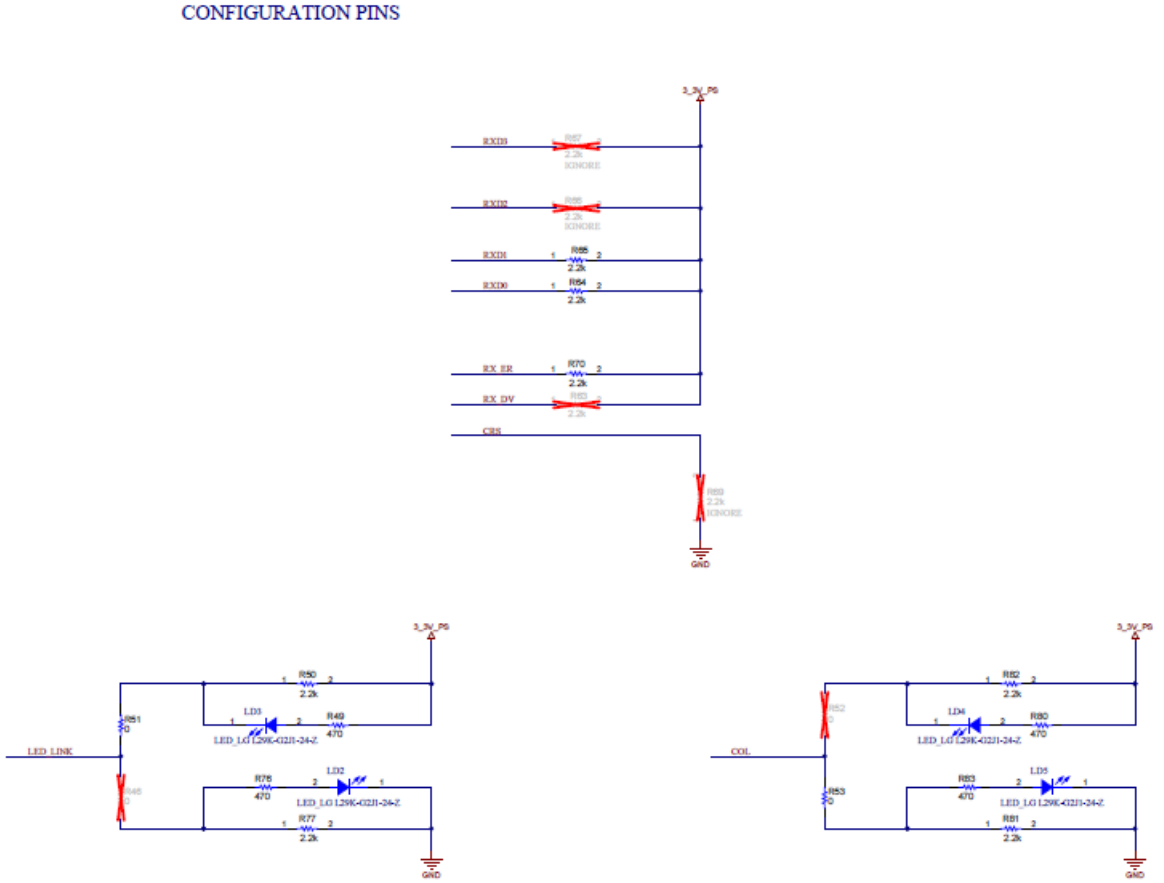

Figure 27. Schematics Page 7

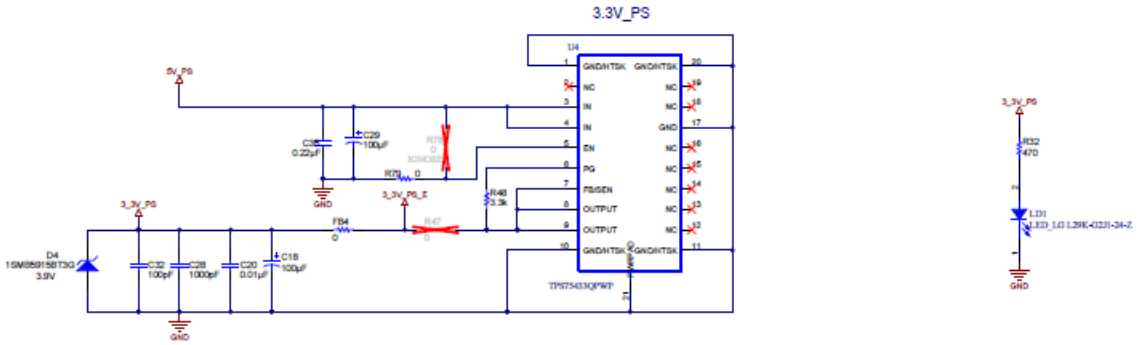

Figure 28. Schematics Page 8

9.2 Bill of Materials

To download the Bill of Materials, see the design files at TIDA-00224.

Table 14. BOM

ITEM	FITTED/NOT FITTED	QTY	REFERENCE	PART DESCRIPTION	MANUFACTURER	MANUFACTURER PART NUMBER
1	Not Fitted	3	C1, C4	CAP CER 1UF 16V 10% X5R 1206	Murata Electronics	GRM31MR61C105KA0
2	Not Fitted	1	C2, C7, C44	CAP CER 0.22UF 6.3V 10% X7R 0603	Kemet	C0603C224K9RACTU
3	Not Fitted	9	C3, C9	CAP, CERM, 33pF, 50V, +/-5%, C0G/NP0, 0603	AVX	06035A330JAT2A
	Not Fitted		C5	CAP, CERM, 0.1uF, 16V, +80/-20%, Y5V, 0603	Kemet	C0603C104Z4VACTU
4	Not Fitted	1	C6	CAP, CERM, 10uF, 35V, +/-10%, X7R, 1206	Taiyo Yuden	GMK316AB7106KL
5	Fitted	1	C8, C11, C49	CAP CER 15PF 50V 5% NP0 0402	TDK Corporation	C1005C0G1H150J050BA
6	Not Fitted	1	C10, C15	CAP, CERM, 0.01uF, 50V, +/-10%, C0G/NP0, 0402	MuRata	GCM155R71H103KA55D
7	Not Fitted	1	C12, C14	CAP, CERM, 100pF, 50V, +/-10%, X7R, 0402	Yageo America	CC0402KRX7R9BB101
8	Fitted	1	C13, C24	CAP, CERM, 10uF, 35V, +/-10%, X7R, 1206	Taiyo Yuden	GMK316AB7106KL
9	Fitted	1	C16, C21	CAP, CERM, 33pF, 50V, +/-5%, C0G/NP0, 0603	AVX	06035A330JAT2A
10	Fitted	1	C17, C25, C32	CAP, CERM, 100pF, 50V, +/-10%, X7R, 0402	Yageo America	CC0402KRX7R9BB101
11	Fitted	1	C18, C29	CAP, TA, 100uF, 10V, +/-20%, 0.6 ohm, SMD	Vishay-Sprague	293D107X0010D2TE3
12	Not Fitted	1	C19, C42, C46	CAP, CERM, 1000pF, 25V, +/-10%, X5R, 0402	MuRata	GRM155R61E102KA01D
13	Fitted	3	C20, C48, C54	CAP, CERM, 0.01uF, 50V, +/-10%, C0G/NP0, 0402	MuRata	GCM155R71H103KA55D
14	Fitted	3	C22, C47, C53, C55	CAP, CERM, 0.1uF, 16V, +/-10%, X7R, 0603	Kemet	C0603C104K4RACTU
15	Fitted	3	C28, C50, C52	CAP, CERM, 1000pF, 25V, +/-10%, X5R, 0402	MuRata	GRM155R61E102KA01D
16	Fitted	3	C30	CAP, CERM, 10uF, 10V, +/-10%, X5R, 1210	Kemet	C1210C106K8PACTU
17	Fitted	1	C35	CAP, CERM, 0.22uF, 16V, +/-10%, X7R, 0603	MuRata	GRM188R71C224KA01D
18	Fitted	3	C37, C38, C40, C56, C57	CAP, CERM, 0.1uF, 50V, +/-10%, X7R, 0603	AVX	06035C104KAT2A
19	Fitted	3	C39	CAP, TA, 10uF, 16V, +/-20%, 2 ohm, SMD	Vishay-Sprague	293D106X0016B2TE3
20	Not Fitted	2	C41, C43, C45	CAP, CERM, 4.7uF, 6.3V, +/-10%, X5R, 0603	Kemet	C0603C475K9PACTU
21	Not Fitted	3	C51	CAP, CERM, 0.1uF, 16V, +/-10%, X7R, 0603	Kemet	C0603C104K4RACTU
22	Fitted	1	D1, D2	Diode, Schottky, 200V, 1A, PowerDI123	Diodes Inc.	DFLS1200-7
26	Fitted	3	D4	Diode, Zener, 3.9V, 550mW, SMB	ON Semiconductor	1SMB5915BT3G
27	Not Fitted	3	FB1, FB2, FB3	FERRITE CHIP 1000 OHM 300MA 0603	TDK Corporation	MMZ1608B102C

Table 14. BOM (continued)

ITEM	FITTED/NOT FITTED	QTY	REFERENCE	PART DESCRIPTION	MANUFACTURER	MANUFACTURER PART NUMBER
28	Fitted	2	FB4, R17, R19, R33, R35, R45, R51, R53, R79, R84	RES, 0 ohm, 5%, 0.1W, 0603	Vishay-Dale	CRCW06030000Z0EA
30	Fitted	1	J1	CONN TERM BLOCK 2.54MM 2POS PCB	On Shore Technology Inc	OSTVN02A150
31	Not Fitted	1	J2	CONN HEADER 3POS 2MM VERT T/H	3M	951103-8622-AR
32	Fitted	2	J4	Receptacle, 0.8mm, 25x2, SMT	Samtec	ERF8-025-05.0-L-DV-K-TR
33	Fitted	1	J53	FDDI, 100 Mb/s ATM, and Fast Ethernet Transceivers	AVAGO	516-1991-ND
34	Fitted	3	L1, L2	INDUCTOR 1.0UH 50MA 0805	Murata Electronics	LQM21NN1R0K10D
35	Fitted	2	LD1, LD2, LD3, LD4, LD5	LED SmartLED Green 570NM	OSRAM	LG L29K-G2J1-24-Z
36	Fitted	9	R1, R2, R3, R4, R5, R6, R7, R8, R10, R11, R23, R24, R25, R26, R27, R28, R62	RES, 100 ohm, 5%, 0.063W, 0402	Vishay-Dale	CRCW0402100RJNED
37	Not Fitted	2	R9, R36	RES, 1.00Meg ohm, 1%, 0.063W, 0402	Vishay-Dale	CRCW04021M00FKED
38	Not Fitted	3	R12, R18, R29, R46, R47, R52, R61, R78	RES, 0 ohm, 5%, 0.1W, 0603	Vishay-Dale	CRCW06030000Z0EA
39	Fitted	3	R13	RES, 33 ohm, 5%, 0.063W, 0402	Vishay-Dale	CRCW040233R0JNED
42	Not Fitted	21	R14, R15	RES, 22 ohm, 5%, 0.063W, 0402	Vishay-Dale	CRCW040222R0JNED
43	Not Fitted	2	R16, R63, R66, R67, R68, R69, R71, R72	RES, 2.2k ohm, 5%, 0.063W, 0402	Vishay-Dale	CRCW04022K20JNED
44	Not Fitted	1	R20, R37	RES, 0 ohm, 5%, 0.125W, 0805	Yageo America	RC0805JR-070RL
45	Fitted	7	R21, R30, R34, R38	RES, 0 ohm, 5%, 0.125W, 0805	Yageo America	RC0805JR-070RL
46	Not Fitted		R31, R59, R60	RES, 4.7k ohm, 5%, 0.1W, 0603	Yageo America	RC0603JR-074K7L
	Fitted	2	R32, R49, R76, R80, R83	RES, 470 ohm, 1%, 0.1W, 0603	Yageo America	RC0603FR-07470RL
47	Fitted	6	R48	RES, 3.3k ohm, 5%, 0.063W, 0402	Vishay-Dale	CRCW04023K30JNED
	Fitted	1	R50, R64, R65, R70, R75, R77, R81, R82	RES, 2.2k ohm, 5%, 0.063W, 0402	Vishay-Dale	CRCW04022K20JNED
49	Fitted	1	R73	RES, 4.87k ohm, 1%, 0.1W, 0603	Vishay-Dale	CRCW06034K87FKEA

Table 14. BOM (continued)

ITEM	FITTED/NOT FITTED	QTY	REFERENCE	PART DESCRIPTION	MANUFACTURER	MANUFACTURER PART NUMBER
50	Fitted	1	R74	RES, 2.00k ohm, 1%, 0.063W, 0402	Vishay-Dale	CRCW04022K00FKED
51	Fitted	4	R120, R121	RES 49.9 OHM 1/10W 1% 0603 SMD	Yageo	RC0603FR-0749R9L
52	Fitted	1	R122, R123, R126, R127	RES, 130 ohm, 1%, 0.1W, 0603	Yageo America	RC0603FR-07130RL
53	Fitted	2	R132, R133, R136, R137	RES, 80.6 ohm, 1%, 0.1W, 0603	Vishay-Dale	CRCW060380R6FKEA
54	Not Fitted	2	U1	IC REG LDO 1.8V 50MA SC70-5	TI	TPS71518DCKR
55	Not Fitted	3	U2	Programmable 1-PLL VCXO Clock Synthesizer With 1.8-V, 2.5-V, and 3.3-V Outputs, PW0014A	Texas Instruments	CDCE913PW
56	Fitted	3	U3	IC, INDUSTRIAL TEMP, SINGLE PORT 10/100Mbs ETHERNET PHYSICAL LAYER TRANSCEIVER, VQFN-32P	Texas Instruments	TLK105LRHBR
57	Fitted	3	U4	IC, Low Dropout Voltage Regulator, 3.3 V, 2.0 A	Texas Instruments	TPS75433QPWP
58	Not Fitted	2	U5	3.3 V and 2.5 V LVCMOS High-Performance Clock Buffer Family, PW0008A	Texas Instruments	CDCLVC1102PW
59	Not Fitted	2	X1	OSC 25.00 MHZ 3.3V HIGH STAB SMD	EPSON	HG-2150CA 25.000M-BXC3
61	Not Fitted	1	Y1	CRYSTAL 25.0MHZ 18PF SMD	CTS-Frequency Controls	445I23D25M00000
64	Fitted	1	Y2	CRYSTAL 25.0MHZ 18PF SMD	CTS-Frequency Controls	445I23D25M00000

NOTE: CABLE FIBER OPTIC DUAL SC-SC 5M, Part Number DK-2622-05 (Digikey - AE10442-ND) is not listed in the BOM, but can used for testing. This is the orange fiber-optic cable pictured in Figure 18 that was used to connect the TI Design brick and the test board.

9.3 Layer Plots

To download the layer plots, see the design files at TIDA-00224.

NOTE: All artwork for the Layer Plots is viewed from the top side.

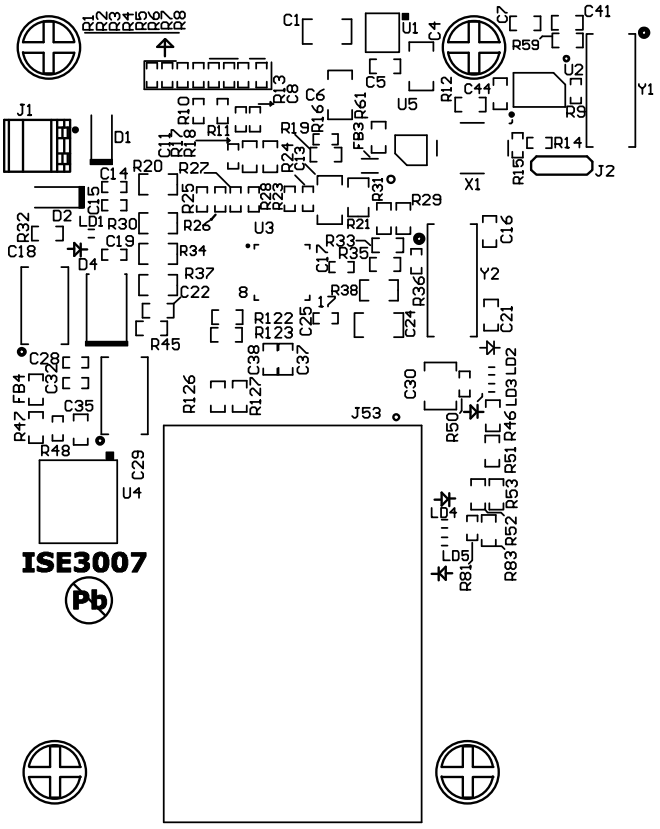

Figure 29. Top Overlay

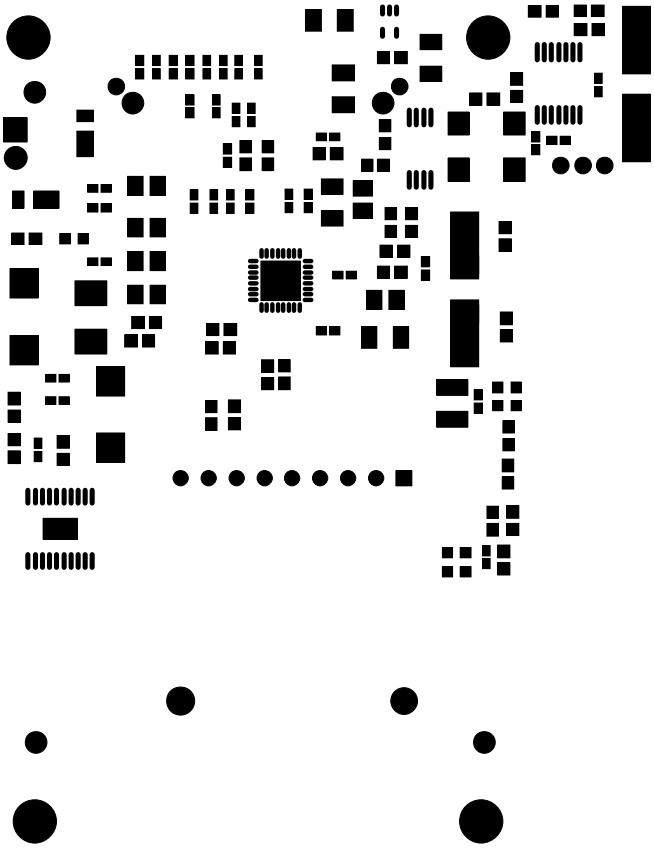

Figure 30. Solder Mask Top

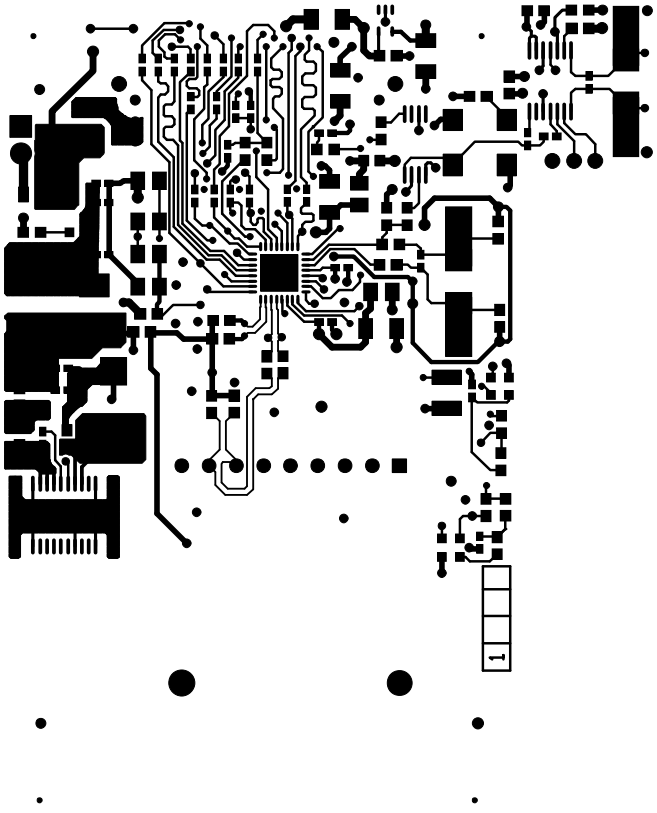

Figure 31. Top Layer

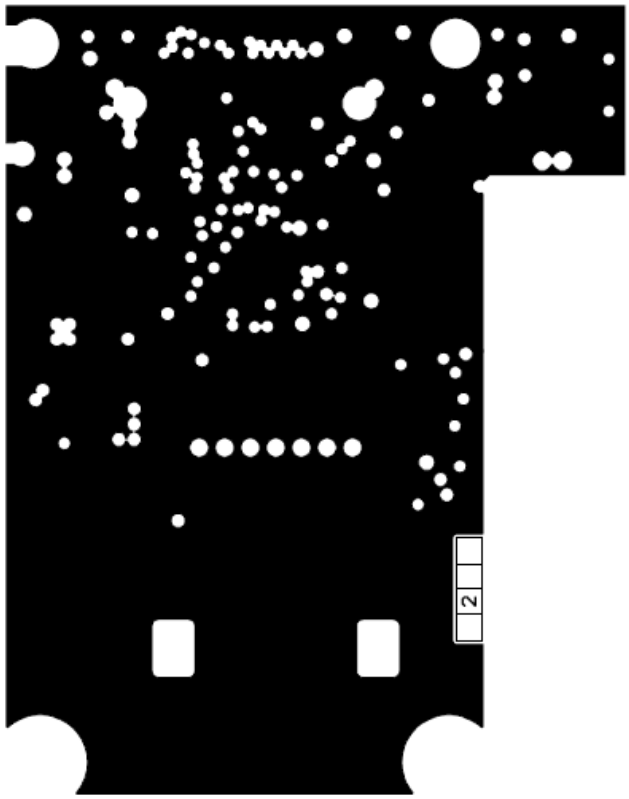

Figure 32. L2, P1

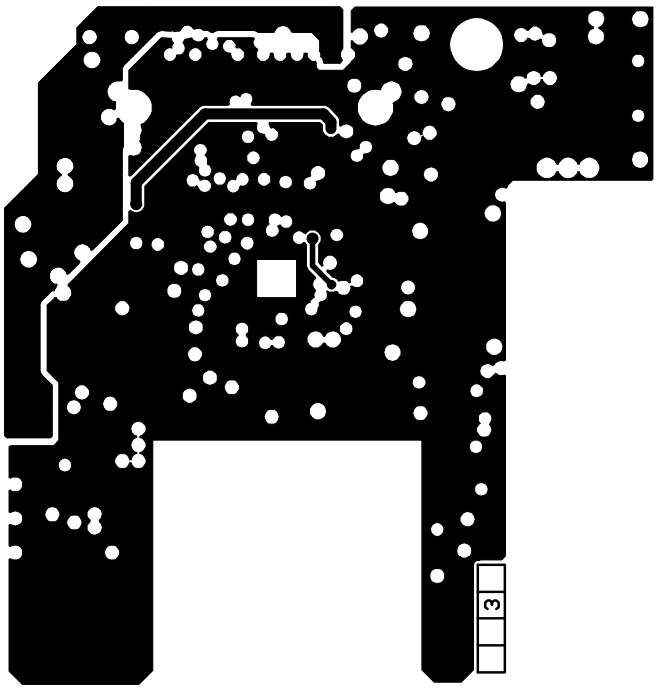

Figure 33. L3_P2

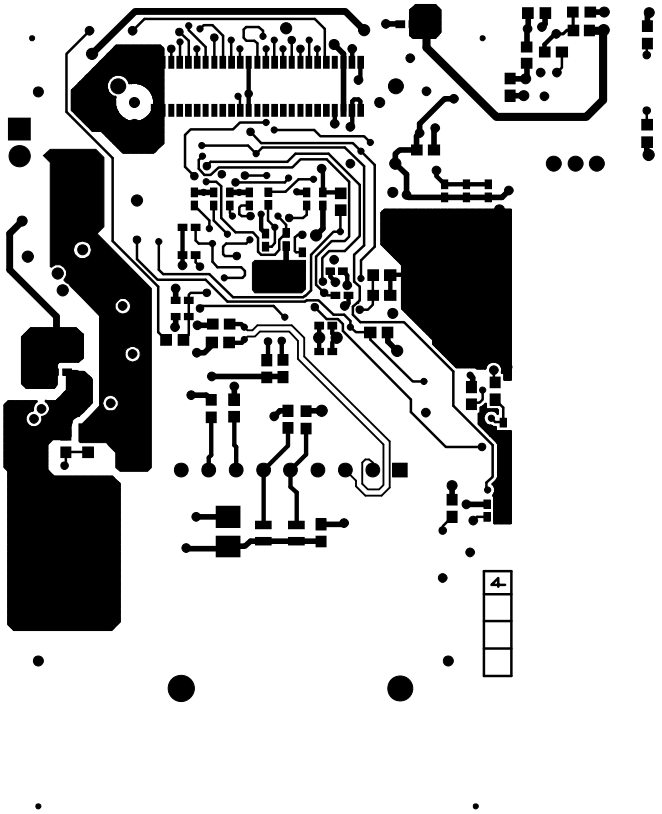

Figure 34. Bottom Layer

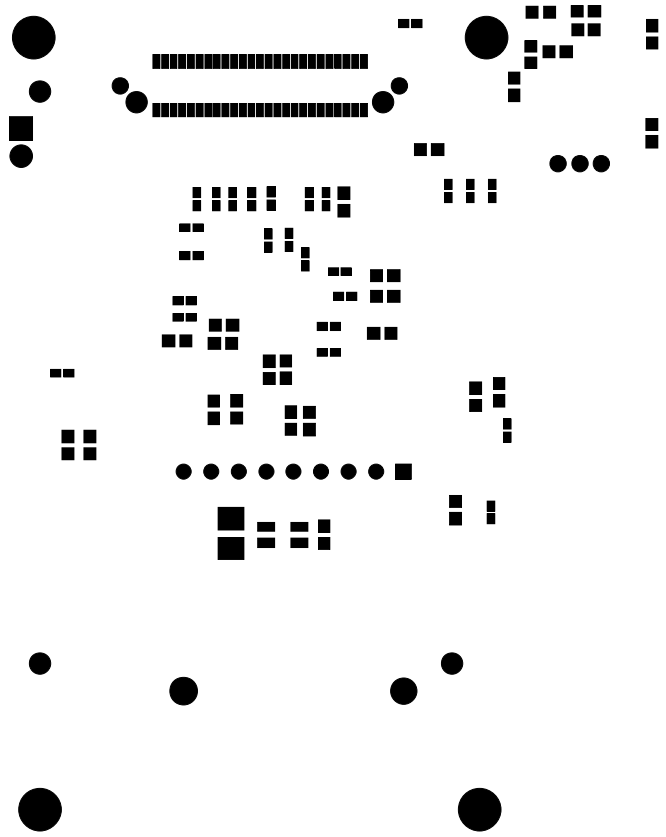

Figure 35. Solder Mask Bottom

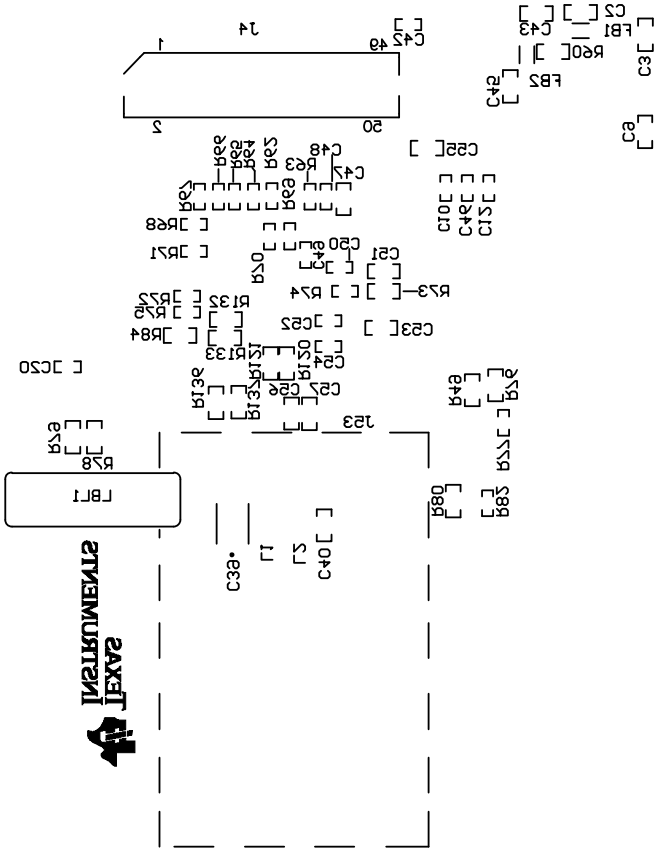

Figure 36. Bottom Overlay

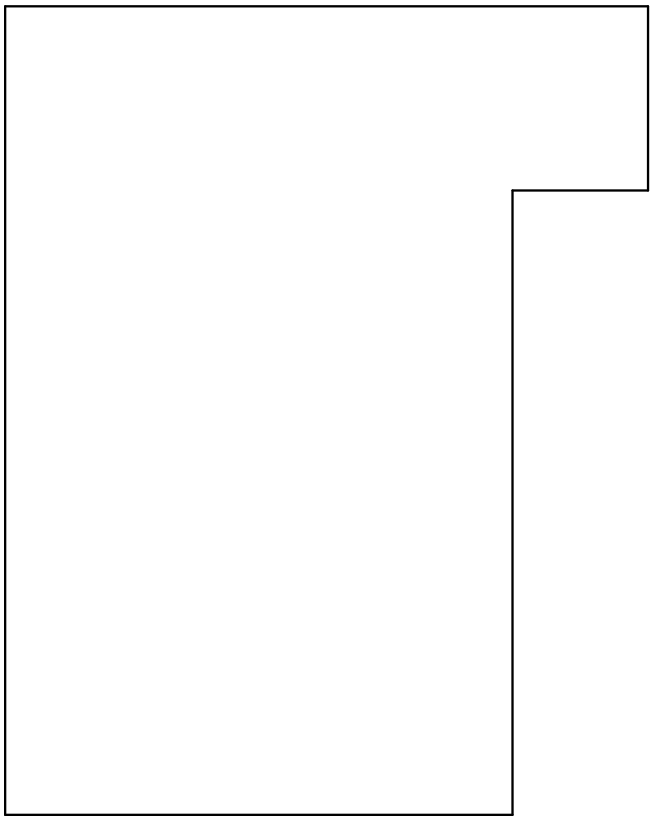

Figure 37. M1 Board Outline

9.4 Altium Project Files

To download the Altium project files, see the design files at TIDA-00224.

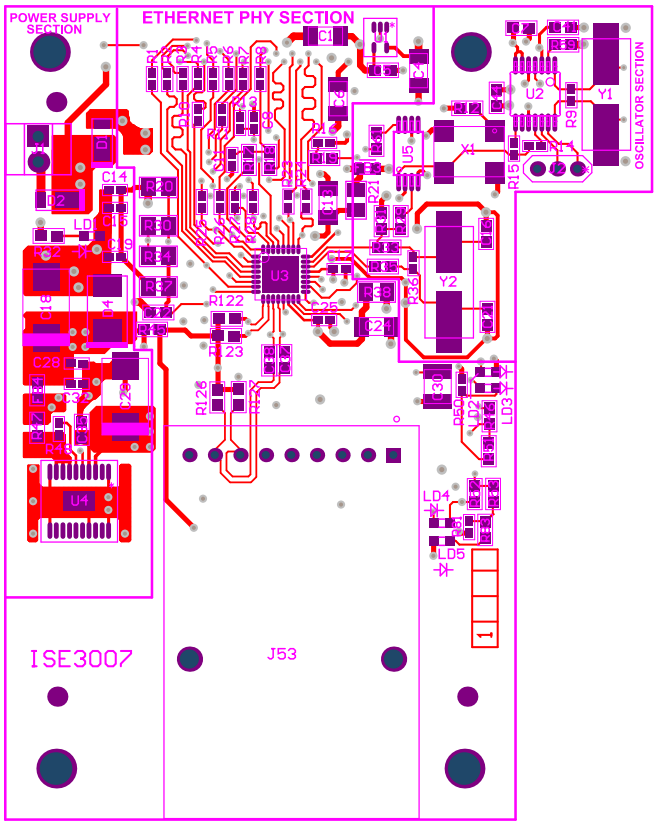

Figure 38. Multilayer Composite Print 1 - Top

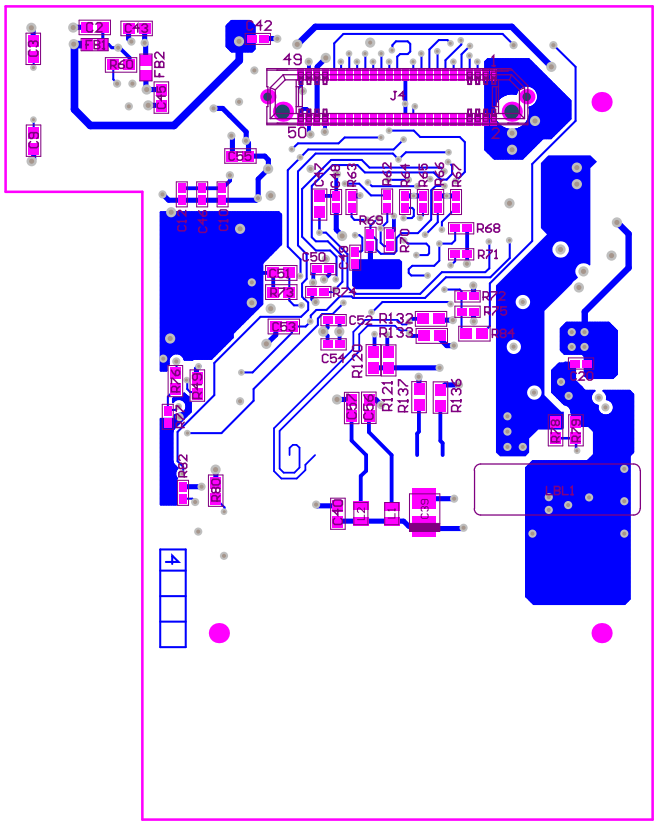

Figure 39. Multilayer Composite Print 2 - Bottom

9.5 Gerber Files

To download the Gerber files, see the design files at TIDA-00224.

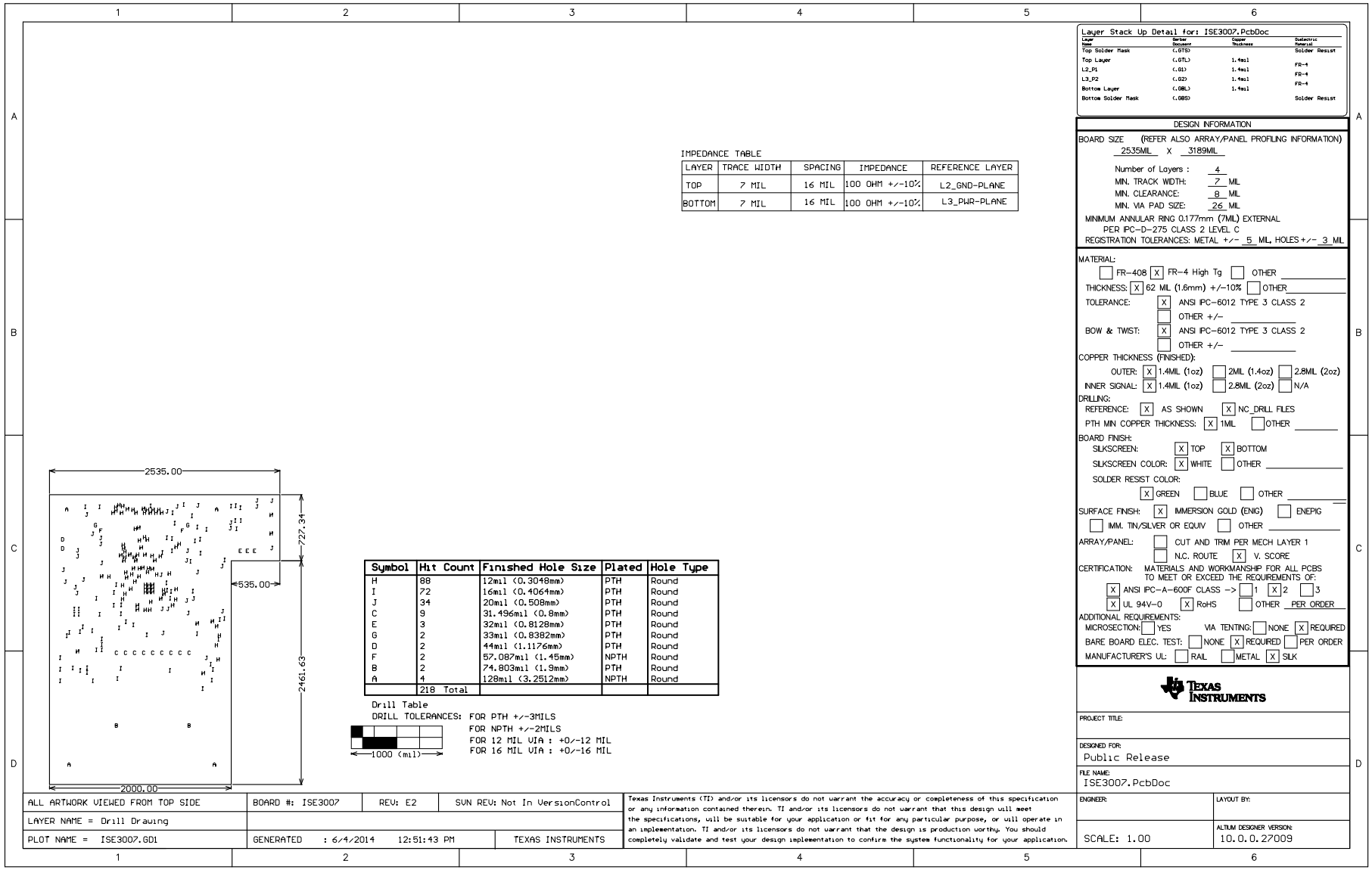

Figure 40. Fabrication Drawing

9.6 Assembly Drawings

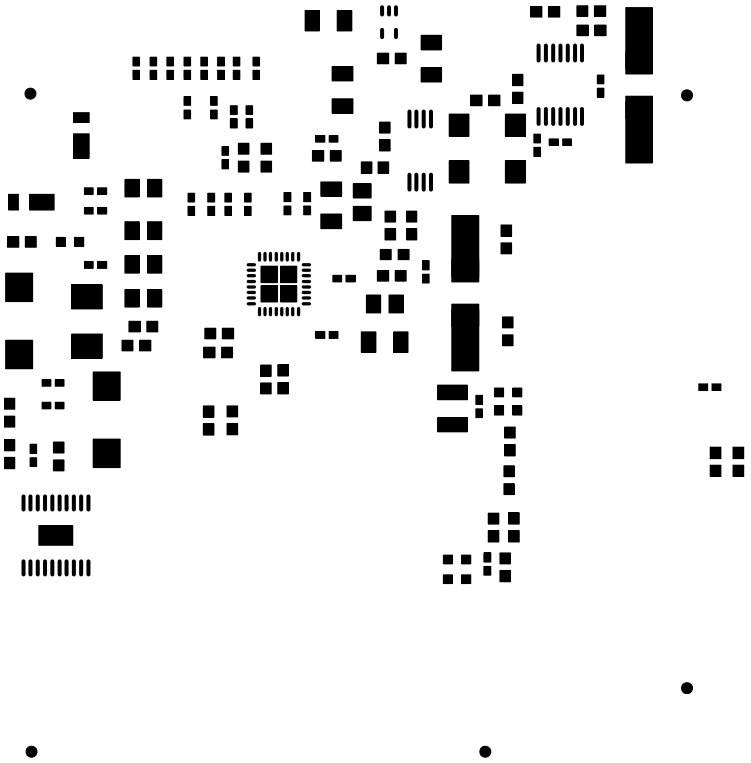

Figure 41. Top Paste

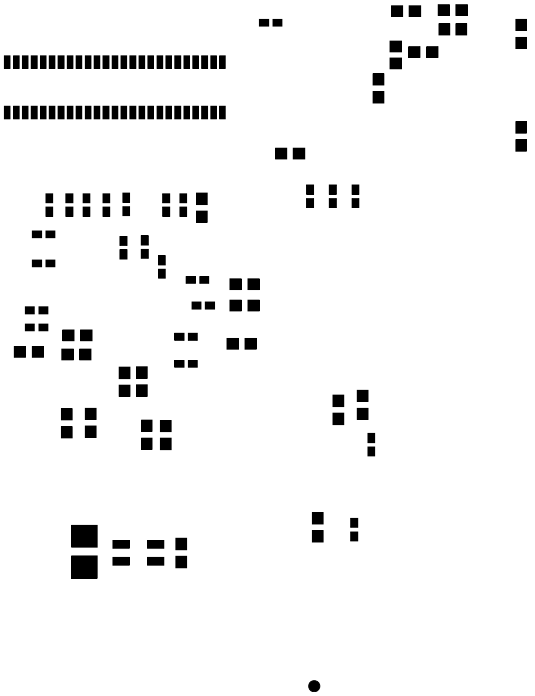

Figure 42. Bottom Paste

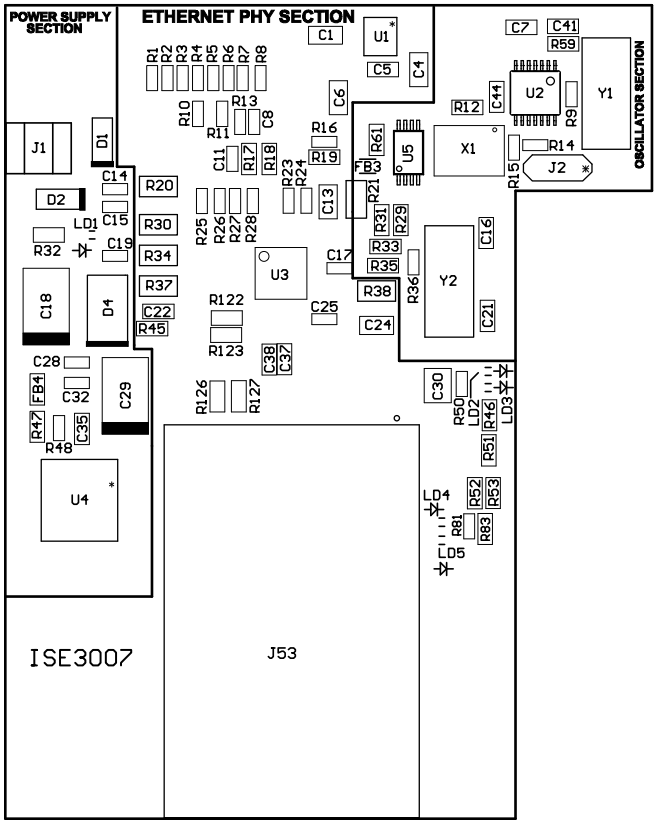

Figure 43. Assembly Top

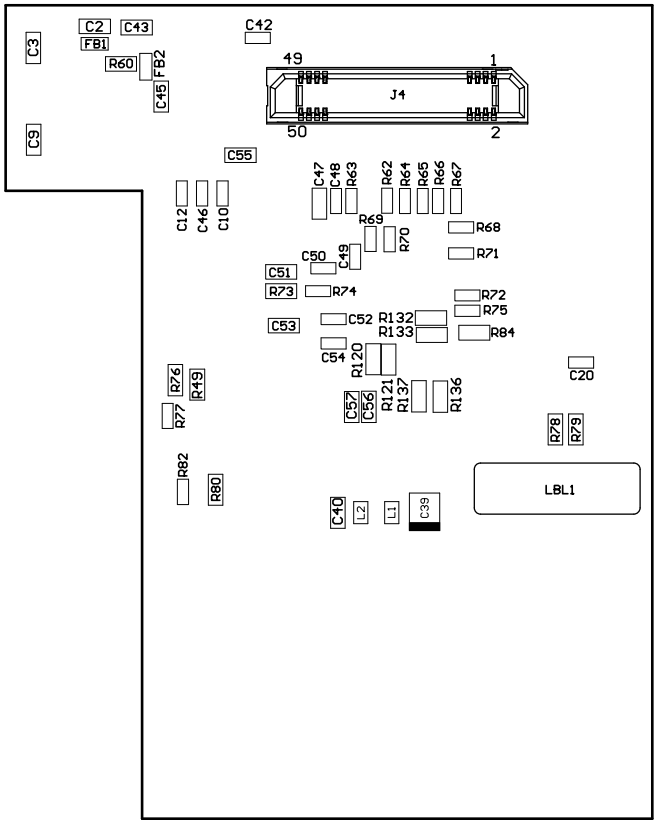

Figure 44. Assembly Bottom

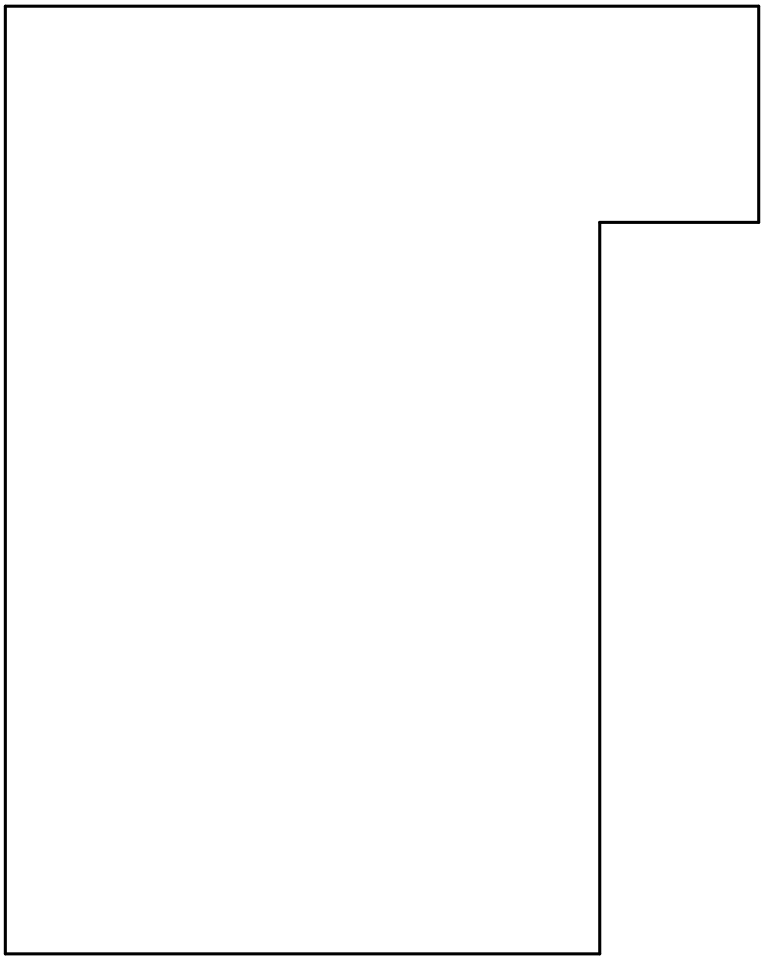

Figure 45. M1 Board Outline

9.7 Software Files

To download the software files, see the design files at TIDA-00224.

10 References

1. *TLK1XX Design and Layout Guide*, TLK1XX Application Report SLVA531
2. *TLK105/6L Customer EVM*, TLK105/6L User's Guide SLLU185
3. *Industrial Temp, Single Port 10/100Mbs Ethernet Physical Layer Transceiver*, TLK105L/6L Data Sheet SLLSEE3
4. *AFBR-5803Z/5803TZ/5803AZ/5803ATZ FDDI, 100 Mb/s ATM, and Fast Ethernet Transceivers*, AFBR-5803Z/5803TZ/5803AZ/5803ATZ Data Sheet AFBR-5803Z/5803TZ/5803AZ/5803ATZ
5. *AN-1509 PhyterDual Flexible Port Switching*, DP-Media-Converter Application Report SNLA086

11 About the Author

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