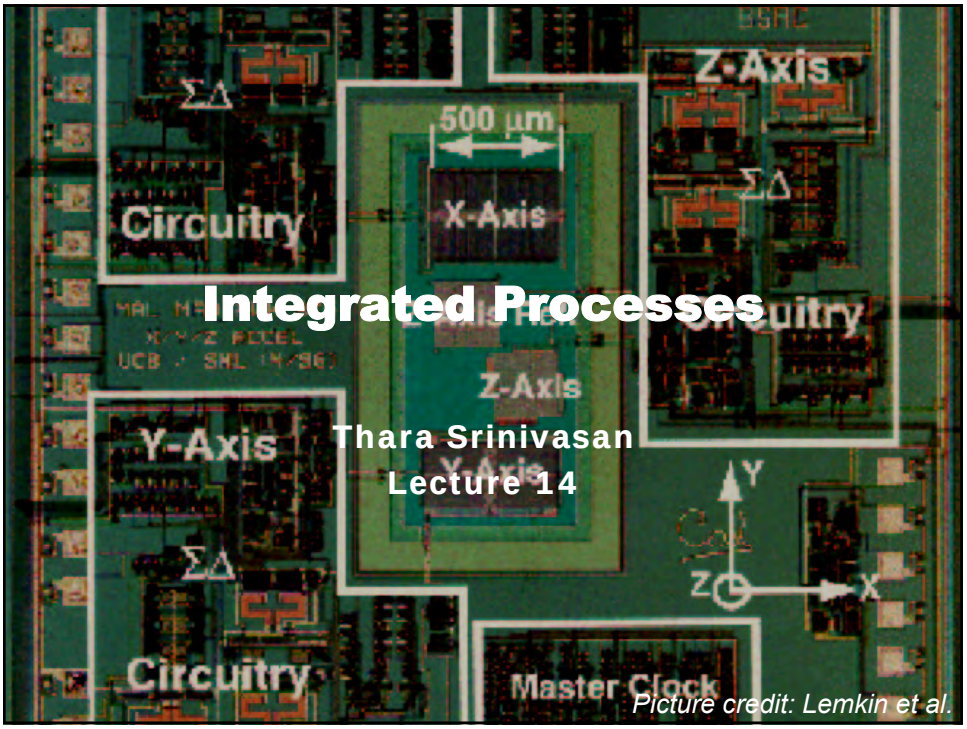
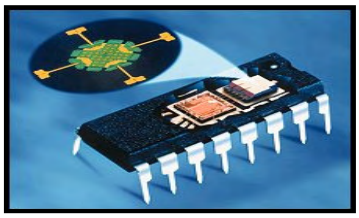


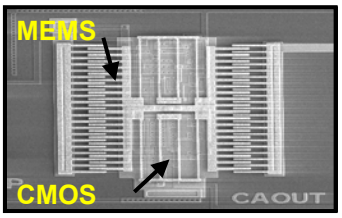

## Lecture Outline

- From reader
  - Bustillo, J. *et al*., "Surface micromachining of MEMS," pp. 1556-9.
  - A.E. Franke *et al*., "Polycrystalline silicon germanium films for integrated microsystems," 160-71.
  - T. J. Brosnihan *et al*., "A Fabrication Process for MEMS Optical Switches with Integrated On-Chip Electronics," pp. 1638-42.
  - C. Bellew, *et al.,* "An SOI Process for Fabrication of …" pp. 1075-9.
- Today's Lecture
  - Hurdles and benefits of process integration
  - Modular processes
    - CMOS before MEMS
    - MEMS before CMOS
  - Interleaved processes
  - MEMS by foundry CMOS

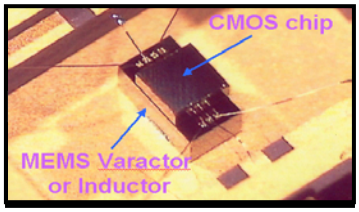
# Types of Integration



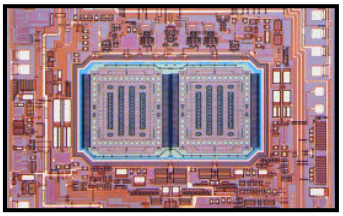
Motorola




Berkeley




Intel



Analog Devices



# Integrated Monolithic MEMS

- Motivation for co-fabrication
  - Improved device performance, higher signal-to-noise ratio
  - Reduced size, power requirement
  - IC compatibility = economical manufacturing
  - Automatic alignment; packaging combined

| | CMOS | Surface Micromachining |
|---|---|---|
| Common features | Si-based, same materials and etching principles | |
| Process Flow | Standard | Application specific |
| Vertical Dimension | ~1 μm | ~1-5 μm |
| Lateral Dimension | <1 μm | 2-10 μm |
| Complexity | >10 masks | 2-6 masks |

*Yun*

# Thermal Budget

- Critical temperatures for Al metallization
  - Degradation at T > 400-450°C
  - Junction migration at T = 950°C
  - Junction spiking
- Critical process temperatures for MEMS

| | Temperature | Material |
|---|---|---|
| LPCVD | 450°C | LTO/PSG |
| | 610 | Low stress polySi |
| | 650 | Doped polySi |
| | 800 | Nitride |
| Annealing | 950 | PSG densification |
| | 1050 | PolySi stress annealing |

*W. Yun, PhD Thesis, BSAC* 5

# Benefits and Hurdles

- Benefits to integration
  - Lower parasitic capacitance and parasitic resistance, greater sensitivity
  - Increased reliability, reduced size and package complexity
- Challenges to integration
  - MEMS layer deposition and anneal temperatures
  - Passivation of CMOS during MEMS etching and release steps
  - Surface topography of MEMS
  - Materials incompatibilities
  - Yield losses multiplied
  - Special purpose electronics may be needed

# This Lecture

- Modular processes
  - CMOS before MEMS
    - UC Berkeley Modular Integration
    - UCB polysilicon germanium
    - SOI MEMS, UCB and Analog Devices
  - MEMS before CMOS
    - Sandia Labs MM/CMOS
- Interleaved CMOS and MEMS
  - Analog Devices BiMEMS
  - Bosch epipoly
- MEMS by CMOS foundry
  - Parameswaran *et al.,* University of Alberta, 1988
  - Fedder *et al*., Carnegie Mellon, 1996

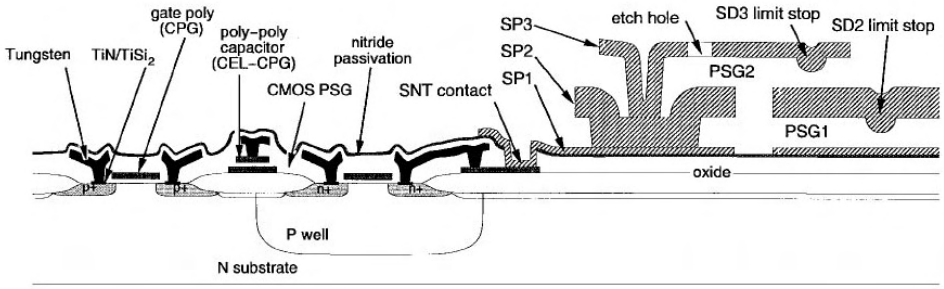


# Modular Processes

- CMOS before MEMS
  - \+ IC foundry can be used
  - \+ Chip area may be minimized
  - – Thermal budget is an issue
- MEMS before CMOS
  - \+ No thermal budget for MEMS
  - – Microstructure topography is an issue
  - – Electronics and MEMS cannot be easily stacked
  - – IC foundries are wary of pre-processed wafers (materials constraints)

# UCB Process

- Refractory metallization (e.g. tungsten), makes possible high-temperature post-processing
- Double-poly, single-metal CMOS, passivated with PSG
- Low-stress nitride for protection from release etch
- MEMS-CMOS interconnect: MEMS ground plane doped poly to CMOS gate poly



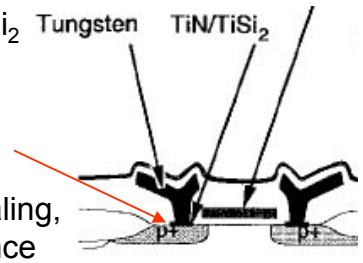

*Yun et al.*





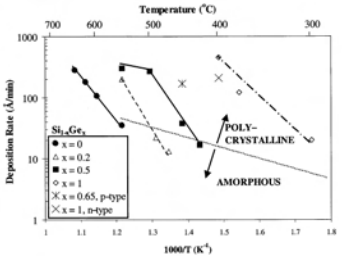
# UCB Process

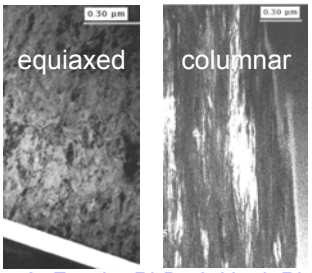
- Issues
  - Tungsten, W, reacts with Si at 600°C to form $WSi_2$ → diffusion barrier is needed; e.g. TiN/$TiSi_2$
- Problems
  - W forms hillocks during annealing, relatively high contact resistance
  - Mainstream CMOS processes are optimized for Al (now Cu)
  - Heavily doped MEMS layers can affect CMOS

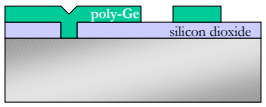


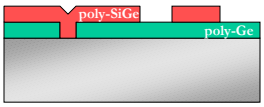
# Polysilicon Germanium

- Poly-$Si_{1-x}Ge_x$
  - Low temperature, Low resistivity with doping
  - n-type poly-Ge structural; $SiO_2$ sacrificial
  - p-type poly-$Si_{0.35}Ge_{0.65}$ structural; poly-Ge sacrificial
- Deposition
  - LPCVD thermal decomposition of $GeH_4$ and $SiH_4$ or $Si_2H_6$
  - Rate >50 Å/min, T < 475°C, P = 300-600 mT
  - At higher [Ge]: rate ↑, T ↓
  - *In-situ* doping, ion implantation




*A. Franke PhD, J. Heck PhD, Howe and King groups*





# Polysilicon Germanium

- Dry etching
  - Similar to poly-Si; F, Cl, and Br-containing plasmas
  - Rate ~ 0.4 μm/min
- Wet etching
  - $H_2O_2$, 90°C: 4 orders of magnitude selectivity between >80% and <60% Ge content.
  - Good release etchant

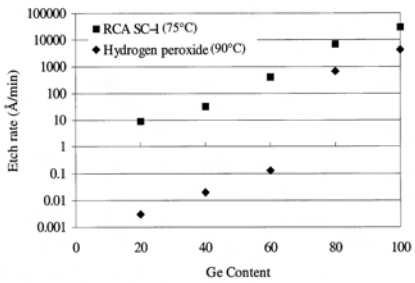
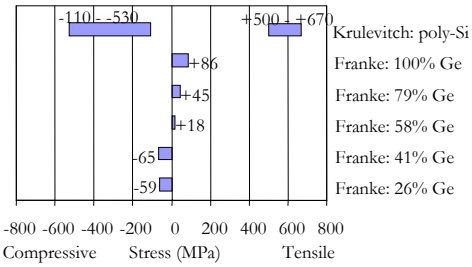


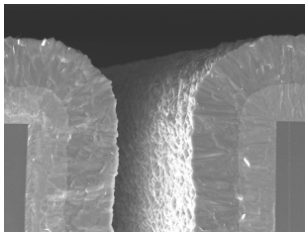

Fig. 2. Etch rate of poly-$Si_{1-x}Ge_x$ films in RCA SC-1, and hydrogen peroxide.

*J. Heck PhD thesis, Howe and King groups*

# Poly-SiGe Mechanical Properties

- Conformal deposition
- Low stress as-deposited
- Films have high roughness
- Young's modulus ~146 GPa (poly-$Si_{0.35}Ge_{0.65}$)
- Fracture strain 1.7% (compared to 1.5% for MUMPS polySi)
- Q = 30,000 for n-type poly-Ge in vacuum
- Poly-SiGe mechanically on par with poly-Si



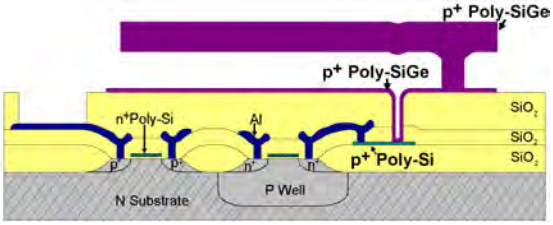
*Franke*

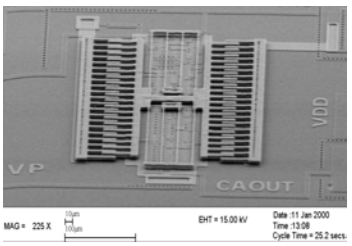




# UCB Poly-SiGe Process

- 3 µm standard CMOS process, Al metallization
- p-type poly-$Si_{0.35}Ge_{0.65}$ structural; poly-Ge sacrificial
- MEMS-CMOS interconnect through p-type poly-Si strap
- Process:
  - CMOS passivated with LTO, 400°C
  - Vias to connection strap opened
  - Ground plane deposited, MEMS built.
  - RTA anneal to lower resistivity (550°C, 30s)



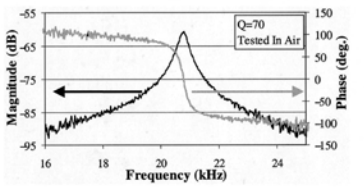




Fig. 18. Frequency response of the integrated poly-SiGe resonator and the CMOS amplifier tested in air.

*A. Franke PhD*

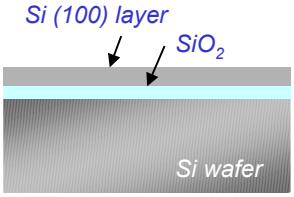
# Integrated SOI MEMS

- To increase resolution of inertial sensor
  - Reduce spring stiffness
  - Increase proof mass

$$F = ma$$

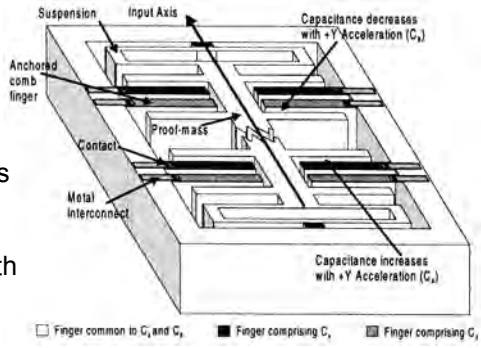
$$F = kx$$

$$x = \left(\frac{m}{k}\right)a$$




Silicon-on-Insulator wafer

- Silicon-on-insulator integrated process
  - MEMS 25× thicker than with poly surface micromachining
  - SCS MEMS: zero stress and stress gradient
  - Integration of high sensitivity structures with circuitry gives 5-25× better resolution



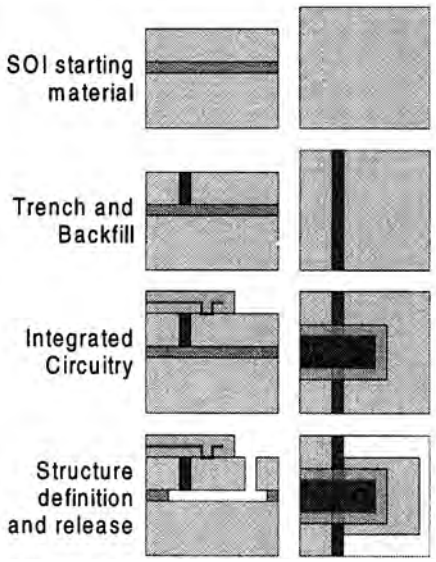

M. Lemkin, PhD, BSAC
Integrated Micro Instruments





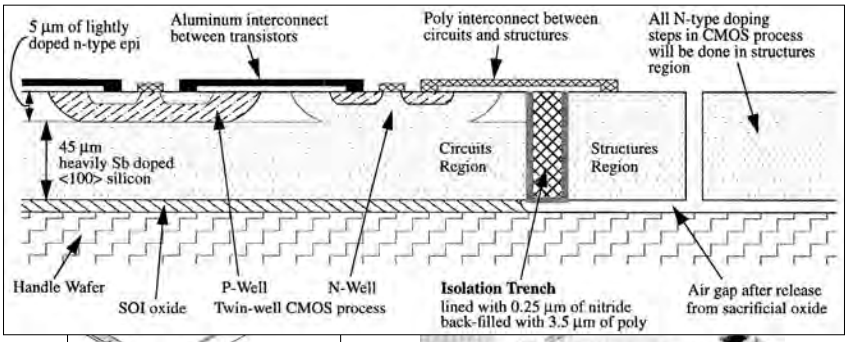
# SOI MEMS Process

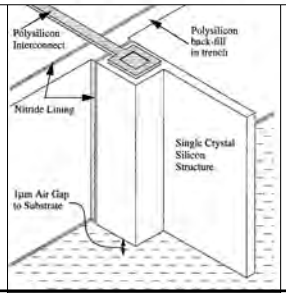
- Trench (2 μm wide) encloses future MEMS region
- Insulating silicon nitride fills trench
- Silicon nitride etched back from wafer surface
- Standard CMOS made and interconnected to future MEMS by metal or doped poly
- MEMS structures defined using deep etch
- Buried oxide etched to release MEMS

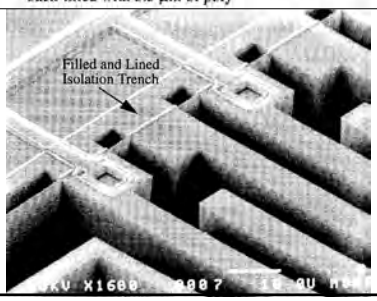



Lemkin et al.

# SOI MEMS




*Brosnihan et al.*





# SOI Accelerometer Parameters

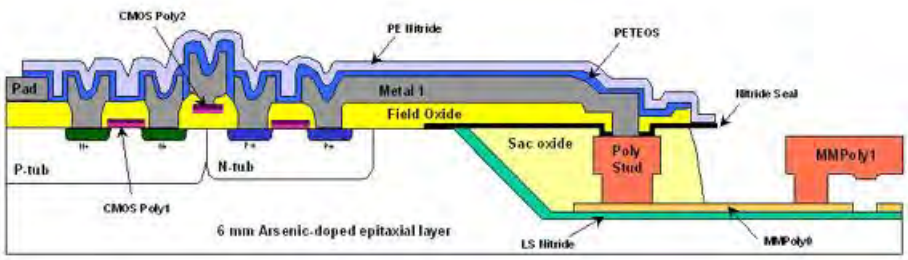
| | |
|---|---|
| • Chip size | 3.4 × 2.9 mm² |
| • Sensor size | 1 × 1.5 mm² |
| • Proof mass | 52 µg |
| • Resonant frequency | 3 kHz |
| • Sense capacitance | 9.7 pF |
| • Full scale | ±1.75 *g* |
| • Power consumption | 5 V x 5 mA |
| • Sensitivity | 102 fF / *g* |
| • Noise floor | 25 µ*g* / √Hz |
| • On-chip A/D conversion | |

*Lemkin et al.*

MEMS → CMOS

# Sandia Embedded Process

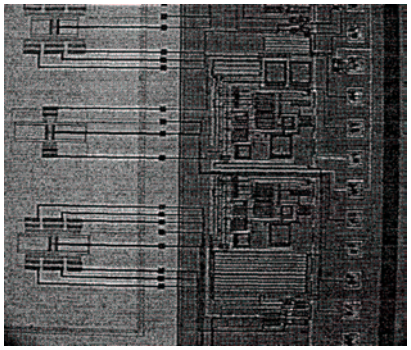
1. Trench etched into Si using KOH
2. MEMS fabricated in trench
3. Trench filled with LPCVD oxide
4. Trench planarized with CMP
5. MEMS stress anneal
6. Trench seal with LPCVD nitride
7. Standard CMOS fabrication next to MEMS
8. CMOS passivated with PECVD nitride
9. Trench opened, MEMS released



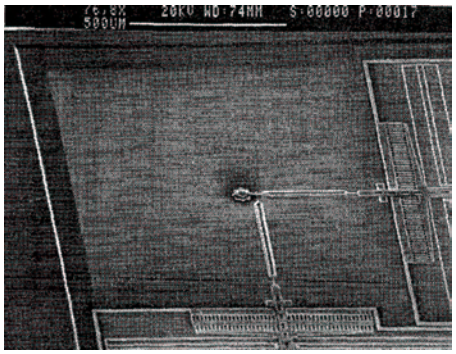



MEMS → CMOS

# Sandia Embedded Process



*Surface micromachined lateral resonators in trench next to CMOS circuitry*

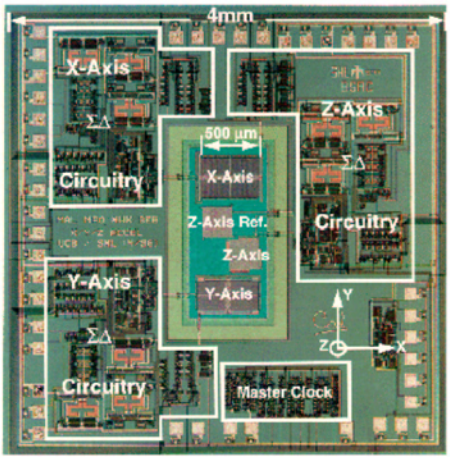


*3-level process*
*12 μm deep trench*

MEMS → CMOS

# Sandia Embedded Process

- 3 axis accelerometer
  - 4 × 4 mm$^2$ chip
  - 3 proof masses to capacitively measure acceleration
    - X, Y: comb finger array
    - Z: parallel-plate capacitor
  - Each sensor has own interface circuitry
  - Differential circuitry allows sensing of fractions of attoFarad changes in capacitance
  - Measures up to ±25 *g*




*M. Lemkin et al.*

*BSAC and Sandia Labs*



# Interleaved and Foundry Processes

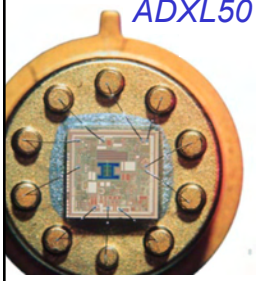
- CMOS and MEMS mixed
  - \+ More control over materials, processes
  - ± Optimize or compromise mechanical and electrical components
  - – Need your own fab
- Foundry processes
  - \+ Economical, reliability and yield high
  - \+ Simple post processing step releases MEMS
  - – Cost of increased chip area
  - – Mechanical properties of CMOS layers compromised

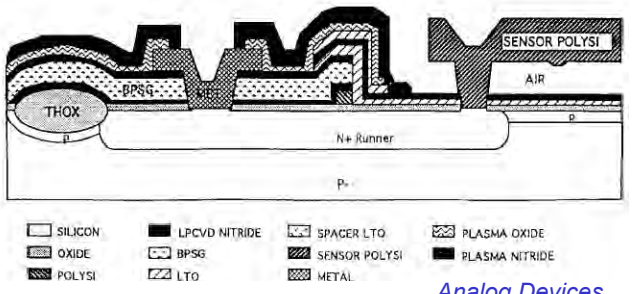
Interleaved 1

# Analog Devices BiMEMS Process

- ADXL50 accelerometer
  - Interleaved MEMS and 4 µm BiMOS fabrication
  - MEMS-CMOS interconnect by diffused n+ runners
  - Relatively deep junctions allow for MEMS poly stress anneal
  - Acceleration to volt transducer
  - Measurement of ±50 *g* accelerations

*ADXL50*






*Analog Devices*



Interleaved 1

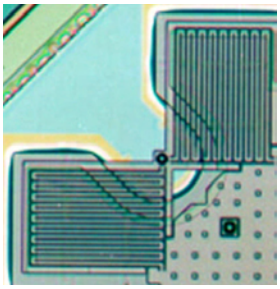
# ADXL150 Specifications

| | ADXL150 | SOI MEMS |
|---|---|---|
| • Chip size | 3 × 3 mm² | 3.4 × 2.9 mm² |
| • Sensor size | 0.6 × 0.7 mm² | 1 × 1.5 mm² |
| • Proof mass | 0.28 µg | 52 µg |
| • Resonant frequency | 12 kHz | 3 kHz |
| • Open-loop displacement | 1.7 nm/*g* | |
| • Sense capacitance | 120 fF | 9.7 pF |
| • Full scale | ±5 *g* | ±1.75 *g* |
| • Shock survival | 1000 *g* | |
| • Power consumption | 5 V x 8 mA | 5 V x 5 mA |
| • Sensitivity | 200 mV/*g* | 102 fF/*g* |
| • Noise floor | 0.6 mg/√Hz | 25 µg/√Hz |

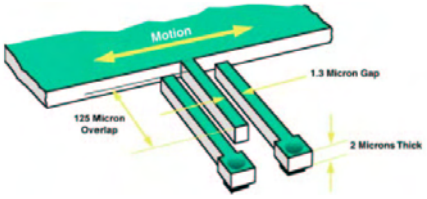
Interleaved 1

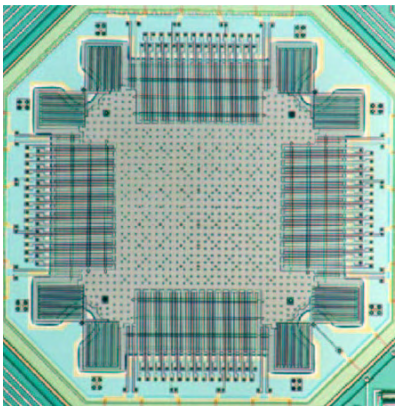
# ADXL202

- ± 2 *g* accelerations
- *X* and *Y* variable capacitors on sides of same larger proof mass
- Spring suspension minimizes cross-axis sensitivity
- Digital output (vs. ADXL50)



*Analog Devices*



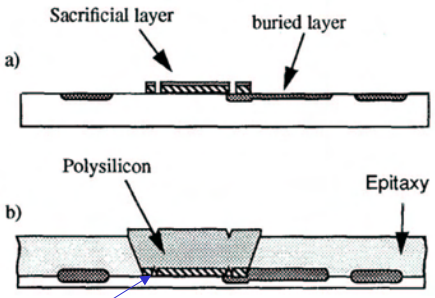



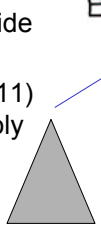


Interleaved 2

# Bosch Epi-Poly Process – 1

- Buried layer defined
- Sacrificial oxide deposited, removed in circuit area and at MEMS anchor points
- Epitaxial deposition, 10μm
  - Monocrystalline above circuit area
  - Polycrystalline above oxide
  - At anchor points, SCS pyramids formed with (111) walls embedded in epipoly
  - Surface is planar



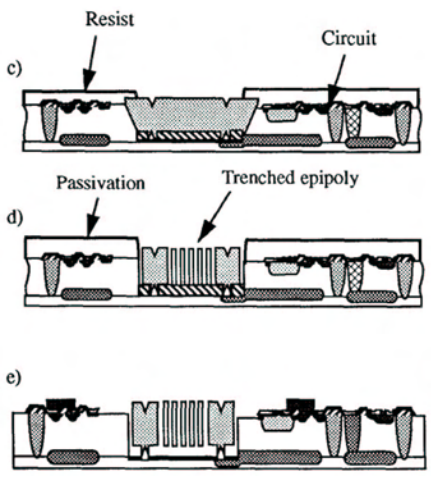



*Offenberg et al. Bosch*

Interleaved 2

# Bosch Epi-Poly Process – 2

- Gate poly patterned
- Doping of gate and MEMS poly
- Dopant drive-in by annealing
- Standard BiCMOS process resumed, ending with metallization and passivation
- Trench etch epipoly structures
- Release using sacrificial oxide etch with HF vapor phase



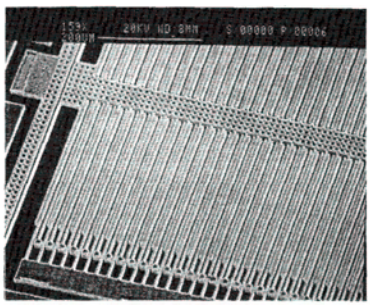

*Offenberg et al. Bosch*

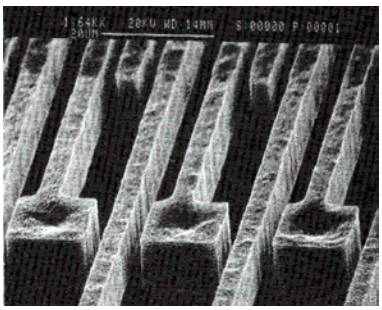


Interleaved 2

# Bosch Results

- As-deposited epipoly has low stress (<4 MPa), negligible stress gradient, and rough surface.
- 10 μm thick epipoly gives stiffness in *z*-direction
- Range ±35*g*
- Sensitivity 20 mV/*g*



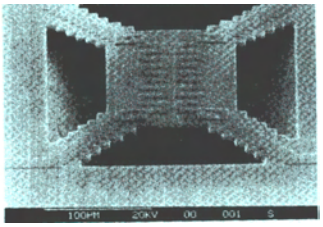


*Offenberg et al., Bosch*

Foundry

# Integrated MEMS by Foundry CMOS

- Fabricate using foundry CMOS
  - Unconventional layout designs
  - Unaltered process sequence
  - Single postprocessing step: isotropic or anisotropic etching
  - \+ Only need to know CMOS design rules vs. processing details
  - \- Mechanical properties compromised
- History
  - Univ. Alberta 1988 (KOH), Cornell 1992 SCREAM process, UCLA 1995 ($XeF_2$), ETH Zurich 1990s, CMU 1996 ASIMPS process ($SF_6$)



*Thermally isolated heater element*

*Parameswaran et al.*

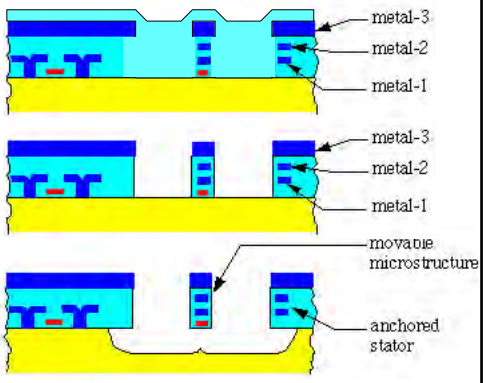
*Univ. of Alberta*

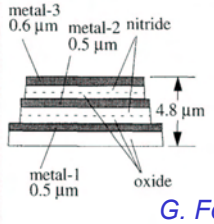


Foundry 1

# Integrated MEMS by Foundry CMOS

- Process
  - Laminated metal/insulator MEMS
  - Made using HP 0.8µm, 3-metal CMOS process at MOSIS foundry
  - Top metal layer used as etch mask for $CHF_3/O_2$ oxide etch
  - Final $SF_6$ isotropic etch releases structures
- Features
  - Independent electrostatic actuation possible due to multiple insulated metal layers

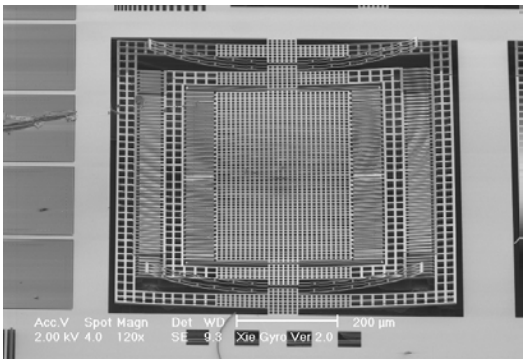


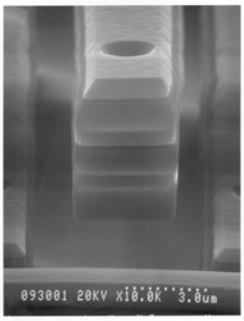




*G. Fedder et al.*

Foundry 1

# Integrated MEMS by Foundry CMOS




- Accelerometer parameters
  - Range ±13 *g*
  - Out-of-plane curl 6 µm
  - Displacement 3.1 nm / *g*
  - Q 1200
  - Noise floor 1 mg/√Hz

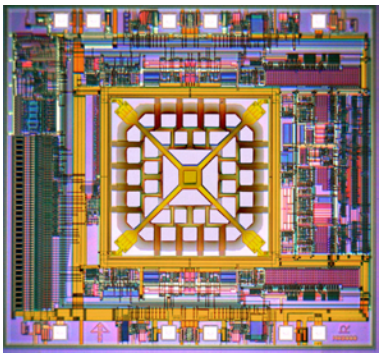
*Courtesy Gary Fedder, Carnegie-Mellon University*



Foundry 2

# MEMSIC Accelerometer

- MEMSIC (Andover, Mass.) dual-axis thermal accelerometer
- Post-foundry CMOS dry bulk micromachining to form thermal isolation cavity
- Sensor consumes large fraction of total chip area → cost of adding "accelerometer function" still high, even if post-process steps are very simple and high-yield



# Summary

- CMOS first
  - State-of-the-art CMOS foundries can be used
  - Thermal budget of metallization to be accounted for
- MEMS first
  - No thermal budget to worry about
  - Possible materials incompatibilites (high dopant structural layers, piezoelectrics)
  - Topography to overcome
- Interleaved
  - Potentially greater control over process steps
  - First commercially proven integrated process
  - Possibly compromises both CMOS and MEMS