INTEL® SILICON PHOTONICS: FROM RESEARCH TO PRODUCT

MARCH 8, 2017

LING LIAO
Principal Engineer
Silicon Photonics Product Division

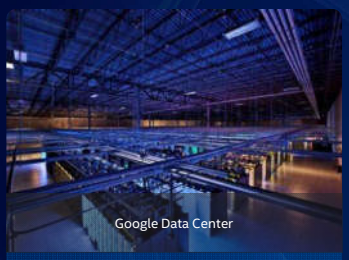
2016 PRODUCT ANNOUNCEMENT AND CELEBRATION

CNET
Intel: Our laser chips will make sites like Google and Facebook faster

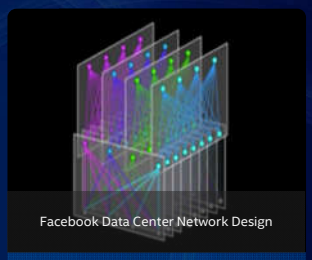
Intel Circuit
Marching Band in RNB Courtyard – Silicon Photonics Harmony Bay PRQ Celebration

EMERGENCE OF HYPER SCALE DATA CENTERS

Data center networks are struggling to keep up with exponential data growth


Google Data Center


Facebook Data Center Fort Worth, Texas


Facebook Data Center Network Design

5 ZB

Worldwide Annual Data Center Traffic (~5X global internet traffic)

>$1B

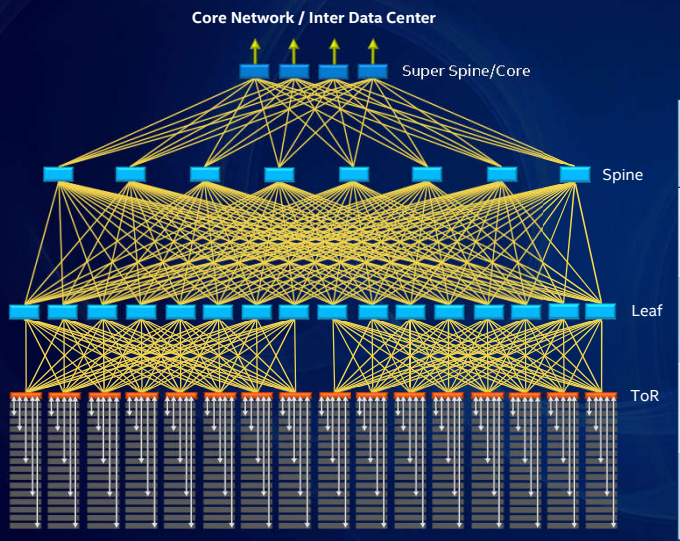
>200K Servers
10K+ switches

45%+

Optical Connectivity as % of Networking Spend

Other names and brands may be claimed as the property of others
Source: Estimates from Facebook, Google, Cisco publications, and Intel network model

NETWORK ARCHITECTURE TODAY

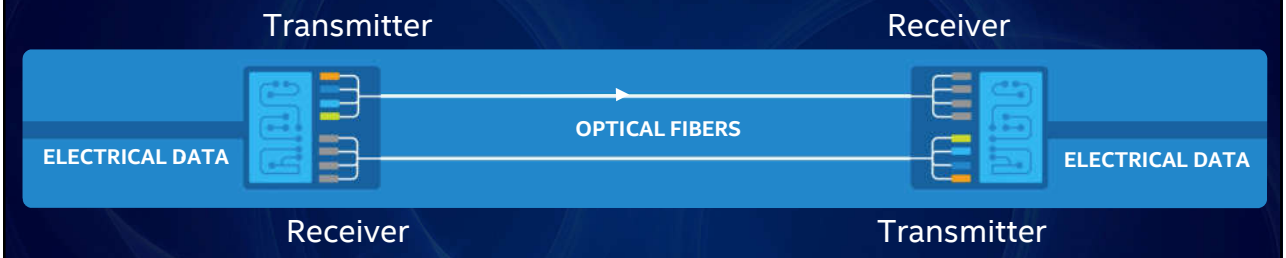


	Different technologies deployed
Inter Data Center 10km-metro	10G/40G/100G DWDM
Spine-Core 500m-2km	40G SMF
Leaf-Spine 300m-2km	40G MMF or SMF
TOR-Leaf 100m-500m	40G MMF or SMF
Server-Top of Rack (TOR) 1m-30m	10G Cu or AOC

Challenges:

- Reach
- Power
- Latency
- Cost
- Scalability

OPTICAL COMMUNICATION



Laser - light source

Modulator – high speed encoder

Detector - light sensor

SILICON PHOTONICS

TRADITIONAL OPTICS	SILICON PHOTONICS
Compound semiconductor platform	All silicon or silicon-compatible platform
Specialized tools and processes	CMOS manufacturing of photonics
Relatively low-degree of integration	High density interconnects made at wafer scale

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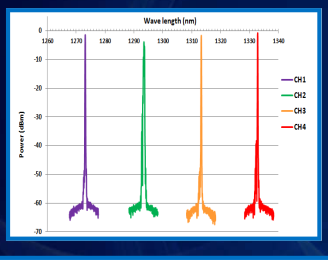
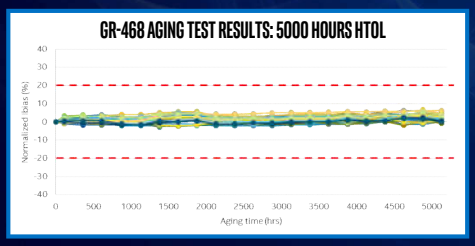
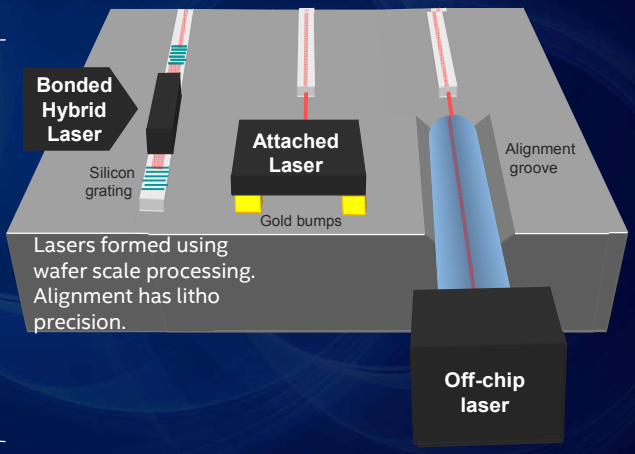
INTEL HYBRID SILICON LASER

Key differentiation: Only SiPh product with on-die lasers

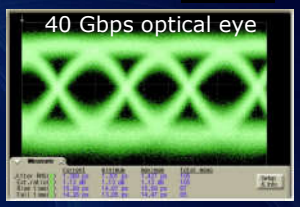






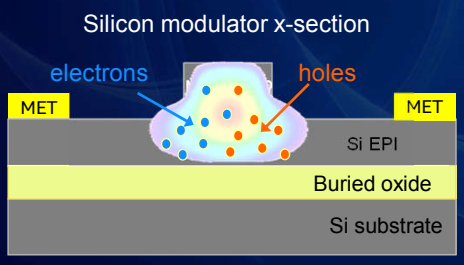
HIGH SPEED SILICON MODULATOR

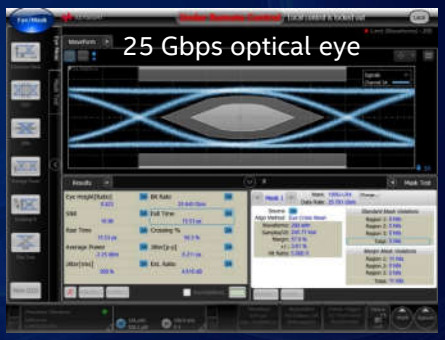
Key tech demos: 1 GHz → 10 Gbps → 40 Gbps



Carrier dispersion:

- Carrier density (ΔN) ➔ refractive index ($\Delta neff$) ➔ optical phase ($\Delta\phi$)
- Devices: MOSCAP and diode



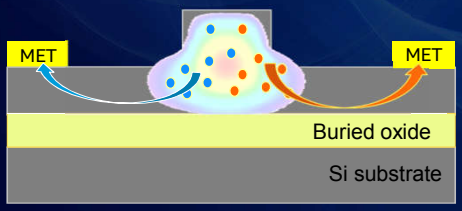


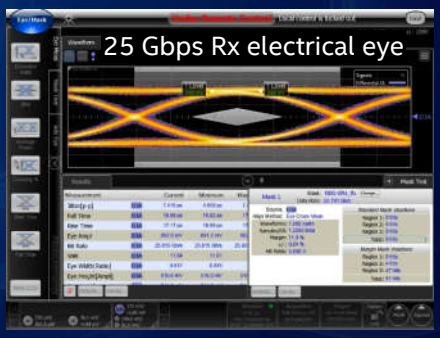
HIGH SPEED SILICON-GERMANIUM DETECTOR

Key tech demos: 40 Gbps PIN, 340 GHz Gain*BW APD

High quality film:
- No visible defects
- low dark current

Ge PIN detector x-section

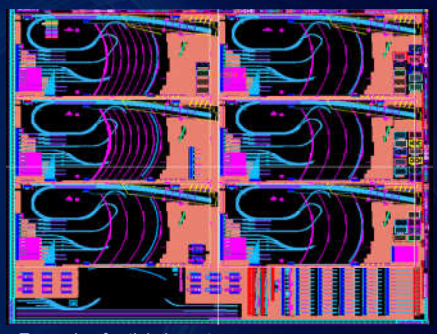




DESIGN: DFX AND PDK

DFM/DFT/DFD early to reduce cost and TTM

Process Design Kit (PDK)
- Standardized Component Library
- Documentation
  - Process design rules
  - Package and Assembly design rules
  - Tapeout procedure
- Automated Verification
  - Design rule check (DRC)
  - Layout vs schematic (LVS): verify device type, connectivity and parameters
  - Parasitic extraction (PEX)

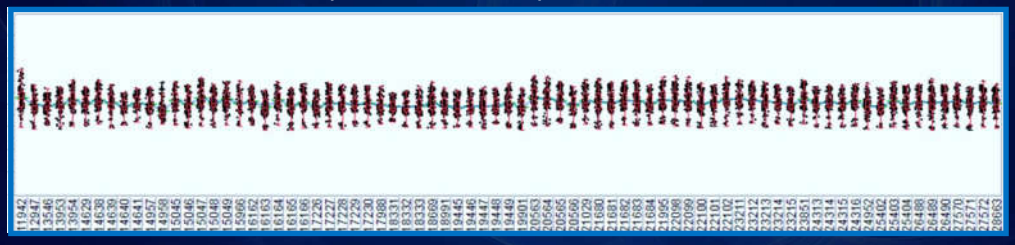


Example of reticle layout:
Note heavy use of polygon (non-Manhattan) layout which makes photonics layout tedious vs CMOS

FAB: ADOPT AND REUSE

Leverage CMOS manufacturing infrastructure and methodologies

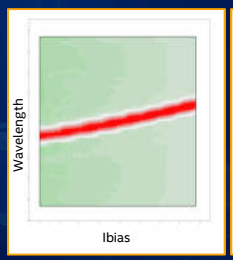
- Cycle time: fast TPT and priority processing can achieve additional 3-4x improvement
- Change control: all changes are documented and reviewed (Whitepapers and xCCB)
- Process control: 1000's of process and tool parameters are monitored and recorded

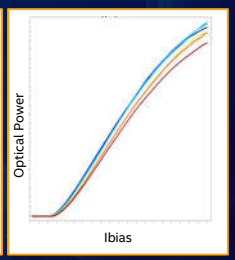


- "Shift-left": in-line data and control/spec limits are used to disposition material early

TEST: ADOPT AND RETROFIT

- Speed
- Accuracy
- Repeatability
- Adaptability





Source: http://www.tel.com

TEST: PROGRESS TO HVM

Basic 200mm

Instruments: Rack
Automation: None
Opt. Alignment: Manual
Lot Info: Manual
Lot Delivery: Hand
Test Start: Manual
Data: Text Files

Automated 300mm

Instruments: Rack
Automation: Some
Opt. Alignment: Auto
Lot Info: Auto
Lot Delivery: Robot
Test Start: Manual
Data: Oracle DB

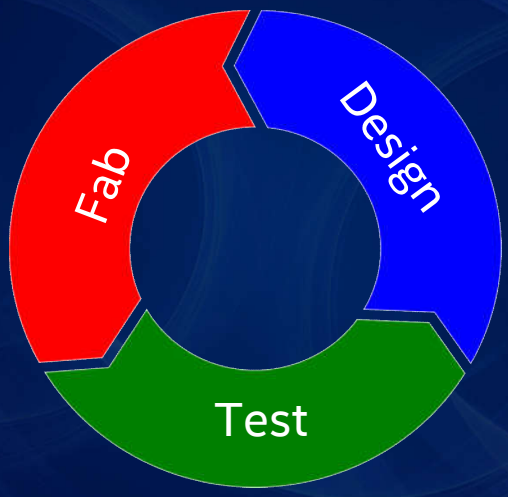
Advanced 300mm

Instruments: Integrated
Automation: Full SECS/GEM
Opt. Alignment: Auto
Lot Info: Auto
Lot Delivery: Robot
Test Start: Auto
Data: Oracle DB

Reduce test costs by driving control and containment through automation.

ACCELERATED CYCLE TIME: THROUGHPUT TIME REDUCTION

10x



5x

100X

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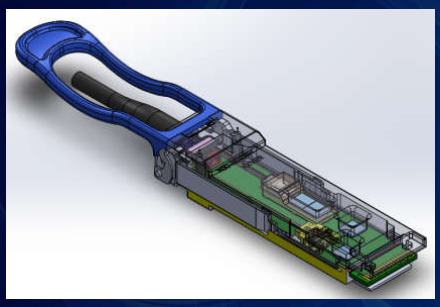
MODULE PACKAGING



- PIC and EIC die placement
- Epoxy attach and cure
- Wirebond/flip-chip
- Plasma clean
- …

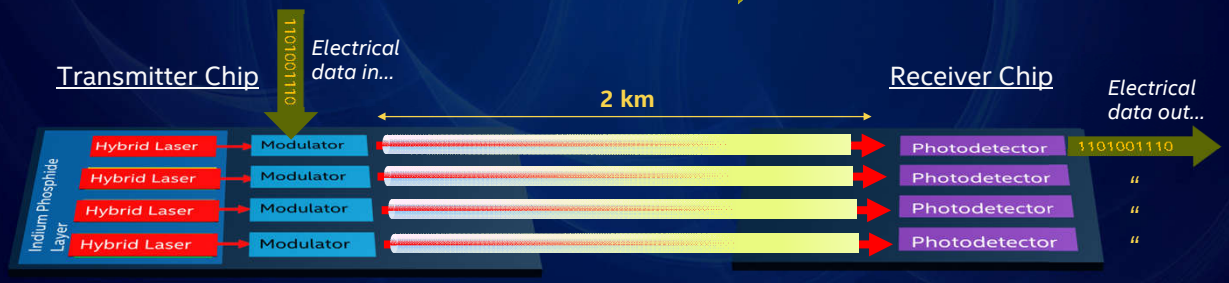
Optical products - unique consideration

- Optical packaging
  - Sub-μm alignment
  - Stack-up tolerance control
  - Mechanical stability over T and life
  - Optical back-reflection control
- Thermal management
  - Assembly process thermal budget
  - Heat dissipation
- Stress management
  - Stress/strain reduction
  - Stress profile managment

INTEL® SILICON PHOTONICS

1st product (100G PSM4 QSFP28)

- **4 x 25 Gbps parallel single-mode**
- **Reach up to 2km (0-70C)**
- **MTP/MPO fiber pigtail or receptacle**

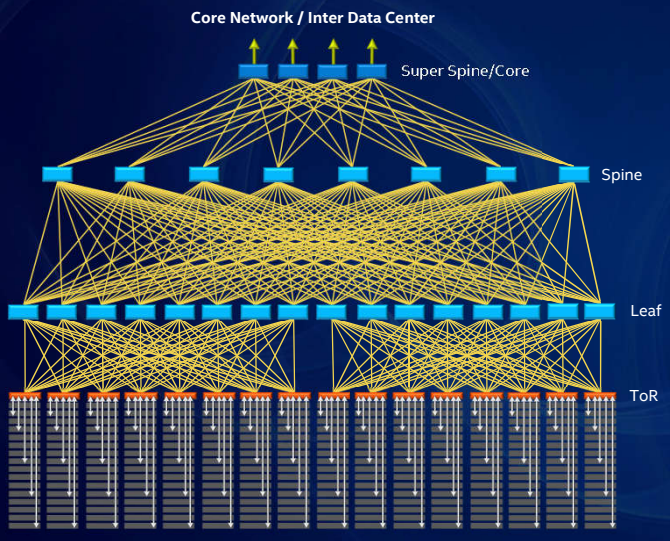


INTEL® SILICON PHOTONICS

2st product (100G CWDM4 QSFP28)

- 4 x 25 Gbps WDM single-mode
- 500m reach (15-55C)
- 2km reach (0-70C)
- 10km reach (0-70C)

NETWORK ARCHITECTURE



	DEPLOYED TODAY	UPGRADING NOW
Inter Data Center 10km-metro	10G/40G/100G DWDM	100/200/400G DWDM
Spine-Core 500m-2km	40G SMF	100G SMF
Leaf-Spine 300m-2km	40G MMF or SMF	
TOR-Leaf 100m-500m	40G MMF or SMF	
Server-Top of Rack (TOR) 1m-30m	10G Cu or AOC	25G Cu or AOC

SiPh Opportunity: flatten the network to bring reduction in power, cost, and latency.

PATH TO TERA-SCALE DATA RATES

Today: 25 Gbps x 4 = 100 Gbps

Scale UP

50 Gbps x 4 = 200Gbps

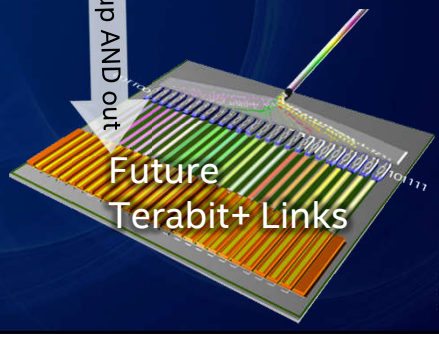
Scale OUT

Speed	Width	Rate
25	x8	200G
50	x4	200G
100	x4	400G
100	x16	>1.6T

Scale up AND out

25 Gbps x 8 = 200Gbps

Scale up AND out



FUTURE OF OPTICAL CONNECTIVITY IN DATA CENTERS

EXPECTED FORM FACTOR EVOLUTION

2016

100G MSA Pluggable

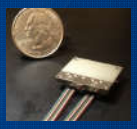
Enabling transition to 100G switch-to-switch connectivity

2018 / 2019

400G MSA Pluggable

Supporting next-generation switch 12.8Tb/s and 50G I/O

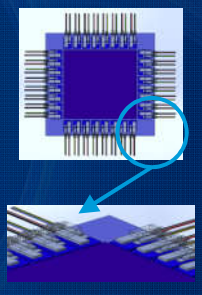
400/800G embedded



Embedded optics for density, signal integrity, and power

2020+

High density integrated

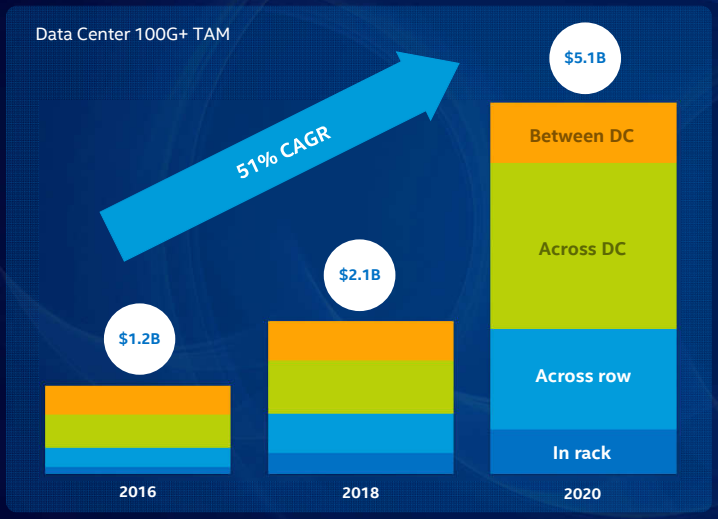


Address electrical I/O constraints
Highest density
Lowest system power

Technology development for miniaturization, high-temp operation, low power process

QSFP-DD image from: http://www.qsfp-dd.com/

DATA CENTER CONNECTIVITY TAM



Data Center total spend on 100G and 400G interconnects

Connected world, machine-to-machine traffic, data analytics & machine learning driving exponential data growth

Continual innovation needed to support data growth

Source: 2015 Intel market model based in part on Dell'Oro, Crehan and Lightcounting 2015 reports

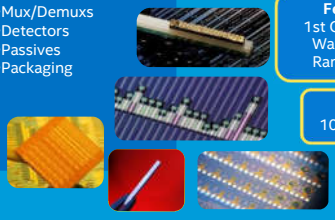
INTEL® SILICON PHOTONICS

Intel Labs | Intel Labs Ventures | DCG

Research, Building Block and Technology Development

Product Development and Commercialization

Building Blocks
- Lasers
- Modulators
- Mux/Demuxs
- Detectors
- Passives
- Packaging



Feb 2004 1 GHz Si Mod

Feb 2005 1st Continuous Wave Silicon Raman Laser

April 2005 10 Gbps Si Mod

Sept 2006 Hybrid Silicon Laser

July 2007 40 Gbps Si Mod

August 2007 40 Gbps PIN Photo-detector

Dec 2008 340 GHz Gain*BW Avalanche Photo-detector

Dec 2009 4x12.5 Gbps POC

Dec 2011 2x25 Gbps POC

Dec 2012 4x25 Gbps POC

2016 Product Launch

2000 → 2017

Spearheaded the field with numerous scientific breakthroughs and POC demonstrations. Achieved commercialization in 2016. Poised to revolutionize data center connectivity.

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