Interfacing the TMS320C55x to SDRAM

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ABSTRACT

The TMS320C55x™ (C55x™) External Memory Interface (EMIF) supports a glueless interface to high-density and high-speed SDRAMs. Both 64-Mbit and 128-Mbit SDRAMs are supported in 16-bit and also 32-bit data widths. The DSP can also provide the SDRAM clock at software selectable submultiples of the C55x DSP CPU frequency. This application report presents the C55x EMIF signals and the necessary signal connections between the DSP and various types of SDRAM. EMIF register bit settings are also discussed.

NOTE: Please consult the latest C55x device datasheets and errata to confirm which silicon revisions support SDRAM before using C55x devices in a particular system application with SDRAM.

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1 C55x SDRAM Interface

The TMS320C55x (C55x) External Memory Interface (EMIF) supports a glueless interface to high density and high speed SDRAMs. Both 64-Mbit and 128-Mbit SDRAMs are supported in 16-bit and also 32-bit data widths. The C55x EMIF can be configured to operate at the following DSP CPU CLKOUT frequency multiples for SDRAM: 1x and 1/2x.

The register bit configurations and address pin mapping to row and column addresses for specific organizations and quantities of SDRAMs are shown in Table 1. For definitions of the register configuration bits (SDACC, SDSIZE, SDWID), see the SDRAM Control Registers.

Table 1. C55x EMIF SDRAM Configuration and Address Pin Mapping

SDRAM Size	Array Organization	SDRAM Chips Used	Config-Bits			CE Spaces Used	I/F	Bank/Row Address	Column Address
			SDACC	SDSIZE	SDWID				
64 Mbit	4M x 16 bit	1	0	0	0	2	SDRAM	BA[1:0] and A[11:0]	A[7:0]
							EMIF	A[14:12], SDA10 and A[10:1]	A[8:1]
64 Mbit	4M x 16 bit	2	1	0	0	4	SDRAM	B [1:0] and A[11:0]	A[7:0]
							EMIF	A[15:13], SDA10 and A [11:2]	A[9:2]
64 Mbit	2M x 32 bit	1	1	0	1	2	SDRAM	BA[1:0] and A[10:0]	A[7:0]
							EMIF	A[14:13], SDA10 and A[11:2]	A[9:2]
64 Mbit	2M x 32 bit	2	1	0	1	4	SDRAM	BA[1:0] and A[10:0]	A[7:0]
							EMIF	A[14:13], SDA10 and A[11:2]	A[9:2]
128 Mbit	8M x 16 bit	1	0	1	0	4	SDRAM	BA[1:0] and A[11:0]	A[8:0]
							EMIF	A[14:12], SDA10 and A[10:1]	A[9:1]
128 Mbit	4M x 32 bit	1	1	1	1	4	SDRAM	BA[1:0] and A[11:0]	A[7:0]
							EMIF	A[15:13], SDA10 and A[11:2]	A[9:2]

The signals provided on the C55x EMIF pins for SDRAM usage are described in Table 2. For a complete listing of all C55x pins, consult the latest device datasheets.

Table 2. C55x EMIF/SDRAM Signal Descriptions

Signal	State	Description
A21 (MSB) to A0 (LSB)	O/Z	22-bit parallel address port. Internal data, program and DMA busses are multiplexed into a single external address bus. Placed in high impedance in hold mode.
D31 (MSB) to D0 (LSB)	I/O/Z	32-bit parallel data port. Internal data, program and DMA busses are multiplexed into a single external data bus. Outputs placed in high impedance in hold mode.
$\overline{CE0}$	O/Z	Active-low chip select for memory space CE0. Placed in high impedance in hold mode.
$\overline{CE1}$	O/Z	Active-low chip select for memory space CE1. Placed in high impedance in hold mode.
$\overline{CE2}$	O/Z	Active-low chip select for memory space CE2. Placed in high impedance in hold mode.
$\overline{CE3}$	O/Z	Active-low chip select for memory space CE3. Placed in high impedance in hold mode.
$\overline{BE}$ [3:0]	O/Z	Active-low byte enables. Placed in high impedance in hold mode.
$\overline{SDRAS}$	O/Z	Active-low SDRAM row strobe. Placed in high impedance in hold mode.
$\overline{SDCAS}$	O/Z	Active-low SDRAM column strobe. Placed in high impedance in hold mode.
$\overline{SDWE}$	O/Z	Active-low SDRAM write enable. Placed in high impedance in hold mode.
SDA10	O/Z	SDRAM A10 address line. Acts as a row address bit during ACTV commands. Also acts as the auto-precharge enable for SDRAM memories during read and write operations. Active high during DCAB. Placed in high impedance in hold mode.
CLKMEM	O/Z	Memory interface clock for SDRAM. Placed in high impedance in hold mode.

2 C55x EMIF SDRAM Interface Operation

The TMS320C55x (C55x) External Memory Interface (EMIF) provides support for industry standard SDRAM commands. These commands and their corresponding pin states are given in Table 3 and Table 4.

Table 3. C55x EMIF SDRAM Commands Descriptions

Command	Description
DCAB	Deactivate (pre-charge) all banks
ACTV	Activate the selected bank and select the row
READ	Input the starting column address and begin the read operation
WRT	Input the starting column address and begin the write operation
MRS	Mode Register Set. Configures SDRAM mode register
REFR	Auto refresh cycle with internal address
NOP	No SDRAM operation

Table 4. C55x EMIF SDRAM Commands Pin States

					SDRAM Address Bus A [15:2]		
Command	**$\overline{CEn}$**	**$\overline{SDRAS}$**	**$\overline{SDCAS}$**	**$\overline{SDWE}$**	**A [15:13]**	**SDA10**	**A [11:2]**
DCAB	0	0	1	0	X	1	X
ACTV	0	0	1	1	ROW	ROW	ROW
READ	0	1	0	1	ROW	0	COL
WRT	0	1	0	0	ROW	0	COL
MRS	0	0	0	0	X	X	MRS
REFR	0	0	0	1	X	X	X
NOP	0	1	1	1	X	X	X
	1	X	X	X	X	X	X

2.1 Address Shift

Because the same EMIF pins address both the row and column addresses, the EMIF interface appropriately shifts the address for proper row and column address selection. SDRAMs use the A10 inputs for control as well as address. The EMIF forces the precharge disable bit (SDA10) to be low during READ and WRT commands, high during DCAB commands, and as the row address A10 during ACTV commands. This prevents the auto-precharge from occurring following a READ or WRT command.

2.2 Timing Requirements

Configurable timing parameters allow EMIF functionality with SDRAMs from a wide range of speed ratings. For more information, see the SDRAM Control Registers. For specific settings, consult the manufacturer’s data sheet for the particular SDRAM.

2.3 Monitoring Page Boundaries

Because SDRAM is a paged memory type, the EMIF SDRAM controller monitors the active row of SDRAM so that row boundaries are not crossed during accesses. The EMIF stores the address of the open page and performs a comparison against that address for subsequent accesses to the SDRAM bank. This storage and comparison is performed separately for each CE space. The number of address bits and page boundaries compared are a function of the page size configured by the SDWID, SDSIZE, and SDACC fields in the EMIF SDRAM Control Registers 1 and 2.

During the course of an access, if a page boundary is crossed, the EMIF performs a DCAB command and starts a new row access (ACTV command). Simply ending the current access is not a condition which forces the active SDRAM row to be closed. The EMIF speculatively leaves the active row open until it becomes necessary to close it. This feature decreases the DCAB ACTV overhead and improves the performance of the interface. However, the EMIF only allows one row to be open at a time regardless of the number of banks that the SDRAM contains.

2.4 SDRAM Initialization

For all CE spaces configured as SDRAM, the EMIF performs the necessary functions to initialize SDRAM. An SDRAM initialization is requested by any write to the EMIF SDRAM Initialization Register. The MTYPE fields of the configuration registers should be properly set before performing the initialization. Figure 1 shows the timing during SDRAM initialization and execution of the MRS command.

The SDRAM initialization sequence is as follows:

1. Three NOP commands are sent to all CE spaces configured as SDRAM.
2. DCAB command is sent to all CE spaces configured as SDRAM.
3. Eight REFR commands are sent to all CE spaces configured as SDRAM.
4. MRS command is sent to all CE spaces configured as SDRAM.
5. SDRAM Initialization Register is cleared to prevent multiple MRS cycles.

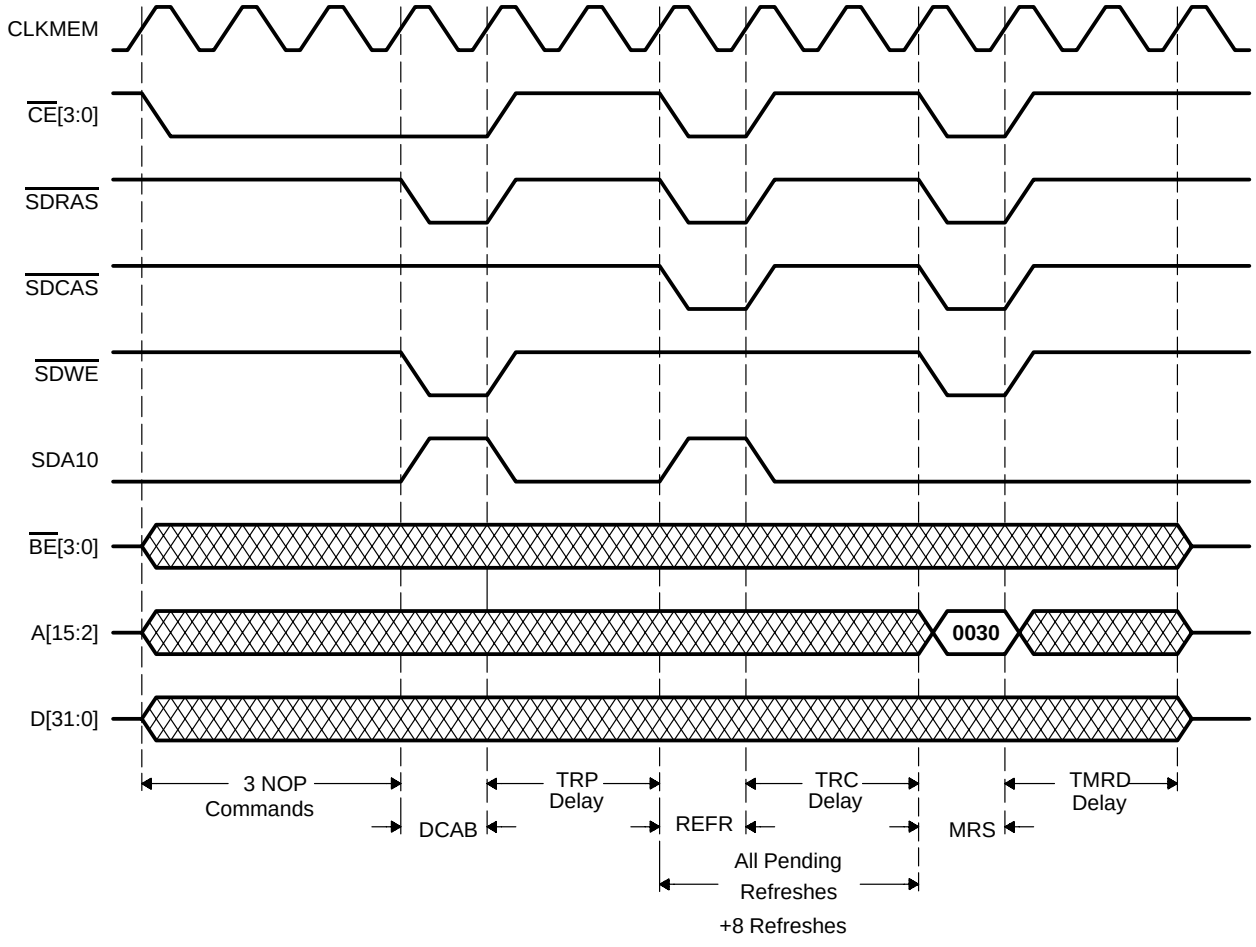

Figure 1. SDRAM Initialization and Mode Register Set (MRS) Command

2.5 Mode Register Set (MRS)

The Mode Register is a register within the external SDRAM memory that dictates the operating characteristics of the SDRAM. The EMIF automatically performs a DCAB command, followed by a MRS command during SDRAM initialization. Like other SDRAM commands generated by the C55x EMIF, MRS commands are sent to all CE spaces configured as SDRAM. The EMIF always uses a Mode Register value of 0x0030 during a MRS command. Figure 2 shows the mapping between mode register bits, EMIF pins, and the mode register value. Table 5 shows the standard SDRAM configuration values selected by the mode register value.

SDRAM Mode Register Bits	11	10	9	8	7	6	5	4	3	2	1	0
C55x EMIF Pins	A13	SDA10	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2
FIELD DESCRIPTION	Reserved		WRITE BURST LENGTH	Reserved		READ LATENCY			SERIAL/ INTERLEAVE BURST	BURST LENGTH		
Value	0	0	0	0	0	0	1	1	0	0	0	0

Figure 2. SDRAM Mode Register Value

Table 5. SDRAM Configuration at MRS

Field	Selection
Write burst length	1
Read latency	3
Serial/Interleave burst type	0 (serial)
Burst length	1

2.6 SDRAM Refresh (REFR)

Refresh cycles are generated by the EMIF with the RFEN bit set to 1 in the SDRAM Control Register. A value of 0 in the RFEN bit disables all refreshes provided by the C55x EMIF. In this case, an external device would be required to execute refreshes.

The refresh command (REFR) is sent to all CE spaces configured as SDRAM by the MTYPE field of the corresponding CE Space Control Register. REFR is automatically preceded by a DCAB command. This ensures that all CE spaces configured as SDRAM are deactivated before a refresh occurs. Page information is always invalid before and after a REFR command. Therefore, a refresh cycle always forces a page miss on the next access. Following the DCAB command, the EMIF begins performing “trickle” refreshes at a rate defined by the PERIOD value in the EMIF SDRAM Period Register, provided no other SDRAM access is pending. The timing diagram for an SDRAM refresh is shown in Figure 3.

When the EMIF or clock generator unit is placed into an IDLE state by software, the SDRAM clock is disabled to save additional power. The EMIF will not issue SDRAM refresh commands, and the data stored in SDRAM will be lost. If an SDRAM refresh were required during this time, external refresh logic would be necessary. For details on C55x idle domains, refer to *TMS320C55x DSP Peripherals Reference Guide* (SPRU317).

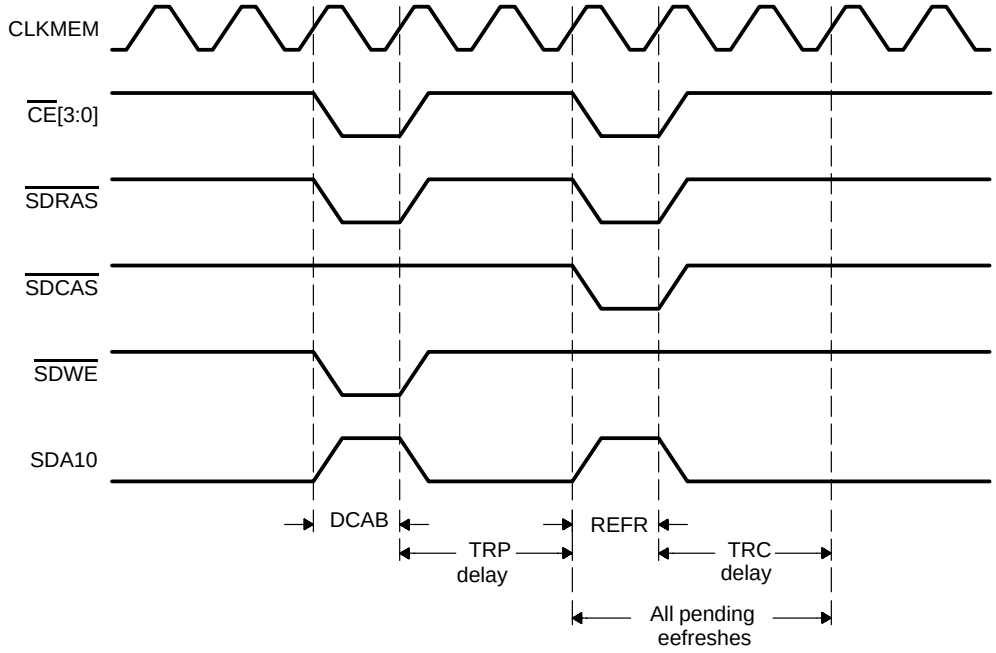

Figure 3. SDRAM Refresh

2.7 Deactivation (DCAB)

The SDRAM deactivation (DCAB) or precharge command is generated by the EMIF to close the active page of memory. DCAB is performed after hardware reset or after a write to the SDRAM INIT register. Also, a DCAB is generated prior to REFR, MRS, and when page boundaries are crossed. During the DCAB command operation, SDA10 is driven high to ensure that all SDRAM banks are deactivated. Figure 4 shows the timing diagram for SDRAM deactivation.

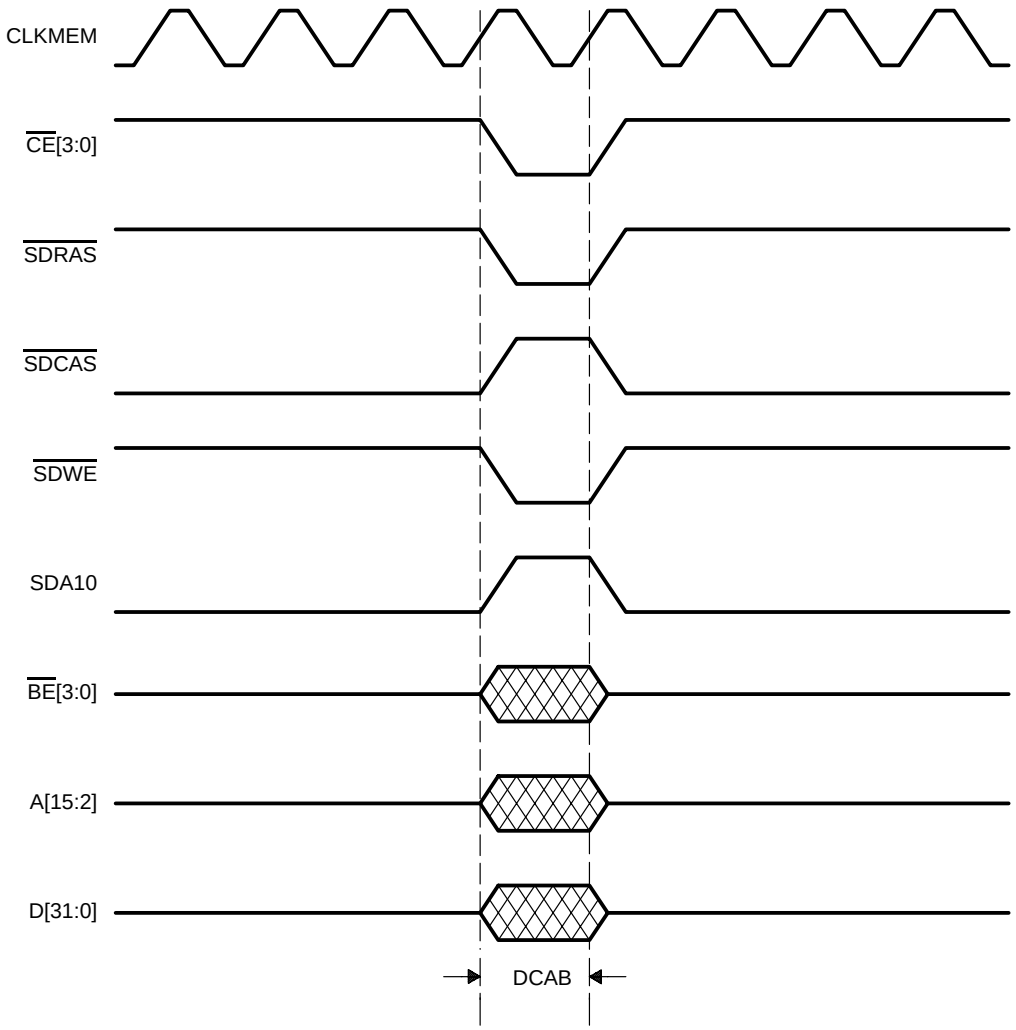

Figure 4. SDRAM Deactivation

2.8 SDRAM Read

During a SDRAM read, the selected bank is activated with the row address during the ACTV command. The EMIF uses a $\overline{CAS}$ latency of 3 and a burst length of 1. The 3-cycle latency causes read data to appear on the data bus 3 cycles after the corresponding column address.

If a refresh cycle or an access to a different page of memory is required, a DCAB cycle is performed to deactivate the bank after the last column access. Delay cycles are inserted between the final read command and the DCAB command to meet SDRAM timing requirements. Note that due to the data latency, the transfer of data actually completes after the DCAB command. If no new access is pending, the DCAB command is not performed until such time that the page information becomes invalid.

An example of a SDRAM read is shown in Figure 5. A burst read example is given in Figure 6.

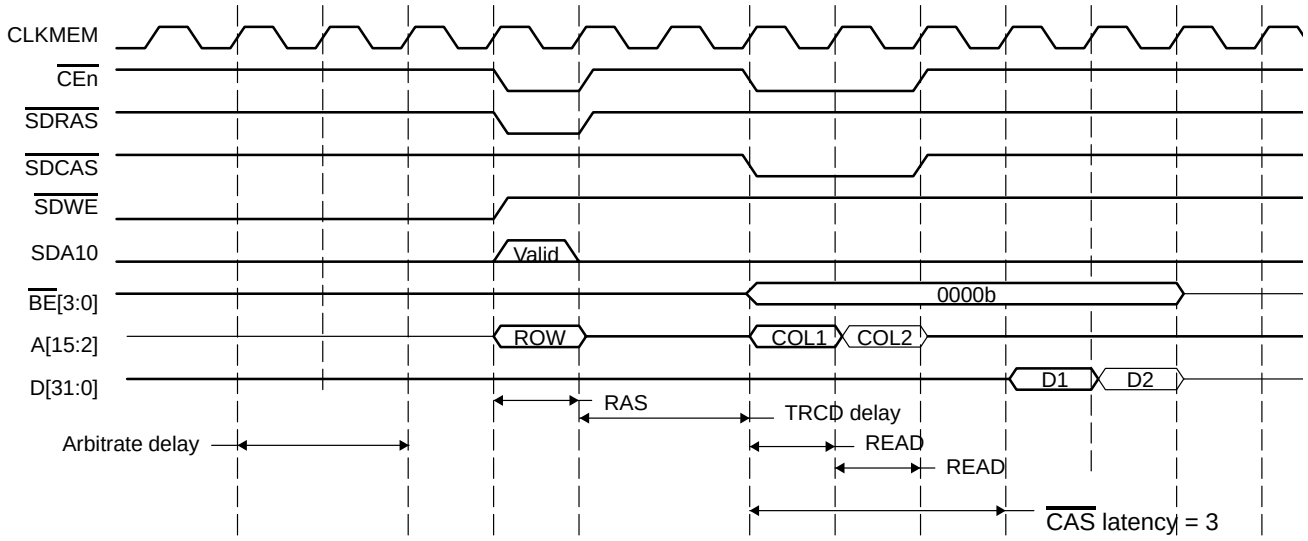

Figure 5. SDRAM Read

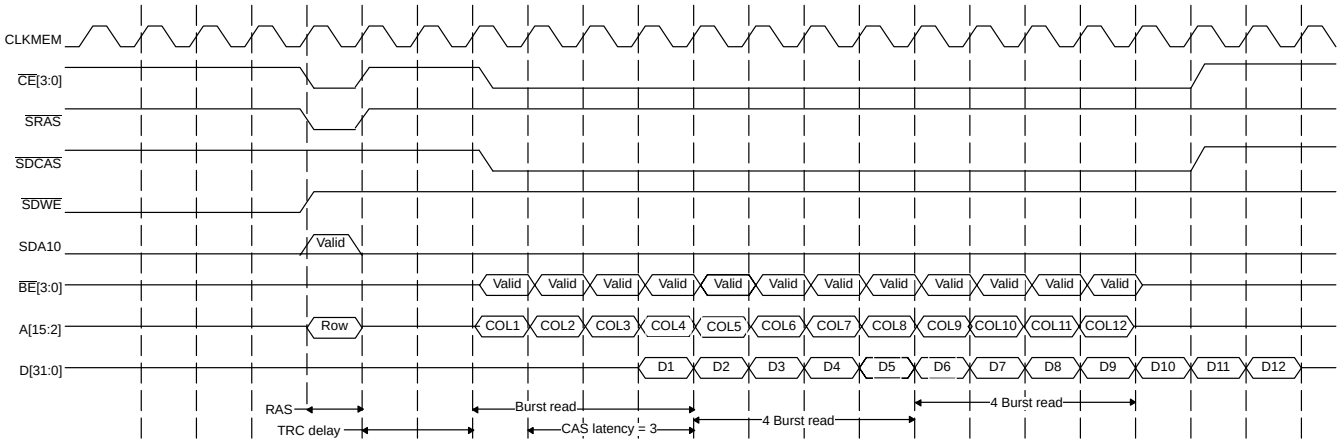

Figure 6. SDRAM Burst Reads

2.9 SDRAM Write (WRT)

All SDRAM writes have a burst length of 1. The bank is activated with the row address during the ACTV command. Unlike SDRAM reads, there is no CAS latency on writes. Therefore, data is output on the same cycle as the column address. Byte and half-word writes are enabled via the appropriate C55x EMIF $\overline{BE}$[3:0] pins connected to the DQM inputs of the SDRAM. Following the final write command, delay cycles are inserted to meet SDRAM timing requirements. If required, the bank is then deactivated with a DCAB command and the memory interface can begin a new page access. If no new access is pending or if an access is pending to the same page, the DCAB command is not performed until such time that the page information becomes invalid. Examples of SDRAM writes are shown in Figure 7.

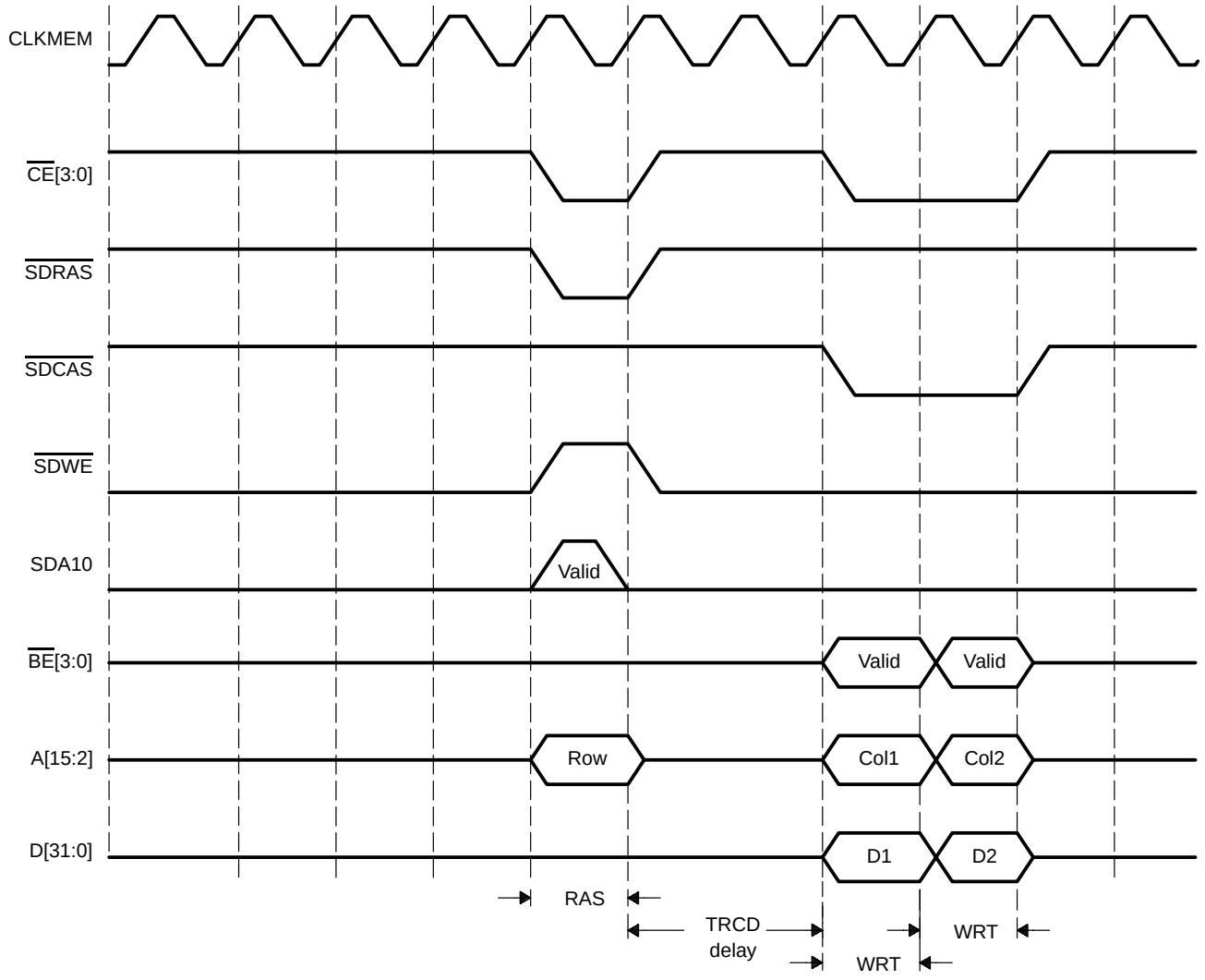

Figure 7. SDRAM Writes

3 C55x EMIF Registers

Configuration of the C55x EMIF is achieved through a set of memory-mapped registers that are addressable through internal I/O memory space. The memory-mapped registers are shown in Table 6.

Table 6. C55x EMIF Memory-mapped Registers

I/O Space Word Address	Name
0x0800	EMIF Global Control Register
0x0801	EMIF Global Reset Register
0x0802	EMIF Bus Error Status Register
0x0803	EMIF CE0 Space Control Register 1
0x0804	EMIF CE0 Space Control Register 2
0x0805	EMIF CE0 Space Control Register 3
0x0806	EMIF CE1 Space Control Register 1
0x0807	EMIF CE1 Space Control Register 2
0x0808	EMIF CE1 Space Control Register 3
0x0809	EMIF CE2 Space Control Register 1
0x080A	EMIF CE2 Space Control Register 2
0x080B	EMIF CE2 Space Control Register 3
0x080C	EMIF CE3 Space Control Register 1
0x080D	EMIF CE3 Space Control Register 2
0x080E	EMIF CE3 Space Control Register 3
0x080F	EMIF SDRAM Control Register 1
0x0810	EMIF SDRAM Period Register
0x0811	EMIF SDRAM Counter Register
0x0812	EMIF SDRAM Initialization Register
0x0813	EMIF SDRAM Control Register 2

NOTE: Shaded areas are not directly related to SDRAM.

3.1 EMIF Global Control Register

The EMIF Global Control Register contains configurable parameters that are common to all CE spaces. The register bit locations and brief parameter descriptions are given in Figure 8 and Table 7. The primary bits of concern for SDRAM in this register are Memory Clock Enable (MEMCEN), Memory Frequency (MEMFREQ), and Write Posting Enable (WPE).

The EMIF has two write posting registers that are enabled/disabled by WPE. If write posting is enabled (WPE = 1), the write posting registers are used to store the write address and data such that the CPU may be acknowledged by the EMIF with zero wait states. The CPU is then free to carry on with the next access and the posted write operations will be run externally as time slots become available. If the next access is for internal memory and not for the EMIF, the internal memory access is able to run concurrently with a slower external memory write operation.

The write posting registers are freely associated with either of the two data-write data buses of the CPU (E and F busses). For example, a section of code that consists of only E bus writes benefits from two levels of write posting. When write posting is disabled (WPE = 0), a request from the E or F bus is acknowledged as the write data is driven onto the external bus. It might be useful during debug to disable write posting. Write posting is disabled at reset of the C55x device. For more details, refer to *TMS320C55x Peripherals Reference Guide* (SPRU317*)*.

15 12	11 9	8	7	6	5	4	3	2	1	0
Reserved	**MEMFREQ**	Reserved	**WPE**	Reserved	**MEMCEN**	Reserved	ARDY	$\overline{\text{HOLD}}$	$\overline{\text{HOLDA}}$	NOHOLD
R, +0	RW, +000	RW, +0	RW, +0	RW, +0	RW, +1	R, +0	R, +x	R, +x	R, +0	RW, +0

NOTES: The following applies to the register diagrams in this document:
1. R means read only.
2. W means write only.
3. RW means both read and write allowed.
4. +0 indicates the reset value is logic-low.
5. +1 indicates the reset value is logic-high.
6. +x indicates the reset value reflects the pin state or is insignificant.
7. **Shaded areas are not directly related to SDRAM.**

Figure 8. EMIF Global Control Register Diagram

Table 7. EMIF Global Control Register Bit Field Description

Field	Description
NOHOLD	External HOLD Disable NOHOLD=0, hold enabled NOHOLD=1, hold disabled
$\overline{\text{HOLDA}}$	Value of $\overline{\text{HOLDA}}$ output
$\overline{\text{HOLD}}$	Value of $\overline{\text{HOLD}}$ input
ARDY	Value of ARDY input. The value of ARDY bit is invalid when no asynchronous accesses are occurring.
MEMCEN	Memory Clock Enable MEMCEN=0, CLKMEM held high MEMCEN=1, CLKMEM output enabled
WPE	Write Posting Enable WPE=0, Write Posting is disabled WPE=1, Write Posting is enabled
MEMFREQ	Memory Clock Frequency – controls the CLKMEM output clock frequency: Value CLKMEM frequency 000 DSP CPU CLKOUT frequency 001 DSP CPU CLKOUT frequency /2 Other Reserved

NOTE: MEMFREQ should be changed when MEMCEN = 0.

3.2 EMIF Global Reset Register

Any write to this register will cause a reset of the EMIF state machine, but does not change the current configuration values. This register cannot be read (see Figure 9).

Figure 9. C55x EMIF Global Reset Register

3.3 EMIF Bus Error Status Register

For asynchronous timeout errors, the EMIF Bus Error Status Register displays the source of the error. The register bit fields are shown in Figure 10, and bit descriptions are given in Table 8. One bit in the range [6:0] is set to indicate the bus source of the error. The CEn region, where the error occurred is given by a single bit in the range [7:10]. A timeout error is indicated by bit 12. This is a read only register that is cleared after every read. **This register does not apply to SDRAM**.

			Memory Range				Bus						
15 13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved	TIME	Reserved	CE3	CE2	CE1	CE0	DMA	FBUS	EBUS	DBUS	CBUS	Reserved	PBUS
R, +0	R, +0	R, +0	R, +0	R, +0	R, +0	R, +0	R, +0	R, +0	R, +0	R, +0	R, +0	R, +0	R, +0

Figure 10. EMIF Bus Error Status Register Diagram

Table 8. EMIF Bus Error Status Register Bit Field Description

Field	Description
PBUS	Bus error on PBUS, NO ERROR=0, ERROR=1
CBUS	Bus error on CBUS, NO ERROR=0, ERROR=1
DBUS	Bus error on DBUS, NO ERROR=0, ERROR=1
EBUS	Bus error on EBUS, NO ERROR=0, ERROR=1
FBUS	Bus error on FBUS, NO ERROR=0, ERROR=1
DMA	Bus error on DMA bus, NO ERROR=0, ERROR=1
CE0	Bus error on CE0 space, NO ERROR=0, ERROR=1
CE1	Bus error on CE1 space, NO ERROR=0, ERROR=1
CE2	Bus error on CE2 space, NO ERROR=0, ERROR=1
CE3	Bus error on CE3 space, NO ERROR=0, ERROR=1
TIME	Asynchronous access timeout, NO ERROR=0, ERROR=1

3.4 C55x CE Space Control Registers

There are four CE spaces supported by the C55x EMIF. Each space is configured by a set of three CE Space Control Registers. The MTYPE field identifies the memory type for the CE space. In CEn Space Control Register 1, bits 14:12, MTYPE=011b selects SDRAM. **The remaining fields in the registers do not apply to SDRAM**. Figure 11, Figure 12, and Figure 13 give the bit arrangements for the CE Space Control Registers. Table 9 contains detailed descriptions of the configuration fields.

15	14 12	11 8	7 2	1 0
Reserved	**MTYPE**	READ SETUP	READ STROBE	READ HOLD
R, +0	RW, +010	RW, +1111	RW, +111111	RW, +11

Figure 11. C55x EMIF CEn Space Control Register 1

15	14 12	11 8	7 2	1 0
EXTENDED HOLD READ	EXTENDED HOLD WRITE	WRITE SETUP	WRITE STROBE	WRITE HOLD
R, +01	RW, +01	RW, +1111	RW, +111111	RW, +11

Figure 12. C55x EMIF CEn Space Control Register 2

15 8	7 0
Reserved	TIMEOUT
R, +00000000	RW, +00000000

Figure 13. C55x EMIF CEn Space Control Register 3

Table 9. EMIF CEn Space Control Registers Field Description

Field	Description
READ SETUP WRITE SETUP	Setup width. Number of DSP clock cycles of setup for address, chip enable ($\overline{CE}$) and byte enables ($\overline{BE}$[0–3]) before read strobe ($\overline{ARE}$) or write strobe ($\overline{AWE}$) falls. For asynchronous read access, this is also the setup time of $\overline{AOE}$ before $\overline{ARE}$ falls.
READ STROBE WRITE STROBE	Strobe width. The widths of read strobe ($\overline{ARE}$) and write strobe ($\overline{AWE}$) in DSP clock cycles.
READ HOLD WRITE HOLD	Hold width. Number of DSP clock cycles that address and byte strobes ($\overline{BE}$(0–3) are held after read strobe ($\overline{ARE}$) or write strobe ($\overline{AWE}$) rises. For asynchronous read accesses, this is the hold time of $\overline{AOE}$ after $\overline{ARE}$ rising.
MTYPE	Memory Type: MTYPE=000b, 8-bit-wide asynchronous interface MTYPE=001b, 16-bit-wide asynchronous interface MTYPE=010b, 32-bit-wide asynchronous interface **MTYPE=011b, 32-bit or 16-bit-wide SDRAM. The SDACC bit in SDRAM Control Register 2 selects between 16 or 32 bits. All SDRAM widths must be the same.** MTYPE=100b, 32-bit wide SBSRAM MTYPE=Other, reserved
Extended Hold Read	Number of DSP clock cycles after the last asynchronous read access in a given region before a write access, or access to a different region, can start. All CEn signals are inactive during this period. Add 1 to the number to include the automatic 1 cycle between region changes.
Extended Hold Write	Number of DSP clock cycles after the last asynchronous write access in a given region before a Write access or access to a different region can start. All CEn signals are inactive during this period. Add 1 to the number to include the automatic 1 cycle between region changes.
TIMEOUT	Length of the bus error timeout. Only valid when the asynchronous MTYPE is selected. TIMEOUT = 0, bus error timer disabled TIMEOUT = N, bus error signaled after N (between 1 and 255) DSP clock cycles.

3.5 EMIF SDRAM Control Registers

The SDRAM Control Registers control SDRAM parameters for all CEn spaces that specify an SDRAM memory type in the MTYPE field of its associated CEn Space Control Register 1. Each CEn space with SDRAM should be compatible with the same refresh, timing, and page characteristics. The delay values in the control registers are in CLKMEM cycles. The register bit fields are shown in Figure 14 and Figure 15. Table 10 contains descriptions for the timing parameters configurable within the SDRAM Control Registers. The nonconfigurable SDRAM timing parameters are shown in Table 11.

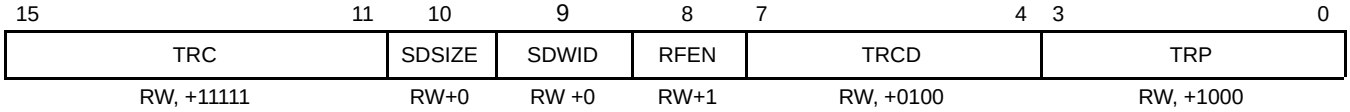

Figure 14. C55x EMIF SDRAM Control Register 1

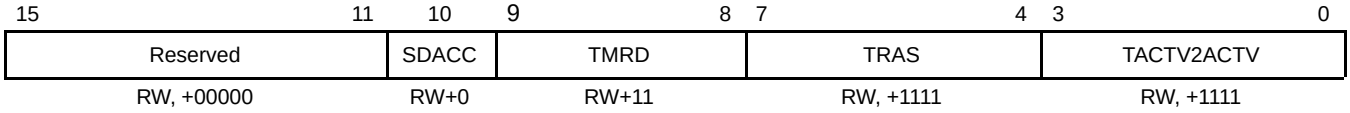

Figure 15. C55x EMIF SDRAM Control Register 2

Table 10. C55x EMIF SDRAM Control Register Field Descriptions

Field	Description
TRC	Specifies Trc ($\overline{\text{SDRAS}}$ Cycle Time) value of the SDRAM in CLKMEM cycles from REFR to REFR/MRS/ACTV command TRC = Trc/SFDCLK – 1
TRP	Specifies Trp ($\overline{\text{SDRAS}}$ Precharge Time) value of the SDRAM in CLKMEM cycles from DCAB to REFR/ACTV/MRS command TRP = (Trp/CLKMEM) – 1
TRCD	Specifies Trcd (Activate to Command or $\overline{\text{SDRAS}}$ to $\overline{\text{SDCAS}}$ Delay) value of the SDRAM in CLKMEM cycles from ACTV to READ/WRITE command TRCD = (Trcd/CLKMEM) – 1
RFEN	Refresh Enable: RFEN = 0, SDRAM refresh disabled RFEN = 1, SDRAM refresh enabled
SDWID	SDRAM Width Select: 0 = x16 width 1 = x32 width
SDSIZE	SDRAM Size Select: 0 = 64 Mbit 1 = 128 Mbit

SDWID	SDSIZE	Type of SDRAM contained by all CE spaces
0	0	4M x 16 bit SDRAMs
1	0	2M x 32 bit SDRAMs
0	1	8M x 16 bit SDRAMs
1	1	4M x 32 bit SDRAMs

Table 10. C55x EMIF SDRAM Control Register Field Descriptions

Field	Description
TRAS	Specifies Tras ($\overline{\text{SDRAS}}$ Active Time) value in CLKMEM clock cycles. TRAS = (Tras/CLKMEM) – 1
TMRD	Specifies Tmrd (Mode Register set to ACTV/DCAB/REFR Delay) value in CLKMEM clock cycles. TMRD = (Tmrd/CLKMEM) – 1
TACTV2ACTV	Specifies Trrd ($\overline{\text{SDRAS}}$ to $\overline{\text{SDRAS}}$ Bank Activate Delay) value in CLKMEM clock cycles. TACTV2ACTV = (Trrd/CLKMEM) – 1
SDACC	SDACC = 0: SDRAM data bus interface is 16 bits wide on D [15:0]. SDACC = 1: SDRAM data bus interface is 32 bits wide on D [31:0]. Use this setting for x32 memories or if two x16 memories are used.

Table 11. Nonconfigurable SDRAM Timing Parameters

Parameter	Description	CLKMEM Cycles
Tcl	CAS latency	3
Trd2dcab	Delay from a READ command to a DCAB command	4
Twr2dcab	Delay from a WRT command to a DCAB command	4
Twr2wr	Delay from a WRT command to another WRT command	1
Trd2rd	Delay from a READ command to another READ command	1
Trd2wr	Delay from a READ command to a WRT command	5
Twr2rd	Delay from a WRT command to a READ command	5

3.6 C55x EMIF SDRAM Period and Counter Registers

The SDRAM Period Register, shown in Figure 16, sets the refresh period in units of CLKMEM cycles. For the minimum refresh period required, consult the SDRAM manufacturer's datasheet. The SDRAM Counter Register, shown in Figure 17, reflects the current value of the refresh counter. Table 12 gives descriptions of the period and counter fields.

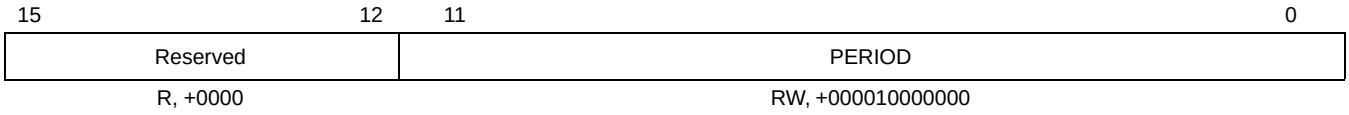

Figure 16. C55x EMIF SDRAM Period Register

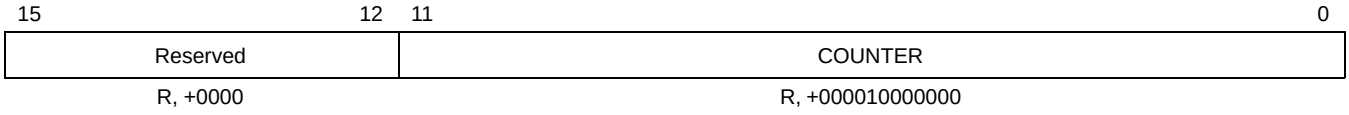

Figure 17. C55x EMIF SDRAM Counter Register

Table 12. C55x EMIF SDRAM Period and Counter Field Description

Field	Description
PERIOD	Refresh period in CLKMEM cycles
COUNTER	Current value of the refresh counter

3.7 C55x EMIF SDRAM Initialization Register

Any write to this register will cause an SDRAM initialization sequence within each CE space configured for SDRAM. After a hardware reset or powering up the C55x device, a write to this register should be performed following configuration of all CE spaces, and prior to accessing SDRAM (see Figure 18). For details on the initialization sequence, refer to SDRAM Initialization.

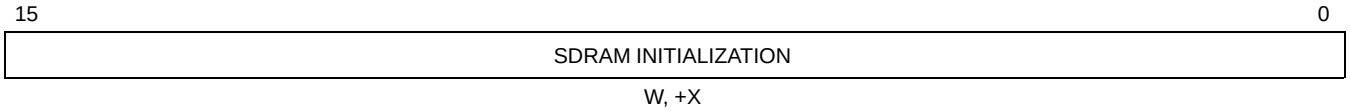

Figure 18. C55x EMIF SDRAM Initialization Register

3.8 C55x Interface to a 64-Mbit (x16) SDRAM

An example of interfacing to a 64-Mbit (4Mx16) SDRAM is shown in Figure 19 and Table 13. Since the limit for a single CE space is 32 Mbits, two CE spaces are used with this particular SDRAM. However, only a single $\overline{\text{CEn}}$ pin corresponding to the beginning of the mapped range is required for use as a chip select for the SDRAM. For this example, only $\overline{\text{CE0}}$ would be connected with $\overline{\text{CE1}}$ left unconnected. The other unused $\overline{\text{CEn}}$ pins (i.e., $\overline{\text{CE2}}$ and $\overline{\text{CE3}}$) can be left unconnected or used for other memory devices.

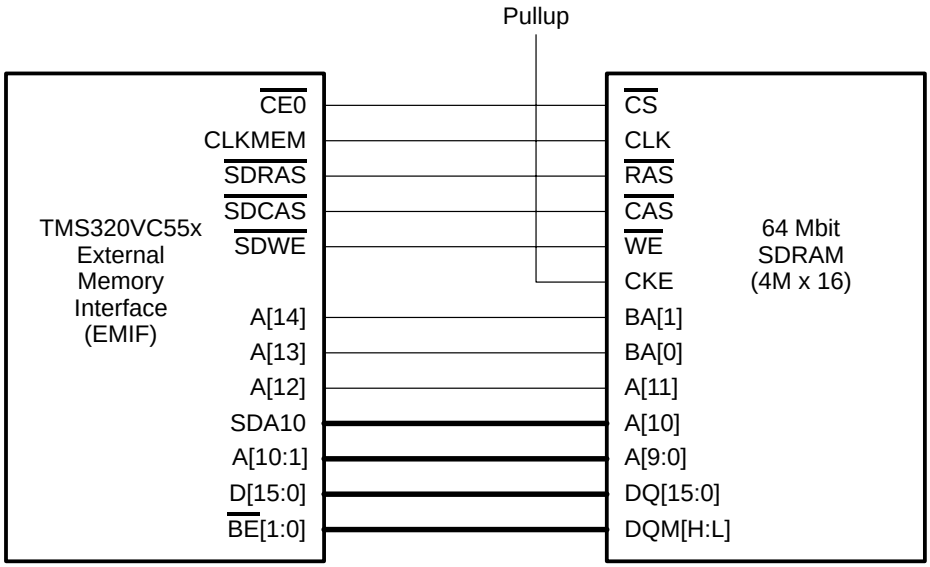

Figure 19. C55x Interface to a 64-Mbit (x16) SDRAM Occupying Two CE Spaces

Table 13. C55x EMIF Configuration for 64-Mbit (x16) SDRAM

SDRAM Size	Array Organization	SDRAM Chips Used	Configuration Bits				CE Spaces Used
			SDACC	SDSIZE	SDWID	MTYPE	
64 Mbit	4M x 16 bit	1	0	0	0	011	2

3.9 C55x Interface to Two 64-Mbit (x16) SDRAMs

An example of interfacing to two 64-Mbit (4Mx16) SDRAMs is shown in Figure 20 and Table 14. This memory configuration will occupy all four 32-Mbit CE spaces with some possible limitations at the bottom and top of the memory map. See the device datasheet for details on these limits for a particular TMS320C55xx device. As in the previous example, only a single $\overline{CEn}$ pin ($\overline{CE0}$) is required for use as a chip select for the SDRAM and the other $\overline{CEn}$ pins ($\overline{CE}$[3:1]) should be left unconnected.

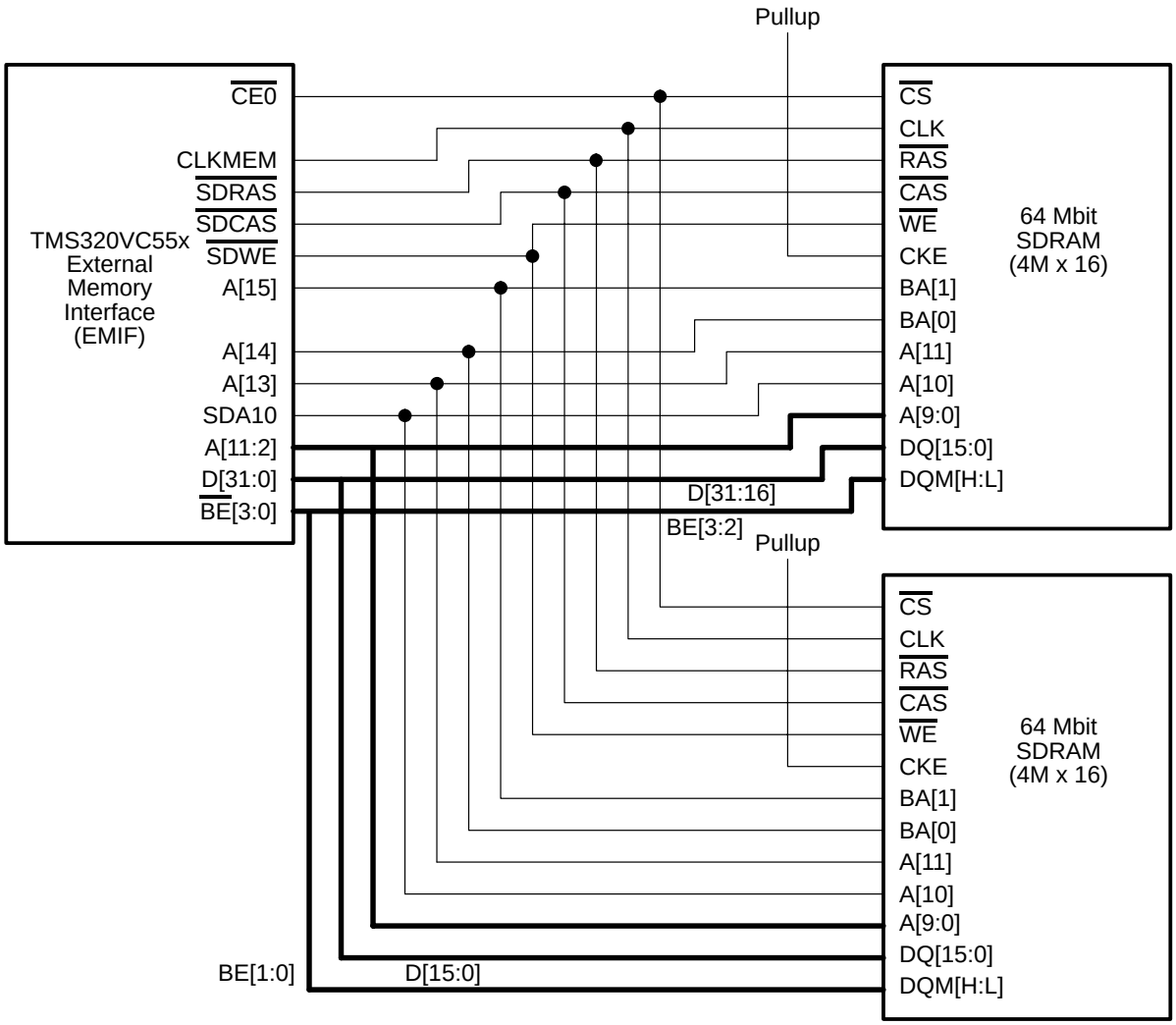

Figure 20. C55x Interface to Two 64-Mbit (x16) SDRAMs Occupying All CE Spaces

Table 14. C55x EMIF Configuration for Two 64-Mbit (x16) SDRAMs

SDRAM Size	Array Organization	SDRAM Chips Used	Configuration Bits				CE Spaces Used
			SDACC	SDSIZE	SDWID	MTYPE	
64 Mbit	4M x 16 bit	2	1	0	1	011	4

3.10 C55x Interface to a 64-Mbit (x32) SDRAM

The next example, shown in Figure 21 and Table 15, uses a single 64-Mbit (x32) SDRAM. Two CE spaces are required with the $\overline{CE0}$ space output connected to the SDRAM and $\overline{CE1}$ left unconnected.

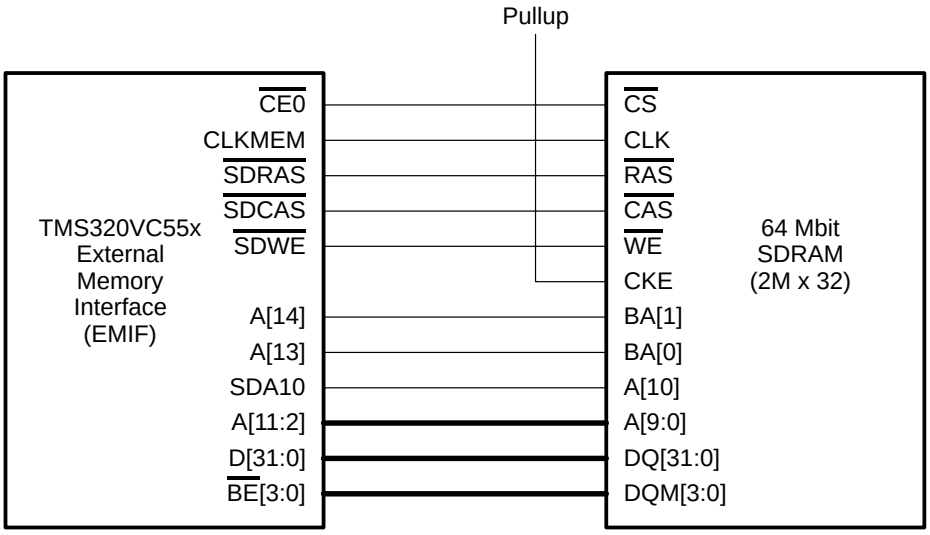

Figure 21. C55x Interface to a 64-Mbit (x32) SDRAM Occupying Two CE Spaces

Table 15. C55 EMIF Configuration for 64-Mbit (x32) SDRAM

SDRAM Size	Array Organization	SDRAM Chips Used	Configuration Bits				CE Spaces Used
			SDACC	SDSIZE	SDWID	MTYPE	
64 Mbit	2M x 32 bit	1	1	0	1	011	2

3.11 C55x Interface to Two 64-Mbit (x32) SDRAMs

An example of two 64-Mbit (2M x32) SDRAMs connected to the C55x EMIF is given in Figure 22 and Table 16. Both SDRAMs require the use of two $\overline{CEn}$ memory spaces. Only single $\overline{CEn}$ pins ($\overline{CE0}$ and $\overline{CE2}$) are needed to separately select the SDRAMs. The unneeded $\overline{CEn}$ pins ($\overline{CE1}$ and $\overline{CE3}$) should be left unconnected.

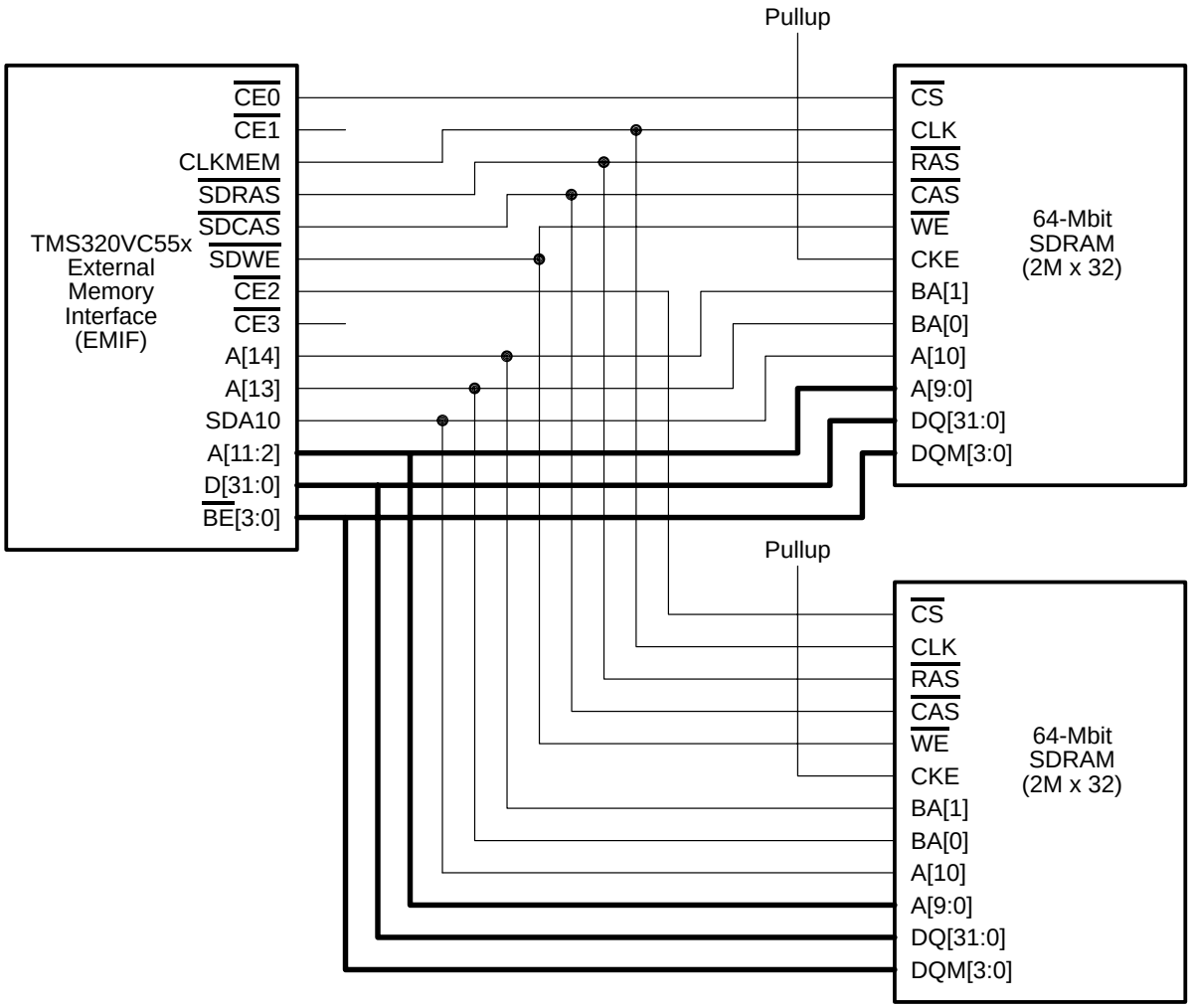

Figure 22. C55x Interface to Two 64-Mbit (x32) SDRAMs Occupying All CE Spaces

Table 16. C55x EMIF Configuration for Two 64-Mbit (x32) SDRAMs

SDRAM Size	Array Organization	SDRAM Chips Used	Configuration Bits				CE Spaces Used
			SDACC	SDSIZE	SDWID	MTYPE	
64 Mbit	2M x 32 bit	2	1	0	1	011	4

3.12 C55x Interface to a 128-Mbit (x16) SDRAM

A single 128-Mbit (8M x16) SDRAM interfaced to the C55x EMIF is shown in Figure 23 and Table 17. All $\overline{CE}$[3:0] memory spaces are occupied with $\overline{CE0}$ used as the SDRAM chip select and $\overline{CE}$[3:1] left unconnected.

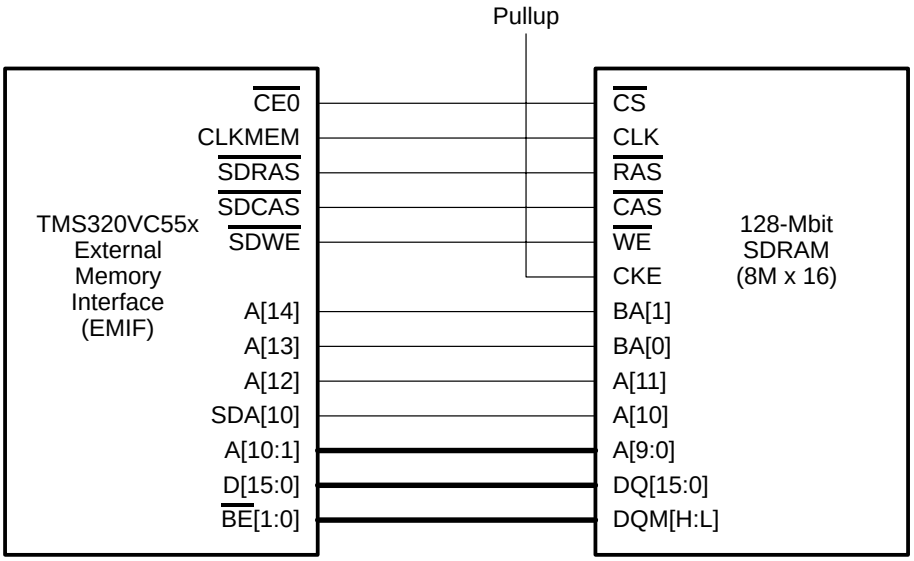

Figure 23. C55x Interface to a 128-Mbit (x16) SDRAM Occupying All CE Spaces

Table 17. C55x EMIF Configuration for 128-Mbit (x16) SDRAM

SDRAM Size	Array Organization	SDRAM Chips Used	Configuration Bits				CE Spaces Used
			SDACC	SDSIZE	SDWID	MTYPE	
128 Mbit	8M x 16 bit	1	0	1	0	011	4

3.13 C55x Interface to a 128-Mbit (x32) SDRAM

A single 128-Mbit (4M x32) SDRAM interfaced to the C55x EMIF is shown in Figure 24 and Table 18. All $\overline{CE}$[3:0] memory spaces are occupied with $\overline{CE0}$ used as the SDRAM chip select and $\overline{CE}$[3:1] left unconnected.

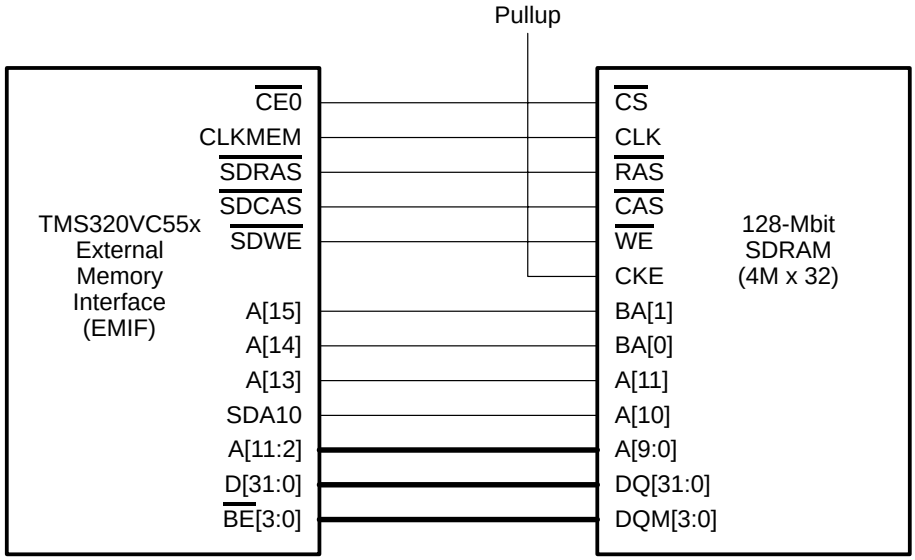

Figure 24. C55x Interface to a 128-Mbit (x32) SDRAM Occupying All CE Spaces

Table 18. C55x EMIF Configuration for 128-Mbit (x32) SDRAM

SDRAM Size	Array Organization	SDRAM Chips Used	Configuration Bits				CE Spaces Used
			SDACC	SDSIZE	SDWID	MTYPE	
128 Mbit	4M x 32 bit	1	1	1	1	011	4

3.14 Example SDRAMs for Use With TMS320C55x Devices

Memories compatible with the Intel PC SDRAM Specification should be compatible with the C55x EMIF. However, the latest manufacturer's datasheets should be consulted prior to system implementation. Table 19 shows some SDRAMs from various manufacturers that meet the sizes supported by the C55x EMIF, and that are also compliant with Intel PC SDRAM Specification.

Table 19. Example SDRAMs for Use With C55x EMIF

Size	Arrangement	Manufacturer	Part Number	Manufacturer's Website
64 Mbit	2M x32	Micron	MT48LC2M32B2	http://www.micron.com
64 Mbit	2M x32	NEC	mPD4564323	http://www.nec.com
64 Mbit	2M x32	Hyundai	HY57V653220B	http://www.hyundai.com
64 Mbit	2M x32	Samsung	K4S643232C	http://www.samsung.com
64 Mbit	4M x16	Micron	MT48LC4M16A2	http://www.micron.com
128 Mbit	4M x32	Micron	MT48LC4M32B2	http://www.micron.com
128 Mbit	8M x16	Micron	MT48LC8M16A2	http://www.micron.com

4 References

1. *TMS320C55x Peripherals Reference Guide* (SPRU317)
2. *TMS320VC5510, Fixed-Point DSP* (SPRS076)
3. PC SDRAM Specification, Rev. 1.7, November 1999, Intel Corp.
4. MT48LC2M32B2, 64-Mb: x32 SDRAM, Rev. 4/00, Micron Semiconductor Products, Inc.
5. MT48LC4M16A2, 64-Mb: x16 SDRAM, Rev. 11/99, Micron Semiconductor Products, Inc.
6. MT48LC4M32B2, 12-8Mb: x32 SDRAM, Rev. 9/00, Micron Semiconductor Products, Inc.
7. MT48LC8M16A2, 128-Mb: x16 SDRAM, Rev. 11/99, Micron Semiconductor Products, Inc.

Appendix A C55x EMIF Block Diagram

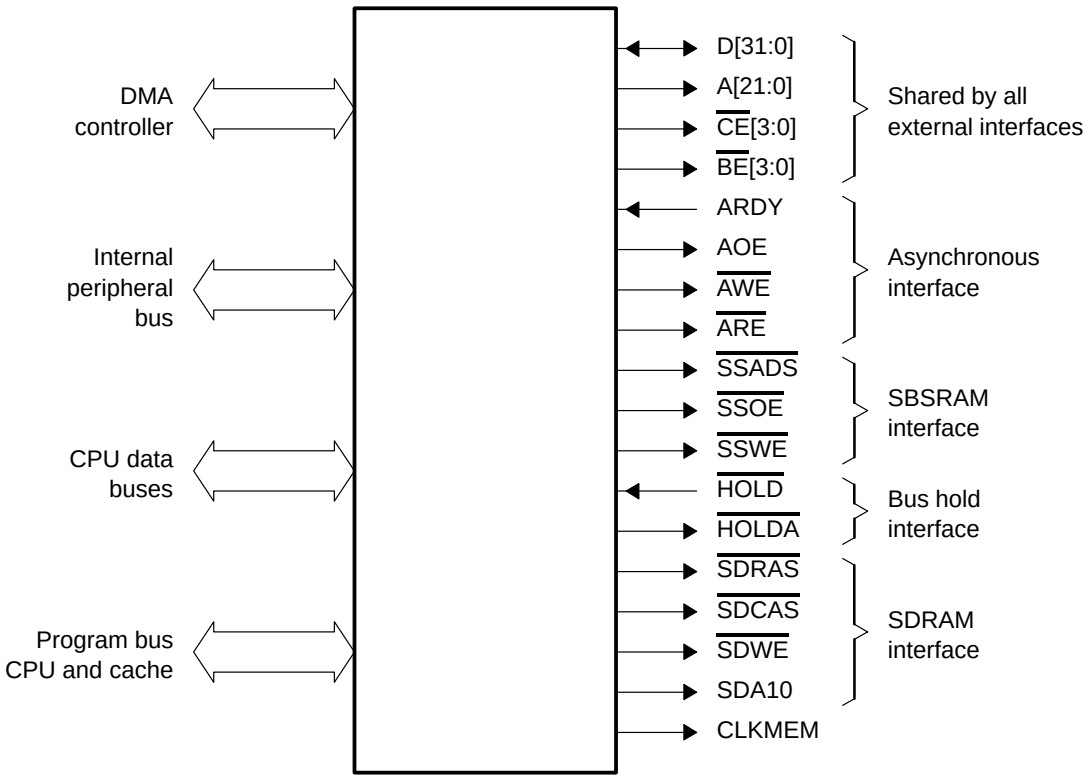

Figure A–1. C55x EMIF Block Diagram

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