EE141- Spring 2002
Introduction to Digital Integrated Circuits

Tu-Th 2:00-3:30pm

203 McLaughlin

What is this class about?

- **Introduction to digital integrated circuits.**
  - » CMOS devices and manufacturing technology. CMOS inverters and gates. Propagation delay, noise margins, and power dissipation. Sequential circuits. Arithmetic, interconnect, and memories. Programmable logic arrays. Design methodologies.
- **What will you learn?**
  - » Understanding, designing, and optimizing digital circuits with respect to different quality metrics: cost, speed, power dissipation, and reliability

Digital Integrated Circuits

- Introduction: Issues in digital design
- The CMOS inverter
- Combinational logic structures
- Sequential logic gates; timing
- Arithmetic building blocks
- Interconnect: R, L and C
- Memories and array structures
- Design methods

Interludium: Administrativia

Instructors

Jan M. Rabaey
jan@eecs.berkeley.edu
Office hours: 231 Cory
Mo 4:00-5:30pm
Tu 1-2pm

Andrei Vladimirescu
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Office hours: 511 Cory
TBD

The TA's

Josie Ammer
Discussion + lab
mjammer@bwrc.eecs.berkeley.edu
Office Hours: 353 Cory
We 10-11:30am

Tufan Karalar
Discussion + lab
tufan@bwrc.eecs.berkeley.edu
Office Hours: 297 Cory
Tu 11am-12:30pm

Jason Hu
Head Lab TA
hujas@bwrc.eecs.berkeley.edu
N.A.

The Web-Site

The sole source of information

http://bwrc.eecs.berkeley.edu/Classes/ee141

- Class and lecture notes
- Assignments and solutions
- Lab and project information
- Exams
- Many other goodies …

Save a tree!

Class Admission

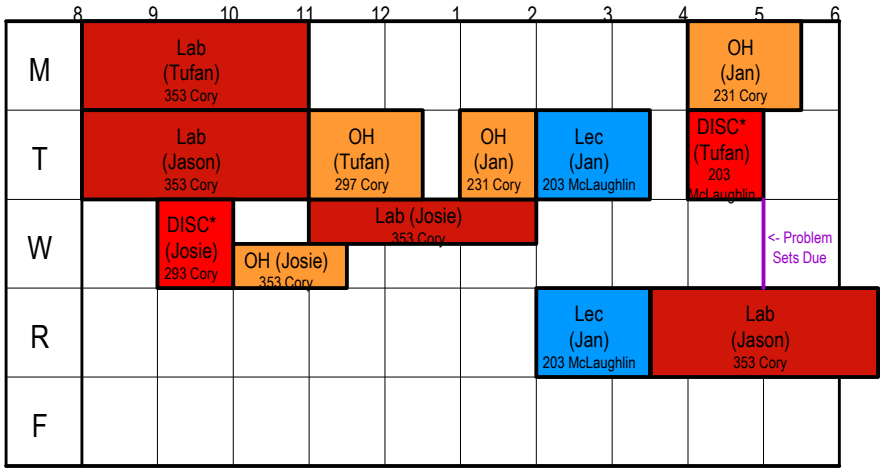
- Class is overenrolled
  - » Class room only seats 65 + 15
  - » But … videotaped
  - » Also webcasted (http://webcast.berkeley.edu)
- Admission priorities
  - » Graduating seniors
  - » First-year grads
  - » Juniors, other grads
  - » Concurrent enrollment

Make sure your name is on the class roll!

Discussions and Labs

- Discussion sessions
  - » Tu 4-5pm, 203 McLaughlin – Tufan
  - » We 9-10am, 293 Cory – Josie
  - » Pick any of the two (the are covering the same material)
- Labs (353 Cory)
  - » Mo 8-11am (Tufan)
  - » Mo 11-2pm -> Th 3:30-6:30pm (Jason)
  - » Tu 8-11am (Jason)
  - » W 11-2pm (Josie)
  - » Pick the one that fits you the best (pending availability) and STICK TO IT!

The EE141 Week at a Glance



* Discussion sections will cover identical material

Class Organization

- 10 Assignments
- A couple of design projects (1 term project)
- Labs: 6 software, 1 hardware
- 2 midterms, 1 final
  - » Midterm 1: Tu, February 6, 6:30-8:30pm
  - » Midterm 2: Th, April 11, 6:30-8:30pm
  - » Final: Fr. May 17, 12:30-3:30pm

Grading Policy

- Homeworks: 10%
- Labs: 10%
- Projects: 20%
- Midterms: 30%
- Final: 30%

Class Material

- Textbook: “Digital Integrated Circuits – A Design Perspective”, by J. Rabaey
- Class notes: Web page + Copy Central (New stuff!)
- Lab Reader:
  - Available on the web page!
  - Selected material will be made available from Copy Central
- Check web page for the availability of tools

Software

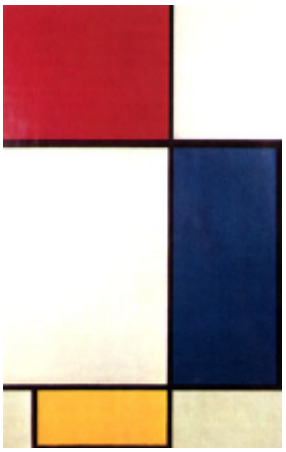
- MicroMagic
  - » Schematic editor: Sue
  - » Layout editor: Max
  - » Online documentation and tutorials
- HSPICE and IRSIM for simulation

Getting Started

- Assignment 1: Getting SPICE to work – see web-page
- NO discussion sessions or labs this week.
- First discussion sessions in Week 2
- First Software Lab in Week 2

Introduction

- Why is designing digital ICs different today than it was before?
- Will it change in future?



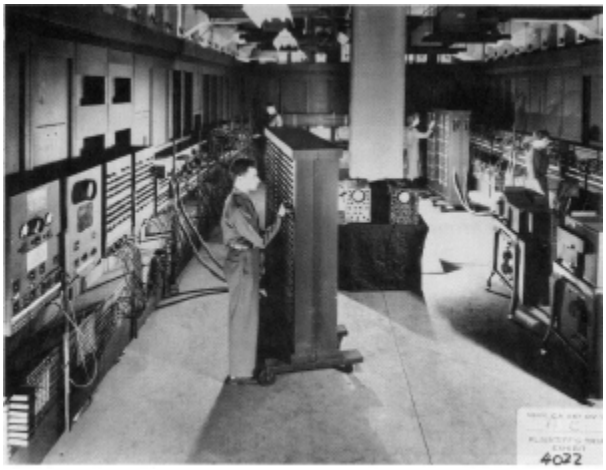
The First Computer

The Babbage Difference Engine (1832)

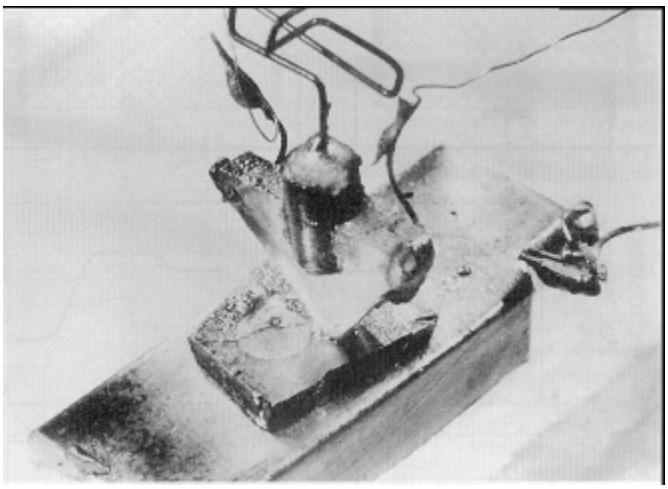
25,000 parts

cost: £17,470

ENIAC - The first electronic computer (1946)

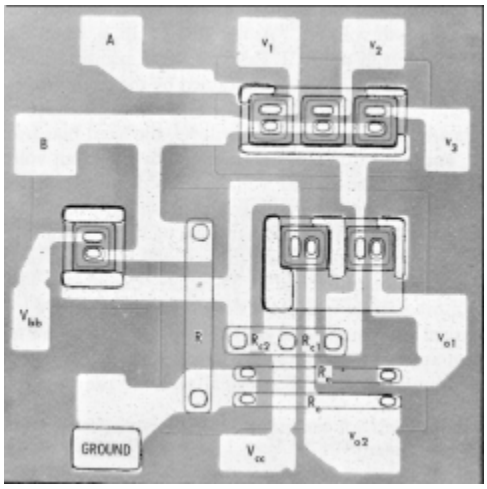


The Transistor Revolution



First transistor
Bell Labs, 1948

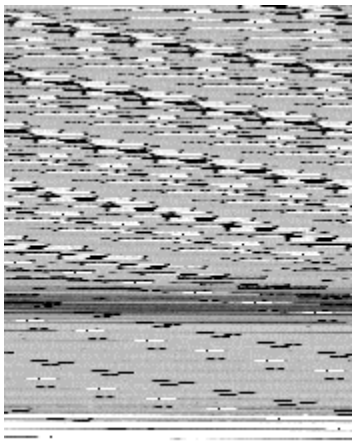
The First Integrated Circuits



Bipolar logic
1960's

ECL 3-input Gate
Motorola 1966

Intel 4004 Micro-Processor

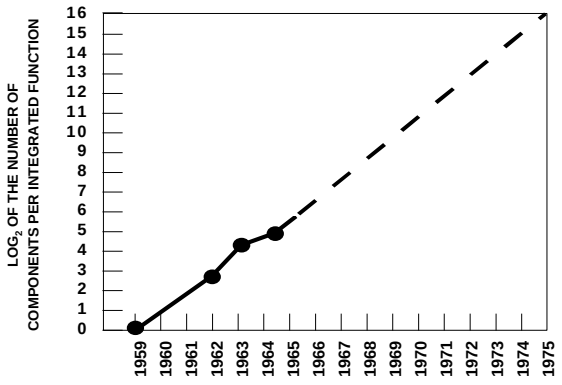


Moore's Law

In 1965, Gordon Moore noted that the number of transistors on a chip doubled every 18 to 24 months.

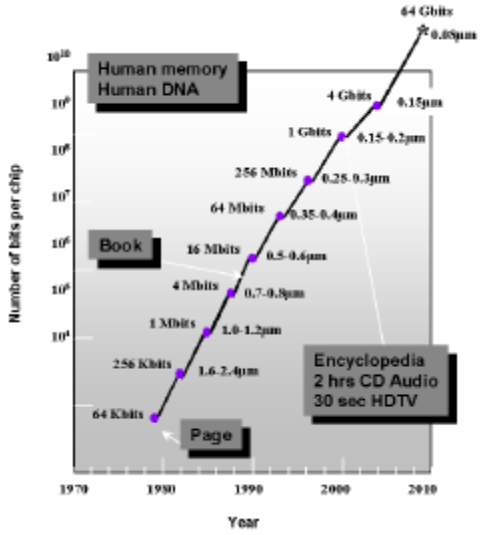
He made a prediction that semiconductor technology will double its effectiveness every 18 months

Moore's Law

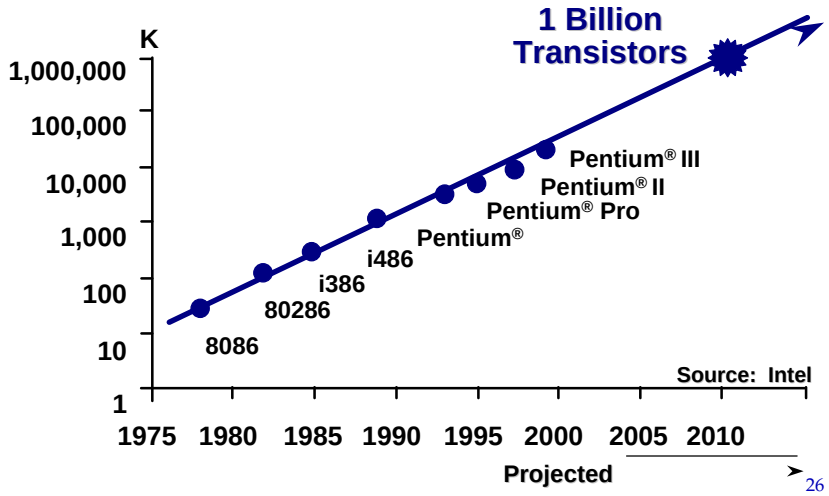


Electronics, April 19, 1965.

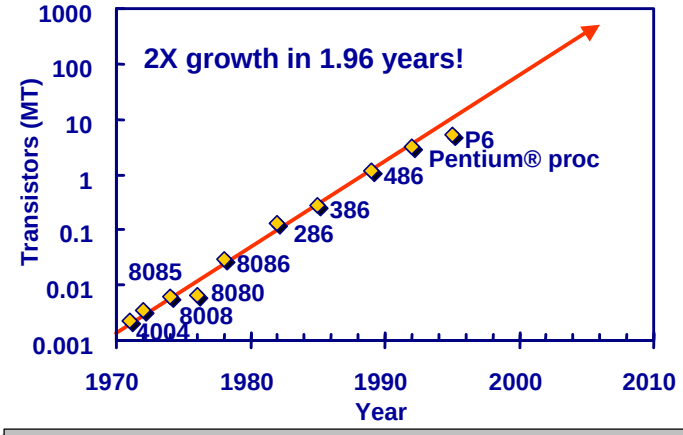
Evolution in Complexity



Transistor Counts



Moore's law in Microprocessors



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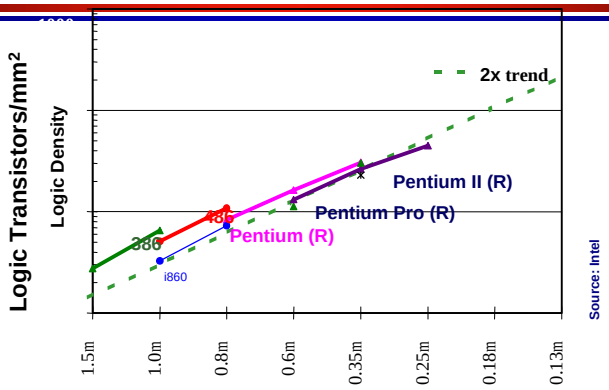
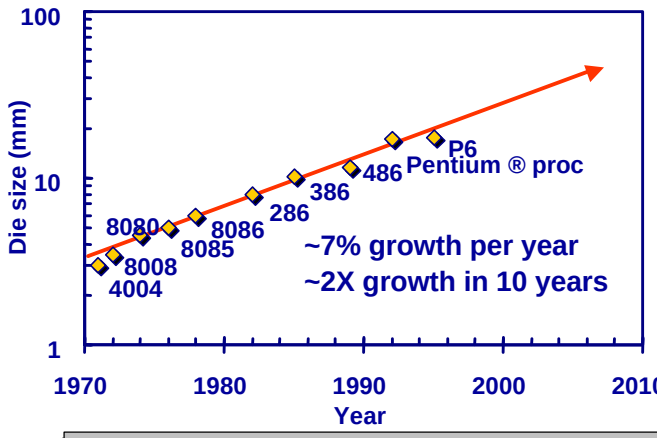
Transistors on Lead Microprocessors double every 2 years

Moore's Law - Logic Density



- Shrinks and compactions meet density goals
- New micro-architectures drop density

Die Size Growth



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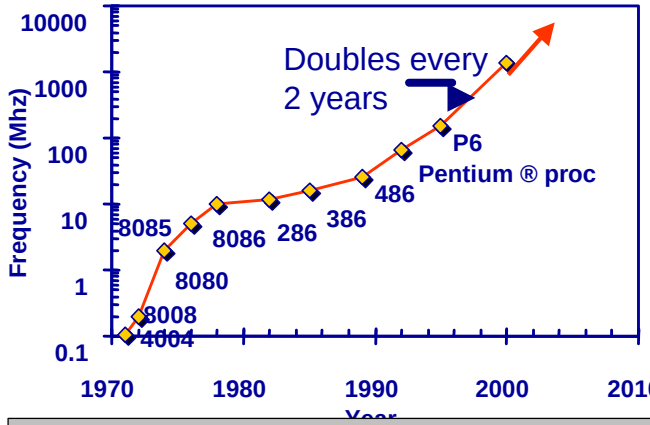
Die size grows by 14% to satisfy Moore's Law

Frequency



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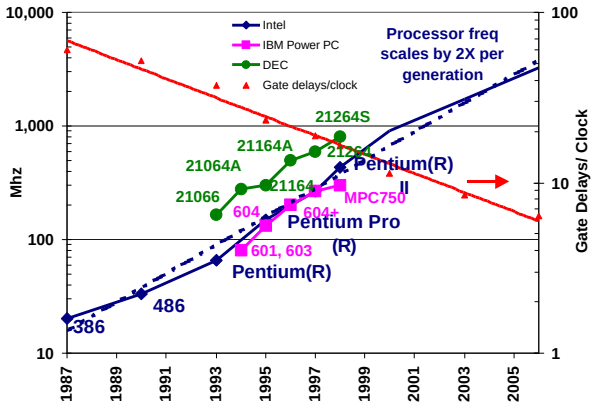
Lead Microprocessors frequency doubles every 2 years

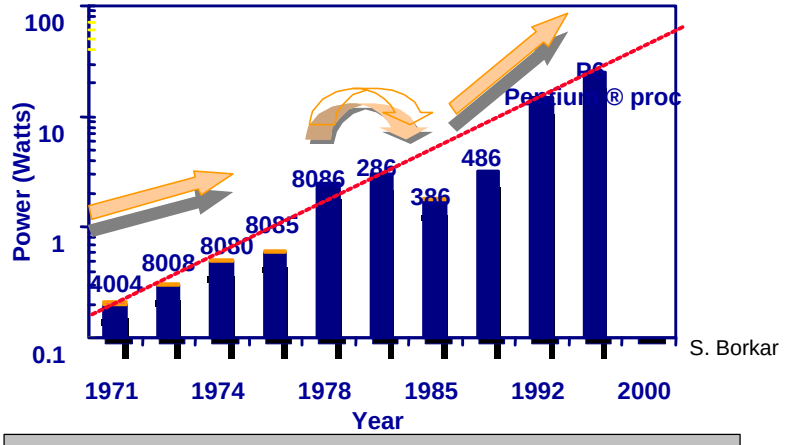
Processor Frequency Trend



V.De, S. Borkar
ISLPED'99

- Frequency doubles each generation
- Number of gates/clock reduce by 25%

Power



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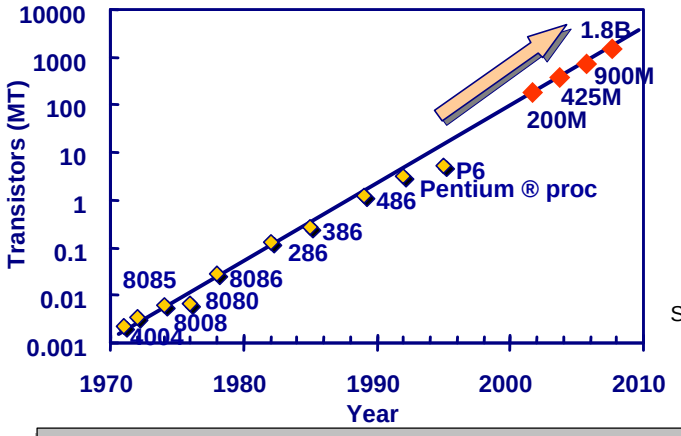
Lead Microprocessors power continues to increase

Obeying Moore's Law…



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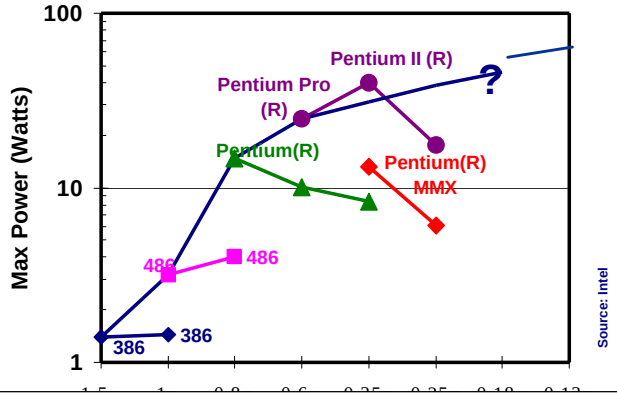
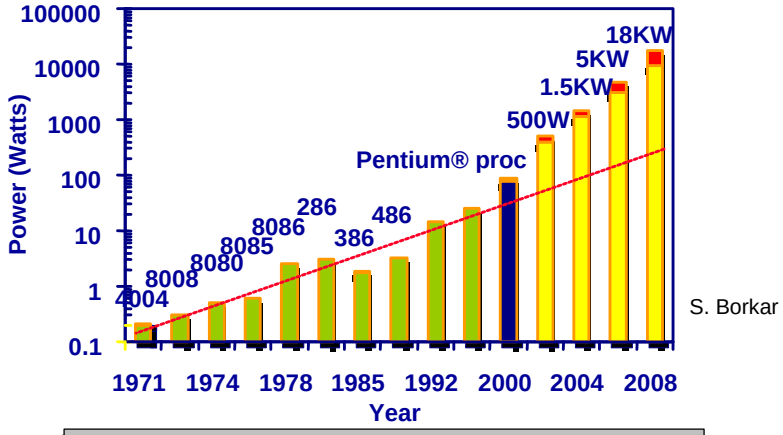
200M--1.8B transistors on the Lead Microprocessor

Processor Power



- Lead processor power increases every generation
- Compactions provide higher performance at lower power

Power will be a problem



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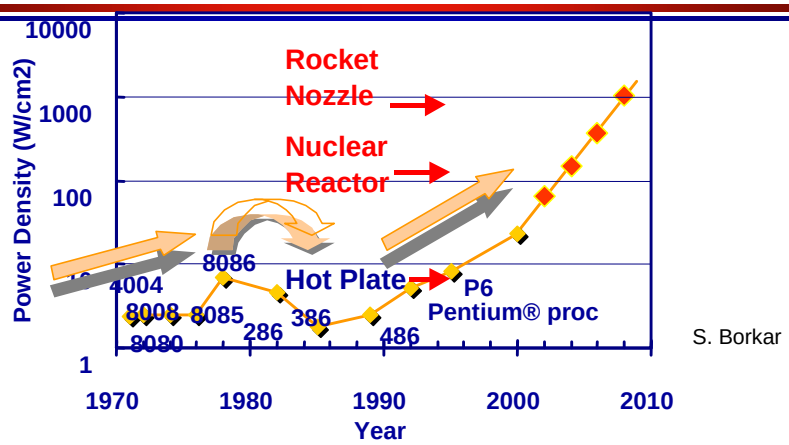
Power delivery and dissipation will be prohibitive

Power density will increase



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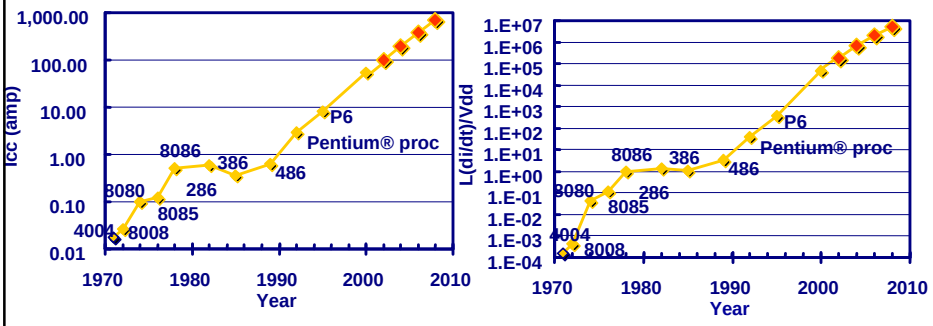
Power density too high to keep junctions at low temp

Power delivery challenges



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High supply currents at low voltage: Challenges: IR drop and L(di/dt) noise

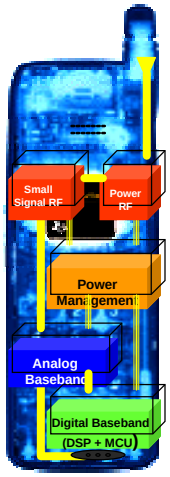
Not Only Microprocessors

Cell Phone

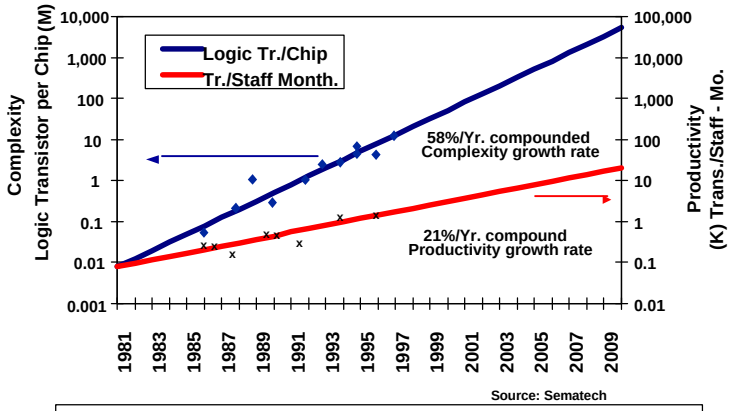
Digital Cellular Market (Phones Shipped)

	1996	1997	1998	1999	2000
Units	48M	86M	162M	260M	435M

(data from Texas Instruments)



Productivity Trends



Complexity outpaces design productivity

Challenges in Digital Design

μ DSM

"Microscopic Problems"

- Ultra-high speed design
- Interconnect
- Noise, Crosstalk
- Reliability, Manufacturability
- Power Dissipation
- Clock distribution.

μ 1/DSM

"Macroscopic Issues"

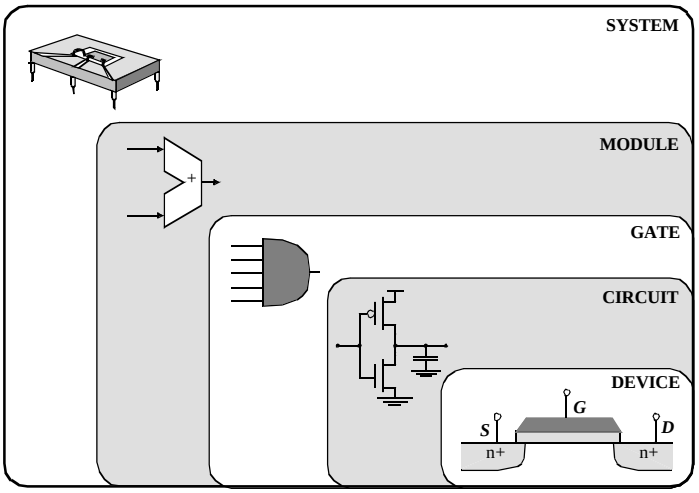
- Time-to-Market
- Millions of Gates
- High-Level Abstractions
- Reuse & IP: Portability
- Predictability
- etc.

Everything Looks a Little Different

?

…and There's a Lot of Them!

Design Abstraction Levels



Why Scaling?

- Technology shrinks by 0.7/generation
- With every generation can integrate 2x more functions per chip; chip cost does not increase significantly
- Cost of a function decreases by 2x
- How to design chips with more and more functions?
- Design engineering population does not double every two years…
- Need to understand different levels of abstraction

Next Class

- Introduces basic metrics for design of integrated circuits – how to measure delay, power, etc.
- Brief intro to IC manufacturing and design