Introduction to LS1 New Dual ARM® Cortex® -A7 Solution

EUF-NET-T0585

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Agenda

- QorIQ LS1 Family Overview and Target Markets
- Positioning the QorIQ LS1 Family
- Deliverables Schedule and Enablement
- Performance Data
- Call to Action
- QorIQ LS1 Family Use Cases
- Core IP Overview
- Trust, Virtualization and Security
- Networking & High Speed IO
- Low Speed IO and Pinout Overview

Comprehensive Portfolio of Embedded Processors Based on ARM Technology

Kinetis Microcontrollers

Design Potential. Realized

Industry's most scalable ultra-low-power, mixed-signal MCU solutions based on the ARM® Cortex™-M and Cortex™-M0+ architectures.

- Consumer
- Industrial

Vybrid Controller Solutions

Rich Apps in Real Time.

Real-time, highly integrated solutions with best-in-class 2D graphics to enable your system to control, interface, connect, secure and scale.

- Consumer
- Industrial
- Automotive

i.MX Application Processors

Your Interface to the World.

Industry's most versatile solutions for multimedia and display applications, with multicore scalability and market-leading power, performance & integration.

- Consumer
- Industrial
- Automotive

QorIQ Processors built on Layerscape Architecture

Accelerating the Network's IQ

Industry's first software-aware, core-agnostic networking system architecture for the smarter, more capable networks of tomorrow – end to end.

- Consumer
- Industrial
- Networking

Freescale has the industry's broadest range of solutions built on ARM® technology for automotive, industrial, consumer and networking applications.

Find your ideal solution at the price, performance and power level you desire, and leverage the extensive software and tool bundles available to speed and ease your design process.

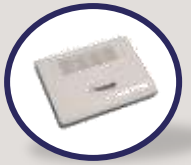
LS1 Processor Family - Target Markets and Applications

Enterprise Networking

- High-speed interfaces
- Security engine
- ECC-protected caches
- Virtualization

Industrial Automation and Control

- Industrial interfaces
- LCD for HMI support
- Industrial protocol support

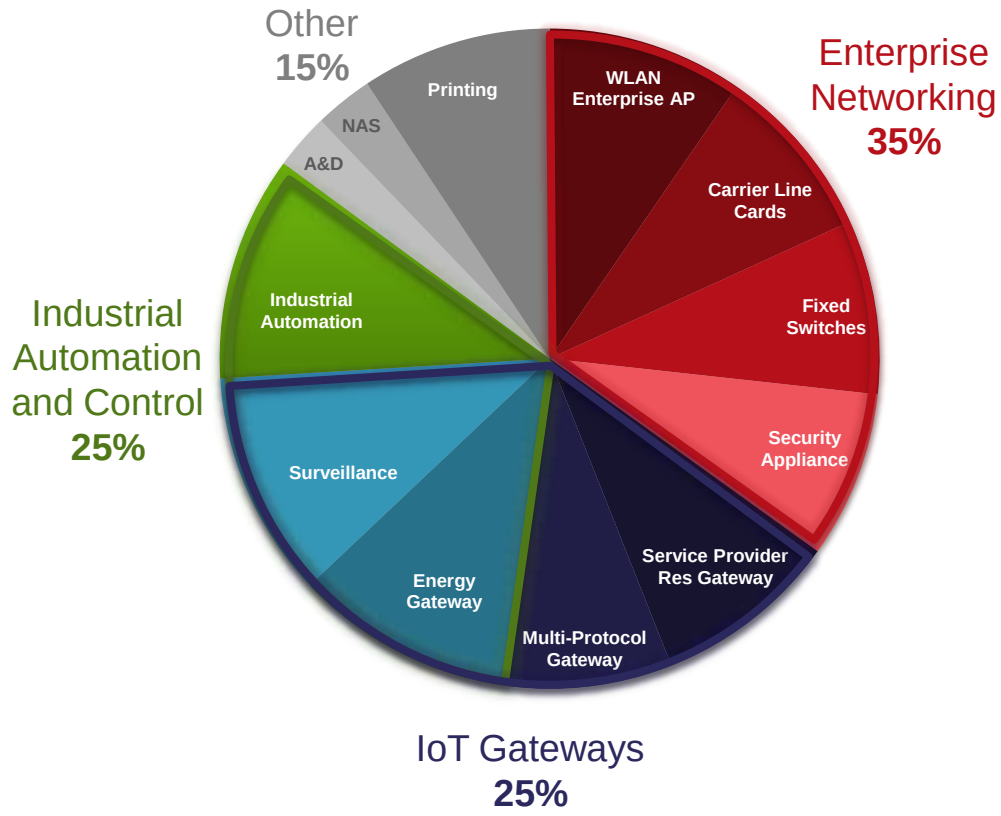


IoT Gateways

- High-speed interfaces
- Multi-protocol support
- High-bandwidth LAN/ WAN support

The LS1 processor family extends Freescale's market leadership

$1.9B SAM in 2015



Source: IDC and IMS Research, World Market for Internet connected Devices, August, 2012

David Kramer, 10/16/13

QorIQ LS1 Processor Family – Differentiated Features

Performance starts with the core

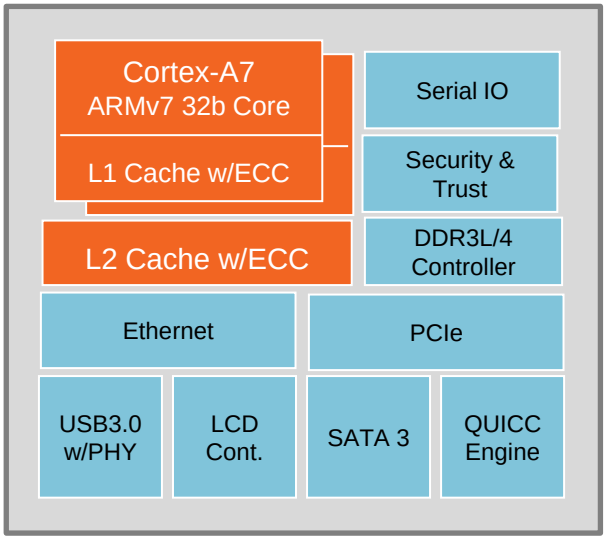
- Dual ARM Cortex-A7 cores delivering **over 6,000 CoreMark®** of performance at **under 3W (typical)** for improved performance without increased power utilization

Defense-in-depth security protection

- **Secure boot**, ARM **TrustZone** and manufacturing protection

Broadest range of peripheral and I/O features in its class

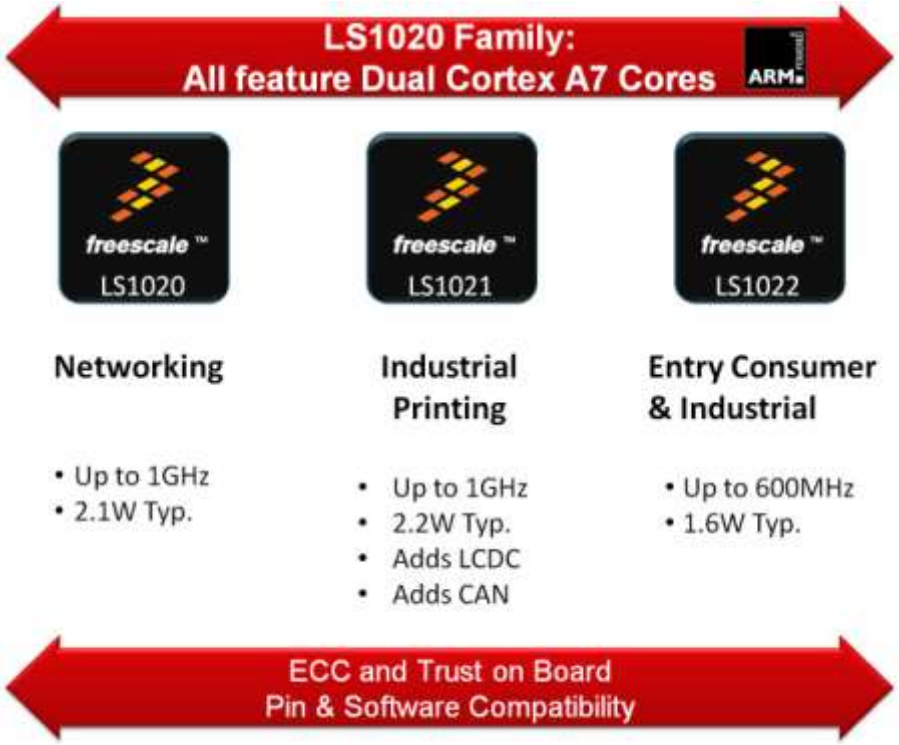
- Only product in its class to offer **ECC protection** for both **L1/L2 caches,** meeting networking requirements for **high reliability**
- **Virtualization support** enables partitioning of CPU resources on low-power parts for increased system productivity
- **First in its class** to offer support for **DDR4** memory ensuring continued **performance efficiency**
- Only communications processor to combine **LCD controller, USB 3.0 with integrated PHY, SD /MMC and SATA3 on a single SoC** to enable lower system-level costs
- **QUICC Engine** provides **proven support** for protocols required in industrial, building and factory automation applications



LS102x Target Applications
Multi-service IoT Gateway
Industrial automation & control
Point of Sale terminals
ATM Machines
Secure Access Point
Hot Spots
Management processor
Smart Energy Gateway
Robotics

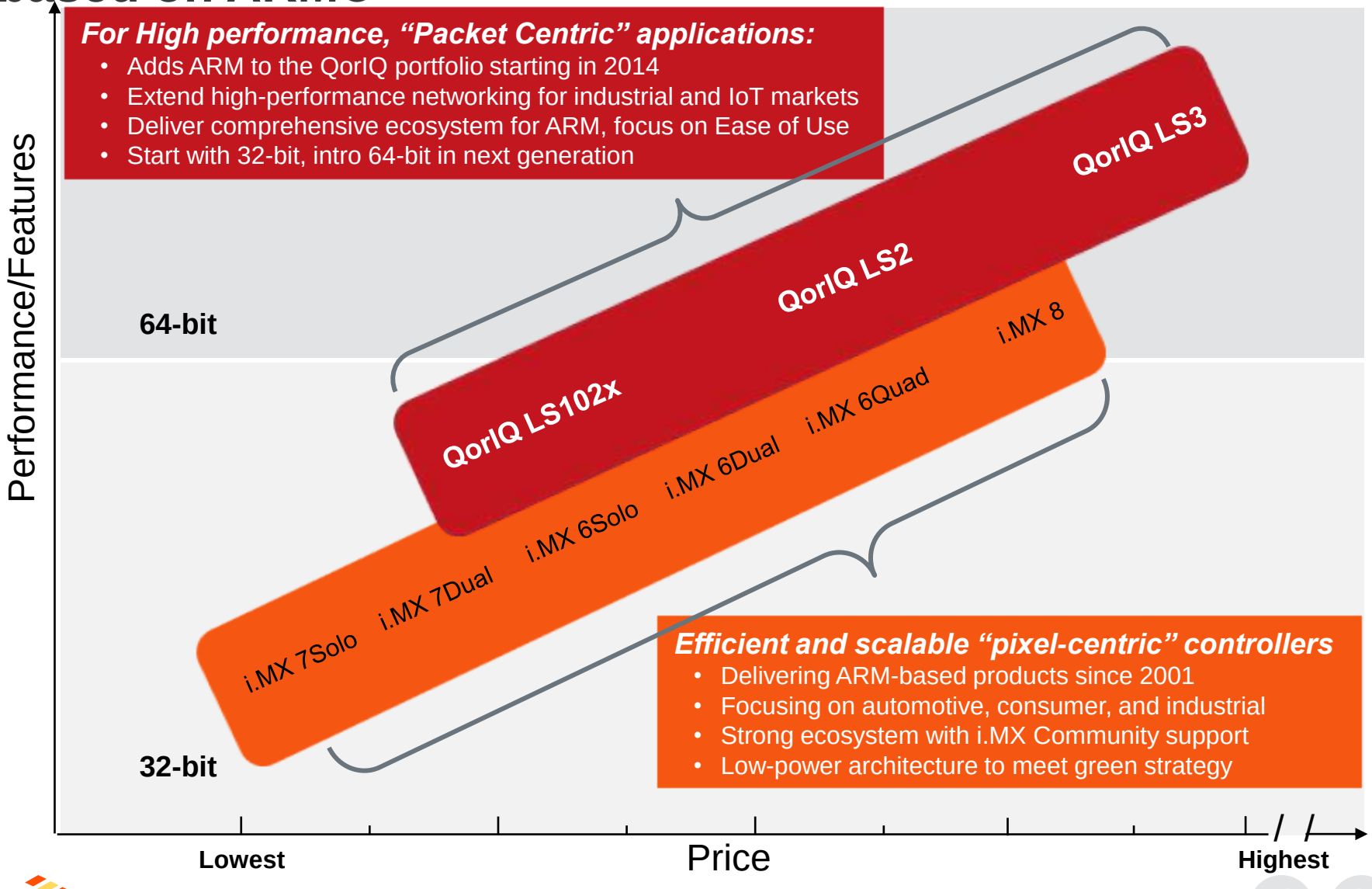
LS102x Product Family Snapshot

	LS1021A	LS1020A	LS1022A
Core Type	ARM Cortex™-A7 MPCore™ + NEON		
Cores/Threads	2 / 2		
Frequency	Up to 1GHz		Up to 600MHz
L1 I/D	32kB / 32kB with ECC		
L2 (Unified)	512kB Shared with ECC		
SRAM	128kB with ECC		
DDR	1x(16/32B +ECC) DDR3L/4 up to 1.6GT/s		DDR3L (8/16B) up to 1.0GT/s
SerDes	4x up to 6.0GHz		1x up to 5GHz
Ethernet	3 x 1GE		2 x 1GE
PCIe	2 x Gen 2.0 (up to 5.0GT/s)		1x Gen 2.0
SATA 3.0	1 up to 6.0GHz		No
USB	1 x USB 3.0 and 1 x USB 2.0		1 x USB 2.0
CAN	Up to 4		Up to 4
TDM/HDLC	2		No
UART/I²C/SPI	Up to 10 / 3 / 2		
I²S	Up to 4		
LCD	1 x Controller	No	
Acceleration	SEC,QE		SEC
	Trusted architecture		
	Pin Compatible 19x19mm, 0.8mm pitch		

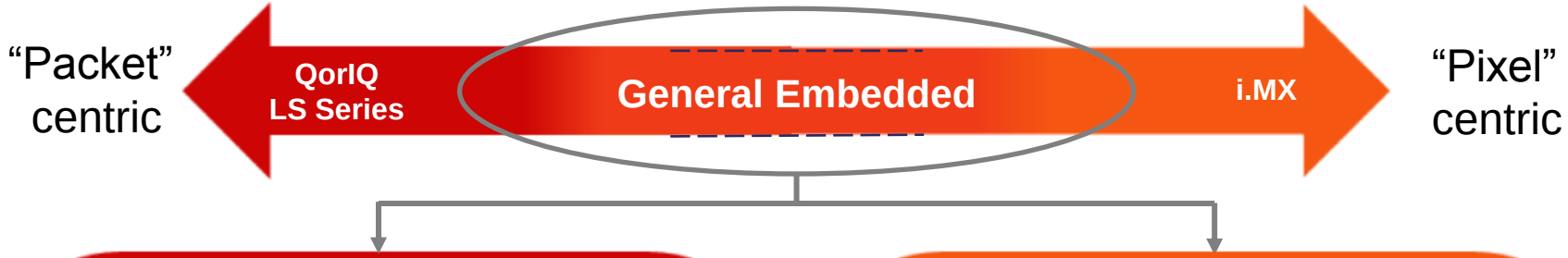


Positioning QorIQ and i.MX Processors

Comparing Price / Performance of Freescale Processors based on ARM®



Customer Application Continuum



Choose QoriQ LS1

when requirements call for:

- Clear choice for *networking applications*
- Support for high bandwidth I/O, coherent PCIe applications & multi-lane SerDes
- Hardware coherency of CPU & accelerators
- High reliability – "always on / always available" enabled by ECC protection
- Application Partitioning and Virtualization
- Security focused performance – security engine, secure boot, Trust Architecture
- Support for industrial protocols: Profibus, RS4xx, others via microcode/QuiccEngine
- Performance focus in a given power envelope and DDR4 support

Choose i.MX

when requirements call for:

- Clear choice for *display-centric* applications
- Graphics acceleration processors
  - 3D, 2D, composition engines
- H/W video acceleration
  - Decode - 1080p60 H.264
  - Encode - 1080p30 H.264
- LPDDR2 enabled battery friendly designs
- Multiple display interfaces
  - RGB, LVDS, HDMI, MIPI
- Camera sensor interfaces
  - Parallel and MIPI
- Microsoft WinCE, Android support needed

LS1 and i.MX6 Security Comparison

- LS1 and i.MX6 support different feature sets of the same compatible Security Engine (SEC)
  - The LS1 SEC engine is *performance* optimized
  - i.MX6 SEC is *power* optimized
- Comparing security protocol throughput performance of both products
  - LS1 SEC raw performance is 5x to 6x higher than i.MX6
- The LS1 SEC engine also features hardware protocol offload support (i.e. IPSec, SSL/TLS) which is not supported by the i.MX6 SEC engine

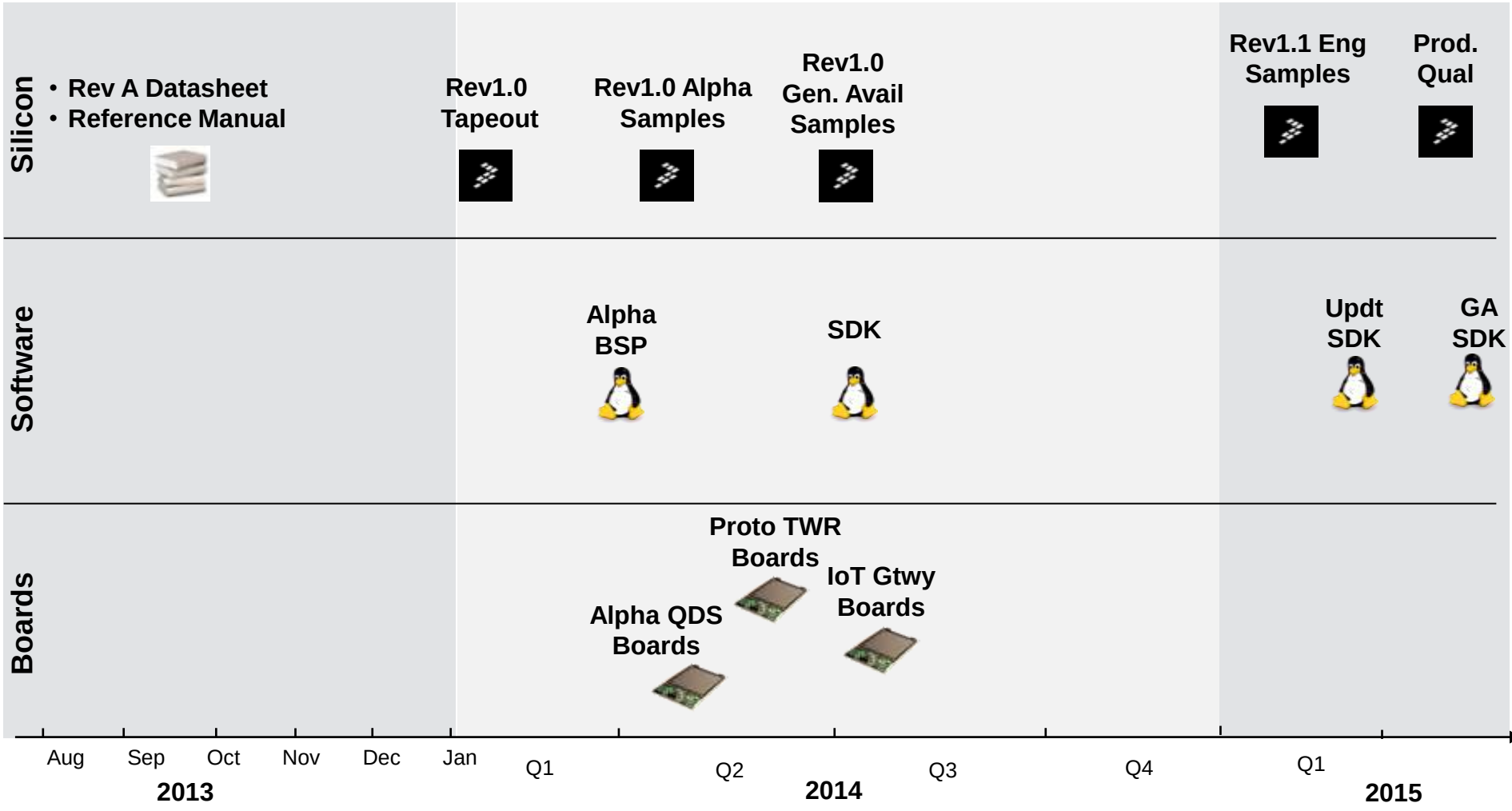
- LS1 raw AES performance is 5x to 6x higher than i.MX6 raw AES performance
- LS1 IPSec performance increases the delta difference (8x to 10x higher compared to i.MX6) since the SEC 5.5 supports IPSec protocol off load

Comparing Features of QoriQ LS1 and i.MX 7 Families

Feature	i.MX 7Solo	i.MX 7Dual	QorIQ LS1022A	QorIQ LS1020A	QoriQ LS1021A
Cores	1x A7 – 1xM0+	2x A7 – 1xM4	2x A7	2x A7	2x A7
Std Temp Freq Ind. Temp Freq	800MHz / 166MHz 500MHz	800MHz / 166MHz	600MHz 600MHz	1GHz 1GHz	1GHz 1GHz
L1/L2 Cache	32K/128K	32K/512K	32K/512K ECC	32K/512K ECC	32K/512K ECC
Memory Interface	LP-DDR2/3 /3L 16-bit 533MHz	LP-DDR2/3/3L 16-bit 533MHz	DDR3L/4 ECC 16-bit 1GHz	DDR3L/4 ECC 32-bit 1.6GHz	DDR3L/4 ECC 32-bit 1.6GHz
Virtualization	N/A	N/A	KVM, IO	KVM, IO	KVM, IO
Threat Protection	Secure Boot / PCIPTS 4.0 compliant	Secure Boot / PCIPTS 4.0 compliant	Secure Boot/ ARM TrustZone PCIPTS 4.0	Secure Boot/ ARM TrustZone PCIPTS 4.0	Secure Boot/ ARM TrustZone PCIPTS 4.0
Accelerators	N/A	N/A	N/A	Security – 2Gbs	Security – 2Gbs
Ethernet Features	2x GbE N/A	2x GbE N/A	2x GbE(line rate) Class/Filter/Fwd	3x GbE(line rate) Class/Filter/Fwd	3x GbE(line rate) Class/Filter/Fwd
Multi-Std SerDes	N/A	1-lane: PCIe2	1-lane: PCIe2, SATA3, SGMII	4-lane: PCIe2, SATA3, SGMII	4-lane: PCIe2, SATA3, SGMII
USB	1x USB2 w/PHY 1xUSB2 HSIC/Host	2xUSB2 w/PHY 1xUSB2 HSIC/Host	1x USB2 ULPI	1x USB3 w/PHY 1x USB2 ULPI	1x USB3 w/PHY 1x USB2 ULPI
Industrial Protocols	N/A	N/A	N/A	HDLC, ProfiBUS, CAN, Ethernet	HDLC, ProfiBUS, CAN, Ethernet
Industrial	Ethernet / CAN	Ethernet / CAN	Ethernet / CAN	Ethernet / Audio	Ethernet / CAN
Camera Interface	20 bit Sensor	20 bit sensor MIPI CSI-2	N/A	N/A	N/A
LCD controller	RGB	RGB, LVDS MIPI-DSI, EPD	N/A	N/A	2D-ACE
Power Management	Full PMIC Embedded	LDO Embedded	N/A	N/A	N/A
Power (Typ)	0.5W	0.8W	2.0W	2.7W	2.8W

Deliverables Schedule and Enablement

QorIQ LS1021A Schedule



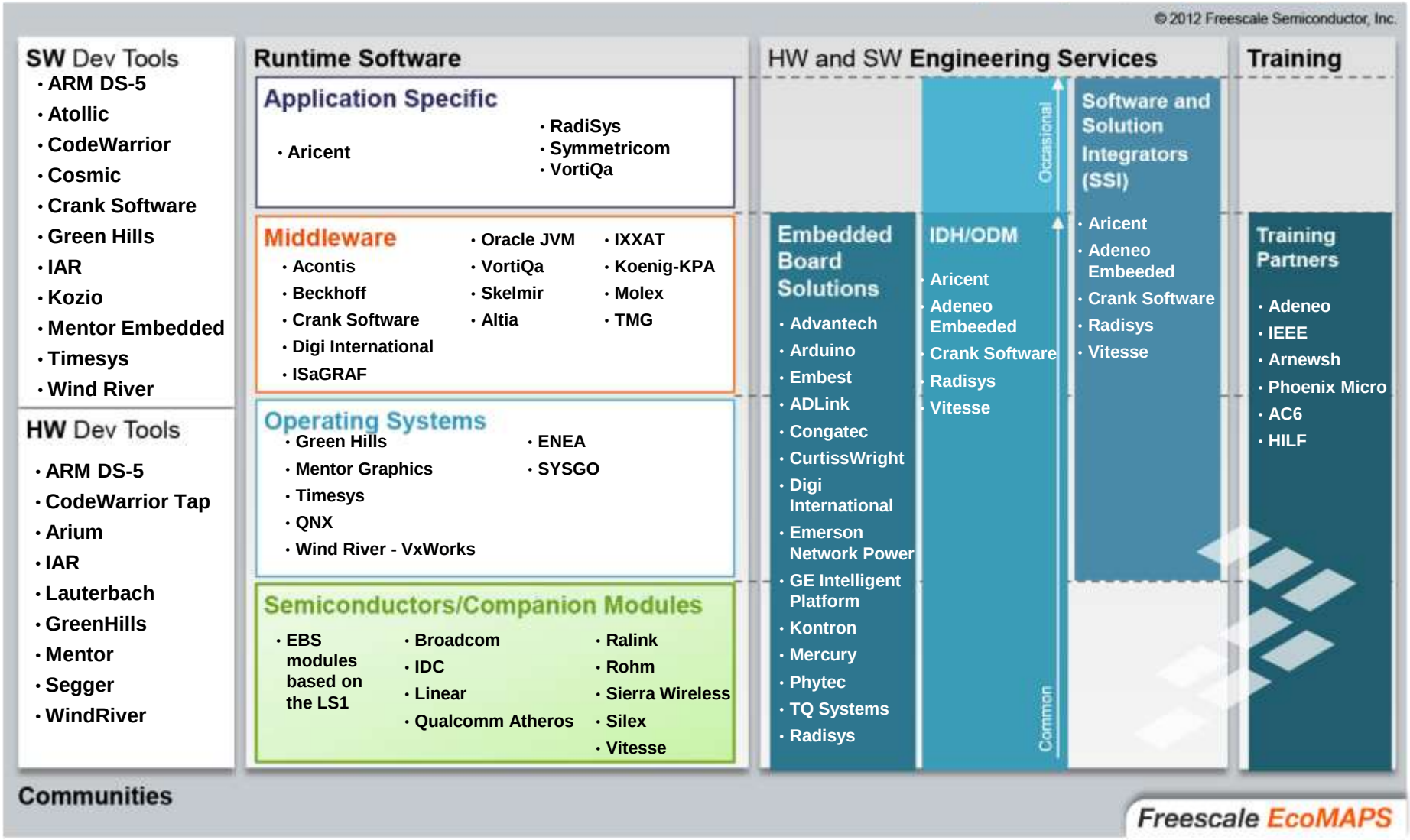
LS1 Family Current Deliverables

LS102xA Family	Version	Availability
LS1021A Reference Manual	Rev. C	Available now
SEC Reference Manual	Rev. A	Available now
LS1021A Hardware Spec	Rev. D	Available now
LS1020A Hardware Spec	Rev. B	Available now
LS1022A Hardware Spec	Rev B	Available now
LS1021A Ball Map	Rev. A	Available now
LS1021A Package Spec.	Rev. A	Available now
LS1021A Product Brief	Rev. A	Available now
TWR-LS1021A Schematics	Rev. A	Available now

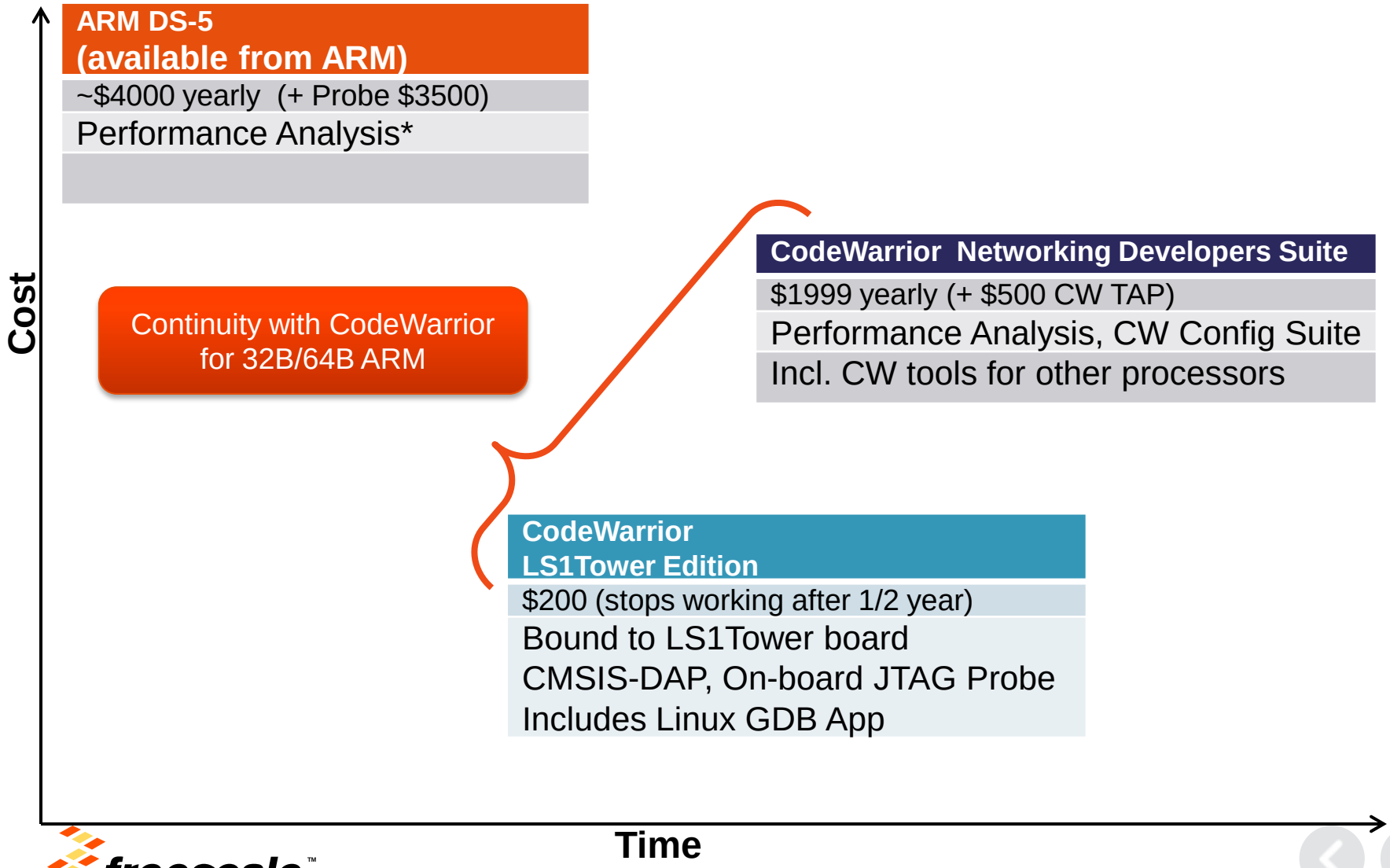
- All now available on: LS1021A Extranet site

EcoMAP: QorIQ LS Series

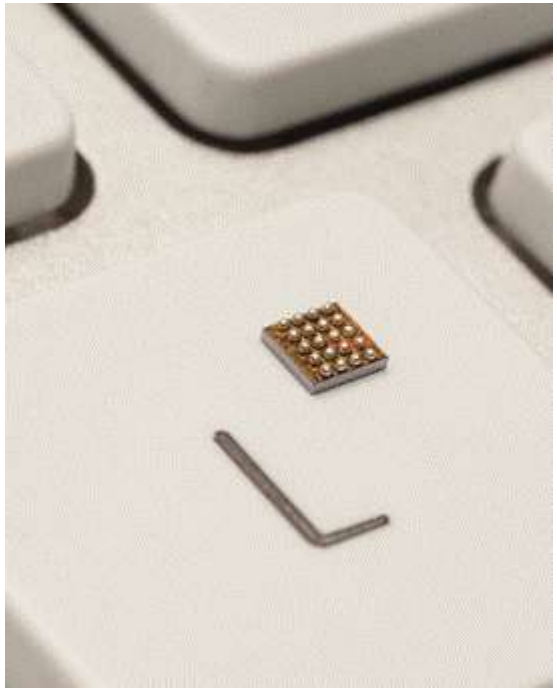
For more partner options, visit freescale.com/partners



ARM Development Tools Roadmap for QorIQ Family



LS1 Family Customer Enablement Boards



Tower-based Evaluation Platform

- **Rapid prototyping platform** for Industrial applications
- **Modular design** supports a range of connectivity options
- **Cost-effective**, open source development platform
- Designed to **simplify product evaluation**

IoT Gateway Reference Design

- **Multi-protocol support** for IoT devices
- **High speed WAN / LAN** for Cloud connectivity
- **Cost-effective**, open source development platform
- Designed to **accelerate time to market**

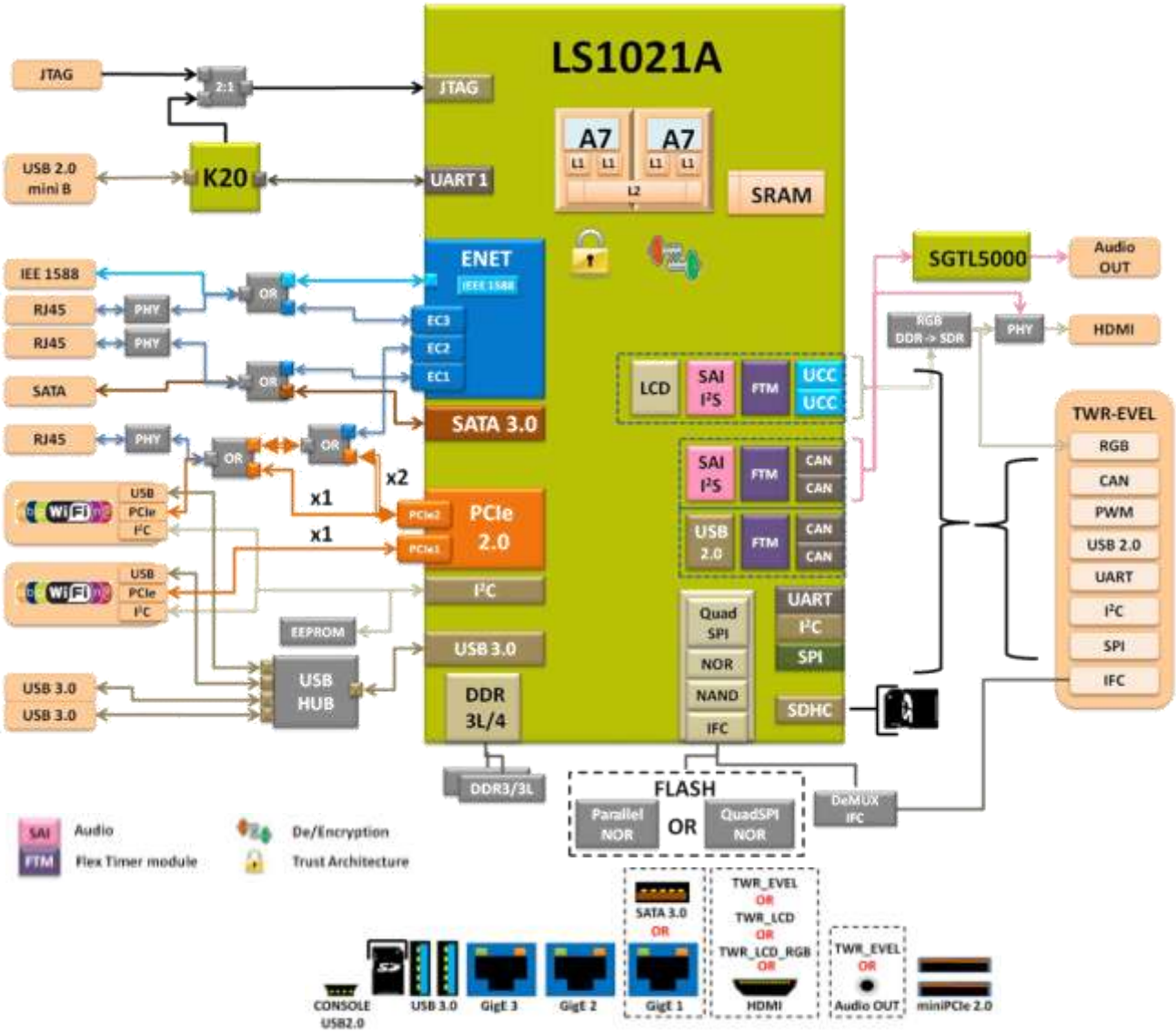
QorIQ LS1 Family Software - Board Support Package (BSP)

Early engineering release for QDS board available April 2014

Functionality Supported:

- **U-Boot**
  - ARM A7 Core initialization in u-boot
  - DDR (static setting)
  - RCW, Serdes
  - UART
  - FlexTimer in u-boot (2-signals output)
  - PCIe RC, Ethernet(e1000)
  - NOR boot
  - I2C and EEPROM
  - DDR (SPD)
  - SD
  - VeTSEC
  - IFC NAND & NOR (Flash programming)
  - USB 2.0
  - NAND boot
  - SD boot
  - ESBC
  - SATA3
  - DSPI driver
- **Linux**
  - ARM A7 Core initialization in kernel
  - DUART in kernel
  - RAMDISK
  - LPUART
  - I2C controller & I2C EEPROMs
  - WDOG
  - eSDHC (SD)
  - DSPI in kernel
  - eDMA & DMAMUX (Same as in Faraday)
  - QE (UART)
  - Power Management (TMU)
  - PCIe (RC mode)
  - eSDHC (SDIO, SDXC)
  - VeTSEC
  - IFC NAND & NOR
  - USB 2.0 (Host, Gadget mode, OTG)
  - GPIO
  - SATA3.0
  - CAAM
  - FlexCAN

TWR-LS1021A Development System



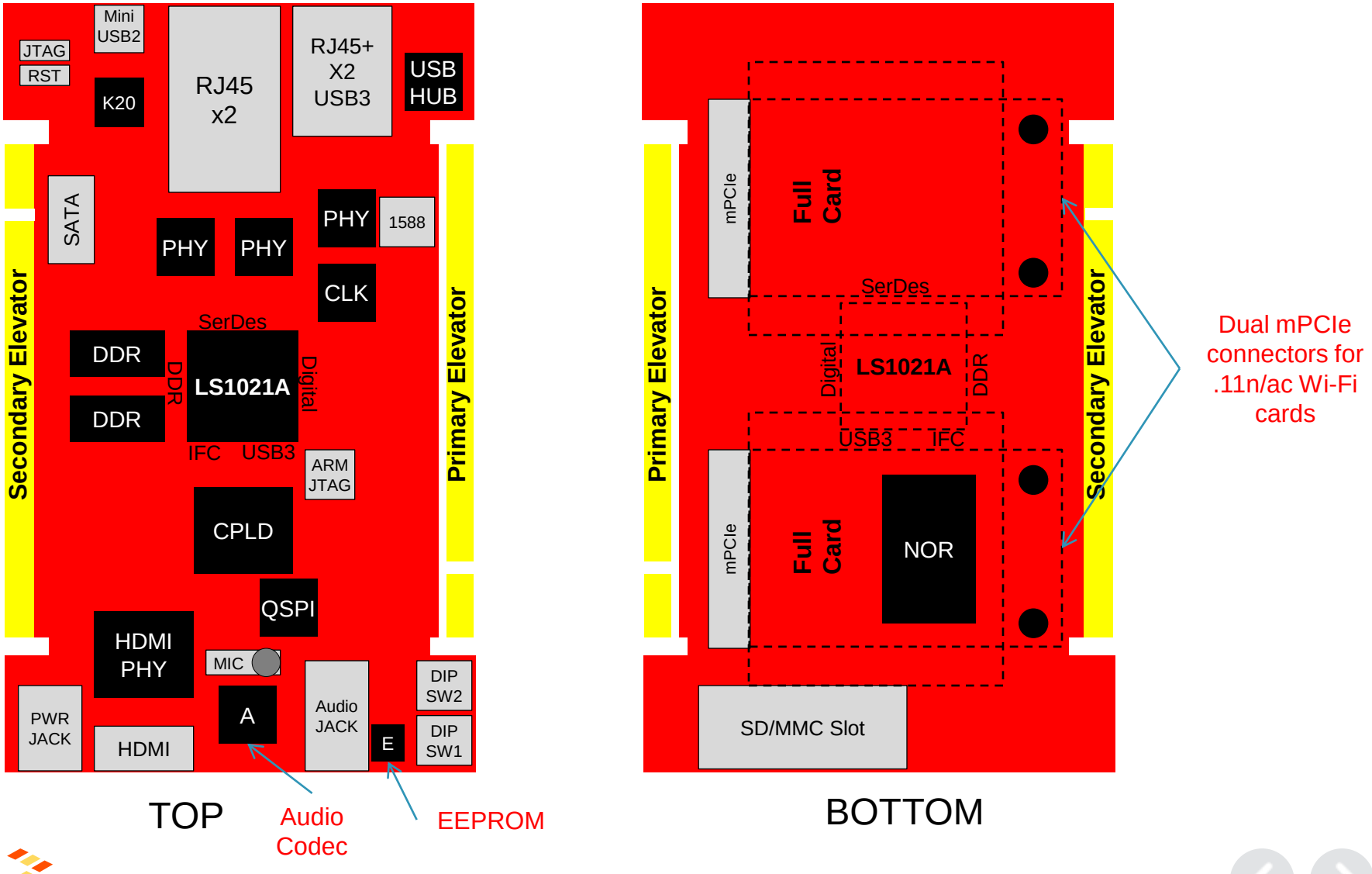
Features

- **Memory**
  - DDR3 1GB
  - Parallel NOR Flash 128MB
    or
    QuadSPI NOR Flash 16MB
- **Connectivity**
  - Up to 3 x RJ45 GigE
  - Up to 1 SATA
  - 2 x USB 3.0
  - 2 x mini PCIe 2.0 (x1 + x1) or (x1 + x2)
  - Display via HDMI or TWR-LCD or TWR-LCD-RGB
  - Audio OUT via HDMI or Jack plug or TWR_EVEL
  - Console port/JTAG via USB 2.0

- **Tower Boards supported via TWR-EVEL**
  - TWR-IND-IO
    2 x CAN, RS485, RS232
    up to 2 boards supported
  - TWR-LCD
  - TWR-LCD-RGB
  - TWR-ETHERCAT-SLV

Generic Connectivity Availability

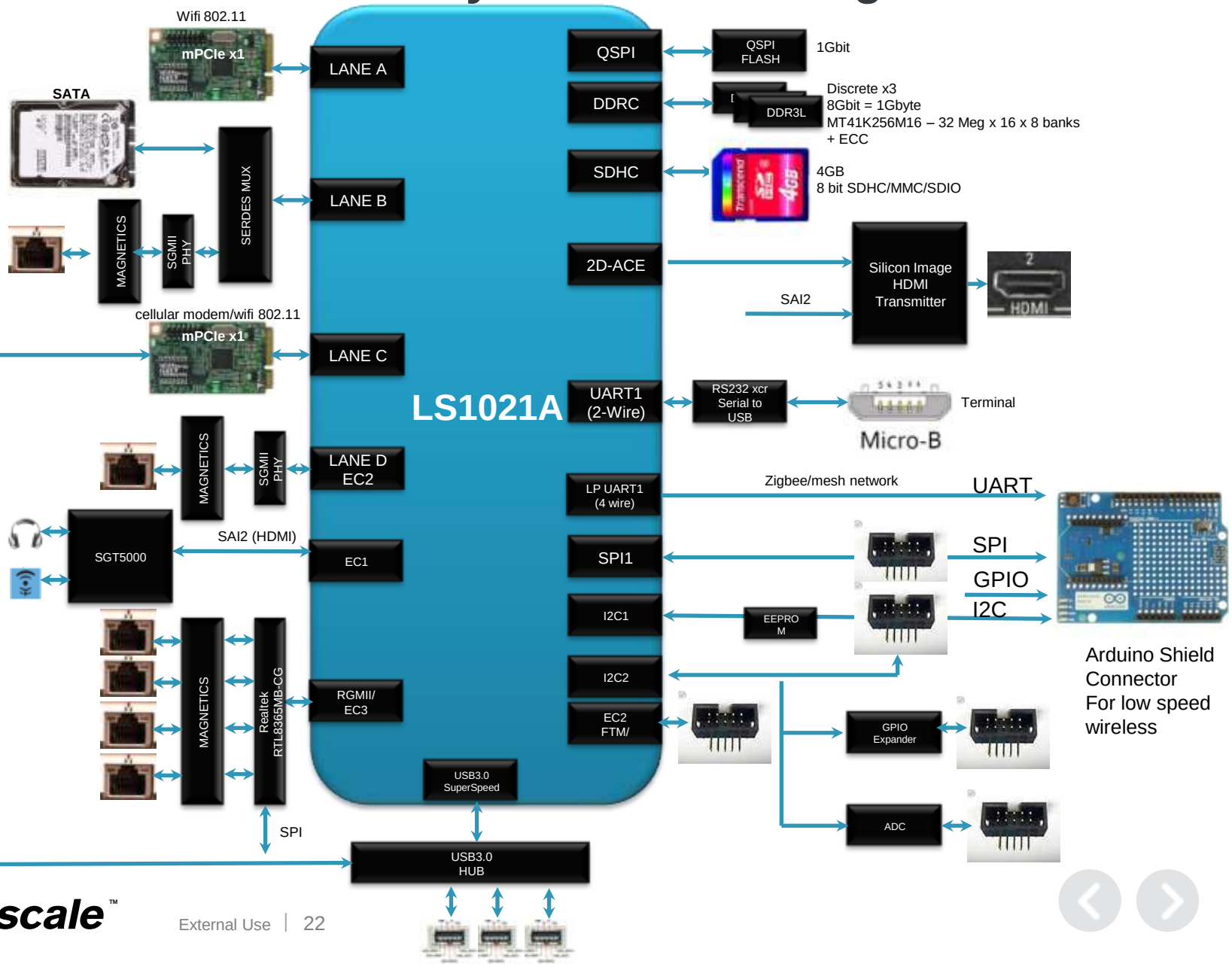
TWR-LS1021A – Tower System Development Platform
(subject to change)



TWR-LS1021A – Tower System Development Platform - Feature Set

- 1 Gb Parallel NOR Flash
- 128Mb Qual SPI Flash
- 1 GB DDR3L
- Full-size SDHC slot—up to 32 GB
- 4Kb EEPROM
- 2x One Gb/s Ethernet (SGMII)
- 1x One Gb/s Ethernet (RGMII)
- 2x mini PCIe (x1) slots
- 1x mSATA slot
- Muxed LCD/QE interface
  - 24-bit LVDS LCD interface
  - 1x HDMI connector
  - 2x QE UART to TWR-ELEV for PROFIBUS or RS485 (external transceiver needed)
- Audio
  - Audio OUT via HDMI or Jack plug
  - Audio IN via onboard mic
- USB 3.0
  - 2x ports—USB-A
  - 2x ports to mini PCIe slots
- 2x SPI bus and 3x I2C bus
- OpenSDA debug support
  - Run-control debug
  - Flash programmer
  - UART to USB converter
- Tower Boards supported via TWR-EVEL
  - TWR-IND-IO(2 x CAN, RS485, RS232, up to 2 boards supported)
  - TWR-LCD
  - TWR-LCD-RGB
  - TWR-SER2
  - TWR-ETHERCAT-SLV
  - TWR-MCLV3PH

QorIQ LS1021A IoT Gateway Reference Design



QorIQ LS1021A IoT Gateway Reference Design – Feature Set

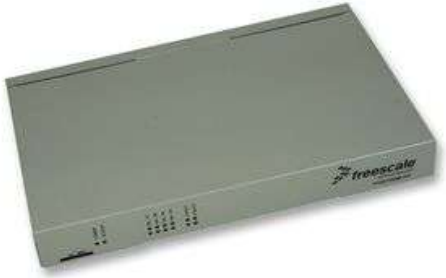
- 1 Gb QSPI NOR Flash
- 1 GB DDR3L
- SDHC slot—up to 32 GB
  - 4 GB populated
- 1x One Gb/s Ethernet (SGMII)
- 1x One Gb/s Ethernet (RGMII)
- 2x mini PCIe (x1) slots
- 1x mSATA slot
- 1x Terminal (USB to UART)
- 1x Four wire LP-UART to Arduino connector (ZigBee)
- Muxed LCD/QE interface
  - 24-bit LVDS LCD interface
  - QE UART to header for PROFIBUS or RS485 (external transceiver required)
- USB 3.0
  - 2x ports—USB-A
  - 2x ports to mini PCIe slots
- 13x GPIO or 8x FTM (PWM)
- 6x Interrupts
- 1x SPI
- I^2C1 bus
  - Board EEPROM
  - Boot EEPROM
  - Arduino Connector
  - Sensors/PHYs, etc., TBD
- I^2C2
  - GPIO expansion
  - ADC
  - Sensors/PHYs, etc., TBD

QorIQ LS1021A IoT Gateway – POC Demo (16-July-14)

Freescale MMA8451Q accelerometer

Arkessa server stores CO2 readings and uses accelerometer values to control the robot

LS1021A-IOT Gateway Platform
(Running Arkessa Client)



Telit HE910 3G modem

Arkessa Database

GSS COZIR CO2 sensor

Performance Data

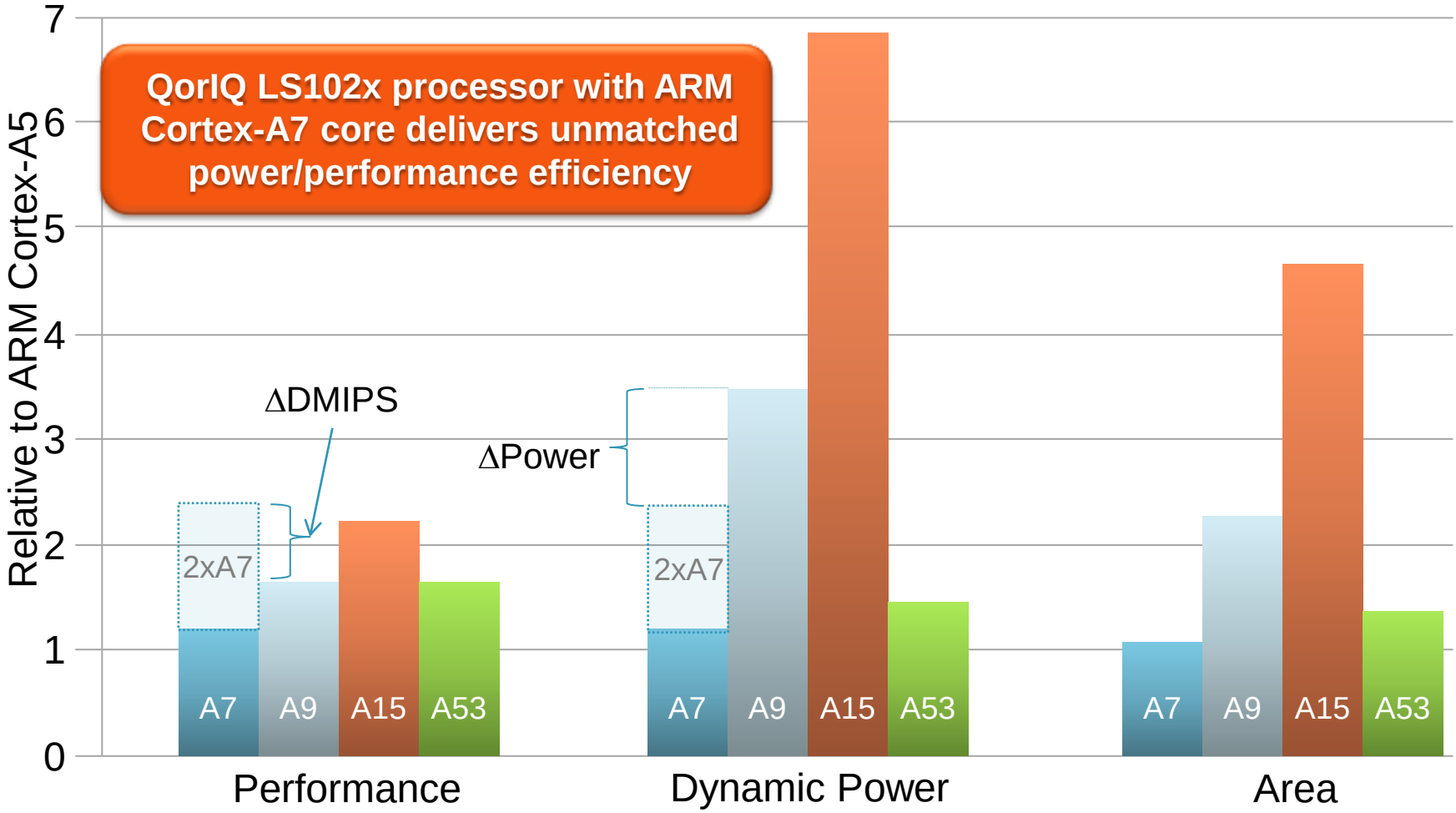
LS102xA Performance Strategy

Key design objective of LS1 family is to deliver the highest level of performance and integration within a sub-4W total design power (TDP) envelope

- Theoretical peak DDR bandwidth: 6.4GByte/s (32-bit * 1.6GHz data rate)
- Theoretical internal bus bandwidth: 4.8GByte/s (128-bit * 300MHz)
- IPfwd: 2Gbps at IMIX packet size
- IPSec: 1Gbps at IMIX packet size
  (up to 2Gbps at large packet size)

NOTE: All performance targets for LS102x are pending actual benchmarking in silicon, these numbers are preliminary and subject to change

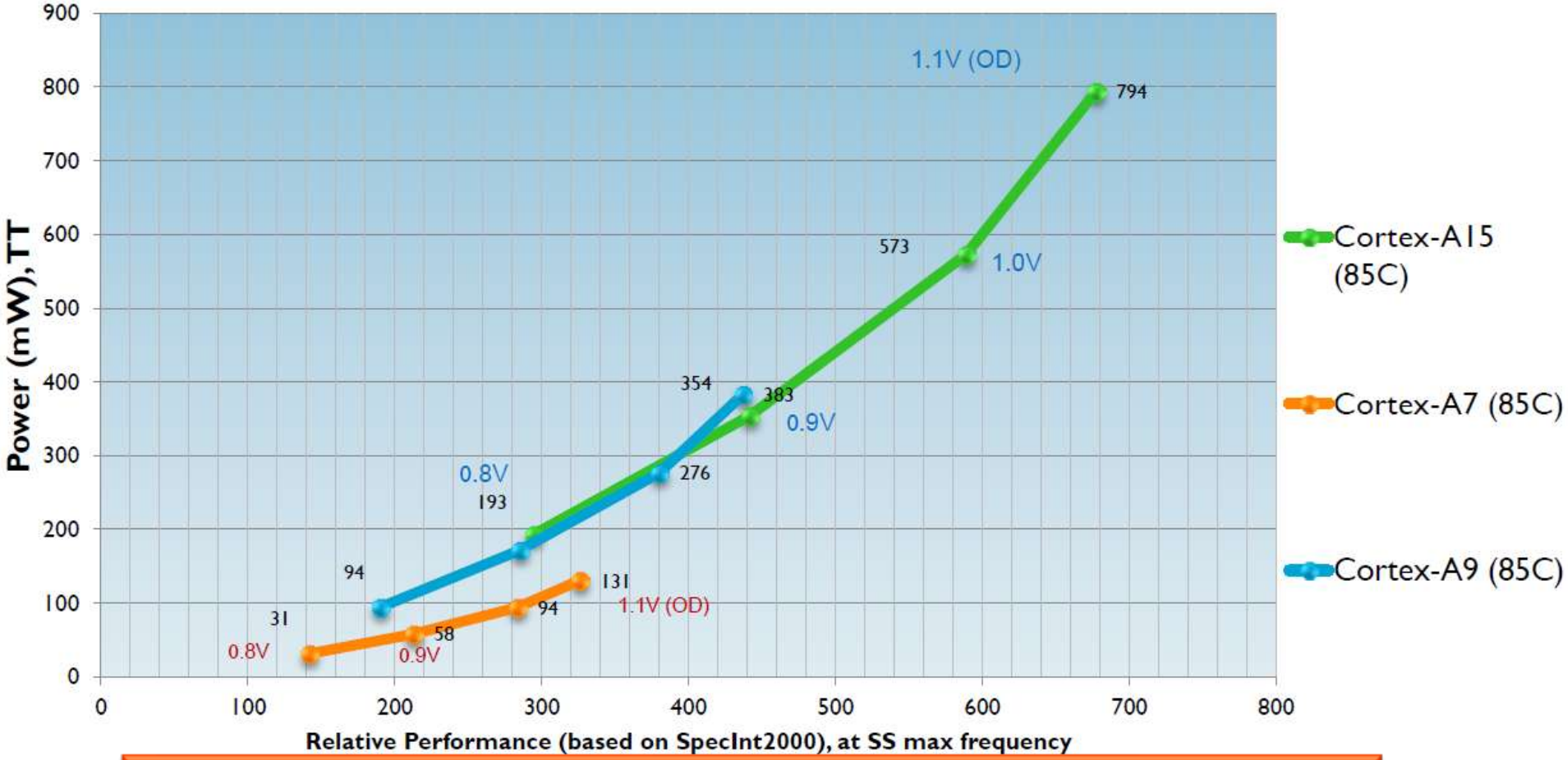
Comparison (2x Cortex-A7 vs 1x Cortex-A9)



Performance is Specint2000 at synthesized frequency
Area is core with Neon + L1 cache, with L2 controller, MP1 configuration, no L2 RAM included
Power measured as Dhrystone at nominal voltage

Cortex A7 = 1.9 DMIPS/MHz
Cortex A9 = 2.5 DMIPS/MHz

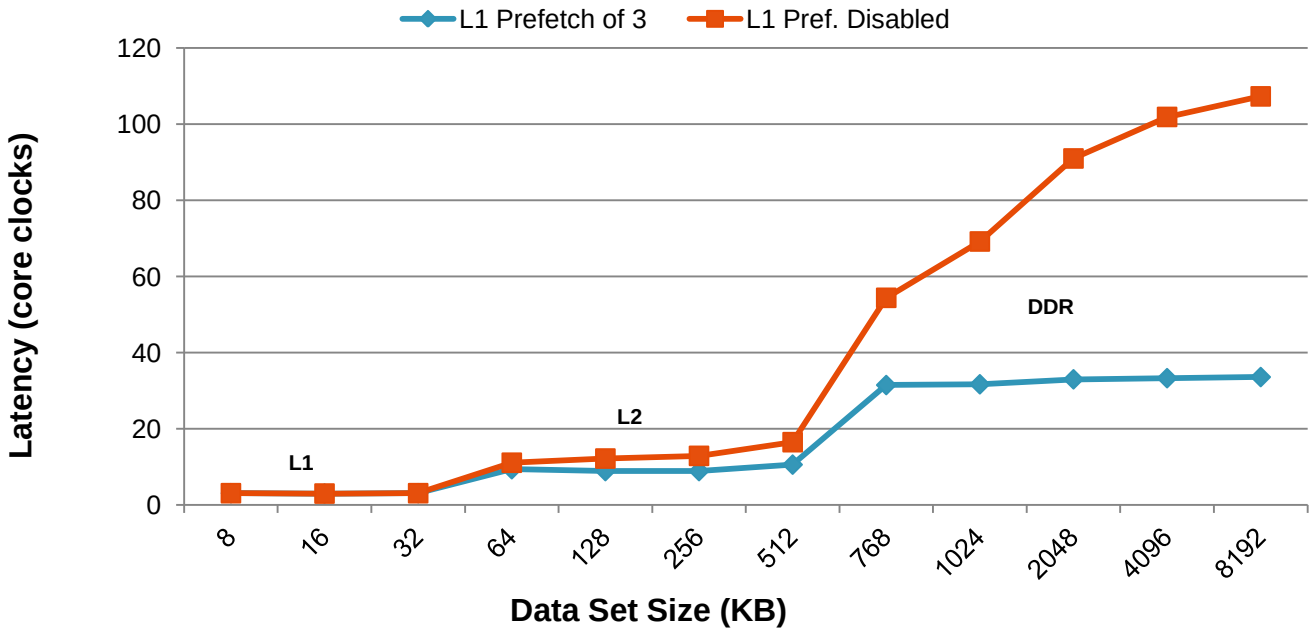
Cortex-A7 Power Advantage



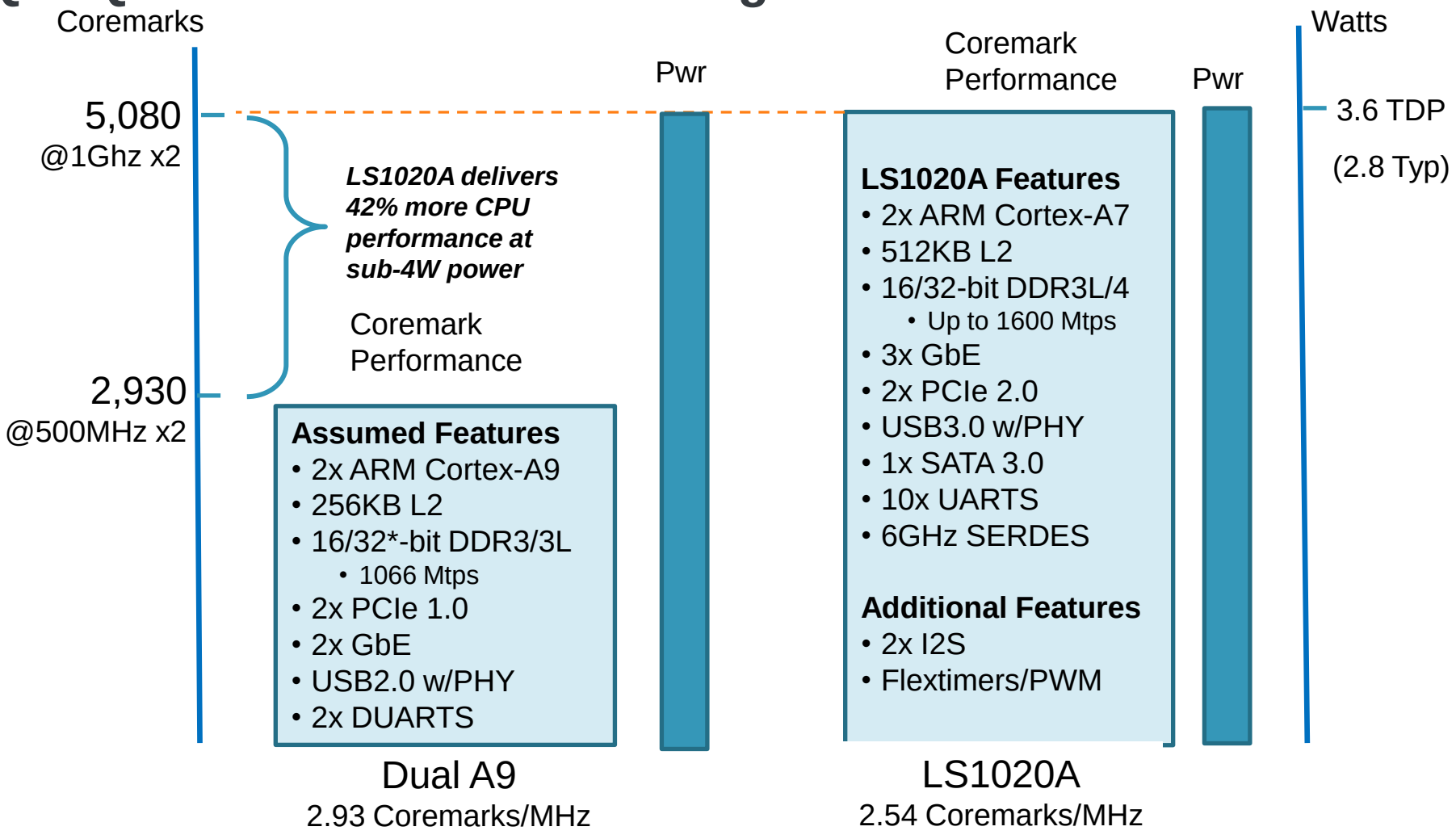
Cortex-A7 gives much lower power for the same performance (and much more performance for power-constrained devices)

LS102xA System Latency

- LS102xA benefits from L1 cache prefetching (new to this class of device)
- Up to 3 outstanding L1 Data cache pre-fetches permitted
- Significant latency improvement, as shown below.



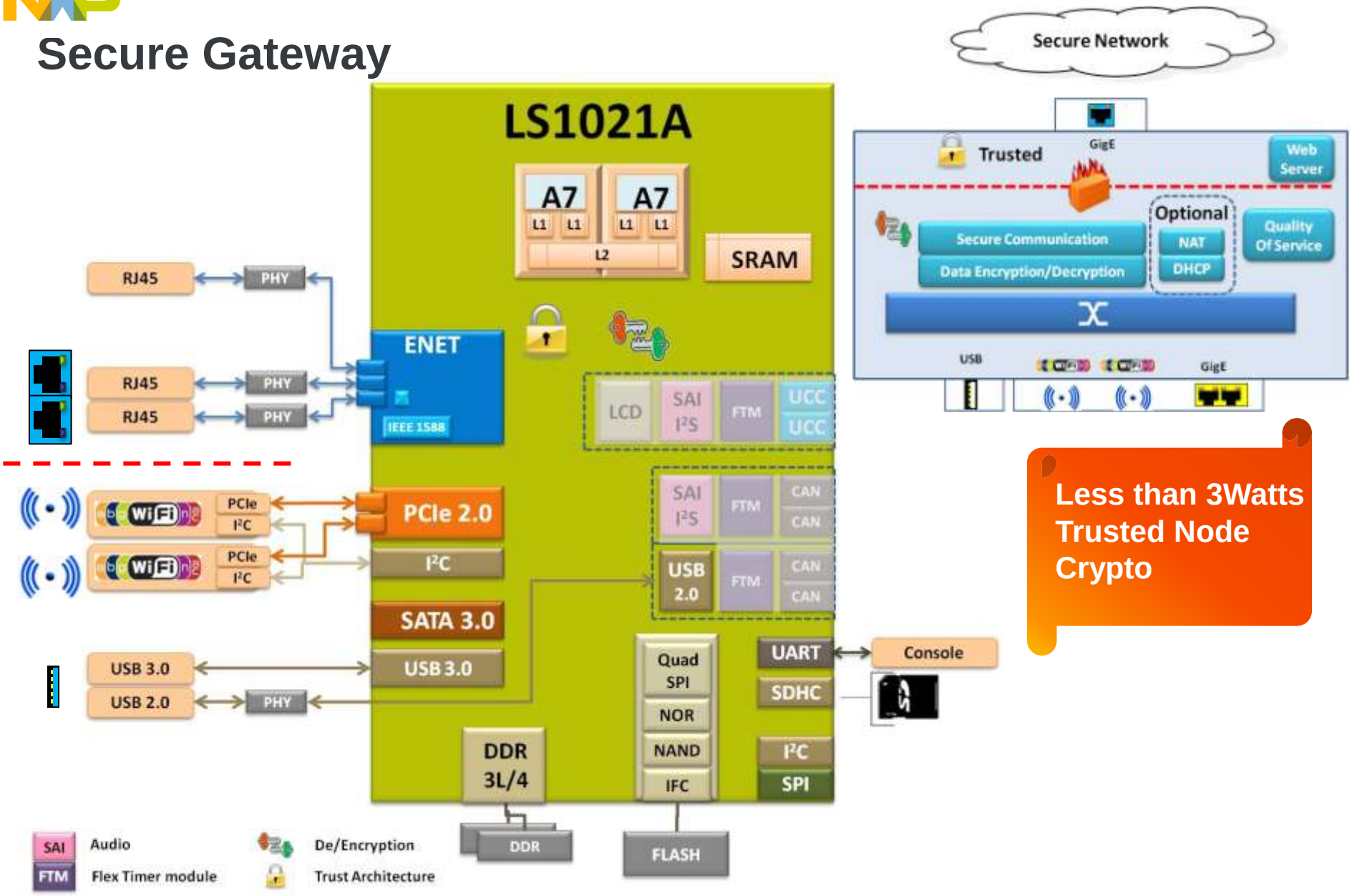
QorIQ LS1020A Processor – Higher Performance at <4W



At same power, 2x ARM Cortex-A7 based QorIQ LS1020 processor achieves 42% higher performance compared to 2x ARM Cortex-A9 based SoC

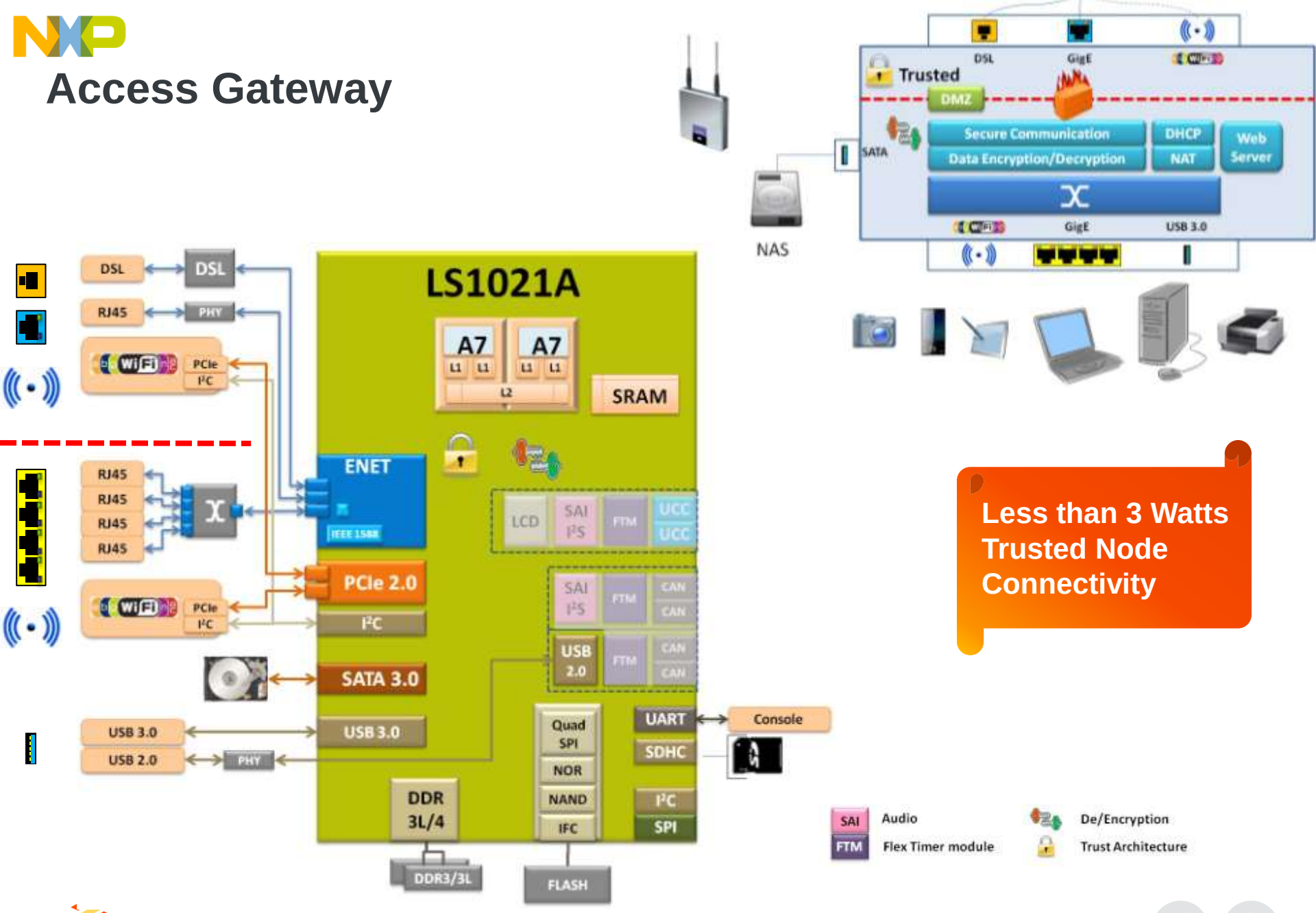
QorIQ LS1 Family Use Cases

Secure Gateway



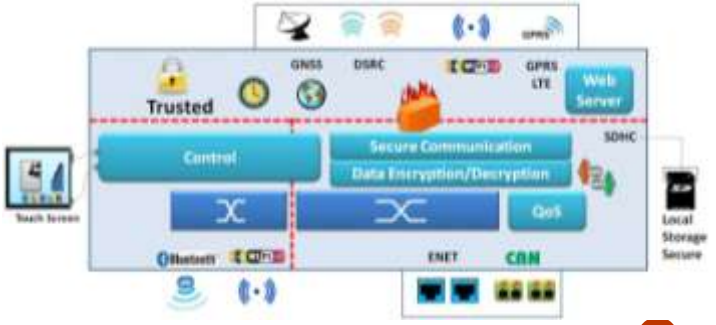
Less than 3Watts
Trusted Node
Crypto

Access Gateway

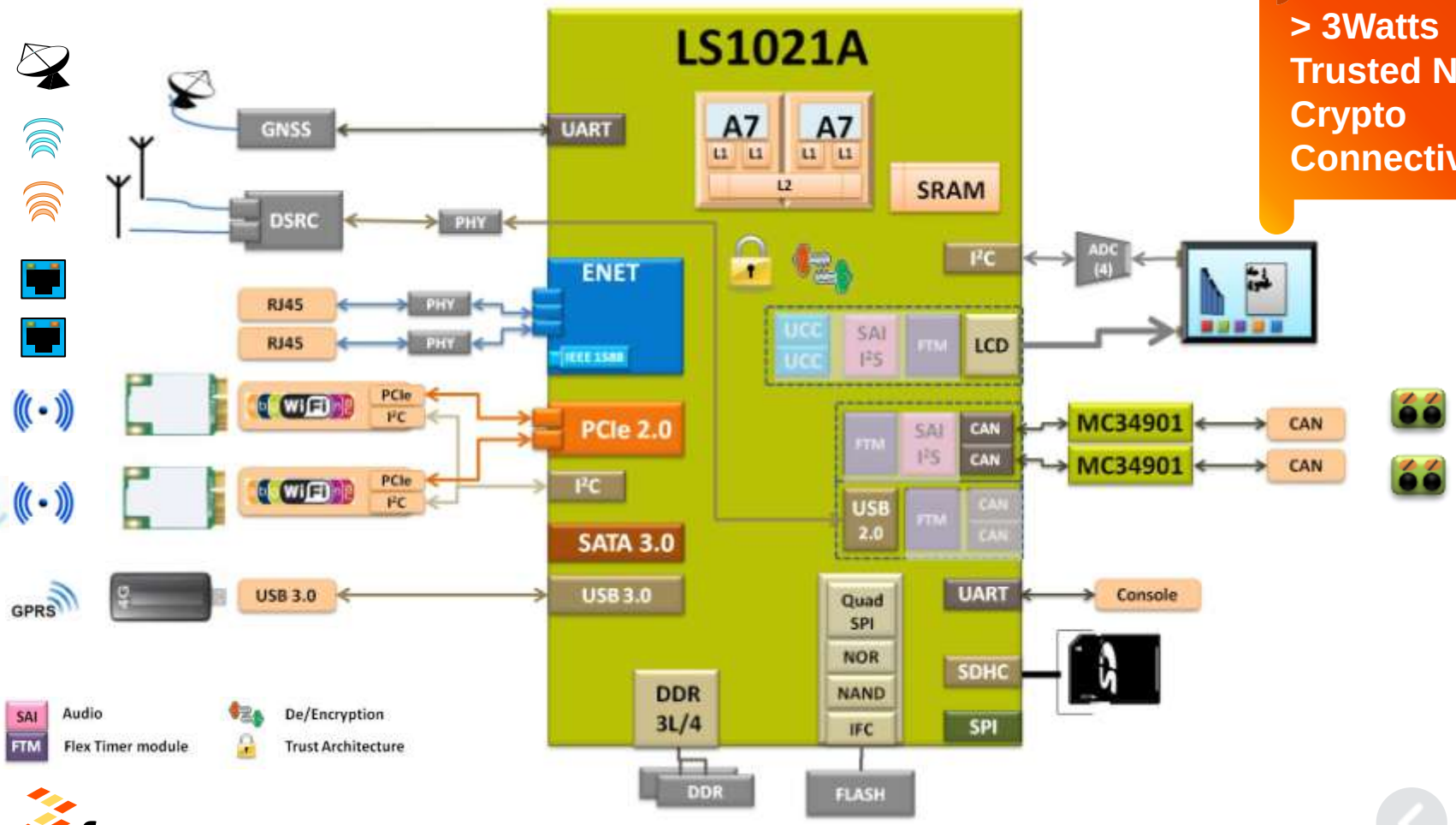


Less than 3 Watts Trusted Node Connectivity

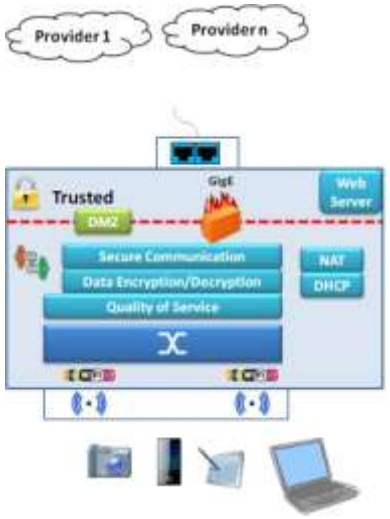
Mobile Wireless Gateway [Car]

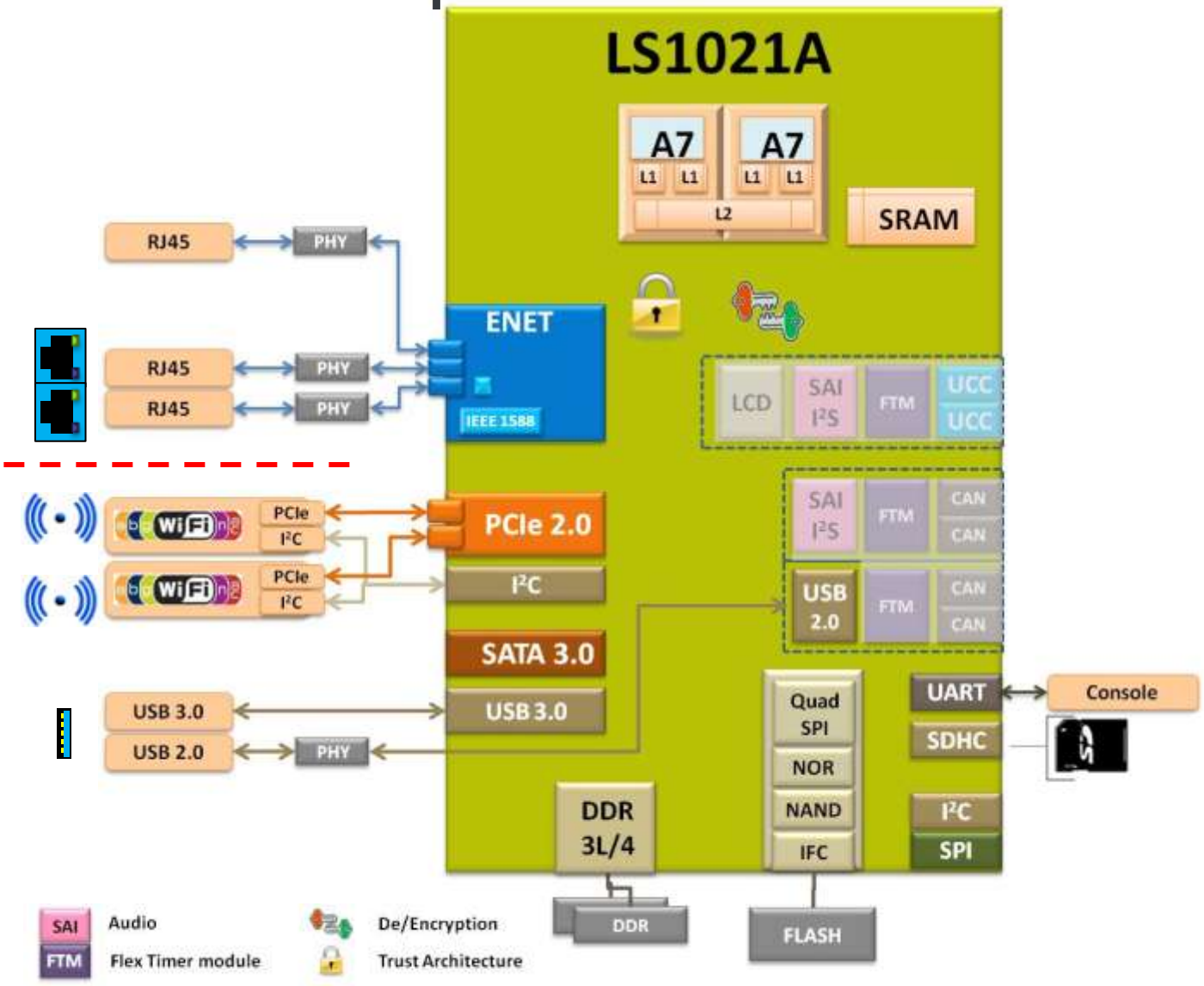


> 3Watts
> Trusted Node
> Crypto
> Connectivity



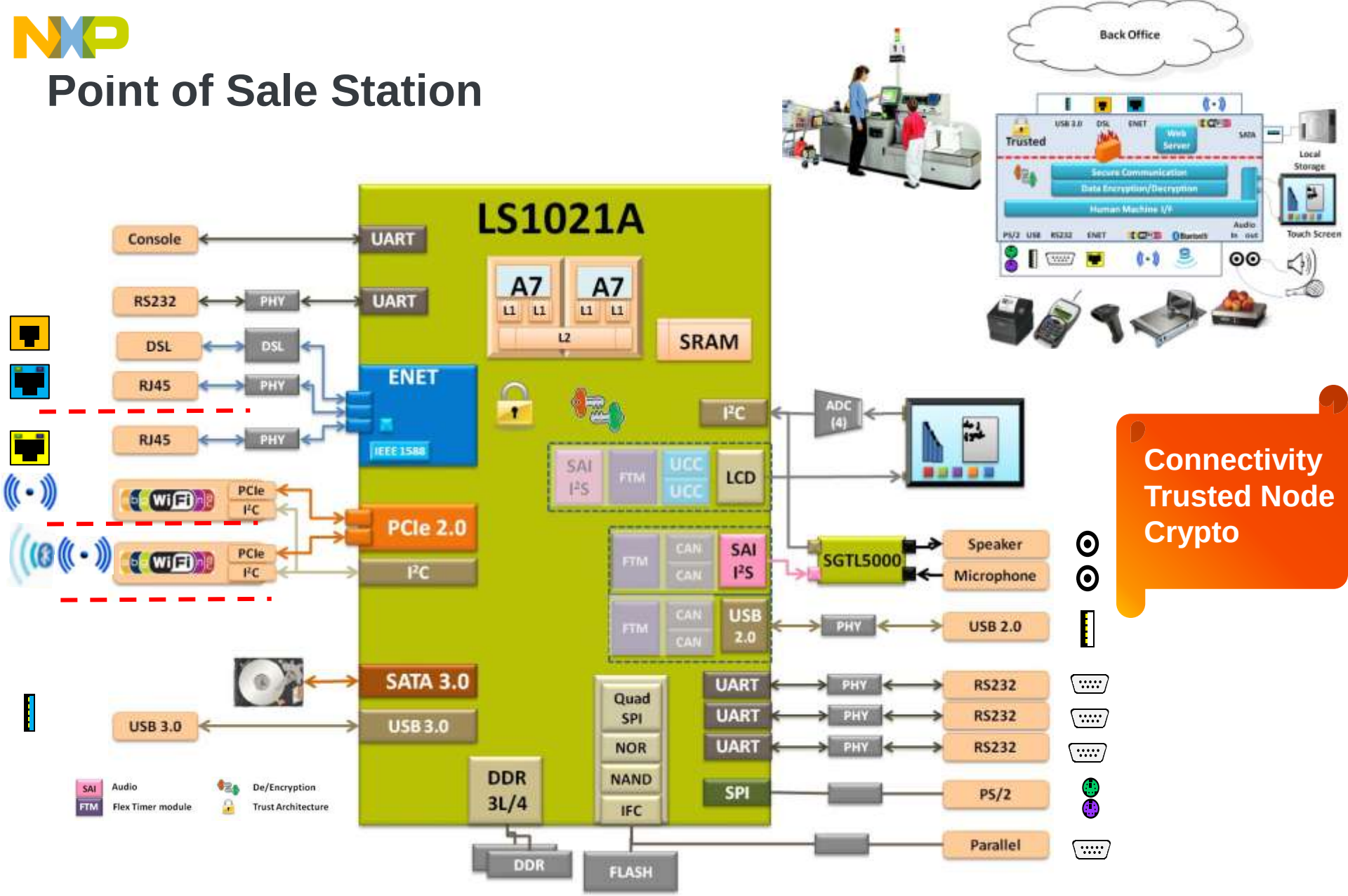
Wireless Hot Spot





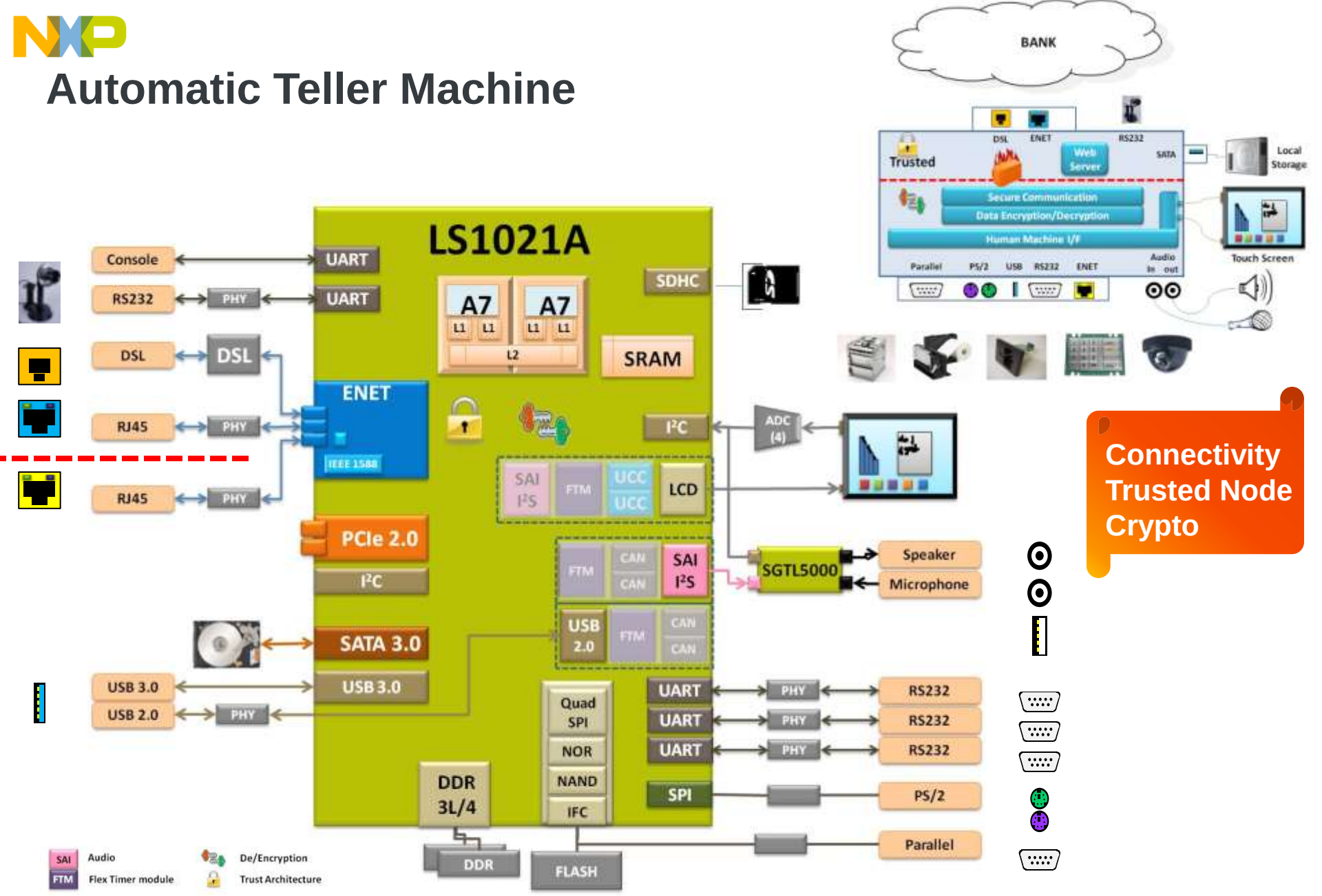
Less than 3Watts
Trusted Node
Crypto

Point of Sale Station



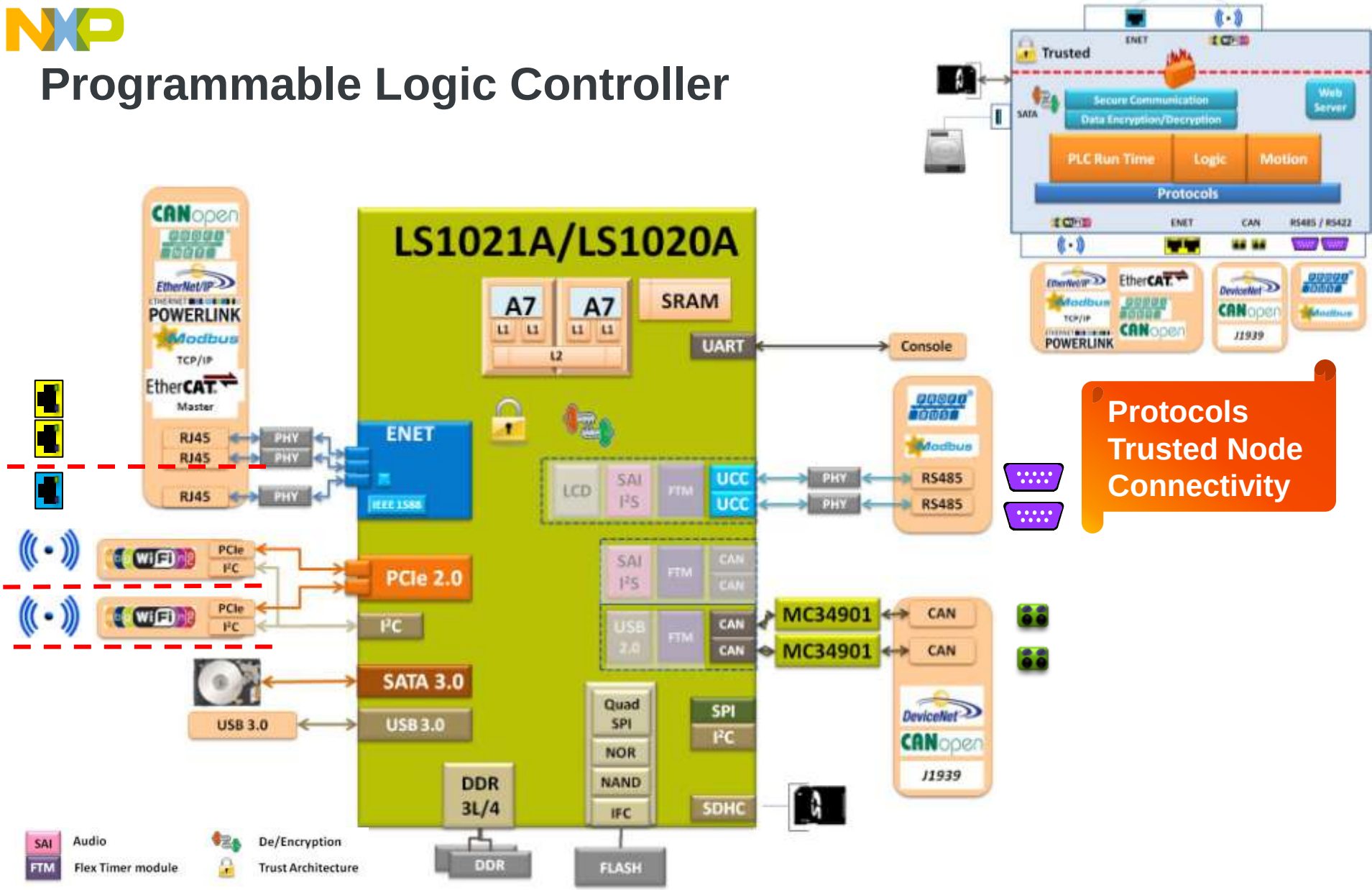
Connectivity
Trusted Node
Crypto

Automatic Teller Machine

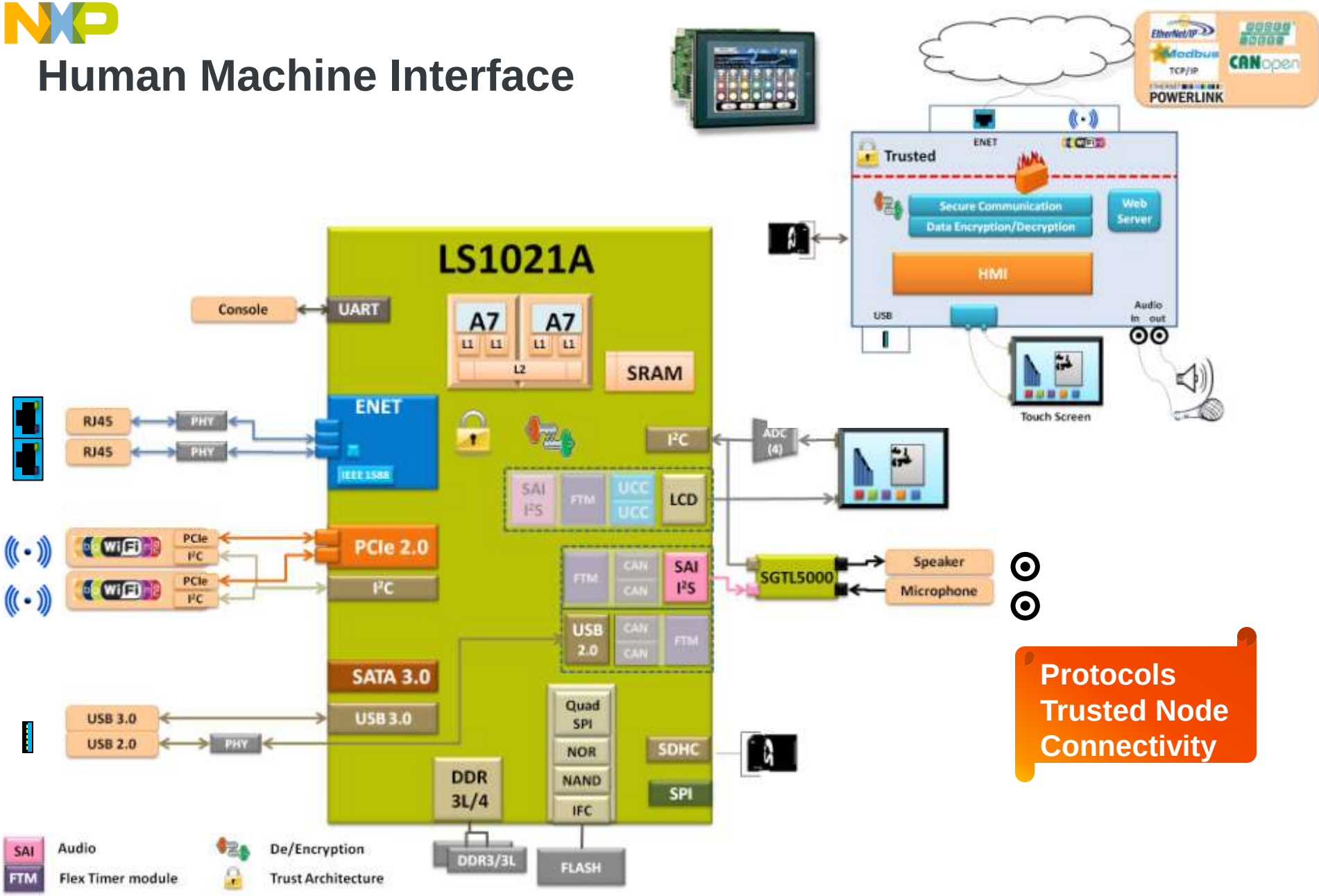


Connectivity
Trusted Node
Crypto

Programmable Logic Controller

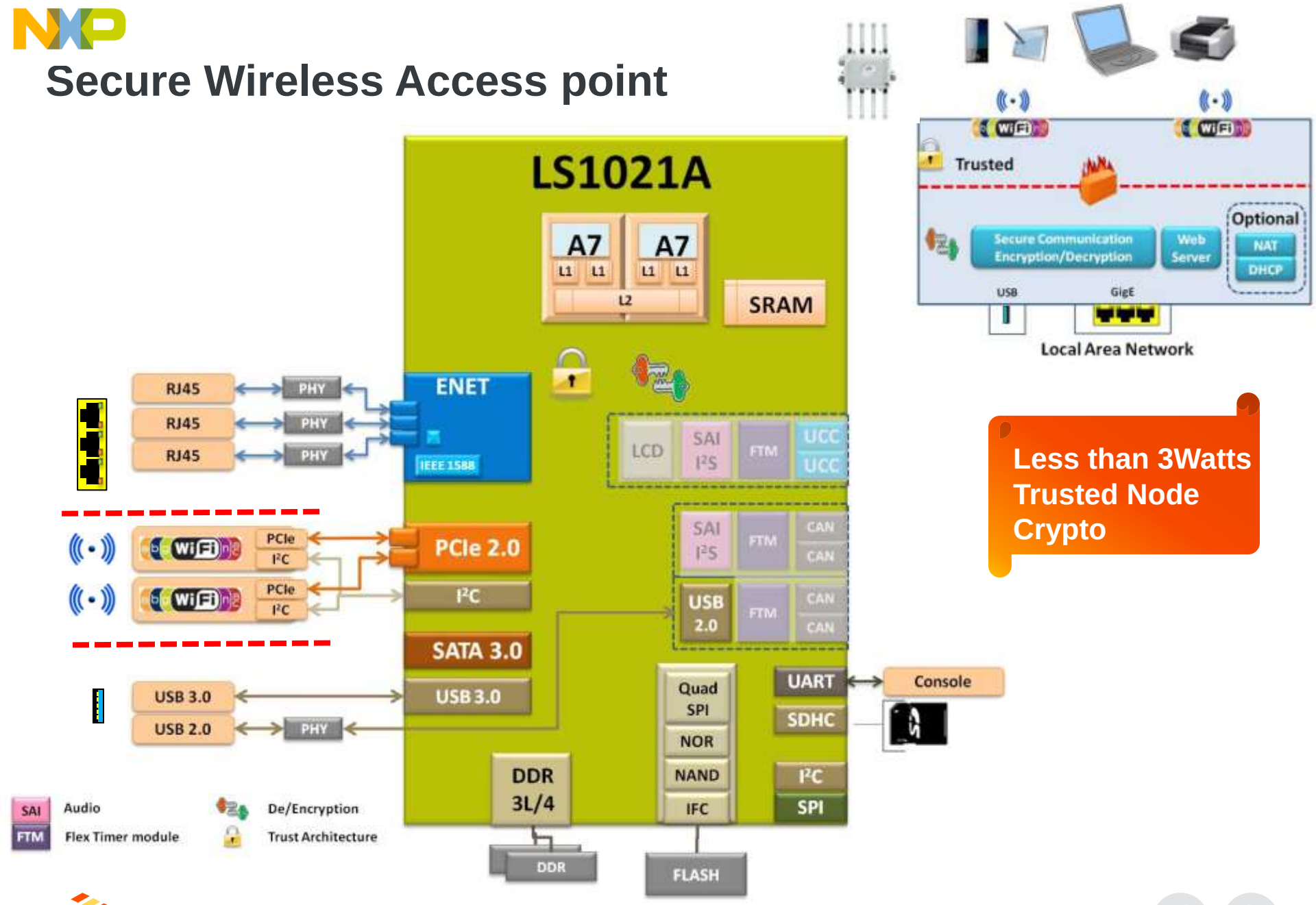


Human Machine Interface



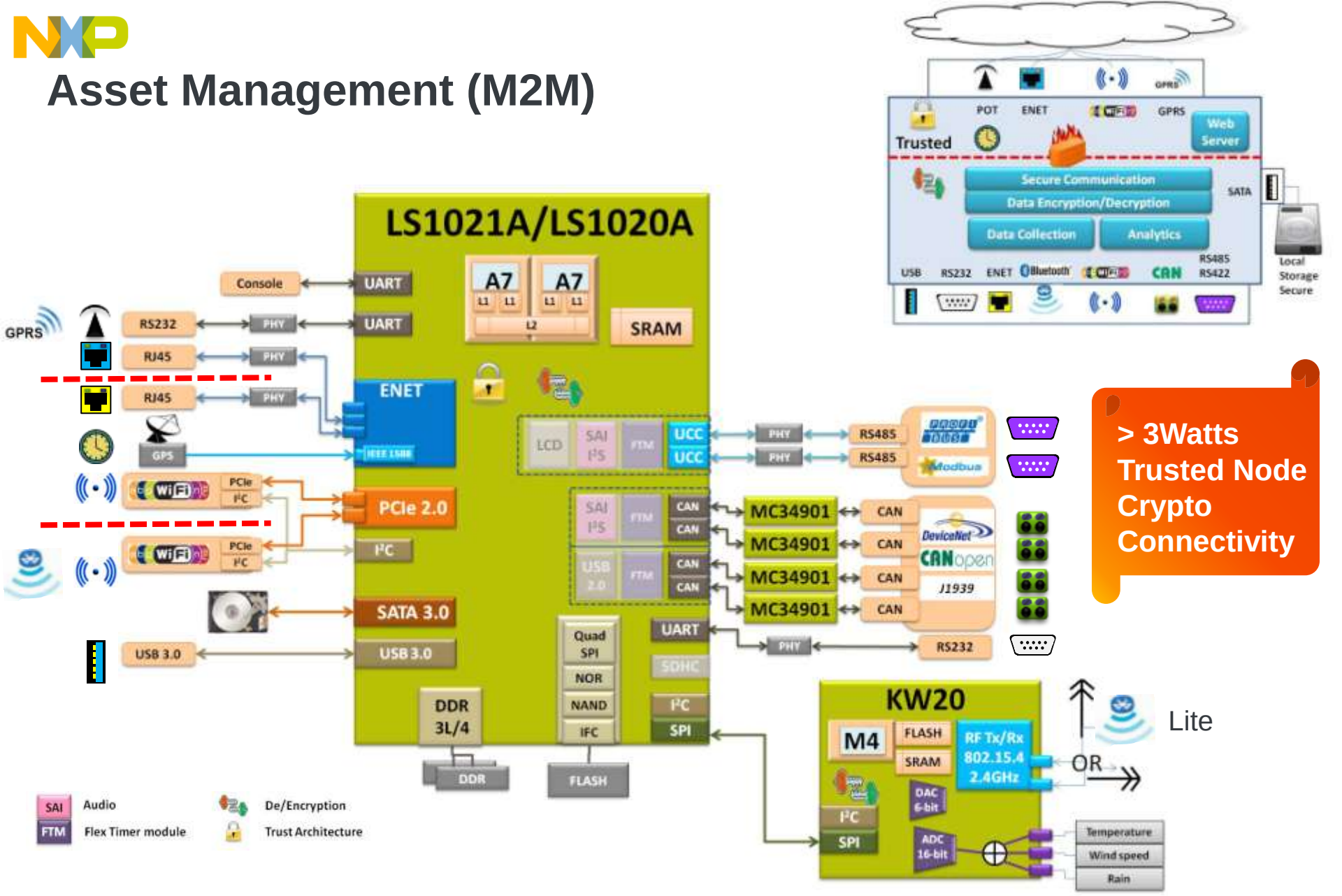
Protocols
Trusted Node
Connectivity

Secure Wireless Access point



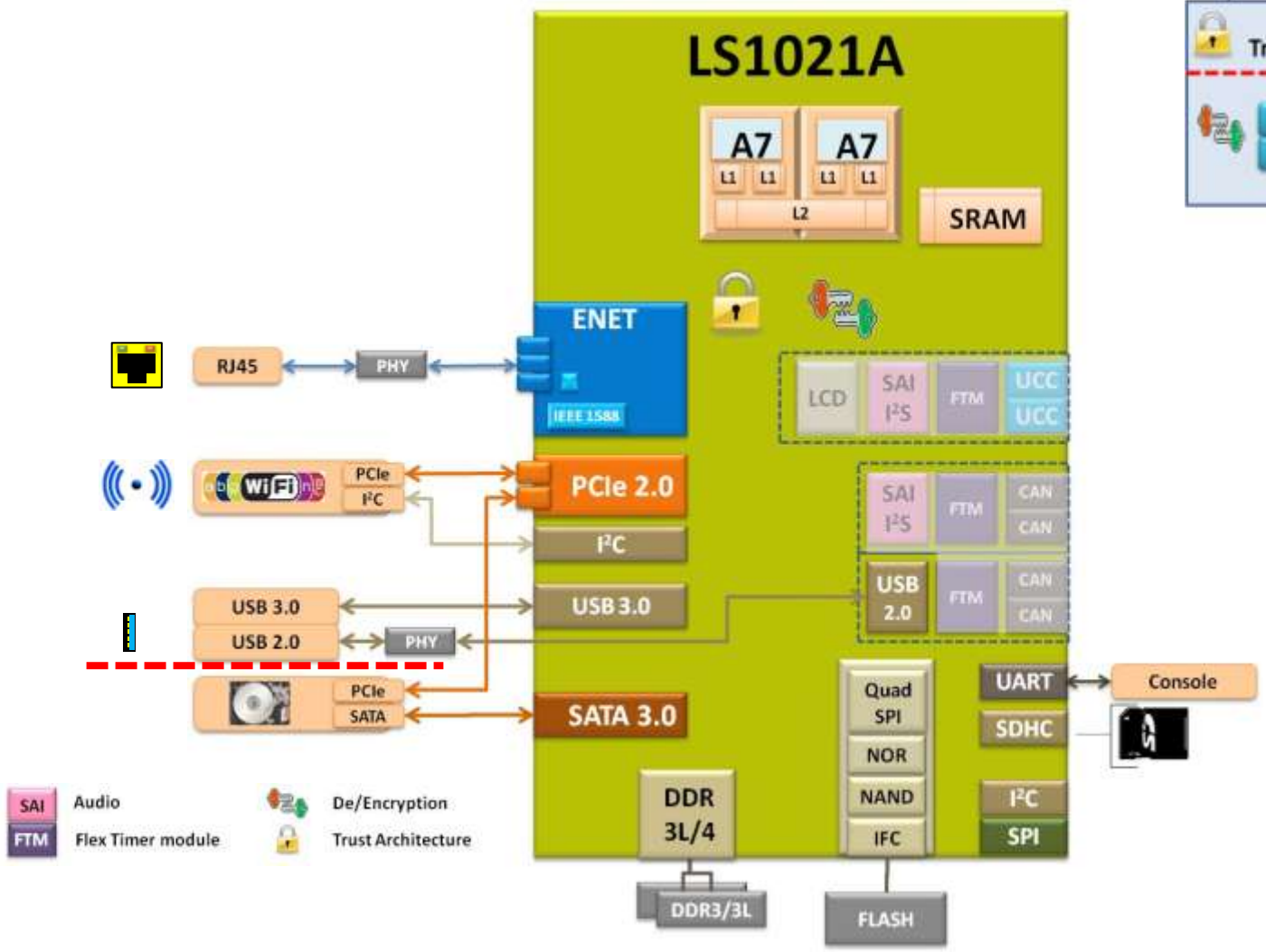
Less than 3Watts Trusted Node Crypto

Asset Management (M2M)



> 3Watts
> Trusted Node
> Crypto
> Connectivity

Secure Network Attached Storage



Less than 3Watts Trusted Node Crypto

QorIQ LS1 Core IP

QorIQ LS1 Family CPU Core Complex and L2 Cache

- Dual ARM **Cortex-A7** cores configured as:
  - Up to 1.0GHz operation
    - Limited to 600MHz on LS1022
  - 32KB I-cache and 32KB D-cache per core **with ECC protection**
  - 512KB shared L2 cache **with ECC protection**
  - FPU and NEON VFPv4 supported
  - CoreSight *Embedded Trace Macrocell* (ETM) supported for debug trace

Interconnect and System IP

- ARM CCI-400 Coherent Interconnect
  - Crossbar w/ 128-bit data buses, operating at up to 300MHz
  - All IP can be hardware coherent if desired
    (like previous QorIQ, but unlike most Cortex-A9 SoCs)
  - Including IO coherency for inbound PCIe (unlike most SoCs)
- ARM GIC-400 Interrupt Controller
  - Analogous to QorIQ MPIC.

- Further details at www.arm.com

QorIQ LS1 Family DDR Memory Controller

- 32-bit Data + 4-bit ECC
  - 16-bit Data + 2-bit ECC, 8-bit Data + 1-bit ECC
  - Only 16-bit Data supported on LS1022
- Operation from 1.0GHz to 1.6GHz
- DDR3L (1.35V) and DDR4 (1.2V) supported
  - Only DDR3L supported on LS1022
- 4 chip selects supported

DMA

- LS102x supports two different DMA Controllers:
  - **eDMA** (as used on i.MX and Vybrid)
  - Used for relatively low-speed offload of data movement to/from low-speed peripherals (SPI, LPUART, SAI, ASRC, FlexCAN)
  - **qDMA** (specific to Digital Networking, formerly known as eDMA)
  - Optimized for high bandwidth to / from DDR and / or PCIe

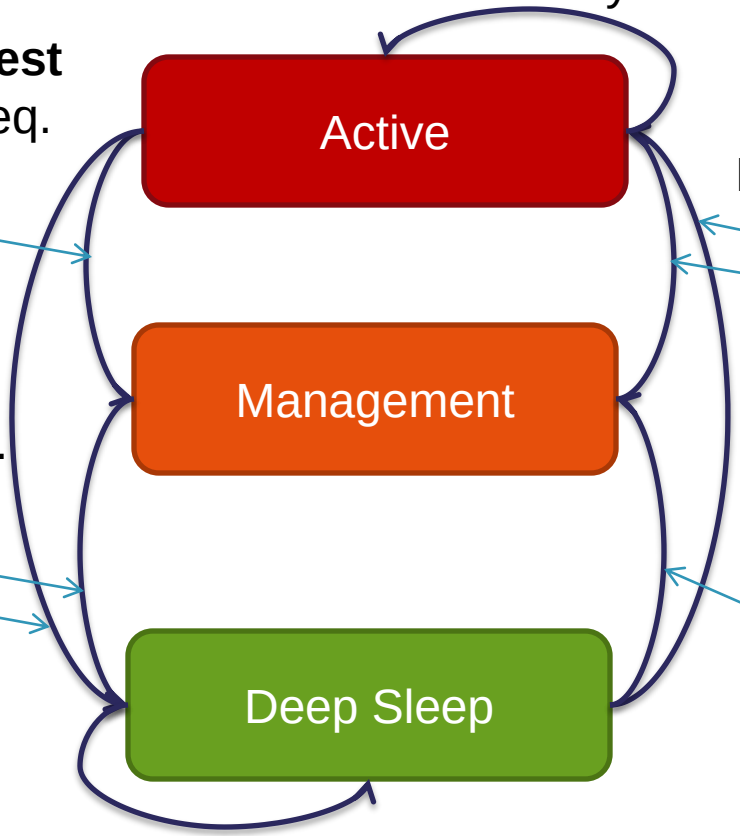
Timers

- QorIQ LS102x processors support **three different Timer-related IP**
  - **FlexTimer** (as used on i.MX and Vybrid)
    - 8 instances of Flextimer (similar to Kinetis K series MCUs and Vybrid F series controller solutions)
    - Can be used either as software general-purpose timer, or for PWM
    - Industrial motor control or dimmable LED control, etc.
  - **Watchdog Timer** (as used on i.MX and Vybrid)
    - 2 instances of Watchdog timer (similar to i.MX 6 series and Vybrid F series controller solutions)
    - Can be used to either raise interrupt or request SoC reset
  - **ARM's Generic Timer**
    - Compatible with Section B.8 of ARMv7-A Architecture Reference Manual
    - Intended for use by software

Network Standby with LS102xA

Primary Application Running
· Performance is maximized
· Connectivity is maximized

Management Request
·Decrease CPU freq.
· Disable some I/O



Primary Application Request
· Restore state
· Restore power
· Increase CPU frequency

No more work
· Save system state.
· Remove power to non-essential components.

Management Request
· Restore power as needed

No useful work
· Performance is zero
· Connectivity is maintained

Goals of Network Standby

1. Minimize power

2. Whatever is connected on the network should not know that the product is in Deep Sleep.
   - No changes needed to legacy software or the rest of the world.

3. Minimize power….

TIP: Optimize for the common case
Home and office networks typically have traffic 24 hours a day (even if “idle”)

Power Management: Deep Sleep

- QorIQ LS102x processors support QorIQ P1022-style Deep Sleep
  - Wake on: RGMII Ethernet, or Timer, or GPIO etc.
- <150mW total SoC power (including IO)
  - Enabling < 0.5W AC system design solutions
- Supports core Dynamic Frequency Scaling (DFS)
  - Same as supported on QorIQ P3/P4/P5 products

QorIQ LS1 Family Trust, Virtualization and Security

QorIQ LS1 Family Security Architecture Overview (p1/3)

- **TrustZone**
  - As per Vybrid and i.MX6
  - Hardware compliant to ARM Trusted Base System Architecture (TBSA v1.0)
  - Enablement of this will be from customers or ecosystem, not Freescale
  - Trusted execution environment for security-critical SW
    - Secure & Normal Worlds (processor modes)
    - Complemented by custom hardware firewalls

- **QorIQ Trust Architecture Secure Boot**
  - As per QorIQ P3/P4/P5 Products
  - Security library embedded in tamper-proof on-chip ROM
  - Authenticated boot: protect against unauthorized SW
    - Verify SW signature during boot
    - RSA-1024/2048 keys anchored to OTP fingerprint (SHA-256)
  - Encrypted boot to protect software confidentiality
    - Decrypt SW during boot
    - AES-128/256 keys protected by HW master key (AES-256)
  - Run every time SoC is reset
  - Image Version Control (on-chip OTP-based)

QorIQ LS1 Family Security Architecture Overview (p2/3)

- **HW Cryptographic Accelerators (SEC 5.5)**
  - **Support for wireline protocols, plus Wi-Fi and Wimax,**
  - Not supported: Kasumi, Snow, ZUC, ARC4
  - Symmetric: AES, DES, 3DES, ARC4
  - Hash & HMAC: MD5, SHA-1, SHA-224, SHA-256
  - Hardware random number generator (SP800-90)
  - Export control support

- **Secure Storage**
  - Programmable TrustZone protected region within On-chip RAM (64Kbytes)
  - Off-chip storage protected by HW master key (AES-256)

- **Secure Real-Time Clock**
  - On-chip, separately-powered real-time clock (1.0V)

- **HW Firewalls**
  - Control access from CPU & DMA peripherals to
    - on-chip peripherals
    - on-chip memory
    - off-chip memory
  - Integrated with TrustZone

QorIQ LS1 Family Security Architecture Overview (p3/3)

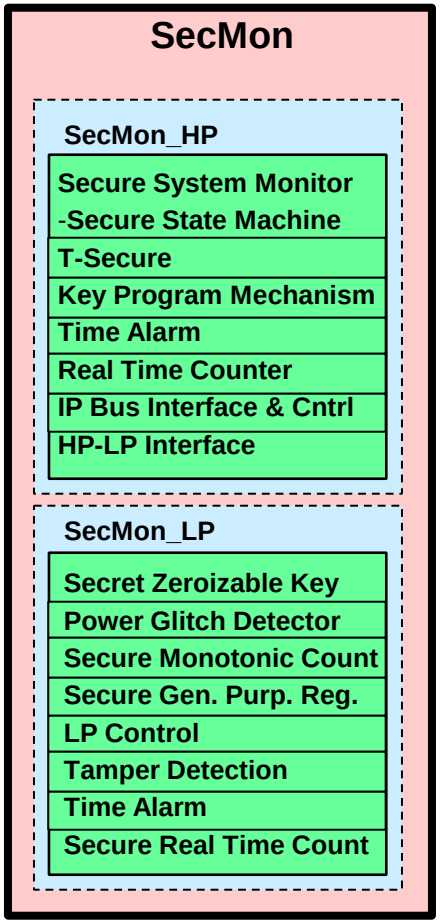
- **Secure Debug**
  - Secure Debug Challenge/Response as per QorIQ P3/P4/P5 products
- **Physical Tamper Detection**

  - Tamper input signal available for:
    - Cover seal
    - Clock, voltage, temperature detectors
    - Active tamper detection
  - Hardware and software tamper response

Secure Monitor (SecMon)

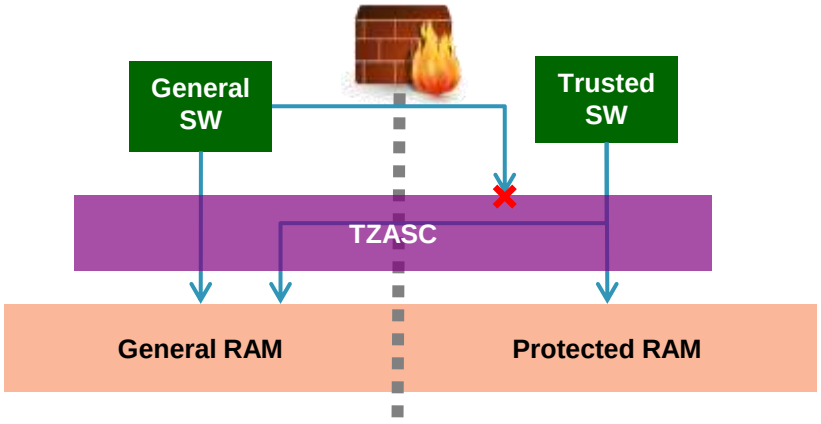
- **SecMon_HP – System Power Domain**
  - System Security Monitor
  - Zeroizable Master Key Programming Mechanism
  - Master Key Control block
  - Non-Secure Real Time Counter with Alarm

- **SecMon_LP – Dedicated Power Domain**
  - Zeroizable Master Key
  - Secure Non-Rollover Real Time Counter with Alarm
  - Non-Rollover Monotonic Counter
  - Power Glitch Detector
  - General Purpose Register
  - Tamper Detection Monitor



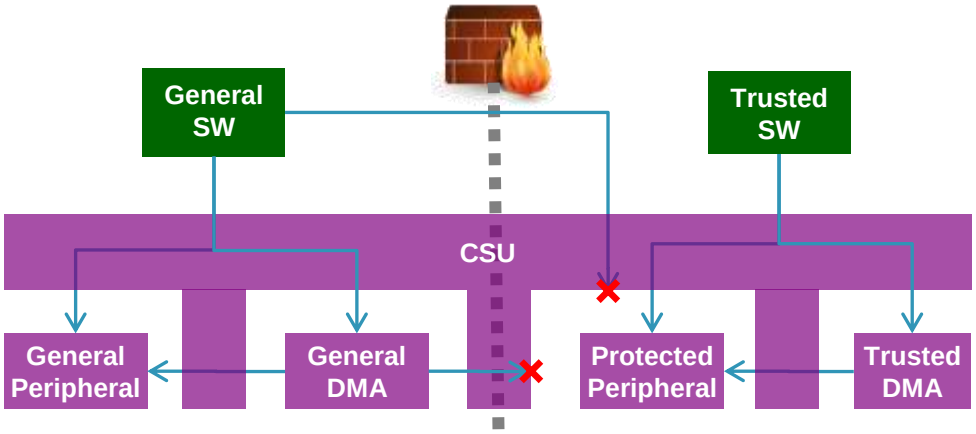
Physical Memory Isolation

- TZASC (TrustZone Address Space Controller)
  - Monitors AXI bus to DDR controller
    - Programmable address regions
      - Secure world access only
      - Shared access
  - Programmed by Secure World
    - Lockable

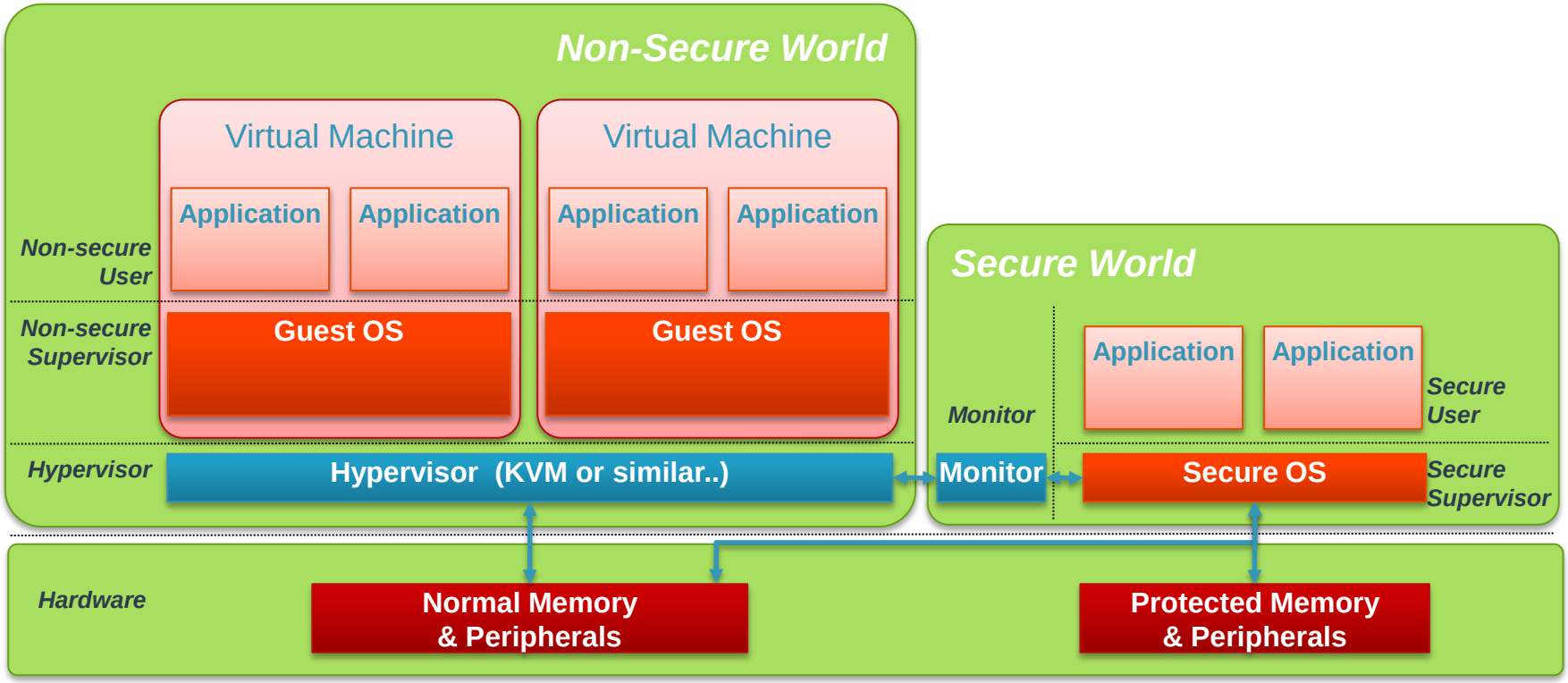


Peripheral Isolation

- CSU (Central Security Unit)
  - Monitors peripheral bus
    - Programmable for each peripheral
      - Secure world access only
      - Shared access
  - Programmed by Secure World
    - Lockable per-peripheral



Virtualization – CPU modes

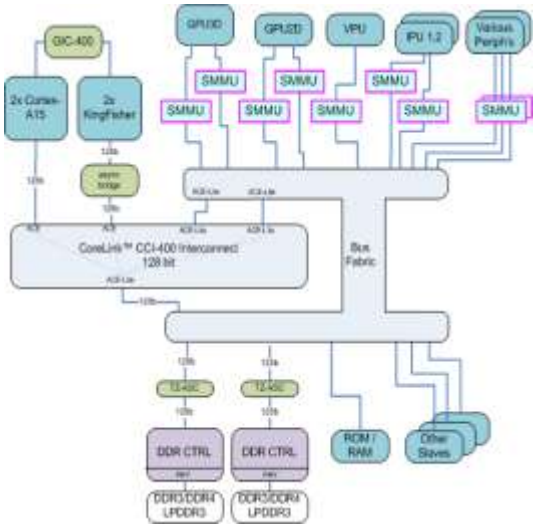


Virtualization Support by S-MMU

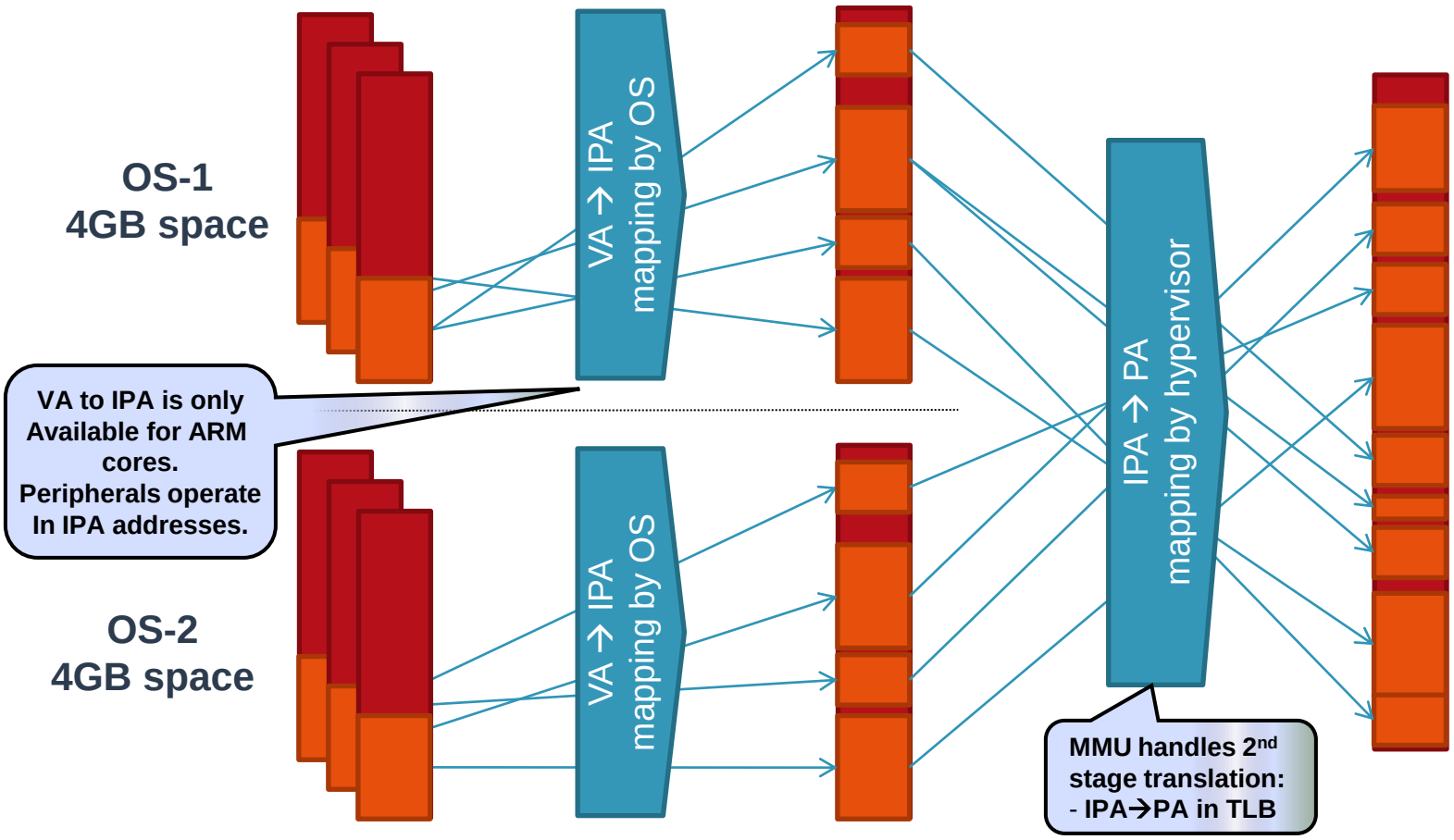
- System-MMU for 2nd stage translation of Intermediate Physical Address (IPA) to Physical Address (PA) addresses
- Analogous concept to PAMU on QorIQ P3/P4/P5

- **Benefits of using System MMU's for virtualizations are:**
  - Full HW Virtualization support (a.k.a. "IO Virtualization")
  - Better performance than SW virtualization ("Para-Virtualization")
  - Simpler (thus faster) porting of the Virtualized ("guest") OS
  - Support for >4GB address space, for 32-bit bus masters

- **S-MMU features:**
  - Up to 64 TLB entries in TLB cache
  - Address translation in HW, for best performance
  - TLB size configurable, to best suite each master needs



Virtualization: 2nd stage address translation



Virtual Address (VA)
for OS and each application
on each VM
Up to 4GB space
Due to HW 32-bit limitation

Intermediate Physical Address (IPA)
for each VM

Per OS - 4GB
(+/- Peripheral space)

Physical Address (PA)

8GB DDR + Peripheral

Networking & High Speed I/O

SATA / USB / VeTSEC

- **SATA**
  - Enhanced from previous generation QorIQ products
  - One SATA Gen1/2/3 controller (up to 6.0 GBaud)

- **USB**
  - 1 USB 3.0/2.0 Host/Device/OTG controller with integrated PHY
    - (Up to 5.0GBaud)
  - Additional USB 2.0 Host/Device/OTG controller with ULPI interface to external PHY
    - (Up to 480Mbps)

- **VeTSEC**
  - Similar to QorIQ P10xx products.
  - 3 Ethernet MACs, supporting RGMII (3), SGMII (2) and MII (2) interfaces.
  - IEEE1588 hardware support.

LS1021A PCI Express 2.0 Controller and SERDES

- 2 PCI Express Controllers can support x1/x2/x4 operation
  - For dual PCIe, maximum of 2-lane operation can be supported
  - Only single lane SERDES supported on LS1022
- MSI supported (but not MSI-X)
- USB 3.0 Phy integrates its own dedicated SERDES

LS102x SERDES Protocol combinations				
SERDES Lanes				
Protocol Options	A	B	C	D
1	PCIe#1 x4			
2	PCIe#1 x2		PCIe#2 x2	
3	PCIe#1 x1	SATA 1	PCIe #2 x2	
4	PCIe#1 x1	SGMII 1	PCIe #2 x1	SGMII 2
5	PCIe#1 x1	SATA 1	SGMII 1	SGMII 2
6	PCIe#1 x2		SATA 1	SGMII 2
7	PCIe#1 x2		PCIe #2 x1	SGMII 2
8	PCIe#1 x2		SGMII 1	SGMII 2
9	PCIe x1	SATA 1	PCIe #2 x1	SGMII 2

LS102x QUICC Engine Feature Overview

- **Summary**
  - Identical to T1040 QE – subset of P1021 QE

- **Protocols and Interfaces**
  - HDLC/Transparent (bit rate up to 70Mbps)
  - HDLC BUS (bit rate up to 10Mbps)
  - Asynchronous HDLC (bit rate up to 2Mbps)
  - UART (including ProfiBus support)
  - BISYNC (bit rate up to 2Mbps)
  - Two TDM interface supporting 64 multichannel, each running at 64Kbps

- **Time Slot Assigner and Two TDM Interfaces**
  - Independent Rx and Tx routing RAM with 512 routing entries each
  - Time slot assigner with bit or byte resolution

LS1021A 2D-ACE
(Two Dimensional Animation and Compositing Engine)

Feature	LS1021	Comments
Resolution	**1280 x 1024@72Hz**	For single plane
	1280 x 768@72Hz	Up to 2 planes (WXGA)
	1024 x 768 @72Hz	Up to 3 planes
	1024 x 768 @60Hz	Up to 4 planes
Blending	4-Planes α-blend / chroma key	
Input Planes	Sub-Plane selection from 16-layers Pixel format per layer Tile Texturing	DCU blends selected pixels from16-layers of images based on priority. Only displayed layers' pixels contribute to input BW.
Input Plane BW	Up to 2.4GByte/s)	Limited by internal memory bandwidth assuming fully populated blend planes
Pixel Formats	32-bit RGB 8+8-bit pallete YCbCr Transparency Luminance	Transparency α-component used to mix foreground/background colors (gradient). Luminance values add to pixel components below the luminance blend plane (intensity).
Cursor	256xH (8K-pixel) 1-bit pixel, blinking	A blend plane can be used for enhanced cursor support
Post-Processing	Gamma Correction Component Dithering Safety Pixel Tagging	DCU supports dithering to improve color depth and pixel tagging to check tagged input pixels are displayed in blended output
Display Interface	24-bit RGB (12-bit DDR pin interface)	

QorIQ LS1 Low-speed I/O Interfaces and Pinout

Low-speed Interfaces

- **Audio**
  - similar to Vybrid F series controller solutions
  - 4 instances of SAI for I2S support (Synchronous Audio Interface)
  - 1 instance of S/PDIF (Sony/Philips Digital Interconnect Format)
  - 1 instance of ASRC (Asynchronous Sample Rate Converter)

- **I2C**
  - 3 instances of I2C (similar to Kinetis K-series and Vybrid F series controller solutions)

- **SPI**
  - 2 instances of regular SPI (similar to Vybrid F series controller solutions)
    - Can operate in master or slave mode

- **UART**
  - 2 instances of 16550-compatible DUARTs (similar to QorIQ P series processors)
    - Can be configured as two 4-wire, or four 2-wire
  - 6 instances of high-speed “Industrial” UARTs (similar to Kinetis L series MCUs)

Low-speed Interfaces (cont.)

- **FlexCAN**
  - 4 instances of FlexCAN as per Kinetis K-series and Vybrid F-series
- **QuadSPI**
  - 1 instance of QuadSPI as per Vybrid F-series
  - It supports 2 serial flash ports. Each port implements 2 chip-select enabling two separate serial flashes to be attached to individual port.
- **SD/MMC**
  - 1 controller supporting SD 2.0, SD 3.0, SDIO 2.0 and eMMC 4.5

QorIQ LS1 Family Customer Pinout

- **GVDD: 89 pins DDR**
- **BVDD: 48 pins external Flash**
  - 28-bit address/16-bit data NOR Flash, or
  - 16-bit parallel NAND + 3x 2-channel PWMs,
  - 16-bit parallel NAND + QuadSPI, or
  - 8-bit parallel NAND + QuadSPI + extra regular SPI, or
  - 8-bit parallel NAND
    (with 3rd I2C also available in several of the above options)
- **DVDD: 8 pins UART**
  - 2x 4-wire UART, or
  - 4x 2-wire UART, or
  - 1x 2-wire UART + regular SPI
- **EVDD/DVDD: 10 pins SD/MMC**
  - 8-bit eMMC (no CD or WP)
  - 4-bit SD/MMC/eMMC + 2nd I2C
  - 3 additional UARTs + 2nd I2C

GPIO is muxed over
Most LVCMOS pins

GVDD = 1.2/1.35V
BVDD = 1.8/3.3V
DVDD = 1.8/3.3V
EVDD = 1.8/3.3V
LVDD = 1.8/2.5/3.3V
OVDD = 1.8V

- **DVDD: 2 pins I2C**
- **OVDD: 7 pins Interrupts**
- **OVDD: 7 pins Debug**
- **OVDD: 5 pins JTAG**
- **OVDD: 13 pins clock, resets, system control, etc.**

QorIQ LS1 Family Customer Pinout (cont.)

- **LVDD: 2 pins Ethernet Management**
- **LVDD: 13 pins “EC1”**
  - RGMII, or
  - 2 CAN interfaces, or
  - 8-channel PWM, or
  - 2 I2S Tx/Rx interfaces, or
  - Combinations of the above
- **LVDD: 13 pins “EC2”**
  - RGMII, or
  - 2 additional CAN interfaces, or
  - 8-channel PWM, or
  - USB 2.0 ULPI, or
  - Combinations of the above
- **LVDD: 13 pins “EC3”**
  - RGMII, or
  - IEEE15888, or
  - 8-channel PWM, or
  - I2S with 6 Rx or Tx data lanes and shared frame syncs/clocking
  - Combinations of the above
- **DVDD: 14 pins “QE”**
  - 2 QE UCC engines for HDLC/TDM or PROFIBUS, or
  - 2 I2S Tx/Rx interfaces, or
  - SPDIF, or
  - 8-channel PWM, or
  - LCD Controller Dual Data Rate interface (also eliminates one UART)

Introducing The QorIQ LS2 Family

Breakthrough, software-defined approach to advance the world's new virtualized networks

New, high-performance architecture built with ease-of-use in mind

Groundbreaking, flexible architecture that abstracts hardware complexity and enables customers to focus their resources on innovation at the application level

Optimized for software-defined networking applications

Balanced integration of CPU performance with network I/O and C-programmable datapath acceleration that is right-sized (power/performance/cost) to deliver advanced SoC technology for the SDN era

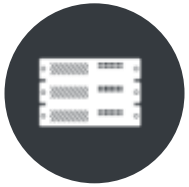
Extending the industry's broadest portfolio of 64-bit multicore SoCs

Built on the ARM® Cortex®-A57 architecture with integrated L2 switch enabling interconnect and peripherals to provide a complete system-on-chip solution

QorIQ LS2 Family

Key Features

SDN/NFV Switching



Data Center

Wireless Access

Unprecedented performance and ease of use for smarter, more capable networks

High performance cores with leading interconnect and memory bandwidth

- 8x ARM Cortex-A57 cores, 2.0GHz, 4MB L2 cache, w Neon SIMD
- 1MB L3 platform cache w/ECC
- 2x 64b DDR4 up to 2.4GT/s

A high performance datapath designed with software developers in mind

- New datapath hardware and abstracted acceleration that is called via standard Linux objects
- 40 Gbps Packet processing performance with 20Gbps acceleration (crypto, Pattern Match/RegEx, Data Compression)
- Management complex provides all init/setup/teardown tasks

Leading network I/O integration

- 8x1/10GbE + 8x1G, MACSec on up to 4x 1/10GbE
- Integrated L2 switching capability for cost savings
- 4 PCIe Gen3 controllers, 1 with SR-IOV support
- 2 x SATA 3.0, 2 x USB 3.0 with PHY

See the LS2 Family First in the Tech Lab!

4 new demos built on QorIQ LS2 processors:

- Performance Analysis Made Easy
- Leave the Packet Processing To Us
- Combining Ease of Use with Performance
- Tools for Every Step of Your Design

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