Introduction to Radiation-Resistant Semiconductor Devices and Circuits

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Abstract

This tutorial paper provides an overview of design considerations for semiconductor radiation detectors and electronics in high radiation environments. Problems specific to particle accelerator applications are emphasized and many of the presented results originated in extensive studies of radiation effects in large scale particle detectors for the SSC and LHC. Basic radiation damage mechanisms in semiconductor devices are described and specifically linked to electronic parameter changes in detectors, transistors and integrated circuits. Mitigation techniques are discussed and examples presented to illustrate how the choice of system architecture, circuit topology and device technology can extend the range of operation to particle fluences $>10^{14}$ cm^{-2} and ionizing doses >100 Mrad.

INTRODUCTION

Radiation-resistant electronics have been integral to the aerospace, nuclear reactor and weapons communities for many years, but only rather recently have they become important for particle accelerators and accelerator-based experiments. The SSC made the design of radiation-resistant detectors and electronic read-out systems a key design consideration for high-energy physics experimentalists. The energy frontier has now shifted to the LHC, which requires even higher luminosities to achieve its physics goals. Even at existing machines, for example the Tevatron at FNAL, radiation-hard electronics are required in the innermost tracking systems. The vertex detector for BaBar at the SLAC B-Factory requires radiation-hard electronics. On the accelerator side, higher beam currents and the increased sophistication of monitoring and diagnostic systems are bringing the need for radiation-resistant electronics to the forefront of designers' concerns.

Although one can argue that vacuum tubes are extremely radiation hard, the complexity of today's electronics systems restricts our focus to semiconductor devices. For all practical purposes this leaves us with silicon and gallium-arsenide devices. For a variety of reasons silicon transistors and integrated circuits comprise the bulk of radiation-hard electronics. In designing SSC and LHC detectors, we have found no compelling justification for GaAs electronics in any radiation-sensitive application. Indeed, in some areas silicon technology provides critical

performance advantages. For these reasons, despite the fascinating physics of compound semiconductors, this tutorial will emphasize silicon technology.

The study of radiation effects in semiconductor electronics and the development of radiation-resistant integrated circuits have formed an active scientific community that has produced a wealth of data and conceptual understanding. Although access to some of these results and techniques is restricted, most of the data and papers are in the public domain and readily accessible, and they provide a valuable resource (see the Bibliography at the end of this paper). Although, much has been published on basic damage mechanisms and on device properties for specific applications, when attempting to apply this information to an area outside the traditional purview of the radiation effects community, key pieces of information needed to link basic damage mechanisms to usable design guidelines are often missing. This was very clear in the development of detectors for the SSC and LHC, where both the application of detectors with deep depletion regions and novel circuit designs combining low-noise, high-speed and low power pushed developments into uncharted territory.

This is a very complicated field and developing a general road map is not easy, but one can apply a few fundamental considerations to understanding the effects of radiation on device types in specific circuit topologies and narrow the range of options that must be studied in detail. That is the thrust of this tutorial. For lack of time, some treatments are sketchier than desirable and the reader should consult the references and the bibliography. This paper originated as a tutorial talk at the 1996 Beam Instrumentation Workshop at Argonne National Laboratory in May, 1996 and will be expanded and modified in response to criticisms and new developments. (1)

RADIATION DAMAGE MECHANISMS

Semiconductor devices are affected by two basic radiation damage mechanisms:

- **Displacement damage**: Incident radiation displaces silicon atoms from their lattice sites. The resulting defects alter the electronic characteristics of the crystal.

- **Ionization damage**: Energy absorbed by electronic ionization in insulating layers, predominantly SiO_2, liberates charge carriers, which diffuse or drift to other locations where they are trapped, leading to unintended concentrations of charge and, as a consequence, parasitic fields.

Both mechanisms are important in detectors, transistors and integrated circuits. Some devices are more sensitive to ionization effects, some are dominated by displacement damage. Hardly a system is immune to either one phenomena and most are sensitive to both.

Ionization effects depend primarily on the absorbed energy, independent of the type of radiation. At typical incident energies ionization is the dominant absorption mechanism, so that ionization damage can be measured in terms of energy absorption per unit volume, usually expressed in rad or gray (1 rad= 100 erg/g, 1 Gy= 1 J/kg= 100 rad). Since the charge liberated by a given dose depends on the absorber material, the ionizing dose must be referred to a specific absorber, for example 1 rad(Si), 1 rad(SiO_2), 1 rad(GaAs), or in SI units 1 Gy(Si), etc.

Displacement damage depends on the non-ionizing energy loss, i.e. energy and momentum transfer to lattice atoms, which depends on the mass and energy of the incident quanta. A simple measure as for ionizing radiation is not possible, so that displacement damage must be specified for a specific particle type and energy.

In general, radiation effects must be measured for both damage mechanisms, although one may choose to combine both, for example by using protons, if one has sufficient understanding to unravel the effects of the two mechanisms by electrical measurements. Even non-ionizing particles can deposit some ionization dose via recoils, but this contribution tends to be very small: $2 \cdot 10^{-13}$ rad per 1 MeV neutron/cm^2, for example. (2)

To set the scale, consider a tracking detector operating at the LHC with a luminosity of 10^{34} cm^{-2}s^{-1}. In the innermost volume of a tracker the particle flux from collisions is $n' \approx 2 \cdot 10^9 / r_\perp^2$ cm^{-2}s^{-1}, increasing roughly twofold in the outer layers due to interactions and loopers. At $r_\perp$=30 cm the particle fluence after one year of operation (10^7 s) is about $2 \cdot 10^{13}$ cm^{-2}. A fluence of $3 \cdot 10^{13}$ cm^{-2} of minimum ionizing particles corresponds to an ionization dose of 1 Mrad, obtained after 1.5 years of operation. Albedo neutrons from a calorimeter could add a yearly fluence of 10^{12} to 10^{13} cm^{-2}.

Displacement Damage

An incident particle or photon capable of imparting an energy of about 20 eV to a silicon atom can dislodge it from its lattice site. Displacement damage creates defect clusters. For example, a 1 MeV neutron transfers about 60 to 70 keV to the Si recoil atom, which in turn displaces roughly 1000 additional atoms in a region of about 0.1 μm size. Displacement damage is proportional to non-ionizing energy loss (3), which is not proportional to the total energy absorbed, but depends on the particle type and energy. Non-ionizing energy loss for a variety of particles has

been calculated over a large energy range. (4) Although not verified quantitatively, these curves can be used to estimate relative effects. X-rays do not cause direct displacement damage, since momentum conservation sets a threshold energy of 250 keV for photons. ^{60}Co γ rays cause displacement damage primarily through Compton electrons and are about three orders of magnitude less damaging per photon than a 1 MeV neutron. (5) Table 1 gives a rough comparison of displacement damage for several types of radiation.

Particle	**proton**	**proton**	**neutron**	**electron**	**electron**
Energy	1 GeV	50 MeV	1 MeV	1 MeV	1 GeV
Relative Damage	1	2	2	0.01	0.1

TABLE 1. Relative displacement damage for various particles and energies.

Displacement damage manifests itself in three important ways:

- formation of mid-gap states, which facilitate the transition of electrons from the valence to the conduction band. In depletion regions this leads to a generation current, i.e. an increase in the current of reverse-biased pn-diodes. In forward biased junctions or non-depleted regions mid-gap states facilitate recombination, i.e. charge loss.

- states close to the band edges facilitate trapping, where charge is captured and released after a certain time.

- a change in doping characteristics (donor or acceptor density).

The role of mid-gap states is illustrated in Fig. 1. Because interband transitions in Si require momentum transfer (“indirect band-gap”), direct transitions between the conduction and valence bands are extremely improbable (unlike GaAs, for example). The introduction of intermediate states in the forbidden gap provides “stepping stones” for emission and capture processes. The individual steps, emission of holes or electrons and capture of electrons or holes, are illustrated in Fig. 1. As shown in Fig. 1a, the process of hole emission from a defect can also be viewed as promoting an electron from the valence band to the defect level. In a second step (1b) this electron can proceed to the conduction band and contribute to current flow, generation current. Conversely, a defect state can capture an

electron from the conduction band (1c), which in turn can capture a hole (1d). This "recombination" process reduces current flowing in the conduction band.

Since the transition probabilities are exponential functions of the energy differences, all processes that involve transitions between both bands require mid-gap states to proceed at an appreciable rate. Given a distribution of states these processes will "seek out" the mid-gap states. Since the distribution of states is not necessarily symmetric, one cannot simply calculate recombination lifetimes from generation currents and vice versa (as is possible for a single mid-gap state, as assumed in textbooks). Whether generation or recombination dominates depends on the relative concentration of carriers and empty defect states. In a depletion region the conduction band is underpopulated, so generation prevails. In a forward biased junction carriers flood the conduction band, so recombination dominates. Fig. 1 also shows a third phenomenon; defect levels close to a band edge will capture charge and release it after some time, a process called "trapping" (Fig. 1e).

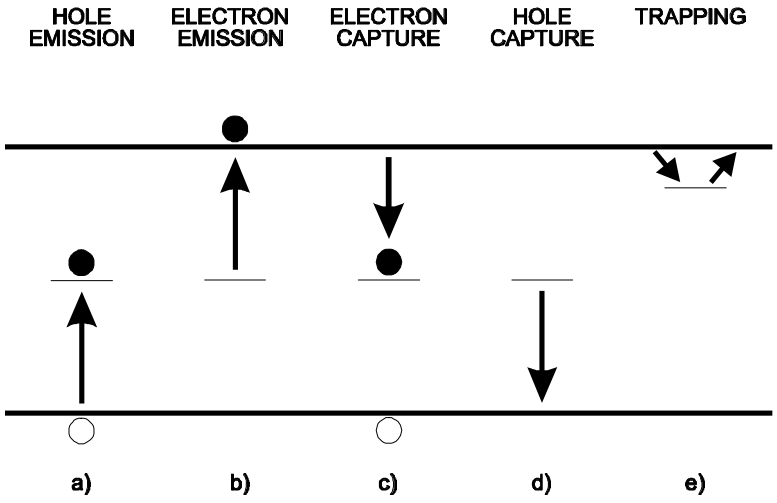

FIGURE 1. Emission and capture processes through intermediate states. The arrows show the direction of electron transitions.

In a radiation detector or photodiode system the increased reverse-bias current increases the electronic shot noise. The change in doping level affects the width of the depletion region (or the voltage required for full depletion). The decrease in carrier lifetime incurs a loss of signal as carriers recombine while traversing the depletion region. As will be shown later, the same phenomena occur in transistors, but are less pronounced, depending on device type and structure. Displacement damage effects will be discussed in more detail in the section on diodes.

Ionization Damage

As in the detector bulk, electron-hole pairs are created in the oxide. The electrons are quite mobile and move to the most positive electrode. Holes move by a rather complex and slow hopping mechanism, which promotes the probability of trapping in the oxide volume and an associated fixed positive charge. Holes that make it to the oxide-silicon interface can be captured by interface traps. This is illustrated in Fig. 2, which shows a schematic cross-section of an *n*-channel MOSFET. A positive voltage applied to the gate electrode attracts electrons to the surface of the silicon beneath the gate. This "inversion" charge forms a conductive channel between the *n*+ doped source and drain electrodes. The substrate is biased negative relative to the MOSFET to form a depletion region for isolation. Holes freed by radiation accumulate at the oxide-silicon interface. The positive charge buildup at the silicon interface requires that the gate voltage be adjusted to more negative values to maintain the negative charge in the channel.

Trapped oxide charge can also be mobile, so that the charge distribution generally depends on time, and more specifically, how the electric field in the oxide changes with time. The charge state of a trap depends on the local quasi Fermi level, so the concentration of trapped charge will vary with changes in the applied voltage and state-specific relaxation times. As charge states also anneal, ionization

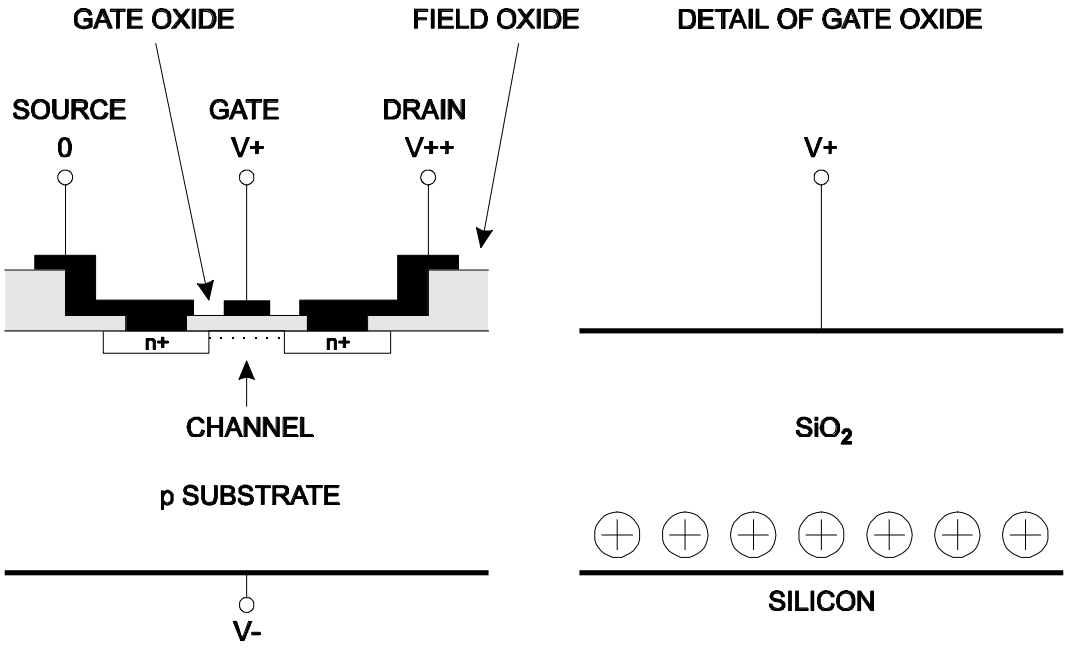

FIGURE 2. Schematic cross section of an n-channel MOSFET (left). A detail of the gate oxide shows the trapped holes at the oxide-silicon interface (right).

effects depend not only on the dose, but also on the dose rate. Fig. 2 also shows a thick field oxide, which serves to control the silicon surface charge adjacent to the FET and prevent parasitic channels to adjacent devices. The same positive charge buildup as in the gate oxide also occurs here, indeed it can be exacerbated because the field oxide is quite thick. For more details, see ref. (6), currently the authoritative text on ionization effects.

In summary, ionization effects are determined by

- Interface trapped charge
- Oxide trapped charge
- The mobility of trapped charge
- The time and voltage dependence of charge states

Although the primary radiation damage depends only on the absorbed ionizing energy, the resulting effects of this dose depend on the rate of irradiation, the applied voltages and their time variation, the temperature, and the time variation of the radiation itself. Ionization damage manifests itself most clearly in MOS field effect transistors, so it will be discussed in more detail in that section.

EFFECTS ON DEVICE CHARACTERISTICS

Radiation Damage in Diodes

Diode structures are basic components of more complex devices, for example bipolar transistors, junction FETs and integrated circuits. Since the properties of diode depletion regions are determined primarily by bulk properties, measurements on diodes will serve to illustrate the effects of displacement damage. Reverse biased diodes with large depletion depths are used as radiation detectors and photodiodes. Because of their large depletion depths, typically hundreds of microns, detector diodes are very sensitive to bulk damage and extensive work by the SSC/LHC community has produced many insights into bulk radiation effects. Affected are the detector leakage current, the doping characteristics, and charge collection.

A theoretical analysis from first principles is quite complex, due to the many phenomena involved. Take doping changes as an example. Si interstitials are quite active and displace either P donors or B acceptors from substitutional sites and render them electrically inactive. These interstitial dopants together with oxygen,

commonly present in the lattice as an impurity, react in very different ways with vacancies to form complexes with a variety of electronic characteristics (see ref. (7) and references therein). Fortuitously, although a multitude of competing effects can be invoked in to predict and interpret experimental results, the data can be described by rather simple parametrizations.

The increase in reverse bias current (leakage current) is linked to the creation of mid-gap states. Experimental data are consistent with a uniform distribution of active defects in the detector volume. The bias current after irradiation

$$I_{\mathrm{det}} = I_0 + \alpha \cdot \Phi \cdot Ad \tag{1}$$

where I_0 is the bias current before irradiation, α is a damage coefficient dependent on particle type and fluence, Φ is the particle fluence, and the product of detector area and thickness Ad is the detector volume. For 650 MeV protons $\alpha \approx 3 \cdot 10^{-17}$ A/cm (8,9) and for 1 MeV neutrons (characteristic of the albedo emanating from a calorimeter) $\alpha \approx 2 \cdot 10^{-17}$ A/cm. (9) The parametrization used in Eq. 1 is quite general, as it merely assumes a spatially uniform formation of electrically active defects in the detector volume, without depending on the details of energy levels or states.

The coefficients given above apply to room temperature operation. The reverse bias current of silicon detectors depends strongly on temperature

$$I_R(T) \propto T^2 e^{-E/2k_B T} \tag{2}$$

if the generation current dominates (10), as is the case for substantial radiation damage. The effective activation energy $E = 1.2$ eV for radiation damaged samples (8)(11)(12), whereas unirradiated samples usually exhibit $E = 1.15$ eV. The ratio of currents at two temperatures T_1 and T_2 is

$$\frac{I_R(T_2)}{I_R(T_1)} = \left(\frac{T_2}{T_1} \right)^2 \exp\left[-\frac{E}{2k_B} \left(\frac{T_1 - T_2}{T_1 T_2} \right) \right] \tag{3}$$

After irradiation the leakage current initially decreases with time. Pronounced short term and long term annealing components are observed and precise fits to the annealing curve require a sum of exponentials. (9) Experimentally, decreases by factors of 2 to 3 have been observed with no further improvement after 5 months or so. (8,5) In practice, the variation of leakage current with temperature is very reproducible from device to device, even after substantial doping changes due to radiation damage. The leakage current can be used for dosimetry and diodes are offered commercially specifically for this purpose.

The effect of displacement damage on doping characteristics has been investigated in the course of detector studies for the SSC and LHC and is still the subject of ongoing study. Measurements on a variety of strip detectors and photodiodes by groups in the U.S., Japan and Europe have shown that the effective doping of *n* type silicon initially decreases, becomes intrinsic (i.e. very little space charge) and then turns *p*-like, with the space charge increasing with fluence. This phenomenon is consistent with the notion that acceptor sites are formed by the irradiation, although this does not mean that mobile holes are created. (13) Initially, the effective doping level N_d-N_a decreases as new acceptor states neutralize original donor states. At some fluence the two balance, creating "intrinsic" material, and beyond this fluence the acceptor states dominate. In addition, there is evidence for a concurrent process of donor removal. (14,15) Since the probability of donor removal is proportional to the initial donor concentration N_{d0}, whereas the formation of defects leading to acceptor states is proportional to fluence, the effective space charge density N_{eff} of *n* type starting material after exposure to a particle fluence Φ is described by (16)

$$N_{eff}(\Phi) = -N_{d0}e^{-c\Phi} + g_c\Phi + g_s\Phi \cdot e^{-t/\tau(T)} + N_Y(\Phi, t, T) \qquad (4)$$

where a negative or positive sign of N_{eff} denotes whether the effective space charge is *n*- or *p*-like. The first term describes the removal of donors and the second the creation of acceptors. c and g_c are constants for a given particle type and energy that describe the stable component of radiation damage. The third and fourth terms describe the time and temperature dependent changes in the effective doping concentration and will be discussed later. For high energy protons the average from many measurements is $c = (0.96\pm0.19)\cdot10^{-13}$ cm^2 and $g_c = (1.15\pm0.09)\cdot10^{-2}$ cm^{-1}. Type inversion from *n* to *p* type silicon occurs at a fluence of about 10^{13} cm^{-2}. Data for 1 MeV equivalent neutrons yield $c = (2.29\pm0.63)\cdot10^{-13}$ cm^2 and $g_c = (1.77\pm0.07)\cdot10^{-2}$ cm^{-1}. (9)

After a proton fluence $\Phi = 10^{14}$ cm^{-2} the acceptor concentration before annealing is 10^{12} cm^{-3}, which requires a bias voltage of 165V for full depletion of a 300 μm thick detector. At first glance, it would seem that beginning with a higher *n* doping level N_{d0} (lower resistivity) would increase overall detector lifetime. Although the inversion fluence increases with larger values of N_{d0}, the difference in doping concentration is negligible at larger fluences since the exponential term quickly becomes insignificant. (15) For example, as shown in Fig. 3 materials with initial doping densities of 10^{12} cm^{-3} and 10^{13} cm^{-3} lie within 15% at $\Phi = 5\cdot10^{13}$ cm^{-2}.

Very high resistivity silicon ($\rho > 10$ kΩcm or $N_d < 4\cdot10^{11}$ cm^{-3}) is often highly compensated, $N_{eff}=N_d-N_a$ with $N_d \sim N_a >> N_{eff}$, so that minute changes to either donors or acceptors can alter the net doping concentration significantly, and the

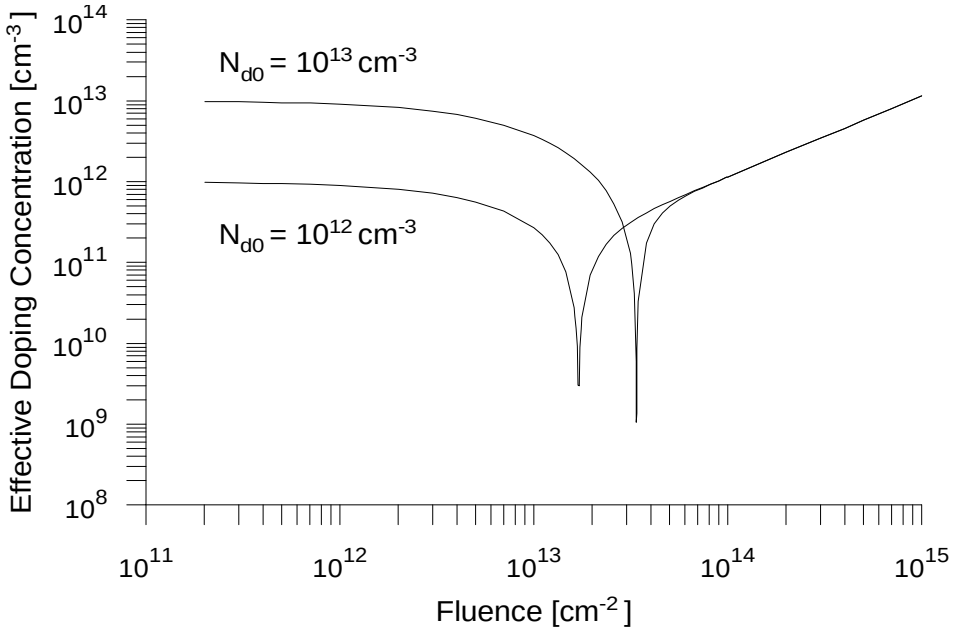

FIGURE 3. Calculated effective doping concentration vs. high-energy proton fluence for silicon with initial donor concentrations N_{d0} of 10^{12} and 10^{13} cm^{-3}.

above equations must be modified accordingly. Moderate resistivity *n* type material (ρ = 1 to 5 kΩcm) used in large area tracking detectors is usually dominated by donors.

Annealing of ionized acceptor states

After defect states are formed by irradiation, their electronic activity changes with time. A multitude of processes contribute, some leading to beneficial annealing, i.e. a reduction in acceptor-like states, and some increasing the acceptor concentration. The third term in Eq. 4 describes the beneficial annealing (17), where g_s= $1.93 \cdot 10^{-2}$ cm^{-1} and τ(T)= $(6 \cdot 10^6) \cdot \exp[-0.175(T-273.2)]$ s (to set the scale, τ(0°C)= 70 d). The fourth term in Eq. 4

$$N_Y(\Phi, t_{1/2}, T) = g_Y \Phi \cdot \left[1 - \frac{1}{1 + g_Y \Phi \cdot k(T) \cdot t} \right] \quad (5)$$

where for 1 MeV neutrons g_Y= $(4.6 \pm 0.3) \cdot 10^{-2}$ cm^{-1} and for 1 GeV protons values of g_Y= $(4.97 \pm 0.23) \cdot 10^{-2}$ cm^{-1} (16) and $(5.8 \pm 0.3) \cdot 10^{-2}$ cm^{-1} (9) have been found. The temperature dependent evolution is determined by

$$k(T) = k_0 \, e^{-E_a / k_B T} \quad (6)$$

Typical parameter sets are k_0 = (0.85+25-0.82) cm^3/s and E_a = 1.16±0.08 eV (16), and k_0 = (520+1590-392) cm^3/s and E_a = 1.31±0.04 eV (9).

Anti-annealing is a concern because of its effect on detector depletion voltage, i.e. the voltage required to collect mobile charge from the complete thickness of the silicon detector. Since this voltage increases with space-charge concentration, antiannealing can easily exceed the safe operating range, especially at high fluences. The relative effect of anti-annealing increases strongly with fluence and temperature, as illustrated in Table 2, which shows the relative increase in doping and required operating voltage. Clearly, low temperature operation is beneficial. Nevertheless, even a low temperature system will require maintenance at room temperature and warm up periods must be controlled very carefully. (9,16)

Fluence [cm^{-2}]	$N_a(t=100\text{h})/N_a(t=0) = V(t=100\text{h})/V(t=0)$		
	0 °C	20 °C	40 °C
10^{13}	1.00	1.02	1.39
10^{14}	1.01	1.21	4.71

TABLE 2. Relative antiannealing after 100 h vs. fluence and temperature

Data on charge collection efficiency are still rather sketchy. The primary mechanism is expected to be trapping of signal charge at defect sites, i.e. a decrease in carrier lifetime τ. Since the loss in signal charge is proportional to $\exp(-t_c/\tau)$, reducing the collection time mitigates the effect. Since either the operating voltage is increased or depletion widths are reduced at damage levels where charge trapping is appreciable, fields tend to be higher and collection times decrease automatically with radiation damage, provided the detector can sustain the higher fields.

Typical measurements have determined the signal charge vs. bias voltage and have taken the plateau value (or the maximum signal charge just below break-down). Lemeilleur et al. (18) find $\Delta Q/Q_0 = \gamma\Phi$, where $\gamma = (0.024\pm0.004)\cdot10^{-13}$ cm^2 for 1 MeV equivalent neutrons. Fretwurst et al. (19) find similar results, with a dependence $1/\tau = \gamma\Phi$, where for holes $\gamma_p = 2.7\cdot10^{-7}$ cm^{2}s and for electrons $\gamma_e = 1.2\cdot10^{-6}$ cm^{2}s for $\Phi > 10^{13}$ cm^{-2} of 1 MeV equivalent neutrons. For a fluence $\Phi = 5\cdot10^{13}$ cm^{-2}s^{-1}, a 400 μm thick detector with a depletion voltage of 130V operated at a bias voltage of 200V would show a decrease in signal charge of 12%. Ohsugi et al. (20) have demonstrated the operation of strip detectors to neutron fluences beyond 10^{14} cm^{-2}, with signal losses of about 10%. Similar results

have been obtained on fully irradiated strip detectors read out by LHC compatible electronics. (21)

The basic detector is insensitive to ionization effects. In the bulk, ionizing radiation creates electrons and holes that are swept from the sensitive volume; charge can flow freely through the external circuitry to restore equilibrium. The problem lies in the peripheral structures, the oxide layers that are essential to controlling leakage paths at the edge of the diode and to preserving inter-electrode isolation in segmented detectors.

The positive space charge due to hole trapping in the oxide and at the interface (see Fig. 2) attracts electrons in the silicon bulk to the interface. These accumulation layers can exhibit high local electron densities and form conducting channels, for example between the detector electrodes. This is especially critical at the "ohmic" electrodes in double-sided detectors, where the absence of *pn* junctions makes operation rely on full depletion of the silicon surface (even without radiation, the silicon surface tends to be n-type, so the ohmic side of n type detectors is inherently more difficult to control). (22,23)

Some detectors include integrated coupling capacitors and biasing networks. Biasing structures such as punch-through resistors and MOSFET structures are subject to ionization damage. Although these devices can remain functional, substantial changes in voltage drop have been reported for punch-through and accumulation layer devices, whereas measurements on polysilicon resistors irradiated to 4 Mrad (65 MeV p) show no effect. (24)

Radiation Damage in Transistors and Integrated Circuits

In principle, the same phenomena discussed for detectors also occur in transistors, except that the geometries of transistors are much smaller (depletion widths <1 μm) and the typical doping levels are higher (>10^{15} cm^{-3}).

Bipolar Transistors

The most important damage mechanism in bipolar transistors is the degradation of DC current gain at low currents. The damage mechanism is the same that causes increased leakage current in detectors, formation of mid-gap states by displacement damage. The difference is that the base-emitter junction is forward biased, so the high carrier concentration in the conduction band tips the balance from generation to recombination (see Fig. 1). The fractional carrier loss depends on the relative concentrations of injected carriers and defects. Consequently, the reduction of DC current gain due to radiation damage depends on current density. For a given collector current a small device will suffer less degradation in DC current gain than a large one.

Since the probability of recombination depends on the transit time through the junction region, reduced base width will also improve the radiation resistance. Base width is strongly linked with device speed, so that the reduction in DC current gain β_{DC} scales inversely with a transistor's unity gain frequency f_T . (25)

$$\frac{1}{\beta_{DC}} = \frac{1}{\beta_0} + \frac{\Phi}{f_T} \tag{7}$$

Since IC technology is driven primarily by device speed, mainstream market forces will indirectly improve the radiation resistance of bipolar transistor processes. Mid-gap states also limit the low current performance before irradiation. Over the past decade, evolutionary improvements in contamination control and process technology have also yielded substantially better low-current performance. Measurements on bipolar transistors from several vendors have shown that processes not specifically designed for radiation resistance are indeed quite usable in severe radiation environments, even at low currents. (26,27,28).

Changes in doping levels have little effect in bipolar transistors. Typical doping levels in the base and emitter are $N_B = 10^{18}$ and $N_E = 10^{20}$ cm^{-3}. In the collector depletion region doping levels are smaller, typically 10^{16}, rising to 10^{18} or 10^{19} at the collector contact. At these levels the change in doping level due to displacement damage ($\Delta N_A \approx 10^{12}$ cm^{-3} at $\Phi = 10^{14}$ cm^{-2}) is negligible, although local device temperatures may be high enough that anti-annealing leads to noticeable effects.

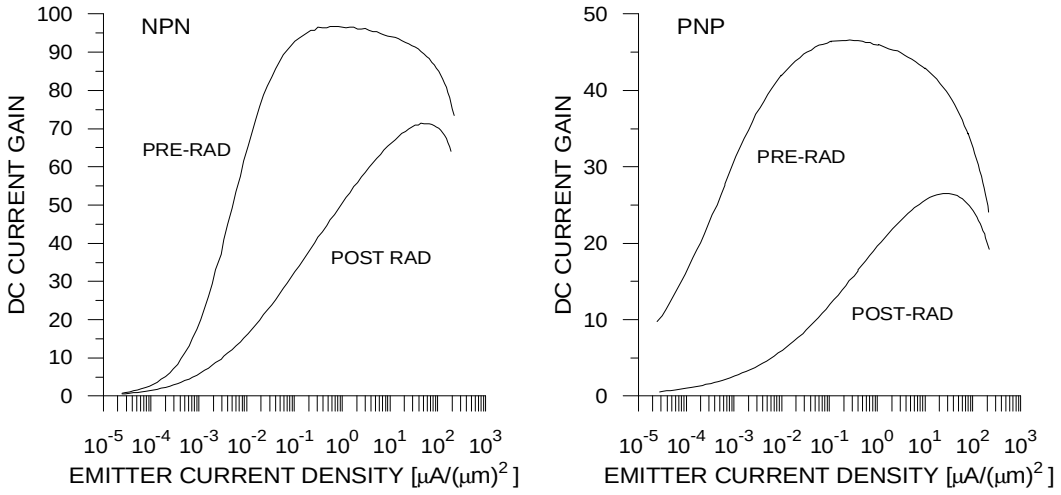

FIGURE 4. DC current gain of npn and pnp transistors before and after irradiation to a fluence of $1.2 \cdot 10^{14}$ cm^{-2} (800 MeV protons).

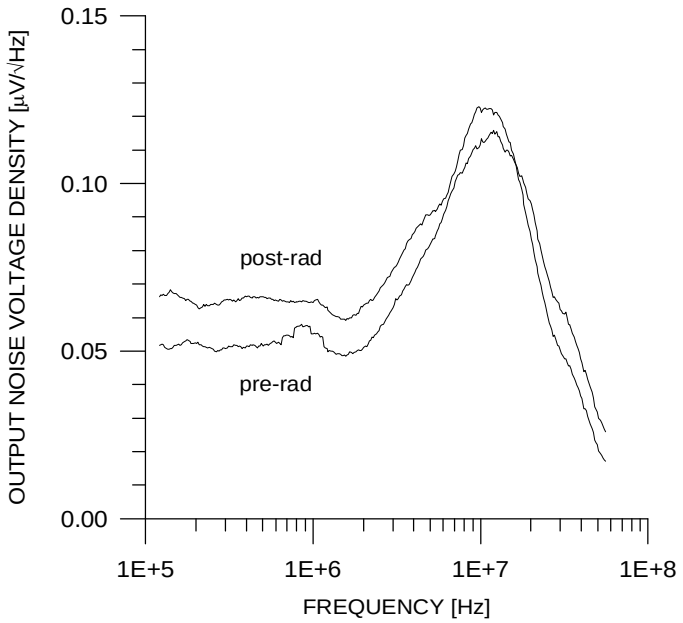

FIGURE 5. Noise of a bipolar transistor preamplifier before and after irradiation to a fluence of $1.2 \cdot 10^{14}$ cm^{-2} (800 MeV protons).

Figure 4 shows measured DC current gain for *npn* and *pnp* bipolar transistors irradiated to a fluence of $1.2 \cdot 10^{14}$ cm^{-2} (800 MeV protons). (26) These devices, fabricated in AT&T's CBIC-V2 high-density complementary *npn-pnp* IC process, exhibit f_T = 10 GHz for the *npn* and 4.5 GHz for the *pnp* transistors. In the CAFE chip designed for the ATLAS silicon tracker (29) the *npn* input device is operated at a current density of about 2 $\mu A/(\mu m)^2$, where the post-rad current gain decreases to about 60% of its initial value. Although a smaller transistor would deteriorate less, the thermal noise contribution of the parasitic base resistance would be excessive, so a compromise is necessary. No measurable changes in transconductance were measured, as expected. The output resistance of these devices decreased by <10% after irradiation. Similar results have been measured on comparable devices fabricated by Maxim (Tektronix) (27,28) and Westinghouse. (30)

Noise degradation has been measured on individual transistors and complete preamplifier circuits. The results are consistent with the measured degradation in DC current gain and no change in transconductance or parasitic resistances, as expected. Figure 5 shows the measured spectral noise density of a monolithically integrated preamplifier before and after irradiation to $1.2 \cdot 10^{14}$ cm^{-2} (800 MeV protons). (26) The gain increased by a few percent after irradiation, so the input noise increase is somewhat smaller than shown.

Junction Field Effect Transistors (JFETs)

JFETs (either silicon or GaAs) can be quite insensitive to both ionization and displacement effects. In these devices a conducting channel from the source to the drain is formed by appropriate doping, typically *n* type. The gate electrode is doped *p* type so that applying a reverse bias voltage relative to the channel will form a depletion region that changes the cross section of the conducting channel. (31) At low values of gate and drain voltages the channel is contiguous and resistive. At higher voltage levels the channel becomes fully depleted near the drain, but the current flow is still determined by the conducting channel near the source. Since the gate voltage now controls both the geometry and potential distribution, voltage-current characteristics become more complex and the device acts much like a controlled current source, i.e. it exhibits a high output resistance.

With respect to radiation effects, the important fact is that device characteristics are determined essentially by the geometry and doping level of the channel. Typical doping levels are 10^{15} to 10^{18} cm^{-3}, so the effect of radiation-induced acceptor states is small. Silicon JFETs exhibit very good radiation resistance. Measurements on both standard commercial devices and custom designed integrated circuits have shown minimal changes in gain at fluences $>10^{14}$ neutrons/cm^2 and ionization doses up to 100 Mrad. (32,33,34). Low frequency noise (f < 100 kHz) may increase by an order of magnitude, but at high frequencies very little change in noise is observed. Measurements of Si JFETs at 90K also exhibit excellent radiation characteristics. (33)

In some applications, analog storage circuitry for example, gate leakage current is important. Generation current in the gate depletion region due to displacement damage can affect the gate current strongly. Measurements on commercial JFETs irradiated by high-energy electrons to 100 Mrad ($\Phi \approx 10^{15}$ cm^{-2}) show the gate reverse current increasing 100 fold from an initial value of 70 pA. (35) Here one should choose the smallest geometry device commensurate with other requirements.

At this point it is worth noting that the superior radiation resistance claimed for GaAs ICs has more to do with the use of JFETs or MESFETs (a Schottky barrier JFET) than the properties of the semiconductor. These devices are more radiation resistant than silicon MOSFETs (discussed below), but suffer from a much lower circuit density.

Metal-Oxide Silicon Field Effect Transistors (MOSFETs)

Within the FET family, MOSFETs present the most pronounced ionization effects, as the key to their operation lies in the oxide that couples the gate to the channel. As described above and illustrated in Fig. 2, positive charge buildup due to hole trapping in the oxide and at the interface shifts the gate voltage required for a given operating point to more negative values. This shift affects the operating points in analog circuitry and switching times in digital circuitry. Reducing the thickness of the gate oxide t_{ox} greatly improves the radiation resistance; gate voltage shifts scaling with t_{ox}^2 to t_{ox}^3 for a given dose have been observed. (6) Thinner gate oxides are required for small channel lengths, so higher density processes tend to improve the radiation resistance even without special hardening techniques. The gate voltage shift is typically expressed in terms of threshold voltage V_T, which roughly marks the onset of appreciable current flow.

Typical threshold shifts for a 1.2 μm radiation-hardened CMOS IC process with a 20 nm thick gate oxide are shown in Fig. 6. (36) After exposure to 5 Mrad(Si) of ^{60}Co irradiation, NMOS thresholds shift by 200 mV and PMOS levels change by 150 mV. For both NMOS and PMOS devices the threshold voltage shifts to more negative values as expected from positive charge buildup in the oxide. The slight upturn above 2 Mrad in the NMOS curve is typical and reflects the buildup of interface states. (6) About 70% of the threshold shifts occur during the first 250 krad, also a typical phenomenon. Measurements to 125 Mrad on a similar process show a total threshold shift of 400 mV for NMOS and 100 mV for PMOS with little increase beyond 10 Mrad. (37)

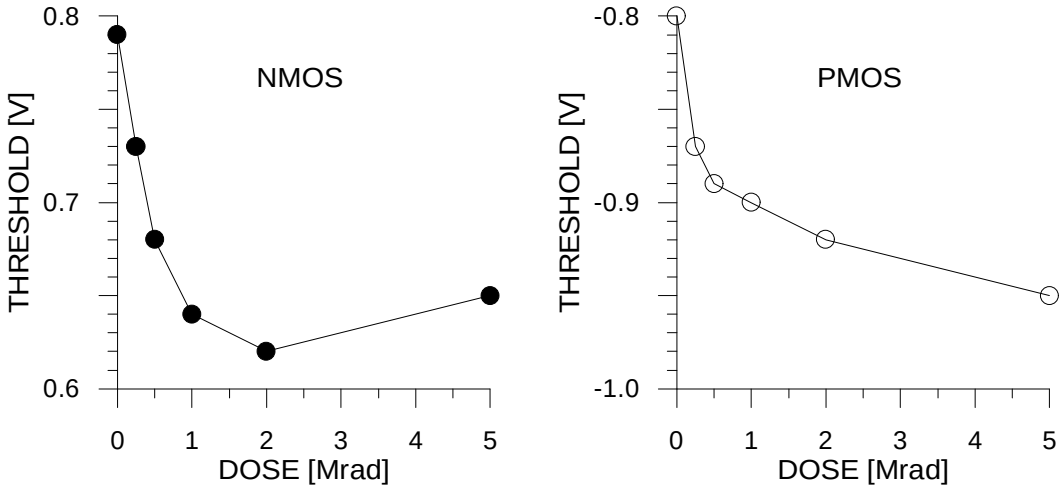

FIGURE 6. Threshold voltage shifts for radiation-hardened NMOS and PMOS transistors vs. ^{60}Co radiation dose.

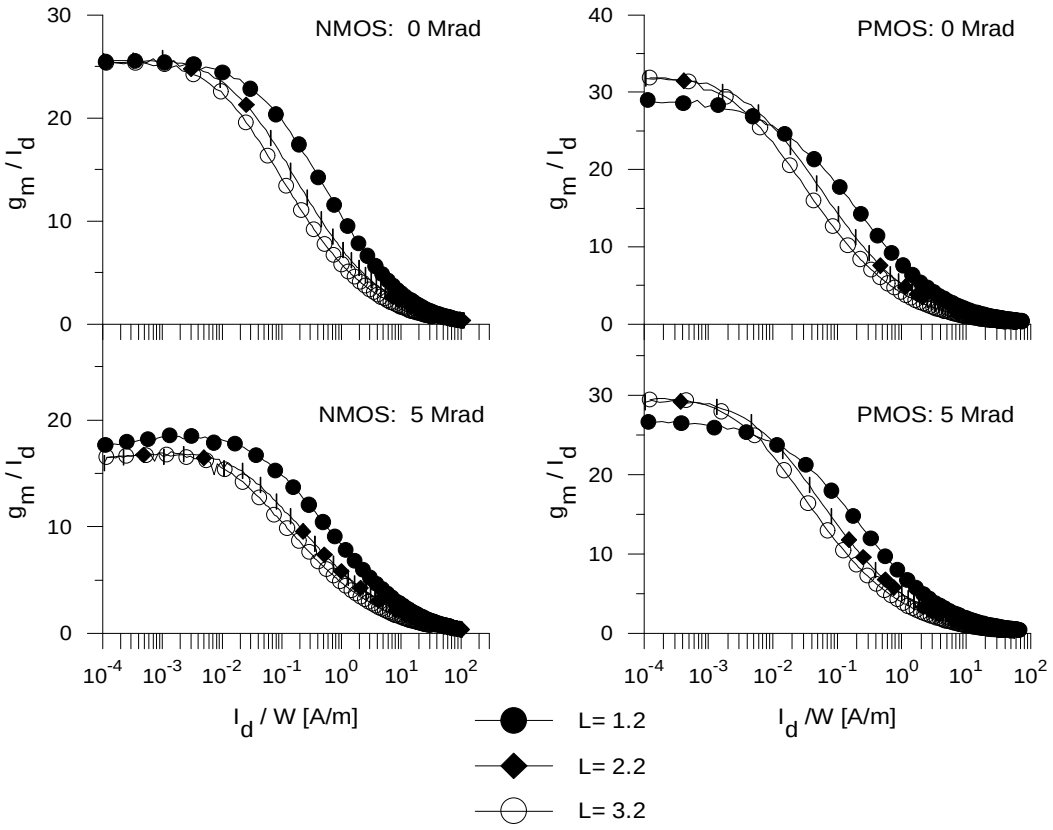

FIGURE 7. Normalized transconductance g_m/I_d vs. drain current I_d/W for NMOS and PMOS transistors with channel lengths of 1.2, 2.2 and 3.2 μm before and after ^{60}Co irradiation to 5 Mrad (Si).

Figure 7 shows the normalized transconductance g_m/I_d vs. I_d/W before and after irradiation. (36) For the selected channel length this representation allows direct scaling to any device width at a given current density. For example, to operate a 1.2 μm NMOS transistor in moderate inversion one might choose a normalized drain current I_d/W= 0.3 A/m, yielding I_d= 0.3 mA for a 1 mm wide transistor. The normalized transconductance g_m/I_d= 15.4 V^{-1} or g_m= 4.6 mS. After exposure to 5 Mrad g_m/I_d= 11.8 V^{-1} or g_m= 3.5 mS. Typically, the NMOS devices suffer a 20 to 30% degradation, whereas the PMOS devices are quite insensitive to radiation, with only a few percent decrease in transconductance at 5 Mrad. About half of the observed change at 5 Mrad occurred before attaining a dose of 1 Mrad.

Extensive noise measurements have been performed at the University of Pennsylvania (38) and by a UCSC/LBNL group. (36) In the latter, spectral noise density was measured over a frequency range of 10 kHz to 10 MHz before and

Type	NMOS	PMOS	NMOS	PMOS	NMOS	PMOS	NMOS	PMOS
Width	75	75	1332	1332	888	888	1332	1332
Length	1.2	1.2	1.2	1.2	2.2	2.2	3.2	3.2
***I_d/W*= 0.03**								
0 Mrad			0.81	0.61	0.64	0.59	0.66	0.50
5 Mrad			2.17	0.84	1.00	0.58	1.50	0.69
***I_d/W*= 0.1**								
0 Mrad	1.10	0.70	1.20	1.10	0.80	0.80	0.80	0.60
5 Mrad	3.80	1.10	3.40	1.60	1.30	0.90	1.70	0.70
***I_d/W*= 0.3**								
0 Mrad	1.60	1.30	2.00	1.70	1.10	1.00	1.10	0.77
5 Mrad	5.00	2.90	4.80	2.70	1.60	1.40	1.20	0.81

TABLE 3. Noise coefficients $\gamma_n = v_n^2 \cdot g_m/4kT$ for NMOS and PMOS transistors of various widths and lengths, operated at current densities I_d/W= 0.03, 0.10 and 0.3 A/m, before and after ^{60}Co irradiation to 5 Mrad(Si). Widths and lengths are given in μm.

after ^{60}Co irradiation to a dose of 5 Mrad(Si). The noise was measured at three representative drain current densities I_d/W. Again, these data can be scaled to any device width, where the noise scales with $W^{-1/2}$. The difference between the NMOS and PMOS results is striking. The NMOS devices show a much greater degradation and the PMOS devices also exhibit substantially less low-frequency noise. The low-frequency noise spectral density of the NMOS devices can be described by $v_n^2 = A_f/q + B$, where q ranges from 0.8 to 1.0 and is constant for all currents for the same geometry. The changes in q after a dose of 5 Mrad are of order 0.1. The noise coefficient A_f is about 1.0 to $1.5 \cdot 10^{-30}$ V^2 pre-rad and 5 to $10 \cdot 10^{-30}$ V^2 post-rad. Before irradiation, A_f scales well with inverse gate area, but no clear pattern is observed after irradiation. The low frequency noise behavior of the PMOS devices is more complex and cannot be parameterized in this simple manner, but the devices exhibit substantially better noise than the NMOS transistors.

White noise was evaluated at high frequencies and is characterized by the noise coefficient $\gamma_n = v_n^2 \cdot g_m/4kT$ to assess the inherent noise properties independent of transconductance. Results for various device geometries and current densities are shown in Table 3. For these measurements the substrate was biased at the source potential.

Again, we see substantially less post-radiation degradation in the PMOS devices. One can also observe the higher intrinsic noise of NMOS short channel devices. Although the observed degradation is quite small in some cases, typically it is quite substantial and would need to be compensated for by a considerably higher operating current. Seller et al. have exposed low-noise preamplifiers fabricated in a rad-hard 1.2 μm bulk CMOS process to a dose of 100 Mrad and measured noise and gain. (37) Gain decreased by no more than 7%, but the increase in equivalent input noise at high frequencies ranged from 20 to 75%. This process is only specified to 5 Mrad, so these results indicate that circuits are still quite usable at much higher doses, if one can accommodate the increase in noise.

Due to the presence of mobile trapped charge, threshold behavior can become quite difficult to predict when the gate voltage changes appreciably with varying duty cycles, as in logic circuitry. Detectors and analog circuitry are simpler by comparison, since the voltage levels are either static or change with a fixed period, as in analog pipelines, for example. In general, when performing ionization damage tests devices must be operated at typical operating voltages and digital circuitry must be clocked at frequencies and patterns approximating typical operation.

Generally speaking, both bulk and SOI (silicon on insulator) CMOS are subject to the effects described above. SOI is often cited as a specifically radiation-hard technology because of its resistance to transient radiation effects, primarily latchup due to photocurrents developed at high intensity bursts of radiation ($>10^6$-10^7 rad/s) typical of nuclear detonations. Although SOI can provide superior device speed because of reduced stray capacitance, this technology is not inherently more resistant to radiation in our applications. If anything, the additional oxide interfaces tend to complicate matters and at this time most radiation-resistant CMOS processes are on bulk silicon.

Radiation Effects in Integrated Circuit Structures

The preceding discussion has emphasized the properties of individual devices. In integrated circuits many devices are placed close together. As mentioned above, the silicon surface is naturally *n*-type, so isolation structures are required to preclude unwanted cross-coupling between devices. Two basic techniques are used:

- junction isolation, where reverse-biased *pn* junctions provide both ohmic and capacitive isolation.

- oxide isolation, where oxide layers with carefully controlled interface properties deplete the adjacent silicon of mobile charge.

More detailed information on these processes can be in texts on IC technology, for example (39).

Junction isolation is very robust, but requires substantial additional space. Oxide isolation allows higher packing densities and is used by most high-density IC processes. All CMOS processes utilize some form of oxide isolation, whereas bipolar transistor processes can be found with both junction and oxide isolation. Under irradiation the oxide layers used for isolation suffer from the same phenomena described for the gate oxide of MOSFETs (see field oxide in Fig. 2). Since isolation oxides are thicker than gate oxides, more electron-hole pairs are formed by incident radiation. Furthermore, the fields in the isolation oxide tend to be much lower, so charge trapping in the oxide will be exacerbated. Developing radiation-hard isolation oxides (field oxides) was a major challenge in the development of high-density radiation-hard CMOS and remains one of the few "secret" process ingredients (for a basic discussion see (6)).

Problems can occur when inherently radiation-hard devices, notably JFETs and bipolar transistors, are used in a non-hardened oxide-isolated processes. Here radiation effects in the isolation structures can severely affect the radiation resistance of the devices. Clues to the importance of such parasitic ionization effects can be gleaned from a comparison of neutron and photon irradiations. Conventional (non-hardened) processes using oxide isolation have yielded good results in measurements to fluences $>10^{14}$ cm^{-2} (27,28), demonstrating that oxide isolation can be acceptable and that the suitability of these processes must be determined case-by-case.

IC processes also use special device structures to facilitate the integration of different device types. A prime example is the lateral *pnp* transistor, a structure more compatible with a standard CMOS process than "classic" vertical bipolar transistors. In a lateral transistor the emitter, base and collector are arranged along the surface of the silicon with large-area exposure to oxide interfaces. Unlike vertical bipolar transistors, lateral devices are very susceptible to ionizing radiation, as surface leakage causes severe degradation of DC current gain. Lateral *pnp* transistors can be used as current sources or high impedance loads, if the biasing circuitry is designed to accommodate substantial increases in base currents.

MITIGATION TECHNIQUES

Although little can be done to reduce radiation damage in a given device, many techniques can be applied to reduce the effects of radiation damage to an overall system. The goal of radiation-hard design is not so much to obtain a system whose characteristics do not change under irradiation, rather than to maintain the

required performance characteristics over the lifetime of the system. The former approach tends to utilize mediocre to poor technologies that remain so over the course of operation. The latter starts out with superior characteristics, which gradually deteriorate under irradiation. Depending on the specific system, these designs may die gradually, although at some fluence or dose a specific circuit, typically digital, may cease to function at all. Clearly, the best mitigation technique is to avoid the problem, either by shielding or by reducing the electronics in the radiation environment to the minimum required to do the job. The latter runs counter to prevailing trends, which favor digitizing as close to the front-end as possible and tend to implement even simple control functions with digital circuitry.

Detectors

Increased detector leakage current has several undesirable consequences.

1. The integrated current over typical signal processing times can greatly exceed the signal.

2. Shot noise increases.

3. The power dissipated in the detectors increases ($I_{det} \cdot V_{det}$)

Since the leakage current decreases exponentially with temperature, cooling is the simplest technique to reduce diode leakage current. For example, reducing the detector temperature from room temperature to 0 °C reduces the bias current to about 1/6 of its original value.

Detector power dissipation is a concern in large-area silicon detectors for the LHC, where the power dissipation in the detector diode itself can be of order 1 to 10 mW/cm^2. Since the leakage current is an exponential function of temperature, local heating will increase the leakage current, which will increase the local heating, and so on, ultimately taking the device into thermal runaway. To avoid this potentially catastrophic failure mode, the cooling system must be designed to provide sufficient cooling of the detector, a challenging (but apparently doable) task in a system that is to have zero mass.

Reducing the integration time reduces both baseline changes due to integrated detector current and shot noise. Clearly, this is limited by the duration of the signal to be measured. To some degree, circuitry can be designed to accommodate large baseline shifts due to detector current, but at the expense of power. AC coupled detectors eliminate this problem. In instrumentation systems that require DC coupling, correlated double sampling techniques can be used to sample the baseline before the signal occurs and then subtract from the signal measurement.

One of the most powerful measures against detector leakage current is segmentation. For a given damage level, the detector leakage current *per signal channel* can be reduced by segmentation. If a diode with a leakage current of 10 μA is subdivided into 100 subelectrodes each with its own signal processing channel, the DC current in each channel will be 100 nA and shot noise reduced by a factor of 10. This is why large area silicon tracking detectors can survive in the LHC environment. Fortuitously, increased segmentation is also required to deal with the high event rate. Pixel detectors with small electrode areas offer great advantages in this regard.

The most severe restriction on radiation resistance is imposed by type inversion, where the net acceptor concentration at some fluence becomes so large that the detector will no longer sustain the required voltage for full depletion. This is especially critical for position-sensing detectors with electrodes on both sides (double-sided detectors), for which full depletion is essential.

One can circumvent the type-inversion limit by using back-to-back single-sided detectors. The initial configuration uses *n* type segmented strip electrodes on *n* bulk, with a contiguous *p* electrode on the backside. Initially, the *pn*-junction is at the backside. This does require full depletion in initial operation, but this is no problem for the non-irradiated device and becomes easier to maintain as increasing fluence moves the bulk towards type inversion. After type inversion the bulk becomes *p* type and the junction shifts to the *n* electrodes, so that the bulk around the electrodes will be depleted and maintain inter-electrode isolation even in partial depletion.

Electronics

The design of the electronic systems is governed by changes in transistor parameters under irradiation, but circuit design and, at a higher level, architecture are equally important. Amplifiers are sensitive to changes in gain, bandwidth, and noise, so that effects on transconductance and noise parameters are important. Comparators used for threshold determination and timing rely critically on threshold shifts. Analog storage cells and switched capacitor systems tend to be sensitive to leakage currents. Digital circuitry is affected by threshold shifts that affect propagation delays and device transconductance, which determines switching speed.

Shorter shaping times improve tolerance to leakage currents. In high rate systems, fast response time is needed anyway, so experimental desires and engineering considerations interfere constructively. Since the system must be designed to tolerate a substantial shot noise current, utilization of bipolar junction transistors becomes very attractive, since the base shot noise becomes a minor

contribution (in contrast to systems that emphasize noise minimization, as in x-ray spectrometry or liquid argon calorimetry).

In general, for use in amplifiers bipolar transistor circuitry is superior to CMOS. In logic circuitry, especially at low overall switching rates, CMOS is advantageous both because of power consumption and circuit density. For example, the on-detector silicon tracker front-end under development for the ATLAS experiment at the LHC uses bipolar transistor technology for the amplifier-pulse shaper-comparator and radiation-hard CMOS for a clock-driven digital pipeline buffer and data readout.

In amplifiers, bipolar transistors offer higher bandwidth for a given power and superior device matching, which is a prime consideration in highly segmented systems with a correspondingly large number of channels. Threshold shifts in bipolar transistors are quite small with excellent matching between devices. JFETs yield excellent noise performance in applications where power consumption and circuit density are not prime considerations. Even when a CMOS front-end is chosen, because of the use of a switched capacitor analog memory, or the desire to combine the analog and digital circuitry on the same chip, amplifiers can be made quite radiation resistant, since the circuitry can be made to adjust for shifts in threshold voltage.

This principle is illustrated by the charge sensitive amplifier in Fig. 8. Transistors Q1 - Q4 comprise a cascode gain stage feeding a source follower Q6. Transistors Q7 - Q10 perform level shifting and biasing. C_F and Q11 form the feedback network. Q11 can be utilized either as a resistor or a switch. When biased as a resistor (R_F), the time constant $C_F R_F$ is chosen to be much larger than the rise time. Q11 also provides continuous DC feedback to bias the gate of the input transistor Q1. When Q11 is used as a switch, it is closed periodically to discharge the feedback capacitor C_F and also provides DC feedback.

The critical parameter that must be controlled to maintain the noise and speed of the amplifier is the transconductance of the input transistor. This in turn is determined by the drain current in Q1, and the biasing circuit must be designed to provide the appropriate gate voltage to maintain this bias current even as the required voltage changes with irradiation. This is accomplished by the current mirror Q4 - Q5, implemented as a matched pair. The desired drain current is applied as an external control bias current I_{CASC}, which is mirrored to the cascode. The DC feedback through Q11 adjusts the gate voltage of Q1 to maintain this current. Even if the MOSFET threshold voltages change substantially with radiation, this circuit will still maintain the correct current, to the extent that the parameters of the mirror transistors Q4 and Q5 track. This scheme does not maintain the DC output level, so baseline shifts must be corrected for by correlated double sampling

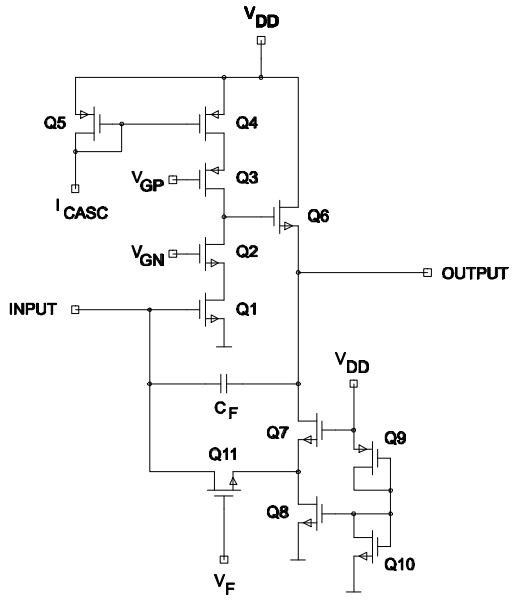

FIGURE 8. Detector preamplifier illustrating the use of current-mirror biasing to maintain the operating current of the input transistor independent of MOSFET threshold shifts during irradiation

or rendered irrelevant by AC coupling. The operating voltage and the gate voltages of the cascode transistors Q2 and Q3 must be chosen somewhat higher than for unirradiated operation to accommodate the threshold shifts, so overall power dissipation will be somewhat higher. Techniques of this type can provide radiation-resistant amplifiers with radiation-soft transistors.

In general, the use of fully differential circuitry and current mirrors yields circuitry whose operating point relies primarily on relative device matching. (40,26,28) Changes in threshold voltages or current gain in adjacent devices tend to track after radiation damage, so the circuit will maintain its operating point. Circuitry should also be designed to minimized single-point failure modes. Failure of common bias networks will cause all associated circuitry to fail. Local biasing with highly parallel architectures reduces these problems These design principles have been applied to 64 and 128 channel bipolar transistor integrated circuits for the readout of strip detectors. (40,26,29) Fig. 9 shows a block diagram.

This system only records the presence of a detector signal, so each channel comprises an amplifier, pulse shaper and threshold comparator. The input transistor is biased through a current mirror, as just described. The gain stages must provide sufficient gain so that the threshold voltage at the comparator is sufficiently high to provide good channel-to-channel and chip-to-chip uniformity. the. Since the first three stages are single-ended to reduce power consumption,

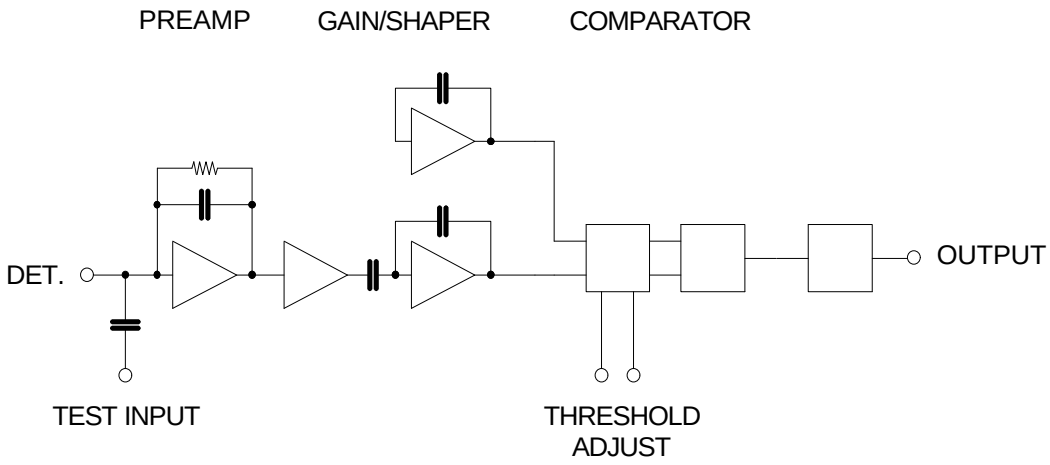

FIGURE 9. Block diagram of a readout channel for strip detectors.

substantial circuit complexity would be necessary to maintain DC stability, so AC coupling is introduced at the input of the third stage. From here on the circuitry is differential. The third stage is still single-ended, but it is replicated as a dummy amplifier to bias the second input of the differential amplifier. The dummy amplifier is included in each individual channel to obtain optimal parameter tracking under radiation damage, and also to maintain a parallel architecture and reduce single-point failure modes. The threshold level is applied differentially to exploit device tracking during irradiation.

The design of CMOS logic circuitry does not offer the flexibility of self-adjusting circuitry. Since the threshold shifts of *n* and *p* MOSFETs are not complementary, circuit switching thresholds change. At high damage levels the device transconductance also suffers due to buildup of interface charge and increased scattering of charge carriers in the channel. Both effects change propagation delays, which can lead to race conditions (mismatches in propagation delays of streams whose results are combined) that cause circuit failure. These problems can be mitigated somewhat by careful design, but they point out a qualitative criterion for radiation resistant system design: complexity. As a general rule, simple logic circuitry can be made more radiation resistant than complex circuitry that requires relative control of many mixed serial and parallel paths. Fully clocked systems avoid this problem, but at substantial penalties in power, speed, and area. Careful consideration should be given before incorporating complete wish-lists of circuitry (on-chip digitization, digital signal processing, microprocessor controlled readout, etc.) in a severe radiation environment (apart from common-sensical considerations such as reliability and maintenance of components that are not accessible without major disassembly). Simplest tends to be best.

IMPLEMENTATIONS

Several ICs for high-energy physics using the radiation-hard CMOS are installed in running experiments. Clock-driven pipelines designed for ZEUS and SDC have been fabricated and tested, and are operating successfully. The SVX IC designed for the CDF silicon vertex detector has been transferred to the rad-hard UTMC process. SVX-H ICs are installed in both CDF and L3 (41) and are providing excellent results. All of these are full-custom designs, which allow control over device and process selection. Otherwise, the use of a non-hardened bipolar transistor IC process (26,28) would be extremely risky. However, full custom technology may not be required in all applications.

In many instrumentation applications discrete designs are suitable. As shown above, bipolar transistors and JFETs can provide very high radiation resistance without resorting to qualified radiation-hard devices. The same typically holds for ECL logic ICs. If the ionizing dose does not exceed several 100 krad, standard sub-micron CMOS may be adequate, because the thinner gate oxides (~ 20 nm) required in short channel devices provide a significant improvement in threshold shift with respect to the 50 nm oxides of earlier 3 μm devices. One caveat is in order, however. The radiation characteristics of standard (non rad-hard) CMOS processes are inherently unpredictable from lot to lot. If devices from a given production run are tested and found satisfactory (including a substantial performance margin), devices from the same lot should be used in the final system. This practice should be followed with any "off the shelf" IC that is not radiation-qualified. Especially if the system is readily accessible for maintenance or replacement, this course may be quite acceptable.

A more reliable approach is to use radiation-qualified transistors and ICs available commercially as standard parts. Power MOSFETs are offered with full specifications to 1 Mrad and limited use to 3 Mrad. Displacement damage is specified to 10^{14} n/cm^2. Operational amplifiers are available with guaranteed specifications to 1 Mrad(Si). CMOS logic ICs (inverters, gates, flip-flops, shift registers) are also specified to 1 Mrad. As mentioned above, the circuit design must accommodate increased propagation delay and reduced clock rates. Devices with higher integration levels are also available, for example 32K x 8 SRAMs specified to 300 krad. 20 MSPS 8 bit flash ADCs implemented in 1.25 μm junction isolated rad-hard CMOS have been tested to 81 Mrad ^{60}Co with no loss in performance (42).

The last example is also a reminder of a phenomenon that has been illustrated above (37) and observed repeatedly. (43) The typical pattern is that parameters change most up to 1 Mrad and then plateau. Modern radiation-hard CMOS devices perform well at doses well beyond their rated maximum dose. The reason for this is the expense of fully qualifying a radiation-hard process in accordance

with the requirements of the military and aerospace agencies, so devices are guaranteed only to the required specification, rather than the capabilities of the fabrication process.

CONCLUSION

Judicious evaluation of the radiation fields coupled with a stringent analysis of application requirements can yield electronic systems capable of performing well to ionizing doses of 100 Mrad and particle fluences of 10^{14} and probably 10^{15} cm^{-2}. Developing radiation-resistant systems does require great attention to detail and substantially more testing effort than conventional designs, but the effort is necessary if we are to exploit the high-luminosity accelerators on the horizon. For many applications we are limited less by technology than by ingenuity.

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