Investigation of MOS-Gated Thyristors and Power Diodes

by

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(ABSTRACT)

The MOS-gated thyristors (MGT) refer to the class of power devices that combine the ease of a MOS gate control with the superior current carrying capability of a thyristor structure for high-power applications. The MOS-controlled thyristor (MCT) is a typical MGT device.

A comprehensive investigation of the reverse-biased safe operating area (RBSOA) characteristics of the MCT has been undertaken. The electrical failure mechanisms of the MCT are discussed, and the relationship between the dynamic avalanche limited RBSOA boundary of the MCT and the lower open-base transistor is identified. An analytical model based on the dynamic current gain concept is proposed to characterize the open-base transistor. For the first time, a RBSOA characteristic equation is developed for the MCT and a unified view of the RBSOA characteristics of the MCT is presented.

The fundamental characteristics of the MCT are compared to those of the insulated gate bipolar transistor (IGBT) at two levels: unit-cell and multi-cell. The investigation of the unit-cell level focuses on the tradeoff between the on-state voltage drop, the turn-off loss, and the RBSOA characteristic. The investigation of the multi-cell level reveals the fundamental difference between the MCT and the IGBT in handling the non-uniform turn-off caused by the internal propagation gate delay of a large-area device. Lack of current saturation capability is identified as the main reason for the severe degradation of the turn-off capability of a large-area multi-cell MCT.

The current saturation and controlled turn-on capabilities can be realized in the MGT devices with dual operation modes. For the first time, a dual operation mode MCT developed with superior current saturation capability is used to demonstrate how the dual operation device

can be beneficial in the switching circuit application. The maximum controllable current density (J_{mcc}) is the most important characteristic of the dual operation mode MGT devices. A first-order analytic model is developed to characterize the J_{mcc} of the dual operation mode MGT structures compatible with the IGBT fabrication process. A new device structure with improved J_{mcc} characteristics is proposed and verified by both simulation and experimental results.

The dissertation also carries out a comprehensive investigation of the development of power diodes. A new power diode, called the Trench Bipolar Junction Diode (TBJD), which has superior dynamic characteristics over the conventional P-i-N diode, is proposed. The TBJD controls the anode injection efficiency of the diode by the action of a reverse active transistor structure integrated into its anode junction. The reverse active transistor helps tailor an optimized on-state carrier profile to improve the diode switching characteristics. A novel self-aligned process is developed to fabricate the TBJD. Experimental characterization of the fabricated TBJD devices shows that the TBJD achieves superior dynamic characteristics without sacrificing the on-state voltage drop and the leakage current characteristics.

To my parents and wife

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Chapter 1 Introduction

1.1 Power Semiconductor Devices

Power semiconductor devices play a crucial role in the regulation and distribution of power and energy in the world. By some estimations, more than sixty percent of all the power utilized in the United States flows through at least one power device, and more often through multiple devices [1]. The performances of power switches and rectifiers have a significant impact on the efficient use of electricity. In the power electronics community, it is well recognized that improvement in system performance in terms of efficiency, size, and weight are driven by enhancements made in semiconductor device characteristics.

Power switches are essential components of all power electronics systems for the regulation of loads. The first power semiconductor switches were thyristors and bipolar transistors developed in the 1950's. Thyristors were used in higher power systems, because their ratings were scaled at a faster pace than bipolar transistors. Gate Turn-off Thyristors (GTO) are now available with ratings of 6000 V and 4000 A. These devices are manufactured from single four-to-five-inch diameter wafers using a mature deep diffusion process technology.

Ever since their introduction in the 1950's, bipolar transistors were favored for low and medium power applications because of their faster switching capability. The ratings for the devices grew steadily until the late 1970's. Since the bipolar transistor is fundamentally a current-controlled device with the magnitude of the collector current determined by the base-driving current, one of the most critical design goals has been to improve the current gain in order to reduce the complexity, size, and weight of the base-driving circuit. Unfortunately, a

severe tradeoff exists between the collector-emitter breakdown voltage and the current gain in the conventional bipolar transistor structure due to their conflicting requirements on the transistor base width. Although continuous improvement of the bipolar transistor structure has greatly alleviated this tradeoff, the fall-off in current gain at typical operating current densities due to high-level injection effects leads to a gain of less than ten [2, 3]. The current gain can be improved by using the Darlington configuration at the disadvantage of a considerable increase in the on-state voltage drop [4]. For these reasons, the bipolar transistor has been displaced by the power MOSFET for low power applications in the 1980's, and for medium power applications by Insulated Gate Bipolar Transistors (IGBT) in the 1990's.

The silicon power MOSFET has become the dominant device technology for low power applications. First, the power MOSFET has very high input impedance in the steady state due to its metal-oxide-semiconductor (MOS) gate structure, and is classified as a voltage-controlled device. Second, in comparison with bipolar transistors, the MOSFET has a very fast inherent switching speed due to the absence of minority carrier injection. The switching time for the MOSFET is dictated by the ability to charge and discharge the input capacitance. Third, the MOSFET has superior ruggedness and a forward-biased safe operating area (FBSOA) when compared with bipolar transistors, which allows the elimination of snubber circuits for protection of the switch during operation.

Unfortunately, the specific on-resistance of the drift region of the conventional power MOSFET increases very rapidly with the increasing breakdown voltage, because of the need to reduce its doping concentration and increase its thickness. Thus, the conventional power MOSFET is not satisfactory for applications that require a breakdown voltage above 300 V due to their high on-state power dissipations.

Recently, a new technology called CoolMOS for higher voltage power MOSFETs has been introduced [5,6]. Based on the new device concept of charge compensation, the specific on-resistance of the 600-V MOSFET has been reduced by a factor of five. However, even with the new technology, the specific on-resistance of the MOSFET is not expected to be satisfactory for applications that require a breakdown voltage above 1200 V.

The high on-resistance problem of a MOSFET at high voltages was resolved in the 1980's by the introduction of the Insulated Gate Bipolar Transistor (IGBT), in which bipolar current conduction is controlled by using a MOS gate structure [7-9]. The cross-section of the planar MOS technology based IGBT and its equivalent circuit are shown in Fig. 1.1. Due to the injection of a high concentration of holes from the P+ substrate into the N- drift region, the IGBT has a much lower forward drop as compared to a power MOSFET structure. Since the input signal for the IGBT shares the high input impedance advantage of the power MOSFET, the IGBT is also classified as a voltage-controlled device. However, unlike the MOSFET, the switching speed of the IGBT is limited by the time taken for removal of the stored charge in the drift region due to injection of holes during the on-state current conduction. The turn-off time for the IGBT is dictated by the minority carrier lifetime, and it is found that the on-state voltage drop of the IGBT increases after lifetime reduction, as observed for all bipolar power devices.

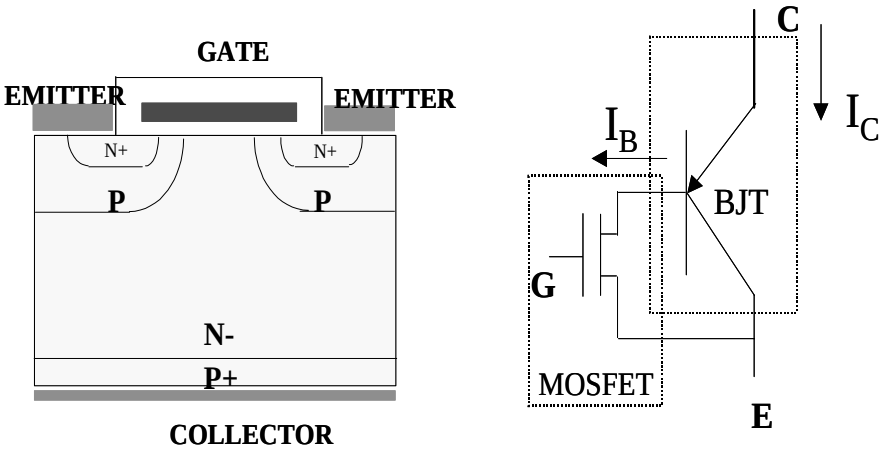

Fig. 1.1 Cross-section view of the IGBT and its equivalent circuit.

In spite of the on-going refinement of the IGBT structure to improve the trade-off between the on-state voltage drop and the turn-off characteristics, its on-state power dissipation still becomes large when designed for operation at high voltages. For this reason, considerable

research has been performed on MOS-Gated Thyristors (MGT), which refers to the class of devices combining a MOS gate control with the current-carrying capability of a thyristor structure, as alternative devices for high power applications.

The first reported MGT structure with current turn-off capability was the MOS-Controlled Thyristor (MCT) [10-12]. In this device, whose cross-section and equivalent circuit is shown in Fig. 1.2, the regenerative action of the thyristor structure is interrupted by short-circuiting the N+ emitter to the P base region by using a P-MOSFET integrated within the P-base region. Although there have been considerable research efforts put into this area and many new MGT structures have been proposed during the past decade, so far the only commercially available MGT device is still the MCT [13-15].

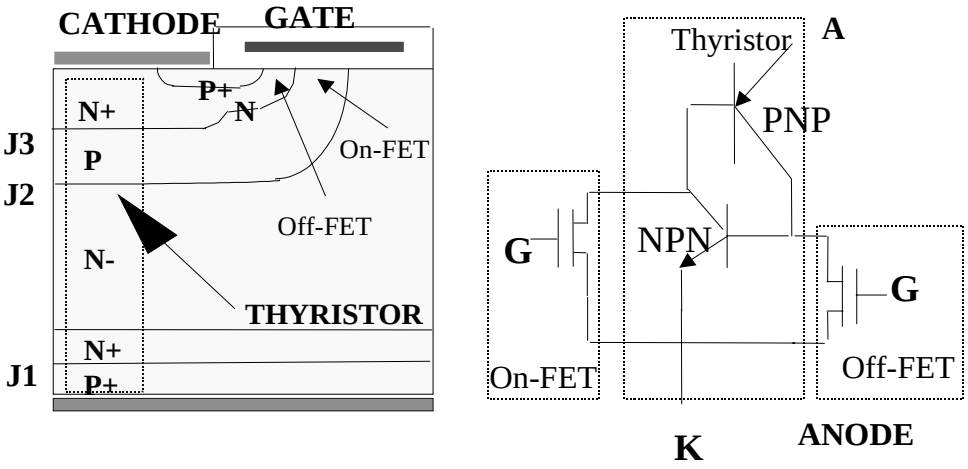

Fig. 1.2 Cross-section view of the MCT and its equivalent circuit.

The ability to control current flowing in a MGT device has been found to be a more challenging problem. The internal regenerative action of the thyristor structure can easily lead to the formation of current filaments that can destroy the device during turn-off. The internal regenerative action of the thyristor structure also accounts for the uncontrollable turn-on

behaviors of the MGT, whose turn-on speed is usually too fast and results in a snappy reverse recovery in the associated diodes.

Since the introduction of modern power switches, such as the IGBT and MGT, diodes in many applications are subjected to higher voltage and current levels, and are required to switch at higher speeds and frequencies. Under these conditions, power diodes with low forward voltage drop, low leakage current, low peak reverse recovery current and low reverse recovery charge are needed in order to decrease the overall power loss in the power electronics circuits.

In high-voltage applications, the P-i-N diodes still dominate due to their low forward voltage drop and reverse leakage current. However, the conventional P-i-N diode suffers from poor dynamic characteristics due to the large amount of charge stored in the lightly doped i-region during forward conduction. On the other hand, the Schottky diode has been limited to low-voltage applications because of its high leakage current and soft breakdown. A high-voltage power diode with improved static and dynamic characteristics to match the performance of the modern power switches is essential in high-voltage power electronics applications.

1.2 Scope of the Work

The research work reported in the dissertation focuses on the following aspects.

1) Investigation of the fundamental device characteristics that distinguish the MCT and the IGBT.
2) Demonstration of new MGT devices with improved performances.
3) Development of a new power diode with superior dynamic characteristics.

The first aspect of this work is carried out by conducting an extensive comparative study between the MCT and the IGBT through numerical simulation. This comparison is especially

important because the IGBT is currently the dominant power switch in medium power applications, and the frontier of its application development is being pushed into the high power range.

The second aspect of this work is focused on the dual operation mode MGT. The dual operation mode MGT device possesses current saturation capability, a feature not available in the conventional MCT. The current saturation capability is one of the most desirable features for a power switch. It provides short-circuit protection for the switch, and is used to achieve controlled turn-on capability. Both simulation and experimental results are provided in the investigation of the dual operation mode MGT.

The third portion of this research work covers the development of a new power diode with superior characteristics compared to the conventional P-i-N diode. The diode research work includes: review of the historical development of the power diodes; analysis of a new diode concept; design and fabrication of the new diode; and experimental characterization of the new diode.

The contributions of the research work are listed below.

1) Identified the static current-voltage locus of the lower open-base transistor as the dynamic avalanche limited reverse-biased safe operating area (RBSOA) boundary of the MCT. An analytical model was proposed to characterize the dynamic avalanche characteristics of the open-base transistor. For the first time, a RBSOA characteristic equation that applies to all MGT devices has been developed.
2) Presented a unified view and design guidelines for the RBSOA characteristics and the trade-off between the on-state voltage drop and the turn-off loss of the MCT.
3) Identified the intrinsic problem of a large-area multi-cell MCT. It was found that the multi-cell MCT is vulnerable to the non-uniform turn-off caused by the internal gate delay because the MCT structure lacks the current saturation capability.
4) Experimentally demonstrated the application of a dual operation mode MCT with superior current saturation capability in a hard-switching circuit.

5) Presented a new dual operation mode MGT structure compatible with the fabrication process of an IGBT. The analytic models developed to describe its maximum controllable current density are verified by simulation and experiment.
6) Proposed a new power diode, called the Trench Bipolar Junction Diode (TBJD), and fabricated the TBJD with a novel self-aligned trench process. It has been shown, by both simulation analysis and experiment characterization, that the TBJD has superior static and dynamic characteristics than the conventional P-i-N diode.

1.3 Organization of the Dissertation

The dissertation is divided into nine chapters, including the introduction and conclusion chapters. Chapters 2 through 5 include the investigation of the MOS Gated Thyristors, and Chapters 6 through Chapter 8 cover the diode work. Within each chapter, except Chapters 1, 7 and 9, there is an introduction section, which provides the background information, and a conclusion section, in which the work and results are summarized. References are listed after each chapter.

Chapter 2 performs a comprehensive investigation of the RBSOA characteristics of the MCT. This chapter discusses the electrical failure mechanisms of the MCT and identifies the relationship between the dynamic avalanche limited RBSOA boundary of the MCT and the lower open-base transistor. An analytical model based on a dynamic current gain concept is proposed to characterize the open-base transistor. A RBSOA characteristic equation is developed and a unified view on the RBSOA characteristics of the MCT is presented.

In Chapter 3, an apple-to-apple MCT vs. IGBT comparison study is undertaken at two levels: unit-cell and multi-cell. The comparison at the unit-cell level focuses on the trade-off among the on-state voltage drop, turn-off loss, and the RBSOA characteristics. The multi-cell level comparison reveals the fundamental difference between the MCT and the IGBT in handing

the non-uniform turn-off due to the internal propagation gate delay of a large-area unit-cell device.

Chapter 4 investigates the switching performance of a dual operation mode MCT with superior current saturation capability in a hard-switching circuit, and demonstrates how a dual operation mode MCT can be beneficial in specific applications.

In Chapter 5, the dual operation mode MOS Gated Thyristor (DMGT) devices that are compatible with the IGBT process are analyzed. A first-order analytic model is developed to characterize the maximum controllable current density (J_{mcc}) in the IGBT mode operation. A new device structure is proposed and compared with two previously reported DMGT structures. Both simulation and experiment results are provided to back up the analytic model.

Chapter 6 first conducts an extensive literature review of the power diode development. The TBJD concept and operation principles are analyzed in detail with the aid of numerical simulation. The process development and fabrication of 600 V, 10 A TBJDs are described in Chapter 7, while the fabricated and packaged TBJDs are characterized in Chapter 8.

Chapter 9 summaries the findings and conclusions of the research work, and proposes possible future work.

Appendix gives the details of the TBJD fabrication process.

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Chapter 2 The Reverse-Biased Safe Operating Area of the MCT

2.1 Introduction

The reverse-biased safe operating area (RBSOA) of a MCT refers to the current-voltage boundary within which the device can be operated without destructive failures during the turn-off transient period [1]. The cause of the destructive failure of power devices can be classified into two categories: thermal and electrical. Although thermal runaway has been a major cause of destructive failure of power devices, it is the electrical failure mechanism that determines the theoretical limitation of the power devices. An isothermal RBSOA study offers insights into the electrical failure mechanism of power devices.

The RBSOA characteristic is arguably the most important characteristics of any power semiconductor device. There are two main types of electrical failure mechanisms of the MCT: current induced latch-up and dynamic avalanche [2]. It has been generally understood that the turn-off capability of the MCT is limited by the onset of latch-up of the thyristor at low voltages, and limited by the onset of dynamic avalanche at high voltages. A reported experimental evaluation of the RBSOA of the MCT observed that, compared to the BJT, the MCT exhibits very different turn-off breakdown characteristics [3]. However, no in-depth theoretical investigation of the electrical failure mechanism of the MCT has been reported in the literature before the paper published through this research work [4].

This chapter performs a comprehensive investigation of the electrical turn-off failure mechanism of the MCT with the aid of two-dimensional numerical simulation. For the first time, the relationship between the RBSOA characteristics of the MCT and the static forward blocking

characteristics of its lower open-base transistor has been identified. The dynamic avalanche limitation of the MCT was analyzed both qualitatively and quantitatively, based on a first-order model proposed to characterize the lower open-base transistor. It was discovered that the dynamic current gain characteristics of the lower open base transistor account for the performance discrepancy between the P and N type MCTs. The impact of the upper-base charge on the RBSOA characteristics of the MCT has also been investigated. A unified view of the theoretical limitations on the RBSOA of the MCT is presented.

2.2 Structure and Operation

Fig. 2.1 shows a cross-section of the unit-cell of a N-type MCT. The cross-section shown is for a non-punch-through MCT. For a punch-through MCT, there is a N buffer layer between the anode P+ emitter and the N- drift regions. The P-type MCT is a complementary device of the N-MCT, and has a reverse polarity in each of the doping regions. The concept and operating principle of the MCT have been well-documented [5-7].

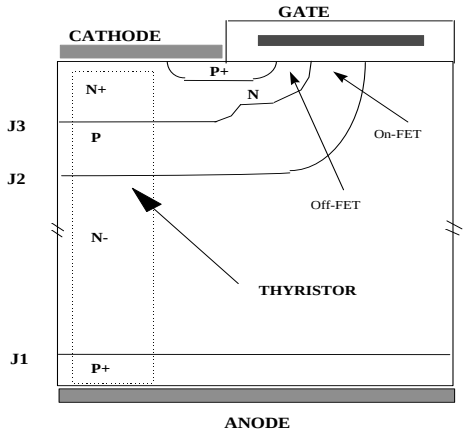

Fig. 2.1 Cross-section of the unit-cell of a N-type MCT.

When a positive voltage is applied to the gate electrode, the turn-on N-MOSFET is conducting, and electrons are supplied to the base region of the PNP transistor from the N+ emitter via the turn-on channel. This results in the injection of holes from the anode into the N- drift region. These holes diffuse across the N- drift region and are collected at the reverse-biased junction J_2, and are then swept into the P base region. If the injection of the holes is strong enough, the holes collected by the base will forward bias the P base/N+ emitter junction J_3 to start the injection of electrons directly from the N+ emitter into the P base region. This triggers the regenerative feedback mechanism between the two coupled transistors within the thyristor structure. The MCT therefore is turned on.

The on-state current conduction in the MCT is accompanied by the injection of a high concentration of both electrons and holes into the lower base or drift region. When the turn-off P-MOSFET is turned on to short the P base/N+ emitter junction of the upper NPN transistor in the thyristor path, all or part of the holes entering the P base region are diverted to the turn-off channel, and, as a consequence, the holding current level of the thyristor increases. The success in turning off the MCT relies on the fact that the latching condition can be broken. Therefore, the amount of current that a MCT can turn off is mainly decided by the conductivity of the inversion channel and the resistance of the upper P base region. As long as the thyristor's latched condition is broken (N+ emitter stops injection), the turn-off then proceeds like an open-base transistor with a rapid current fall followed by a current tail while excess carriers inside the N- drift recombine.

The simulated N-MCT devices are chosen to have a turn-off channel length of 0.5 μm and a turn-on channel length of 4 μm. The N- drift region has a doping concentration of 5×10^{13} cm^{-3} and a thickness of 400 μm. The N+ emitter and the P base region have a surface concentration of 1×10^{19} cm^{-3} and 2×10^{17} cm^{-3}, and a junction depth of 2.5 μm and 7 μm, respectively. The simulated P-MCT has the same doping profile as the N-MCT except with a reversed doping polarity. The lifetime of the electron is assumed to be seven times that of the

hole in the simulation, unless otherwise indicated. This ratio is based on experimental results obtained on irradiated MCTs and diodes [8].

2.3 Maximum Controllable Current Density

As discussed before, the turn-off of the MCT relies on breaking the regenerative action of the thyristor structure through the action of the turn-off MOSFET. For switching applications, it is essential that the MCT operate within the range of the current densities that can be interrupted by the gate. The highest current density that can be interrupted by the gate is defined as the Maximum Controllable Current Density (J_{mcc}) of the MCT.

When the turn-off MOSFET is turned on to short the P base/N emitter junction of the upper NPN transistor of a N-MCT, the holes entering the P base region are diverted to the turn-off channel. Consider the cross-section of the N-MCT shown in Fig. 2.1. The voltage drop at the center of the P base (V_B), due to the flowing of the hole current along the turn-off path, is given by $V_r = I_h(R_P + R_{SP} + R_{CH})$, where, R_P, R_{SP}, and R_{CH} are the P base lateral resistance below the N+ emitter, the spreading resistance between the channel and P base region, and the channel resistance of the turn-off MOSFET, respectively. Assuming the channel resistance is dominant, then

$$V_B = \alpha_{PNP} JAR_{CH} \tag{2.1}$$

where α_{PNP} is the current gain of the lower PNP transistor, J is the current density and A is the total area of the unit cell. Assuming the turn-off P-MOSFET is operated in the linear region, the channel resistance is given by

$$R_{CH} = \frac{L_{CH}}{W_{CH}\mu_{IS}C_{OX}(V_G - V_T)} \tag{2.2}$$

In Eq. 2.2, L_{CH} is the channel length, W_{CH} is the channel width of the half-unit cell, U_{IS} is the hole mobility in the inversion layer, C_{OX} is the specific capacitance of the gate oxide, V_G is the applied gate bias, and V_T is the threshold voltage. Substituting Eq. 2.2 into Eq. 2.1, and considering the fact that the turn-off MOSFET will fail to interrupt the emitter junction injection when the voltage drop at P base exceeds the build-in potential (V_{bi}) of the emitter junction, the maximum controllable current density can then be derived as

$$J_{mcc} = \frac{\mu_{IS}C_{OX}(V_G - V_T)V_{bi}}{\alpha_{PNP}L_{CH}}\frac{W_{CH}}{A} \tag{2.3}$$

The MCT is not able to turn off current densities higher than its maximum controllable current density value. Therefore, the J_{mcc} given by Eq. 2.3 imposes a current limitation line in the RBSOA of the MCT. One primary design goal for a MCT device is a high J_{mcc} capability. The J_{mcc} is determined by various geometrical and technology parameters as shown in Eq. 2.3. According to Eq. 2.3, the J_{mcc} of the MCT can be increased by either reducing the channel length (L_{CH}) or increasing the off-channel density (W_{CH}/A), which is defined as the channel width (W_{CH}) within a unit area (A).

2.4 Dynamic Avalanche Limitation

2.4.1 Correlation between the Dynamic and Static Characteristics

If the on-state current density of the MCT is lower than its J_{mcc}, injection from the upper emitter will cease after the turn-off MOSFET is turned on. The cessation of the injection at the

N+ emitter cuts off the base-driving electron current of the lower transistor. Since the device is typically turning off an inductive load, the current flowing through the lower transistor of the MCT remains constant. The constant current is sustained by extracting stored carriers out of the drift region. As a result, the depletion region is developed, and the anode voltage of the MCT starts to rise with respect to the cathode. During a clamped inductive turn-off, a successful turn-off is accomplished when the inductive current is totally bypassed by the free-wheeling diode after the voltage rises to the clamped value.

Fig. 2.2 shows the simulated voltage and current waveforms of the P-MCT in gating off two inductive loads at a clamped voltage of 400 V. In the case of turning off a 600 A/cm^2, the anode voltage climbs to 400 V, then the current begins to decrease, and a successful turn-off is accomplished.

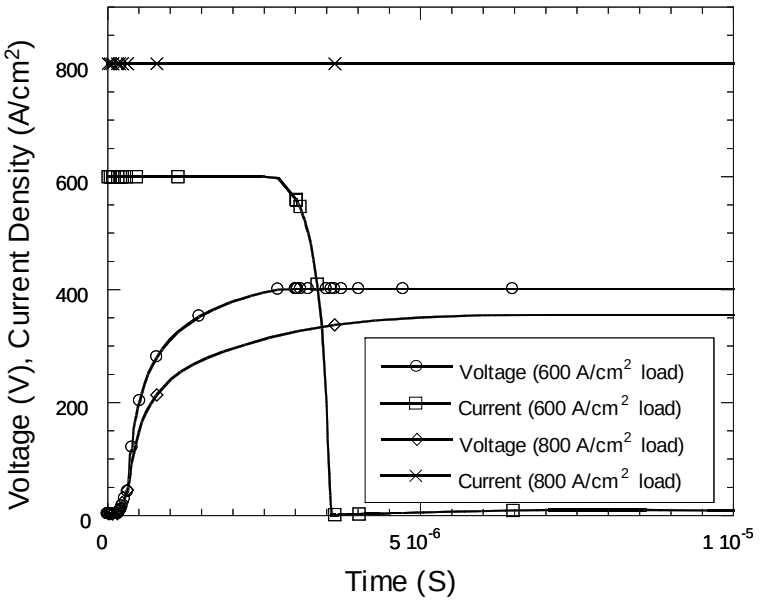

Fig. 2.2 Simulated voltage and current waveforms of the P-MCT in gating off two different inductive loads at a clamped voltage of 400 V.

However, during the process of building up the voltage, a large number of carriers exist inside the depletion region due to the inductive load. The electric field generated by the voltage may therefore be sufficiently high to initiate avalanche. With the onset of avalanche at a high electric field, the constant load current across the depletion region can then be supported by the drift of carriers generated by the avalanche multiplication. If the free carriers generated in the space charge region are sufficient to carry the inductive load current, the load current will stop extracting stored carriers. As a consequence, the depletion region will no longer expand, and the voltage will stop rising. If the terminal voltage of the MCT enters a saturation state before it rises to the clamped voltage value, as in the case of gating off an 800 A/cm^2 load in Fig. 2.2, the turn-off is considered unsuccessful due to the dynamic avalanche.

Fig. 2.3 shows the experimental voltage and current waveforms of a P-MCT tested in an snubberless inductive turn-off circuit. The voltage of the device is saturated at 1000 V due to the avalanche while carrying a 22 A constant current. The turn-off will fail if the clamped voltage is higher than 1000 V.

The avalanche happens during the turn-off transient, and therefore is a dynamic phenomenon. However, from the electrical failure mechanism point of view, only the avalanche which results in a saturation of terminal voltage will cause a turn-off failure; otherwise the inductive load will continue to force the anode voltage of the MCT to the clamped voltage. When a turn-off failure due to dynamic avalanche happens, both the anode voltage and the anode current will no longer change with time. Therefore, this can be considered as a quasi-static characteristic. If the load current and the saturation voltage are taken as a pair of operating points, these points must also be on the locus defined by the terminal voltage and current of the MCT in its forward blocking state. In other words, the dynamic avalanche limitation boundary, and hence the RBSOA of the MCT, are indeed imposed by the locus of the MCT in its forward blocking state. The correlation between the dynamic RBSOA and the static forward blocking characteristics has also been reported in an independent parallel work on the IGBT [9].

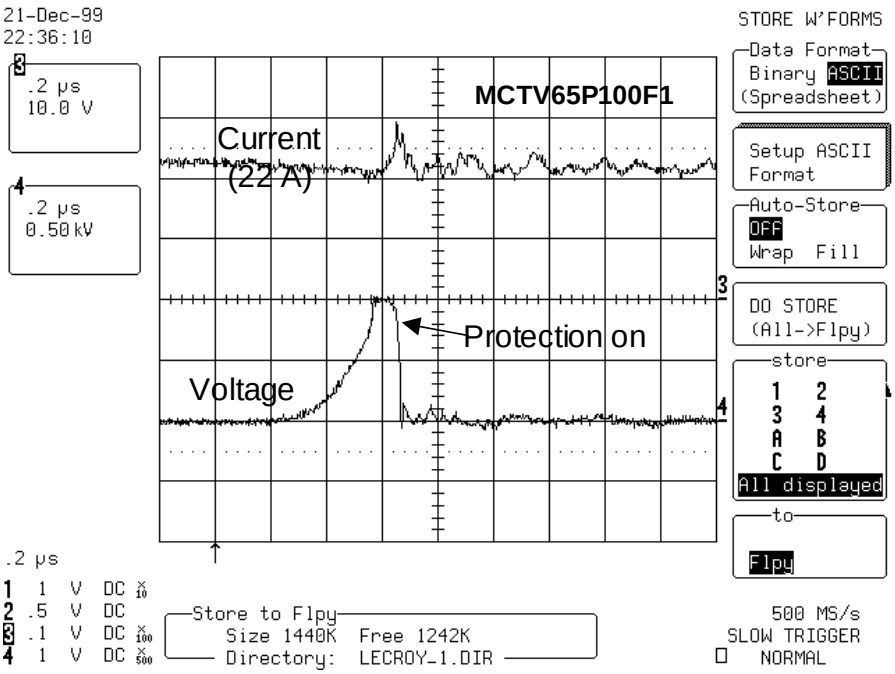

Fig. 2.3 Experimental current and voltage waveforms of a P-MCT during a snubberless inductive turn-off.

To verify the above statement, several sets of simulations were carried out on the P-MCT shown in Fig. 2.2. The maximum initial current density that can be successfully turned off under each specified clamped voltage was marked as a RBSOA point, and the resulting RBSOA of the P-MCT is shown in Fig. 2.4. In another set of simulations, the forward blocking current-voltage curve of the P-MCT after the static breakdown was obtained and is also shown in Fig. 2.4. It is shown that these two curves fit well at high voltages, a region which is generally described as the dynamic avalanche-limiting region. Since an MCT acts as an open-base transistor in series with a turn-off MOSFET when the current is lower than its J_{mcc} value during its forward blocking state, the forward blocking current-voltage curve of the MCT is essentially the current-voltage locus of its lower open-base transistor. It is the lower open-base transistor that determines the dynamic avalanche characteristics of the MCT. In the next section, a first order analytic model is proposed to characterize the lower open-base transistor of the MCT.

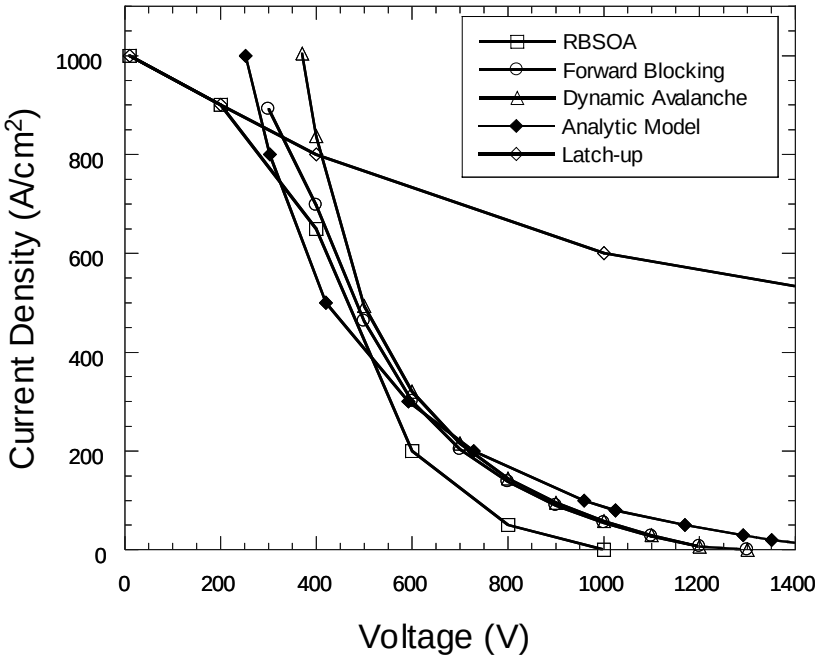

Fig. 2.4 Limiting factors of the RBSOA of the P-MCT.

2.4.2 Analytical Model of the Lower Transistor

The lower open-base transistor of a MCT has a different structure from traditional bipolar power transistors. Traditional bipolar power transistors have a narrow base necessary for a high current gain and a wide collector region used to support the high voltage, while the lower open-base transistor of the MCT relies on a wide base region to withstand the voltage. The static breakdown voltage of an open-base transistor is termed BV_{CEO}, and is given by [1]

$$BV_{CEO} = BV_{pp}(1-\alpha_o)^{\frac{1}{n}} \tag{2.4}$$

where α_o is the common base current gain of the open-base transistor, BV_{PP} is the parallel plane junction breakdown voltage, and n is a constant, which has different values for NPN and PNP transistors. It needs to be noted that α_o is the common base current gain of the open-base transistor at a very low leakage current level.

During the high-current and high-voltage operation of the open-base transistor, the current in the depletion region is supported by the drift of both electrons and holes under the influence of strong impact ionization created by the high electric field. Due to the high electric field prevalent in the depletion region, the electrons and holes can be assumed to be transported through the depletion region at their saturated velocities. Consequently, the electron and hole concentration in the drift region are related to the corresponding current densities J_n and J_p by

$$n = \frac{J_n}{qv_{sat,n}} \tag{2.5}$$

and

$$p = \frac{J_p}{qv_{sat,p}} \tag{2.6}$$

where $v_{sat,\,n}$ and $v_{sat,\,p}$ are the saturated velocities for electrons and holes, respectively. Assuming the doping concentration in the base region is N_B, the net charge in the drift region of the PNP transistor is then given by

$$N = N_B - \frac{J_n}{qv_{sat,n}} + \frac{J_p}{qv_{sat,p}} \tag{2.7}$$

The saturated velocity of electrons is believed to be higher than that of holes in the high field region [1]. Assume $v_{sat,h} = v_{sat}$ and $v_{sat,n} = \rho v_{sat}$, then ρ is a ratio factor greater than unity.

The carrier current density can be expressed as $J_p = \alpha J$ and $J_n = (1-\alpha)J$, where J is the total current density and α is the dynamic current gain, which is defined as the ratio of minority current to the total current in the drift region of the open-base PNP transistor. Eq. 2.7 can then be rewritten as

$$N = N_B + Q \tag{2.8}$$

where Q is the net free carrier charge defined by

$$Q = \frac{J}{q v_{sat} g_1}(\alpha - g_2) \tag{2.9}$$

and

$$g_1 = \frac{\rho}{1+\rho}\ ,\ g_2 = \frac{1}{1+\rho} \tag{2.10}$$

The electric field distribution in the drift region is determined by the net charge N. Poisson's equation in the drift region is

$$\frac{dE(x)}{dx} = -\frac{q}{\varepsilon} N = -\frac{q}{\varepsilon}(N_B + Q) \tag{2.11}$$

The presence of the free carrier charge Q alters the electric field distribution in the drift region as shown in Fig. 2.5. It can be seen that the electric field in the drift region varies linearly with distance, as in the case of a reversed biased junction, but its rate of variation is dependent upon the free carrier charge Q, which is a function of current density J and dynamic current gain α. Assume the electric field distribution when the static breakdown starts to initiate is indicated

by the curve ‘a’ in Fig. 2.5. As the current increases, the free carrier charge Q will step in, and change the slope of the electric field profile. If the value of Q is positive, the slope of the electric field profile is shown by curve ‘c’. If the value of Q is negative, the slope will be changed to curve ‘b’.

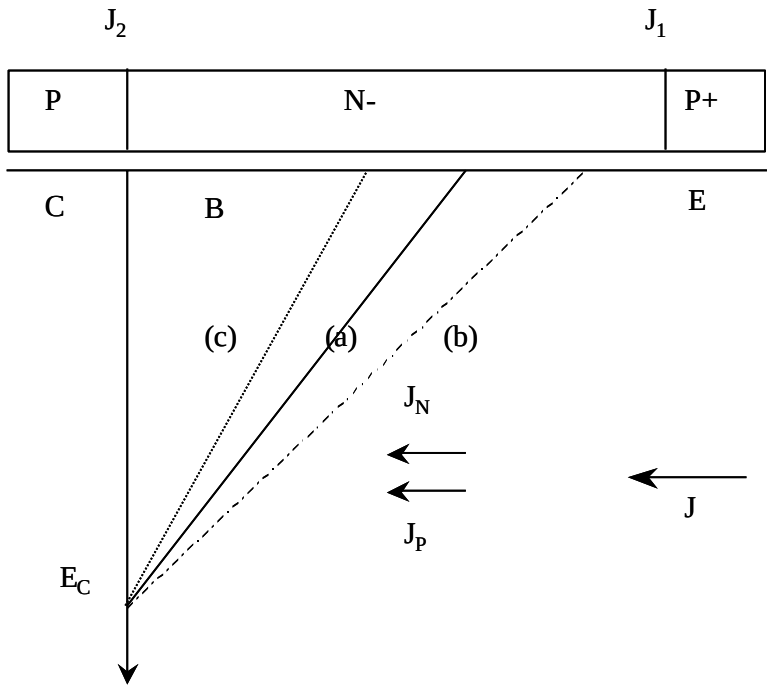

Fig. 2.5 Electric field distribution in the drift region of the open-base PNP transistor of a N-MCT.

After the onset of avalanche in the drift region of the open-base transistor, the peak electric field can be assumed to be a fixed value E_c. Assuming a triangle-shaped electric field, the voltage supported by the drift region, therefore, is reversed proportional to the net charge N by

$$V = \frac{E_c^2 \varepsilon}{2qN} \tag{2.12}$$

Substituting Eq. 2.8 into Eq. 2.12 will give rise to

$$V = \frac{E_c^2 \varepsilon}{2qN_B[1+\frac{J}{qN_B v_{sat} g_1}(\alpha - g_2)]} \tag{2.13}$$

Since the blocking voltage when the current is very small is the static breakdown voltage of the open-base transistor, i. e., BV_{CEO}, Eq. 2.13 can then be expressed as

$$V = \frac{BV_{CEO}}{[1+\frac{J}{qN_B v_{sat} g_1}(\alpha - g_2)]} \tag{2.14}$$

Eq. 2.14 is the characteristic equation for the lower open-base PNP transistor of the N-MCT at high-voltage and high-current states. The lower open-base NPN transistor of the P-MCT has the same characteristic equation as Eq. 2.14, except with

$$g_1 = g_2 = \frac{\rho}{1+\rho} \tag{2.15}$$

The dynamic current gain appearing in Eq. 2.14 is not a constant value, and itself is also a function of the current density J. Since the root locus of Eq. 2.14 sets the dynamic avalanche limitation boundary of the MCT, it is this dynamic current gain α of the lower open-base transistor that determines the dynamic avalanche limited RBSOA of the MCT. The characteristic equation also indicates that the current-voltage curve will exhibit a snapback if the dynamic current gain value is higher than the value of g_2. The higher the dynamic gain, the more severe the snapback. The value of g_2 can be considered a critical gain, which determines whether the device can achieve a full static blocking capability or not. If the saturated velocity of electrons is

assumed to be the same as that of holes, i. e., ρ=1, the critical gain for both P-MCT and N-MCT will be 0.5. In the simulation using Silvaco's Atlas [10], the saturated velocity of electrons is about 1.0×10^7 cm/sec, and that of holes is about 0.8×10^7 cm/sec. Therefore, the critical gain for P-MCTs is about 0.56, while the critical gain for N-MCTs is 0.44.

2.4.3 Dynamic Current Gain Characteristics

The common base current gain α_o is a function of the lower transistor doping profile, base/collector voltage, transistor type, temperature, and current level [11]. Among these, the current dependence can be significant. However, the dynamic current gain characteristics of an open-base transistor at high-current and high-voltage states have not yet been reported in any literature. In this study, the dynamic current gain value of lower transistors was extracted from the simulation data. The ratio of the minority carrier current to the total current in the drift region was measured and considered as the dynamic current gain α.

Fig. 2.6 shows the calculated dynamic current gain value of the lower NPN transistor of the P-MCT as a function of the current density. The origin point represents α_o, the current gain used to determine the static breakdown voltage BV_{CEO}. The α_o is about 0.67. It is shown that the peak dynamic current gain is about 0.86, which happens when the current is around 10 A/cm^2. The dynamic current gain of the P-MCT will stay as high as 0.8 in the range of several hundred amperes per square centimeter, the typical operating current level of the MCT. Substitute the gain values shown in Fig. 2.6 into Eq. 2.14, and the calculated voltage versus the current locus defined by the first-order model is then superimposed in Fig. 2.4. It basically fits other curves obtained from the simulation.

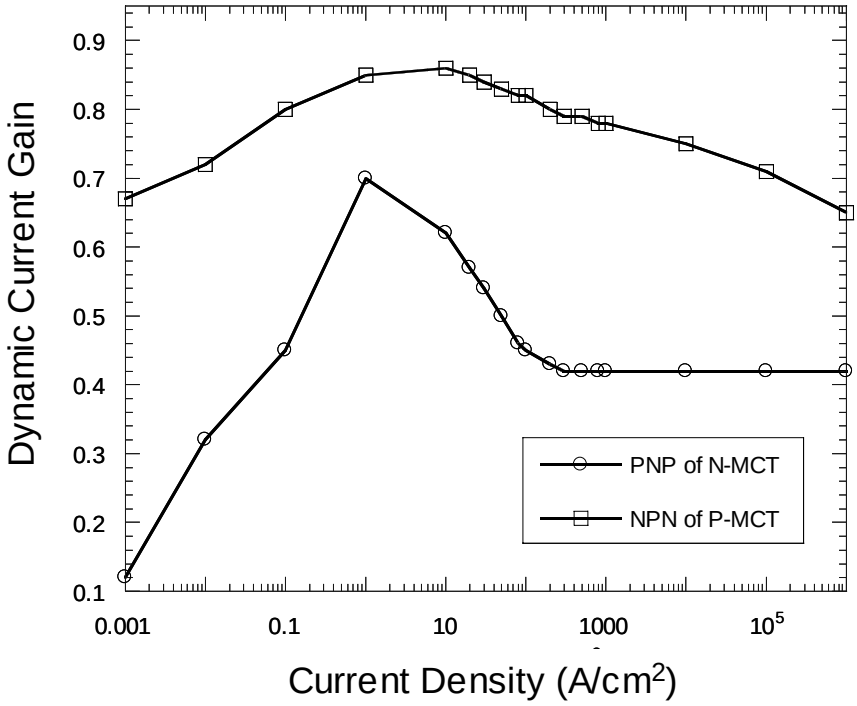

Fig. 2.6 Calculated dynamic current gain value of the lower transistors of MCTs as a function of current density.

According to Eq. 2.14, a relatively square RBSOA is possible if the high-current dynamic current gain of the MCT can be suppressed. Fig. 2.6 also shows the calculated dynamic current gain of the open-base transistor of the N-MCT. The α_o is about 0.12. The dynamic current gain initially jumps up to about 0.70 when the current is about 1 A/cm^2, and gradually stabilizes to a level of 0.42 at about 100 A/cm^2. In terms of the blocking voltages, it will drop below BV_{CEO} first, then stop declining at a certain current level, and will finally move back to BV_{CEO} and beyond at high current densities, since the gain value 0.42 is slightly less than the critical gain 0.44. From the viewpoint of RBSOA, this is a favorable characteristic, since the dynamic avalanche limitation only governs a narrow range of voltages, thus making a relatively square

RBSOA possible. Based on the dynamic gain characteristics of the lower transistors, this is more likely to happen in the N-MCT with a lower PNP transistor.

The dynamic current gain characteristics of the lower PNP transistor account for the relatively square RBSOA achieved for the N-MCT. As shown in Fig. 2.7, the lowest forward blocking voltage is about 2000 V for the lower PNP transistor of the N-MCT. Below 2000 V, the RBSOA boundary is limited by the current latch-up, which is less sensitive to the voltage; thus, the N-MCT has a relatively square RBSOA.

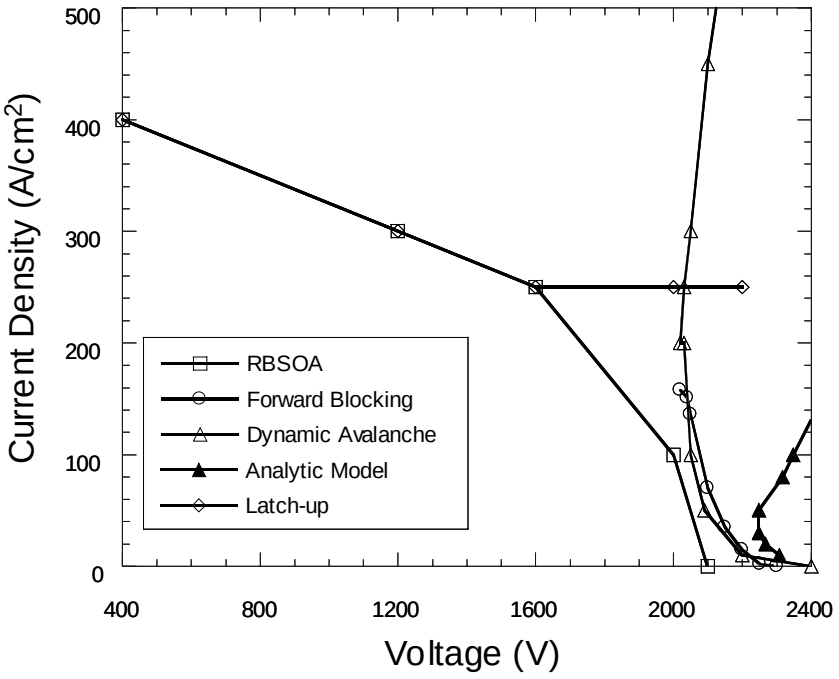

Fig. 2.7 Limiting factors of the RBSOA of the N-MCT.

The simulated voltage versus the current locus of the lower transistors of both the N-MCT and the P-MCT in the forward blocking state are shown in Fig. 2.8 over a wide range of current densities. The static breakdown voltage of the PNP transistor of the N-MCT is about

2400 V, 900 V higher than that of the NPN transistor of the P-MCT. Besides this difference, the lower PNP transistor shows distinct I~V characteristics when compared to the lower NPN transistor. Instead of losing a tremendous amount of voltage blocking capability, as shown by the NPN transistor of the P-MCT with the current increase, the voltage blocking capability of the PNP transistor of the N-MCT stops declining around 100 A/cm^2, and starts to increase beyond that current density.

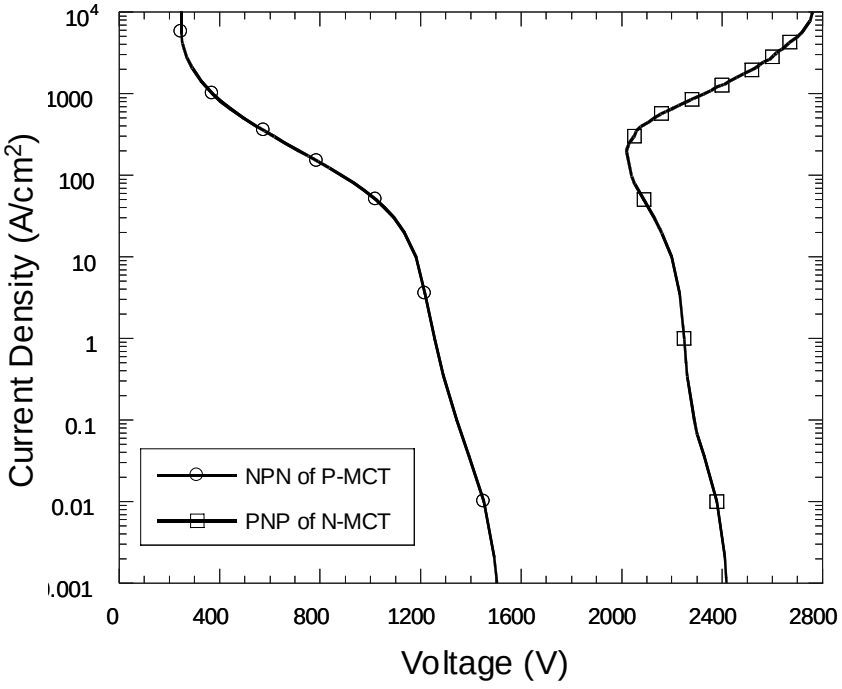

Fig. 2.8 Simulated forward blocking capability of the lower transistors of the MCTs.

It has been experimentally confirmed that the P-MCT has lost a substantial amount of forward voltage blocking capability compared to the N-MCT [12]. The dynamic current gain characteristics of the lower transistor account for the de-rated forward blocking capability of the

P-MCT. In comparison with the N-MCT, the P-MCT first loses some static breakdown voltage (BV_{CEO}) due to its relatively high common base current gain α_o and higher impact ionization rate of electrons; the latter is expressed in the form of a lower n value in Eq. 2.4. Aside from that, the dynamic current gain characteristics of the P-MCT reduce its forward blocking capability even further, as predicted by Eq. 2.14.

From the above discussion, it is clear that a lower transistor with a low dynamic gain is needed in order to obtain a good forward blocking capability and hence a square RBSOA. Among the factors that determine that common base current gain α_o, doping profile of the lower transistor is one of the design parameters that can be optimized.

To investigate the impact of the doping profile on the dynamic gain characteristic, a punch-through P-MCT with a varied lower base buffer charge has been studied. This PT P-MCT has a similar top MCT structure to that of the NPT P-MCT except the former has a narrower drift region. The simulated dynamic current gain characteristics of the lower NPN transistor with a varied buffer charge are shown in Fig. 2.9. This figure shows that increasing the buffer charge can reduce the current gain, thus improving the RBSOA of the P-MCT, as shown clearly in Fig. 2.10. However, the dynamic current gains of the P-MCT are still higher than the critical gain value of 0.56, and the strong voltage-dependent RBSOA characteristic has not yet been changed. The dynamic current gain of all these transistors will eventually merge toward the same value at an extremely high current level. This gain characteristic suggests that, with the increase of the current level, the dynamic current gain characteristic of the lower open-base transistor depends more and more on the intrinsic properties of carriers such as the impact ionization rate, the saturated velocity, etc., while the doping profile will gradually lose its control on the dynamic gain characteristic.

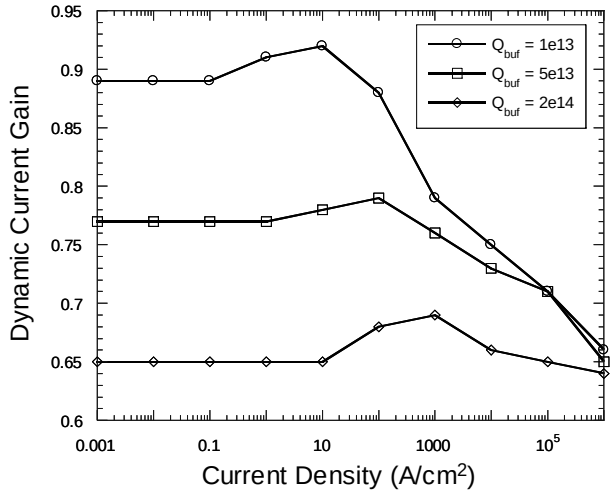

Fig. 2.9 Calculated dynamic current gain value of the lower NPN transistor of a PT P-MCT with a varied lower-base buffer charge.

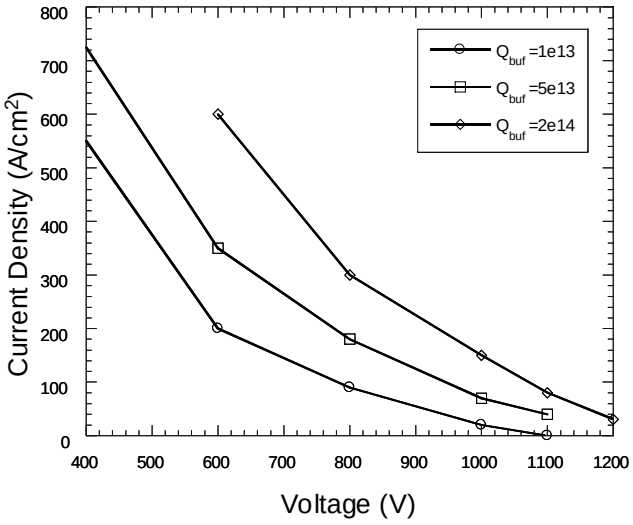

Fig 2.10 Dynamic avalanche limited RBSOAs of the PT P-MCT with a varied lower-base buffer charge.

2.5 Unified View of The RBSOA of the MCT

2.5.1 Upper-base Modulation Effect

As stated at the beginning of this chapter, there are two main types of electrical failure mechanisms of the MCT: current induced latch-up and dynamic avalanche. The current induced latch-up limitation is characterized by Eq. 2.3, which calculates the J_{mcc} capability of the turn-off MOSFET of the MCT. The dynamic avalanche limitation is described by Eq. 2.14, which characterizes the lower open-base transistor of the MCT. Therefore, the combination of Eq. 2.3 and Eq. 2.14 determines the RBSOA boundary of the MCT.

The simulated RBSOA boundary imposed by the latch-up limitation individually, as well as that imposed by the dynamic avalanche as discussed in previous sections, is then superimposed on the simulated RBSOA curve, and shown in Fig. 2.4 for the P-MCT, and in Fig. 2.7 for the N-MCT. These two figures confirm that the RBSOA of the MCT is limited by the onset of the latch-up at low voltages, and by dynamic avalanche at high voltages. While the latch-up limitation is relatively insensitive to the operating voltage, the dynamic avalanche limitation could be either strongly voltage-dependent, as shown in the P-MCT, or insensitive to the operating voltage, as observed in the N-MCT. A relatively square RBSOA, which is mainly current-limited, has been achieved for the N-MCT.

During the study, a drastic loss of current control capability in the transition region between the latch-up limitation and the dynamic avalanche limitation boundaries has been observed in some devices. As shown in Fig 2.11, the RBSOA boundary of a 2400-V N-MCT (case I) is substantially lower than the latch-up limitation (J_{mcc}) line in the range of 1200 V to 2000 V. The reason for the degradation of the RBSOA characteristics was found due to a strong upper-base resistance modulation effect, which occurs in the MCT with a relatively low charge in the upper base.

During the turn-off phase of building up the voltage, the expansion of the depletion region into the upper-base region increases the lateral resistance of the upper base. This base resistance modulation effect is particularly pronounced when the MCT has a shallow upper base with a low charge. The lateral resistance may cause current crowding during the turn-off transient, and triggers the injection from the emitter junction. The injected carriers will undergo a multification process due to the existence of a high electric field in the upper-base/lower-base junction, and eventually makes the device reenter a state of latch-up. This failure mechanism can be viewed as the joined effect of dynamic latch-up and dynamic avalanche, and it has been demonstrated that increasing the upper-base charge can eliminate the degradation of the turn-off capability due to the upper-base resistance modulation effect. A sharp transition between the two distinctive limitation boundaries has been achieved on the N-MCT by increasing the upper-base charge from $2x10^{12}$ to $3x10^{12}$, as shown in Fig. 2.11.

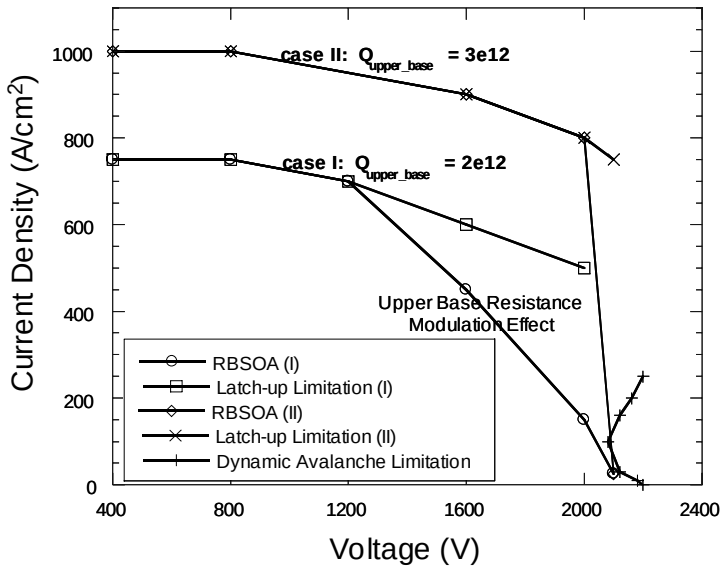

Fig. 2.11 Limiting factors of the RBSOA of a N-MCT with a varied upper-base charge.

2.5.2 P-MCT vs. N-MCT

Based on the polarity of the device, the MCTs can be classified into two categories: N-type MCTs and P-type MCTs. The N-MCT has a P-type turn-off MOSFET and a lower PNP transistor, while both the turn-off MOSFET and the lower transistor of the P-MCT are N-type.

According to Eq. 2.3, the P-MCT has a higher J_{mcc} value than the N-MCT because the mobility of the electrons in the turn-off N-MOSFET of the P-MCT is two to three times higher than that of the holes in the turn-off P-MOSFET of the N-MCT. Therefore, the P-MCT is a superior structure from the J_{mcc} point of view. However, the P-MCT has a very poor dynamic avalanche characteristic because of the lower NPN transistor. The strong voltage-dependent RBSOA characteristics of the P-MCT eventually diminish the benefit of its high J_{mcc} capability. Although the N-MCT has a P-type turn-off MOSFET with a lower J_{mcc} value when compared to its complementary P-MCT, the N-MCT, with a PNP transistor as the lower transistor, has much better dynamic avalanche limited RBSOA characteristics. Therefore, the N-MCT is preferred not only from the application point of view, but also from the RBSOA point of view. Besides the better RBSOA characteristics, the N-MCT also has better turn-off characteristics, such as the turn-off loss, than its P-type counterpart [8].

Based on the above discussion, one would not expect Harris Semiconductor's first MCT product to be a P-MCT. The reason for this lay in the device channel densities practical at that time. The problem with making the N-type MCT was never the vertical device tradeoff, such as the dynamic avalanche limited RBSOA, or the turn-off loss characteristics, but the fact that the turn-off P-MOSFET was not able to reach a channel density (W_{CH}/A) that would allow a J_{mcc} at about 400 A/cm ^{2} at 150 ^{o}C to make an N-MCT practical [8].

During the past several years, the off-FET channel densities have increased to the point where a N-MCT with a J_{mcc} at several hundreds of amperes per square centimeter can be made. The latest reported N-MCT has been able to turn off 1100 A/cm^2 at room temperature, and greater than 500 A/cm^2 at 150 ^{o}C by using an off-FET channel density of 25 m/cm^2, twice that of the old generations of the MCT [8]. It has been experimentally confirmed that the N-MCT has a square RBSOA [13].

2.6 Conclusion

This chapter performed a comprehensive theoretical investigation of the electrical failure mechanisms of the MCT, and, for the first time, identified the dynamic avalanche limited RBSOA boundary of the MCT as the voltage versus current locus of the lower open-base transistor in its high-current forward blocking state.

A first-order analytical model, based on the concept of dynamic current gain, was developed to characterize the high-current forward blocking characteristics of the lower open-base transistor of the MCT. A characteristic equation for the dynamic avalanche limited RBSOA boundary of the MCT was developed. It was found that the difference between the dynamic current gain value and a constant critic gain determines the RBSOA boundary.

It is the dynamic current gain characteristic of the lower open-base transistor that accounts for the performance discrepancy between the P-MCT and N-MCT. The impact of the doping profile on the dynamic current gain characteristic has also been investigated, and it has been found that the dynamic current gain characteristic will eventually depend on the intrinsic properties of the carriers, and the doping profile will gradually lose its control with the increase of current.

Since the MCT, the IGBT, and other MGT devices all behave as open-base transistor in the turn-off transient, the RBSOA limitations due to the dynamic avalanche are essentially the same for all these devices. Therefore, the analytical model developed for the dynamic avalanche limitation of the MCT can also apply to other bipolar power devices such as the IGBT.

Finally, a unified view on the limiting factors of the RBSOA of the MCT was presented. It was concluded that the strong voltage-dependent RBSOA characteristics of the P-MCT eventually diminish the benefit of its high J_{mcc} capability, and the N-MCT is preferred not only from the application point of view, but also from the RBSOA point of view. It was also found

that a high upper-base charge is necessary in order to achieve a relatively square RBSOA in the N-MCT.

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Chapter 3 MCT vs. IGBT Comparison

3.1 Introduction

Power switches are essential components in power regulation of the load for all power electronics systems. The continuous development of power electronics technology has opened up wide applications for power semiconductor devices. Power MOSFET is used widely in low-voltage and high-frequency applications. However, the on resistance of the power MOSFET increases very rapidly with the increasing voltage rating due to the lack of conductivity modulation, and this makes it unsuitable for high-voltage applications. Currently, the Insulated-Gate Bipolar Transistor (IGBT) is the primary candidate for medium-power applications. This chapter focuses on the basic device issues and uses modeling to compare the MCT's advantages and disadvantages to the IGBT's.

In the comparison of power devices, it is common to perform a tradeoff not only between the on-state voltage drop (V_F) and the turn-off loss (E_{off}), but also between the on-state voltage drop and the reverse-biased safe operating area (RBSOA) [1]. In the first portion of the chapter, this three-way tradeoff investigation is undertaken on the unit-cell level of the MCT and the IGBT to emphasize their fundamental device characteristics.

Multi-cell devices are necessary to scale the current handling capability of a MCT or an IGBT from the order of milliamperes for a unit-cell to the order of amperes as needed for application. The gate connection of a multi-cell device generally is composed of a layer of polysilicon connected to a thin strip of metal at the perimeter of the die, which in turn makes contact with the gate lead of the package. The effective gate resistance seen by the unit-cells

located at the center position of the die is far greater than that seen by the unit-cells on the perimeter. With the increase of the device area, the gate delay between the center and the periphery of the multi-cell device becomes more and more pronounced. In a large-area multi-cell MCT, propagation of the gate signal to all parts of the devices does not occur simultaneously, and is the major limitation in achieving a uniform turn-off of the multi-cell MCT.

The second portion of this chapter investigates the on-set of current filament in a multi-cell MCT due to the gate delay and compares it to that in an IGBT. It is found that formation of current filament during the turn-off due to the gate delay is an intrinsic problem of a large-area multi-cell MCT.

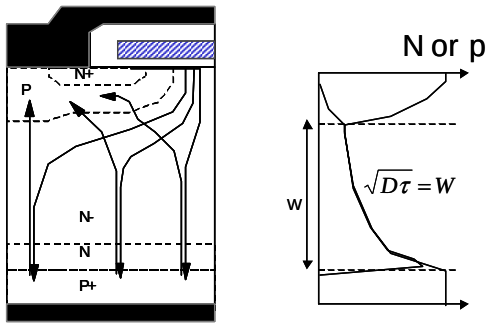
3.2 Three-way Tradeoff of Unit-cell Devices

3.2.1 Optimized On-state Carrier Profile

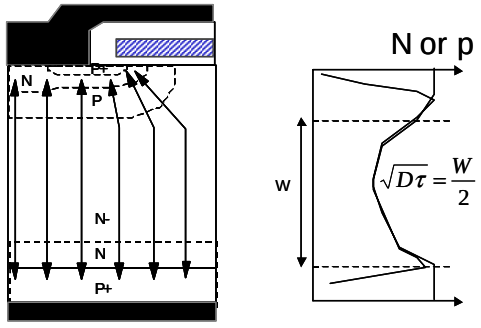
Fig. 3.1 shows the basic unit-cell structures of a N-type MCT and a N-type IGBT, which are very similar except that the MCT replaces the IGBT's emitter short with a P-channel MOS short. The on-state carrier distribution profiles are shown alongside the cross-section view of the unit-cell structures to illustrate the main difference in the carrier modulation levels in the MCT and the IGBT. Essentially these figures show that the modulated carrier density falls exponentially as it moves away from the emitting junction. The fall-off rate of the carrier modulation level is characterized by the ambipolar diffusion length. Among the carriers injected from an emitter, only 1/e portion of them can reach the point that is L_a away from the emitter. The ambipolar diffusion length (L_a) of a bipolar device at high level injection is defined as [2]

$$L_a = \sqrt{D_a \tau_{HL}} \tag{3.1}$$

where D_a is the ambipolar diffusion coefficient, and τ_{HL} is the high-level carrier lifetime. In order to maintain a certain level of modulation in the long N- drift region for a low on-state voltage drop, the ambipolar diffusion length infers a certain level of carrier lifetime, and therefore a certain level of turn-off speed limitation for both the MCT and the IGBT. Assuming the diffusion length L_a must equal W, the thickness of the N- drift region, for the least carrier modulation level in the IGBT, the L_a needs to be only W/2 to have an equivalent modulation level for the MCT due to the double-side injection. For this reason, the MCT can have a much lower carrier lifetime to achieve a similar level of modulation as the IGBT.



(a) IGBT



(b) MCT

Fig. 3.1 Basic unit-cell structures and their on-state carrier distribution profiles: (a) N-MCT and (b) N-IGBT.

Fig. 3.2 shows the simulated on-state carrier (hole) profiles of the 1200-V MCT and IGBT with the same lower transistor doping profile. In the on state of the MCT, carriers are injected into the N- drift region from both ends of the thyristor structure. The carrier profile of the MCT is similar to a P-i-N diode with the carrier concentration at its highest at both junctions [2]. In the on state of the IGBT, carrier injection only occurs at the collector P+/N junction. Therefore, the carrier concentration of the IGBT is highest near the collector end, and falls exponentially as it moves toward the emitter end. Since the carrier modulation level determines the voltage drop across the long N- drift region, the on-state voltage drop of the IGBT is higher than that of the MCT given the same carrier lifetime condition due to the lower modulated carrier profile of the IGBT. As shown in Fig. 3.2, the on-state voltage of the IGBT is 0.8 V higher than that of the MCT when the same high-level carrier lifetime (τ_{HL}=1.4 us) is assumed in the simulation. The IGBT with the same on-state voltage drop as the MCT has a higher carrier lifetime (τ_{HL}=2.4 us) to enhance its modulation level.

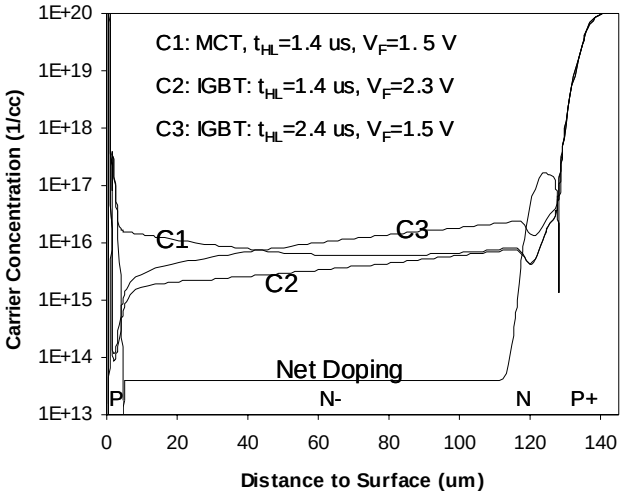


Fig. 3.2 Simulated on-state carrier (hole) profiles of the 1200 V MCT and IGBT.

During the turn-off of a MCT, the injection of electrons from the upper emitter will cease after the turn-off P-MOSFET is turned on to bypass the hole current entering the P base. Similarly, the electron current carried by the N-MOSFET of an IGBT will discontinue after the IGBT is turned off. Both the turn-off of the MCT and that of the IGBT cut off the base-driving electron current of the lower transistors. The subsequent open-base transistor turn-off process is similar in both devices. In an inductive turn-off, the current flowing through the device and hence the lower transistor remains constant. The constant current is sustained by extracting stored carriers out of the N- drift region. As a result, a depletion region is developed, and the voltage across the devices starts to rise. For the MCT or the IGBT, the upper P/N- junction of the device is the main voltage-blocking junction. Carriers stored in this region have to be removed before the devices can sustain forward blocking voltage. After the voltage rises to the clamped voltage, the depletion region will no longer expand, and the residue carriers stored in the N- drift region near the anode end are removed through a recombination process. The recombination process accounts for the current tail in the turn-off current waveform. The turn-off current tail increases the overall turn-off loss. Compared to the MCT with the same on-state voltage drop, the IGBT has a larger current tail because of the higher carrier concentration in the N- drift region near the anode end, and a longer current tail due to the higher carrier lifetime it assumes. Therefore, the IGBT has a larger turn-off loss (E_{Off}) compared to the MCT under the same on-state voltage condition.

For bipolar power devices such as the MCT and the IGBT, the turn-off speed is limited by the time taken for removal of the stored charge in the drift region. The turn-off characteristics, such as turn-off time and turn-off loss, therefore are related to the modulation level. It is found that the on-state voltage drop (V_F) increases after reduction of the modulation level, as observed for all bipolar power devices. Therefore, there is always a tradeoff between the V_F and the turn-off characteristic. From the above discussion on the turn-off process, it is clear that an optimized on-state modulation profile in the drift region of the MCT or the IGBT should have a higher modulation level near the main voltage-blocking junction (the cathode end for the N-type devices

or the anode end for the P-type devices) to maintain a low on-state voltage drop, and have a lower modulation level near the remote emitter junction (the anode end for the N-type devices or the cathode end for the P-type devices) to reduce the current tail and improve the turn-off characteristics.

In a conventional IGBT structure, injection only occurs at the remote collector P+/N junction. The modulation profile of the IGBT is not an optimized one from the viewpoint of the tradeoff between the V_F and the turn-off characteristics. A great deal of attention has been focused on the injection enhancement effect in the IGBT for boosting the carrier modulation level near the emitter end of the IGBT [3].

In a MCT, injection occurs at both ends of the device. The sum of the current gains of the upper and lower transistors equals unit to maintain the regenerative action of the thyristor structure in the on state. To improve the tradeoff between the V_F and the turn-off characteristic, the MCT should be designed with a high-gain upper transistor and a low-gain lower transistor to achieve the optimized carrier modulation profile.

Besides the carrier lifetime adjustment, the buffer charge is one of the most important design parameters used to adjust the current gain characteristics of the lower transistor of the MCT. Similarly, the upper-base charge is one parameter used to adjust the current gain characteristics of the upper transistor. In the next section, the impact of the buffer and the upper-base charges on the V_F vs. E_{off} tradeoff and the RBSOA characteristics of the MCT will be investigated and compared to those of the IGBT.

The simulated devices are built from the same starting wafer. The drift regions of the simulated 1200-V MCT has a doping concentration of 5×10^{13} cm^{-3} and a thickness of 100 μm. The comparative IGBT has the same collector, buffer, and drift regions as the MCT, while its cathode structures are optimized accordingly. This is as close to an apple-to-apple comparison as can be made. The devices are “electron irradiated” by setting the electron and hole lifetimes in the drift region at different levels with electron lifetime being seven times the hole lifetime, presumably the ratio seen using electron irradiation [4].

3.2.2 Impact of Buffer Charge

In this study, the width of the N buffer region is fixed at 25 um, and the buffer charge varies from 1e13 to 1e14 cm^{-2}. For each buffer charge variation, the first set of simulations calculated the on-state voltage drop (V_F) of the device over a wide range of carrier lifetimes. The gate voltage was 15 V in the V_F simulations. The second set of simulations was then carried out to calculate the inductive turn-off loss (E_{off}) of the device over the same range of carrier lifetime by using the mix-mode simulation feature of the simulator ATLAS [5]. Fig. 3.3 shows the schematic of the simulation circuit. In the E_{off} calculation, the device was assumed to turn off an inductive load of 100 A/cm^2 for the 1200 V devices under a clamped voltage of half of their rated voltage. The gate voltage was ramped down from 15 V to –15 V within 100 ns to initiate the turn-off process. The third set of simulations calculated the dynamic avalanche limited RBSOA boundary of the device by tracing out the forward blocking current-voltage characteristics of the device. The correlation between the dynamic avalanche limited RBSOA boundary and the forward blocking characteristics of the MCT has been identified in ref. [6].

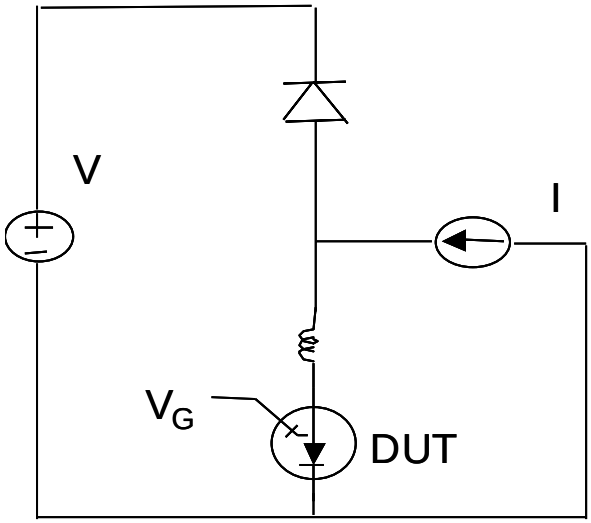
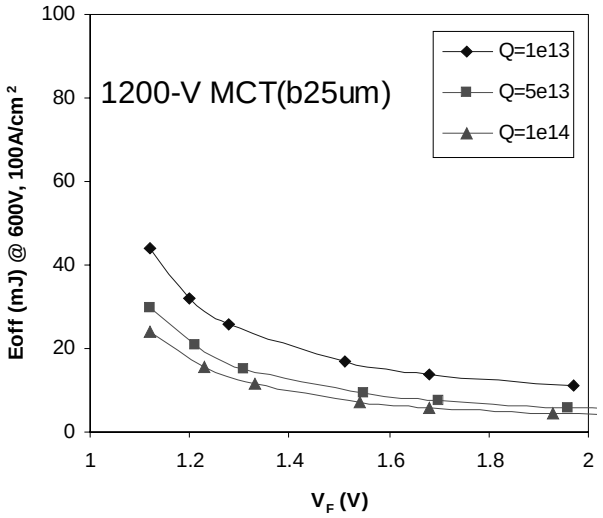


Fig. 3.3 Schematic of the simulation circuit.

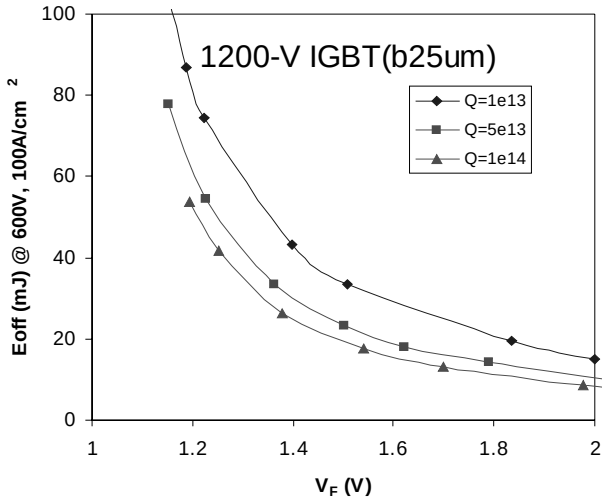
The tradeoffs between the V_F and the turn-off loss per cycle (E_{off}) of the MCT and the IGBT with varied buffer charge were obtained by combining the results of the first and second sets of simulation experiments, as shown in Fig. 3.4. The simulation results confirm that both the MCT and the IGBT with a higher buffer charge offer a better V_F vs. E_{off} tradeoff, and the MCT has a better V_F vs. E_{off} tradeoff compared to the IGBT. These characteristics are consistent with the previous discussion of the optimized on-state carrier profile. The devices with higher buffer charges have less stored charge near the buffer region due to the lower current gain of their lower transistors. During the turn-off, the device current will cease only after these stored carriers have been totally recombined. How fast the current tail will decrease mainly depends on the carrier recombination rate in this region. The structures with higher buffer charges have faster recombination rates since the carrier lifetime is doping concentration dependent [5].

Although increasing the buffer charge improves the V_F vs. E_{off} tradeoff of both the MCT and the IGBT, the improvement is more pronounced in the MCT. Fig. 3.5 shows the V_F vs. E_{off} tradeoff comparison between the MCT and the IGBT with two different buffer charges (Q). In the case of Q=1e13, the E_{off} of the MCT is slightly higher than one half of that of the IGBT under the same voltage condition, while in the case of Q=1e14, the E_{off} of the MCT is lower than one half of that of the IGBT.

In the comparison of power devices, it is common to perform a tradeoff not only between the on-state voltage drop and the turn-off loss, but also between the on-state voltage drop and the RBSOA characteristics. There are two main types of limitations on the RBSOA boundary of the MCT: current induced latch-up and dynamic avalanche [6]. The dynamic avalanche limitation is related to the lower transistor, and the current induced latch-up limitation is mainly related to the cathode geometric parameters. Therefore, only the dynamic avalanche limited RBSOA characteristic is considered in this vertical V_F vs E_{off} tradeoff study. Fig. 3.6 shows the dynamic avalanche limited RBSOA boundary of the devices under the same V_F condition. It is clearly shown that the MCT, as well as the IGBT, with a higher buffer charge has a larger RBSOA since the heavily doped buffer reduces the dynamic current gain of the lower transistor, thus improving the RBSOA characteristics [6].

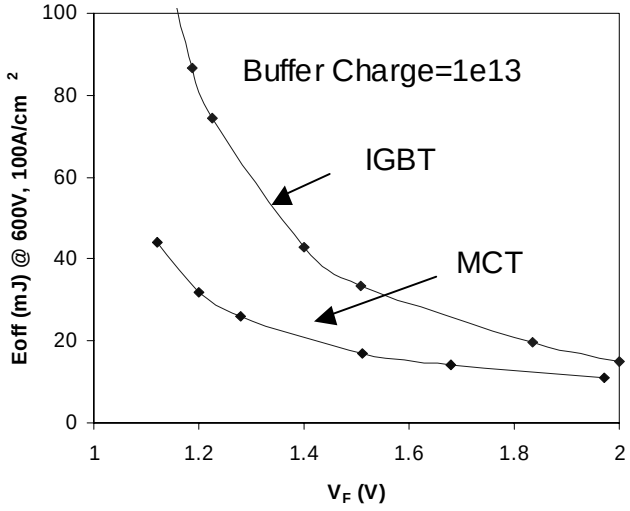


(a) MCT

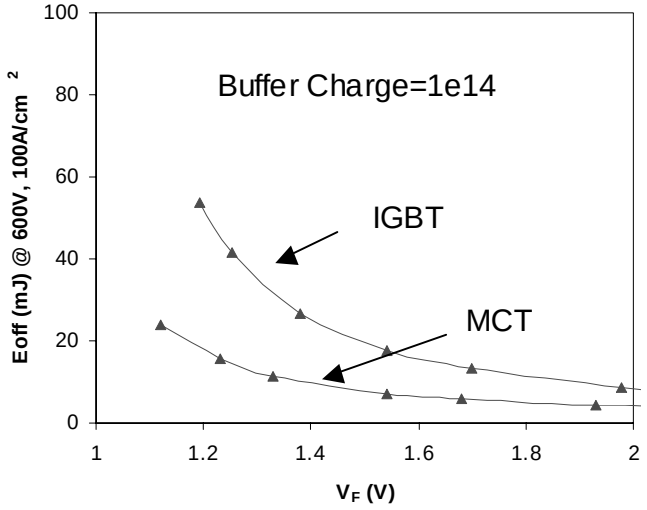


(b) IGBT

Fig. 3.4 Tradeoffs between the V_F and the turn-off loss per cycle (E_{off}) with varied buffer charge: (a) MCT and (b) IGBT.

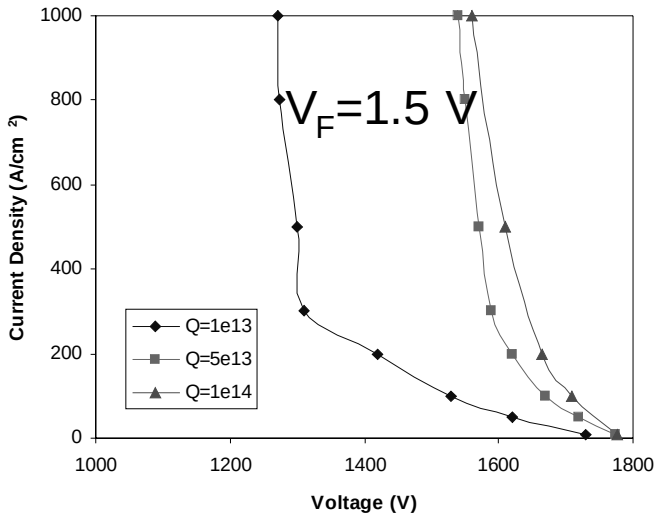


(a) buffer charge=1e13

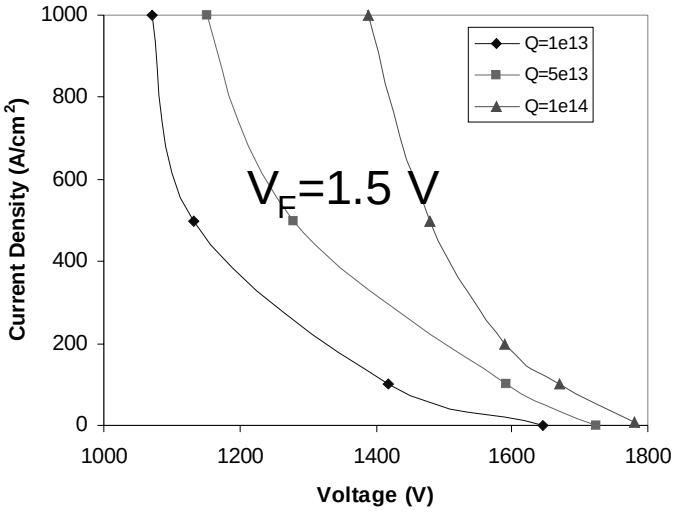


(b) buffer charge=1e14

Fig. 3.5 V_F vs. E_{off} tradeoff comparison between the MCT and the IGBT with two different buffer charges (Q): (a) Q=1e13 and (b) Q=1e14.



(a) MCT



(b) IGBT

Fig. 3.6 Dynamic avalanche limited RBSOA characteristics of the devices under the same V_F condition: (a) MCT and (b) IGBT.

The simulation experiment also shows that the dynamic avalanche limited RBSOA of the MCT is even bigger than that of the IGBT under the same V_F condition. In this study, the MCT and the IGBT have the same lower transistor structure, which determines the RBSOA characteristics investigated. Under the same V_F condition, the MCT can be "irradiated" harder than the IGBT because the upper transistor also contributes to the carrier injection, so the current gain of the lower transistor of the MCT is lower than that of the IGBT. Therefore, the dynamic avalanche limited RBSOA of the MCT is bigger than that of the IGBT. However, it needs to be pointed out that the overall RBSOA of the MCT is still smaller than that of the IGBT because of the lower current limitation level of the MCT.

Although the above V_F vs. E_{off} tradeoff investigation is based on the N-type devices, the same conclusion also applies to the P-type devices. Compared to the N-MCT, the P-MCT has a similar low on-state voltage drop due to the inherent thyristor structure with two coupled NPN and PNP transistors. However, compared to the N-IGBT, the P-IGBT has a much higher on-state voltage drop due to higher voltage drop across the P-MOSFET. Therefore, the superiority of the P-MCT over the P-IGBT is more pronounced than that between the N-MCT and the N-IGBT in terms of the V_F vs. E_{off} tradeoff.

Fig. 3.7 compares the V_F vs. E_{off} tradeoffs for the 1200-V P-type devices to those for the N-type devices. Although the N-type devices have better V_F vs. E_{off} tradeoffs than their complementary P-type devices, the superiority of the MCT over the IGBT in terms of the V_F vs. E_{off} tradeoff is more pronounced in P-type devices, which makes the MCT an attractive candidate in P-type power devices.

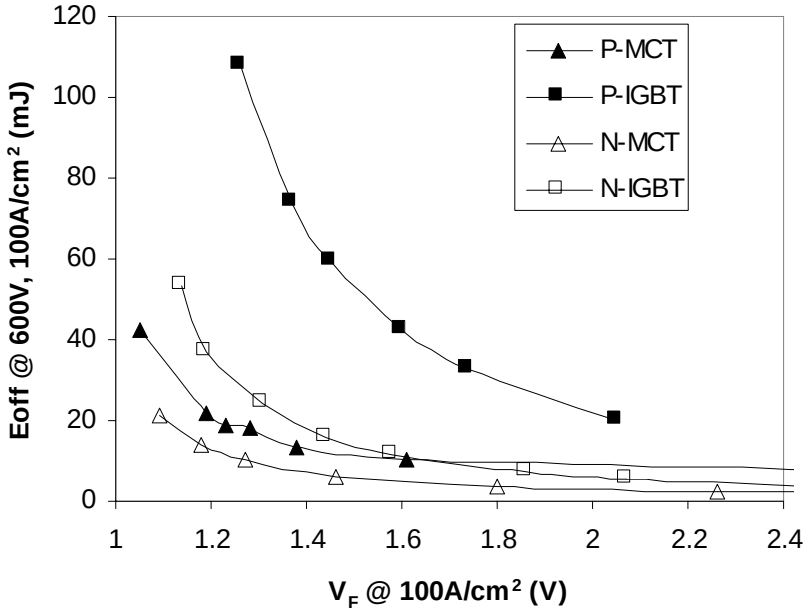


Fig. 3.7 V_F vs. E_{off} tradeoffs for the 1200 V devices.

3.2.3 Impact of Upper-base Charge

In the on-state of the MCT, the sum of the upper and lower transistor gains equals unity, i. e. $\alpha_{npn}+\alpha_{pnp}=1$. In order to reduce the gain of the lower transistor to improve the dynamic characteristics of the MCT, the gain of the upper transistor needs to be increased to maintain the unity sum of gain requirement. From the standpoint of this vertical tradeoff, an optimized MCT structure should have a low-gain lower transistor and a high-gain upper transistor. A high-gain upper transistor requires a low upper-base charge (Q_{UB}).

However, a low upper-base charge means a high upper-base sheet resistance. The upper-base lateral resistance, along with the channel resistance of the turn-off MOSFET, is part of the resistance that determines the maximum controllable current density (J_{mcc}) of the MCT. To improve the J_{mcc} capability, which has been the major concern of the MCT, a deep upper base

with high upper-base charge has been widely used in the conventional MCT design. It is the J_{mcc} requirement, not the vertical V_F vs. E_{off} tradeoff, that dictates the upper-base design of the MCT. This is particularly true in the N-MCT, whose J_{mcc} capability is intrinsically lower than the P-MCT due to the turn-off P-MOSFET integrated in the N-MCT.

Fig. 3.8 shows the V_F vs. E_{off} tradeoff of a P-MCT with varied upper-base charge. As expected, the P-MCT with the lowest upper-base charge has the best tradeoff. The effect of the upper-base charge on the tradeoff is less pronounced when the thyristor is not fully latched, and the on-state voltage drop of the device is high. When the thyristor structure comes out of latch, the effect of the upper transistor on the V_F vs. E_{off} tradeoff diminishes, as clearly shown at high V_F ranges in Fig. 3.8.

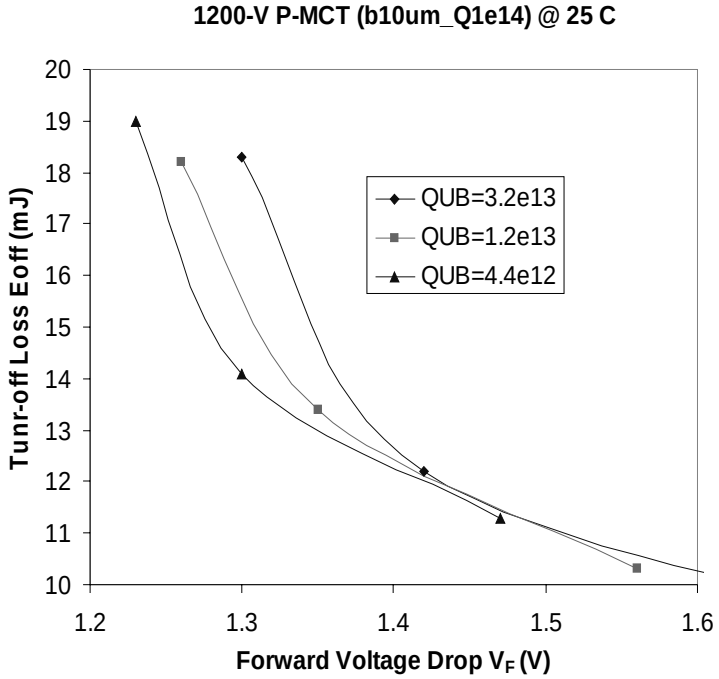


Fig. 3.8 V_F vs. E_{off} tradeoff of a P-MCT with varied upper-base charge (Q_{UB}).

3.4 Non-uniform Turn-off in Multi-cell Devices

3.4.1 Turn-off Failure Due to Gate Delay

The maximum controllable current density (J_{mcc}) is one of the most important characteristics of the MCT. The J_{mcc} value given by Eq. 2.3 is calculated based on a single MCT unit-cell. Multi-cell devices are necessary to scale the current handling capability of the MCT from the order of milliamperes for a unit-cell to the order of amperes as need for application. A modern MCT or an IGBT is composed of tens of thousand of unit-cells connected in parallel on the same die. The J_{mcc} of a multi-cell MCT has been found to be strongly affected by an inhomogeneous current distribution within the device and decreases rapidly with increasing die area [2].

Most of the investigation work on the turn-off failure of the MCT due to inhomogeneous current distribution has been focused on the structural inhomogeneities of the MCT, such as the interruption of the upper base by the turn-on cell, existence of device boundary, etc. [7-9]. Other work has been focused on the parallel failure of MCT devices with mismatched device parameters, such as the switching speed [10].

The research work here focuses on the fundamental device characteristics that distinguish the MCT from the IGBT in term of scaling up current. The multi-cell devices are assumed to consist of identical unit-cells. This assumption excludes the paralleling failure mechanism due to the difference between structure or process parameters of the unit-cells.

Each unit-cell of the MCT starts to turn off when its gate voltage crosses the threshold voltage of its turn-off MOSFET. The propagation delay between the application of the gate signal and the threshold crossing depends on the RC time constant as seen by the unit-cell. Both the MCT and the IGBT rely on polysilicon for the gate connection. As shown in Fig. 3.9, the gate connection generally is composed of a layer of polysilicon connected to a thin strip of metal at the perimeter of the die, which in turn makes contact with the gate lead of the package. Therefore, the effective gate resistance seen by the unit-cell located at the center position of the

die is far greater than that seen by the unit-cell on the perimeter. As a result, propagation of the gate signal to all parts of the device does not occur simultaneously. With the increase of the device area, the gate delay between the center and the periphery of the device becomes more and more pronounced.

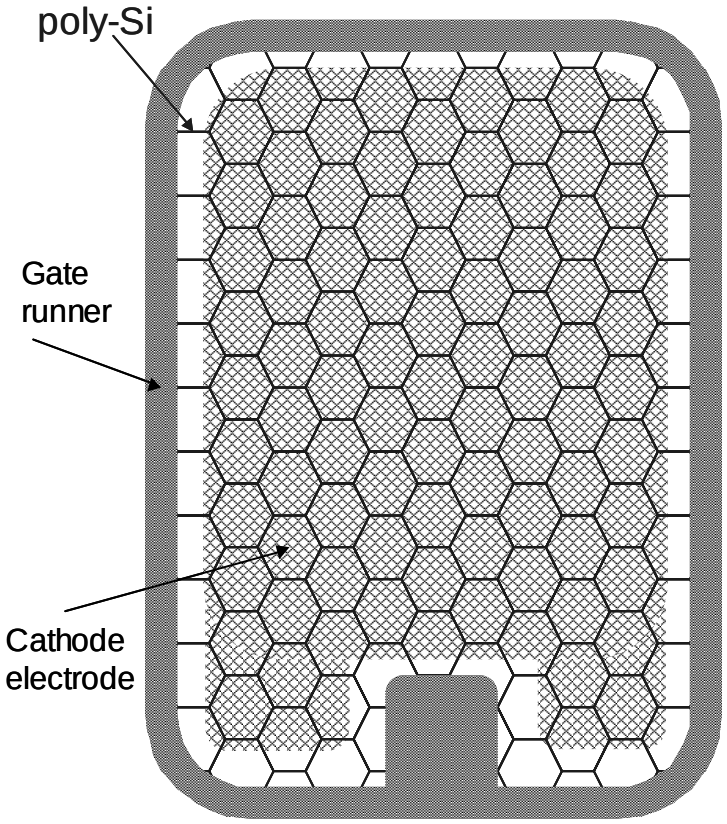


Fig. 3.9 Typical layout of a multi-cell MCT.

Gate delay will cause current from the turned-off cells to commute to the cells which are still on and form current filament. If the current filament exceeds the maximum controllable current density of the individual unit-cell, turn-off of the multi-cell MCT will fail. The internal propagation gate delay is the major limitation in achieving a uniform turn-off in a large-area

multi-cell MCT. One important observation during the development of the MCT is the dramatic decrease of the measured turn-off capability of the device with the increase of the device area. The gate delay is the main reason for the degradation of the turn-off capability.

The work presented here investigates the on-set of current filament in the multi-cell MCT due to the gate delay and compares it to that of the IGBT. It is found that formation of current filament during the turn-off due to the gate delay is an intrinsic problem of the multi-cell MCT.

3.4.2 Modeling Approach

Ideally, an accurate investigation of the onset of current filament in a multi-cell device should be studied by directly simulating the multi-cell device. However, considering the capability and simulation efficiency of the currently available numerical simulator, a complete simulation of the multi-cell device is virtually impossible because of the huge number of finite elements needed to describe the multi-cell device. A simplified modeling approach is needed. The focus of the investigation work here is not trying the match the simulation result with the experimental data. Instead, the investigation work is focused on the fundamental characteristic that distinguishes the MCT from the IGBT in terms of turn-off failure due to the gate delay.

Fig. 3.10 shows the simplified modeling approach for studying the effect of the gate delay on the onset of current filament in a multi-cell device. Two lumped devices are used to represent the multi-cell device with internal gate delay. Device A simulates the unit-cells on the perimeter that are normally turned off, and device B simulates the unit-cells with a turn-off delay (t_d). N stands for the ratio of the area of device A to that of device B. The total area of the multi-cell MCT is assumed to be one centimeter square.

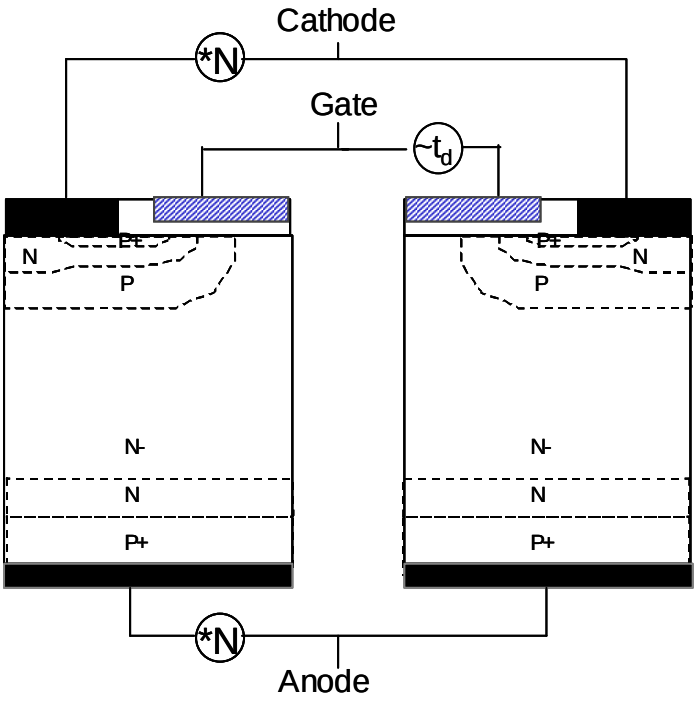


Fig. 3.10 Simplified modeling approach to study the effect of the gate delay on the onset of current filament in a multi-cell device.

The multi-cell device is assumed to carry an inductive load of 100 A in the on state. Since both device A and B have identical unit-cells, the load current is evenly distributed between these two devices, and they carry a forward current density of 100 A/cm^2. Due to the existence of area ratio, the current carried by device A is N times that carried by device B. The gate voltages of device A and B are ramped down from +15 V to –15 V at a ramp rate of 300 V/μs with a delay of t_d between the two gate signals to initiate the non-uniform turn-off. The schematic of the simulation circuit is the same as that shown in Fig. 3.3.

As a result of the turn-off of device A, the anode voltage of the devices tends to rise. However, due to the gate delay, the turn-off process of device B lags behind that of the device A. Since the anodes of devices A and B are tied together, the interaction between the two devices causes the current redistribution. Device B tends to take over more current since the device is still

on. If the current redistribution results in a current filament beyond the maximum controllable current density (J_{mcc}) capability of device B, the multi-cell device will fail to turn off. In the isothermal simulation, in which the thermal effect is neglected, device B will eventually carry all the load current initially shared between device A and device B.

The J_{mcc} of the MCT is typically lower than that of the IGBT for the same process parameters and design rules. The J_{mcc} of the MCT can be improved by increasing the off-FET channel density through a fine line cathode design. However, the difference in the J_{mcc} value is not the only factor that distinguishes the MCT from the IGBT. Instead, the most important factor that makes the multi-cell MCT vulnerable to gate delay is that the MCT lacks current saturation or current limiting capability.

The anode voltage of the multi-cell device tends to rise after the turn-off of device A. Whether the anode voltage of the multi-cell device will follow the loci of a single unit-cell turn-off is mainly determined by the area ratio N, due to the interaction between device A and device B. For a multi-cell device with a large area ratio N, the loci of the anode voltage will be very close to that of a single unit-cell turn-off until device B takes over most of the current.

For the thyristor-based devices such as a MCT, the rise of the anode voltage causes the current across device B to increase exponentially if the upper-emitter injection of device B is still on. If the turn-off of device B is not quick enough after the turn-off of device A, the current across device B will quickly exceed its J_{mcc} capability. On the other hand, the situation is different in an IGBT with current saturation capability. The current saturation feature of the IGBT limits the current across device B and prevents the current from running out of bounds when the collector voltage of device B is forced to rise due to the turn-off of device A. As a result, the multi-cell IGBT is less sensitive to the gate delay, and more likely to survive a non-uniform turn-off. The difference between what occurs in device B of a multi-cell MCT and that in an IGBT when the anode/collector voltage is increased is illustrated in Fig. 3.11.

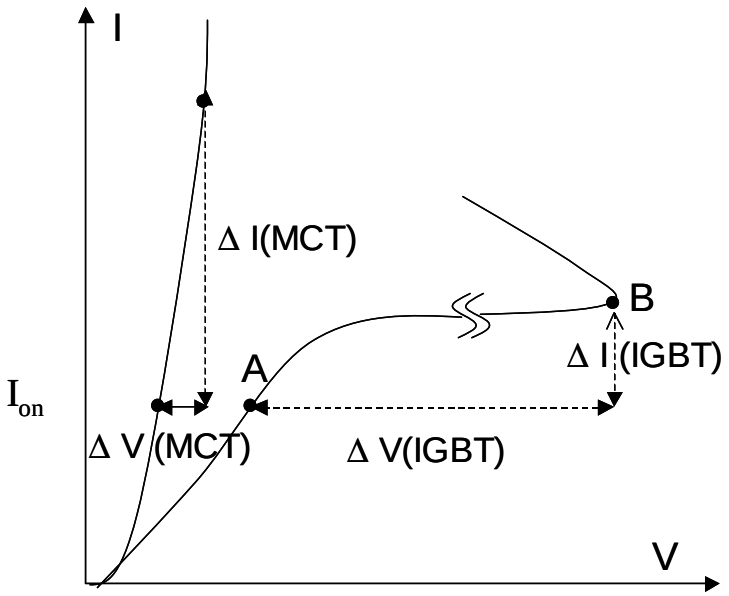


Fig. 3.11 The difference between what occurs in device B of a multi-cell MCT and in that of an IGBT when the anode voltage rises.

The simulated unit-cells of the 1200 V MCT and IGBT have the same cell structure and same doping profile in each layer. The two-dimensional numerical simulation is performed by using MEDICI [11].

3.4.3 Results and Discussion

Fig. 3.12 shows the simulated current and voltage waveforms of device B during the turn-off of a multi-cell MCT. At time 0, the gate of device A is ramped down from +15 V to –15 V within 100 ns. The delay (t_d) for the gate signal of device B is assumed to be 40 ns and 50 ns, respectively. The area ratio N is assumed to be 1000.

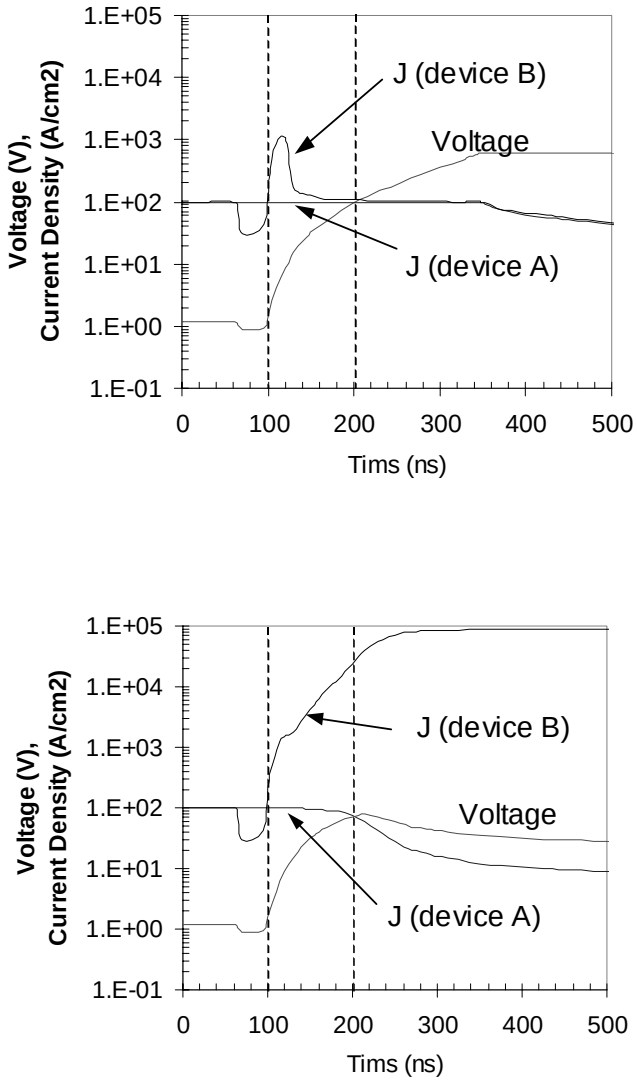


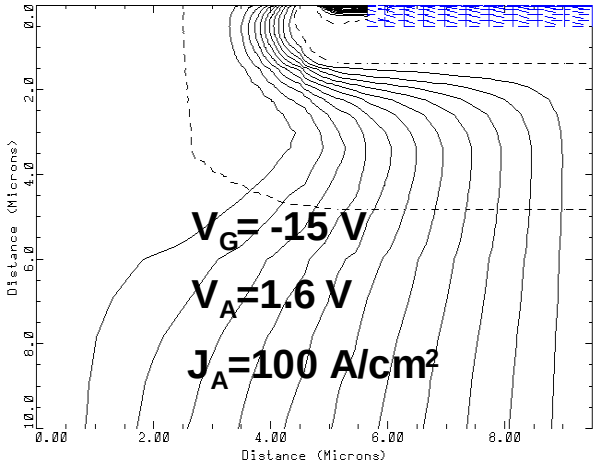
Fig. 3.12 Simulated current and voltage waveforms of devices A and B during the turn-off of a multi-cell MCT: (a) gate delay t_d=40 ns and (b) t_d=50 ns.

After a short period of dipping, the anode voltage of the multi-cell device starts to rise. The dipping of the anode voltage occurs during the short period in which the turn-off MOSFET

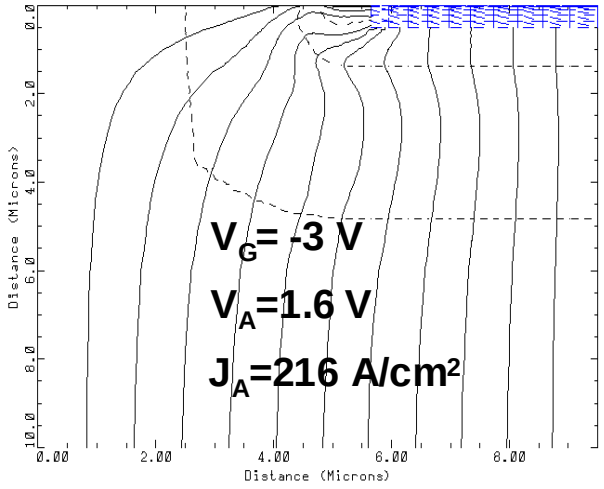
of device A starts to bypass the hole current while the upper emitter injection is still on. After the upper emitter injection ceases, the lower PNP transistor of device A loses its base-driven electron current. The load current across device A is supported by extracting stored carriers out of the drift region.

Due to the turn-off delay, device B is still on when the anode voltage of the multi-cell device starts to rise. Fig. 3.13 shows the current flow lines of devices A and B at t=100 ns in the case of t_d=40 ns. The instant gate voltage, anode voltage, and anode current density of the devices are labeled in the figures. It should be noted that the on-state voltage drop (V_F) of the unit-cell MCT measured at a current density of 100 A/cm^2 is about 1.2 V. Fig. 3.13a shows that the upper emitter injection has been fully turned off, and the turn-off channel bypasses all the current entering the upper P base in device A. On the other hand, Fig. 3.13b shows that the turn-off channel just starts to bypass hole current, and the emitter injection is still on in device B. Since the anode voltage of the device A is coupled to that of device B, the current density across device B rises to 216 A/cm^2 from its initial 100 A/cm^2 to reflect the change in anode voltage, which increases 0.4 V to 1.6 V.

For the thyristor-based MCT, the current across the still-on device B will rise drastically in response to the further increase of anode voltage. The operation of device B under this condition is similar to a short-circuit condition. During an inductive turn-off, the total current flowing through devices A and B remains constant before the anode voltage rises to the diode-clamped voltage set at 600 V. However, the current will redistribute between devices A and B due to the dramatic increase of the current across device B. More current will be transferred from device A to device B until the latter is fully turned off. The transferring of current from device A to device B will slow down the process of extracting the carriers and building up the depletion layer in device A. Therefore, the rise rate of the anode voltage will also be slowed down after more amd more current is squeezed into device B.



(a) Device A



(b) Device B

Fig. 3.13 Current flow lines of device A and device B at t=100 ns during the turn-off of a multi-cell MCT with a gate delay t_d=40 ns.

How the interaction between device A and device B behaves is related to the area ratio N. For a multi-cell device with a high area ratio between device A and device B, the absolute current value across device B is very small compared to that across device A, even when device B has a much higher current density than device A. Therefore, it is device A that mainly determines the anode voltage rise rate of the multi-cell device. The effect of device B on the anode voltage starts to surface only when its current value becomes comparable to that of device A. When that occurs, the current density of device B may have exceeded its maximum controllable current density (J_{mcc}) and the turn-off may then fail.

To ensure a successful turn-off, the current filament within device B should not exceed its J_{mcc} capability. Since the current filament in device B increases rapidly with the increase of the turn-off delay, the turn-off of a multi-cell MCT is very sensitive to the gate delay. Fig. 3.12a shows a successful turn-off when the gate delay is 40 ns, and a failed turn-off when the gate delay is 50 ns. Fig. 3.14 shows the current flow lines of device B at four different time steps when the gate delay is 50 ns. It is clearly shown that the turn-off fails because the current filament exceeds the J_{mcc} capability of device B.

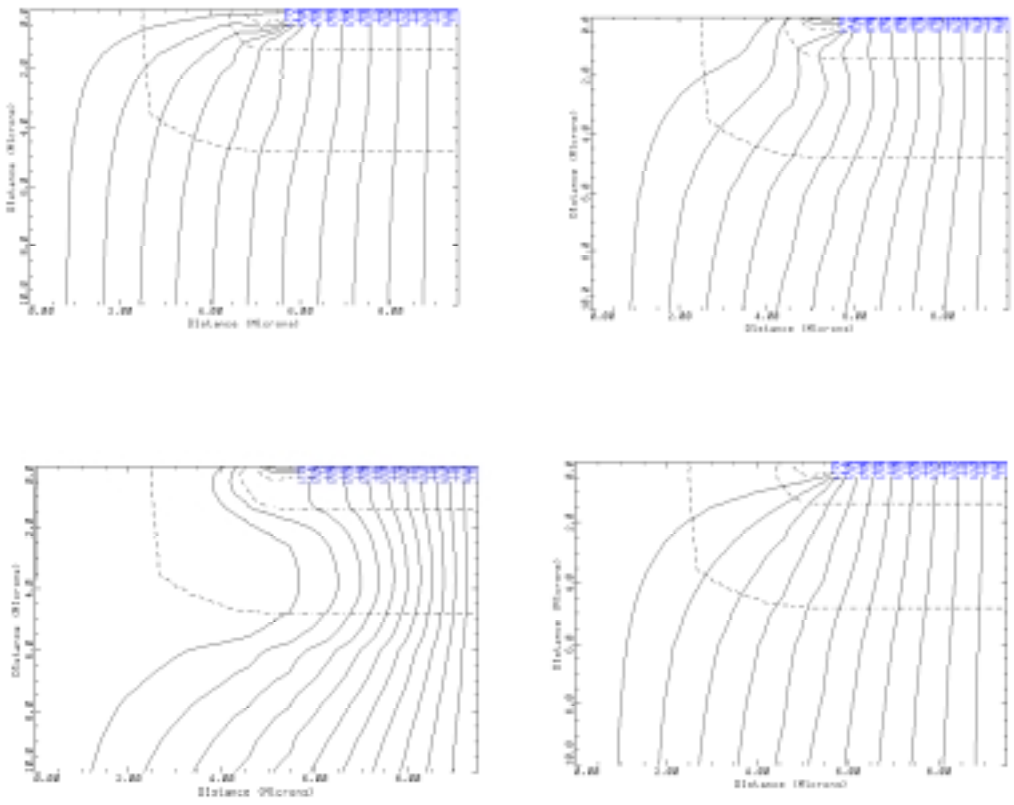


Fig. 3.14 Current flow lines of device B at four different time steps during the turn-off of a multi-cell MCT with a gate delay t_d=50 ns.

It should be pointed out that the J_{mcc} of the unit-cell of the simulated MCT is over 2000 A/cm^2. Nevertheless, the turn-off of the multi-cell MCT with an area ratio of 1000 fails at 100 A/cm^2 when the gate delay is longer than 50 ns. Further enhancement of the J_{mcc} capability of the unit-cell will improve the turn-off capability of the multi-cell MCT. However, given the exponential relationship between the anode voltage and the current in the thyristor-based devices, the enhancement in the J_{mcc} capability of the unit-cell will not significantly improve the turn-off capability of the multi-cell MCT. The problem that a large-area multi-cell MCT is vulnerable to

gate delay cannot be simply solved by increasing the J_{mcc} capability of the unit-cell. The only solution to this problem is to minimize the internal gate delay within a large-area multi-cell MCT. This can also explain the observation that a multi-cell MCT fail to turn off if the gate voltage rise-time is longer than a critical value [10], because a slow gate signal tends to increase the internal gate delay.

The turn-off of a multi-cell IGBT is different. Due to its current saturation feature, the IGBT is able to sustain high voltages while limiting the conducting current in its forward conducting state [2]. The operating area, within which the device possesses the current saturation capability, is something referred to as the forward-biased safe operating area (FBSOA). The current saturation characteristic of the IGBT helps keep the current across device B bounded when device B is still on and the collector voltage starts to rise due to the turn-off of device A.

The multi-cell IGBT is able to survive a non-uniform turn-off because the IGBT possesses the current saturation capability. The current saturation capability of the IGBT is only limited by the parasitic thyristor structure of the IGBT. As shown in Fig. 3.11, if the current-voltage goes beyond point B, the inherent parasitic transistor structure of the IGBT will latch, and the IGBT will lose its current limiting capability. This puts a limitation on the non-uniform turn-off capability of the multi-cell IGBT.

Fig. 3.15a shows a successful turn-off of the multi-cell IGBT when the gate delay is as long as 200 ns. The current saturation feature of the IGBT is clearly shown in the current waveform of device B. Further increase of the gate delay will run the current-voltage out of the maximum saturation capability of the IGBT, and will subject the IGBT to a turn-off failure due to the unbound current filament formed in device B as shown in Fig. 3.15b. The latch-up of the parasitic thyristor structure in device B of the multi-cell IGBT is clearly shown in Fig. 3.16, which shows the current flow lines of device B at t=240 ns in the case of t_d=300 ns.

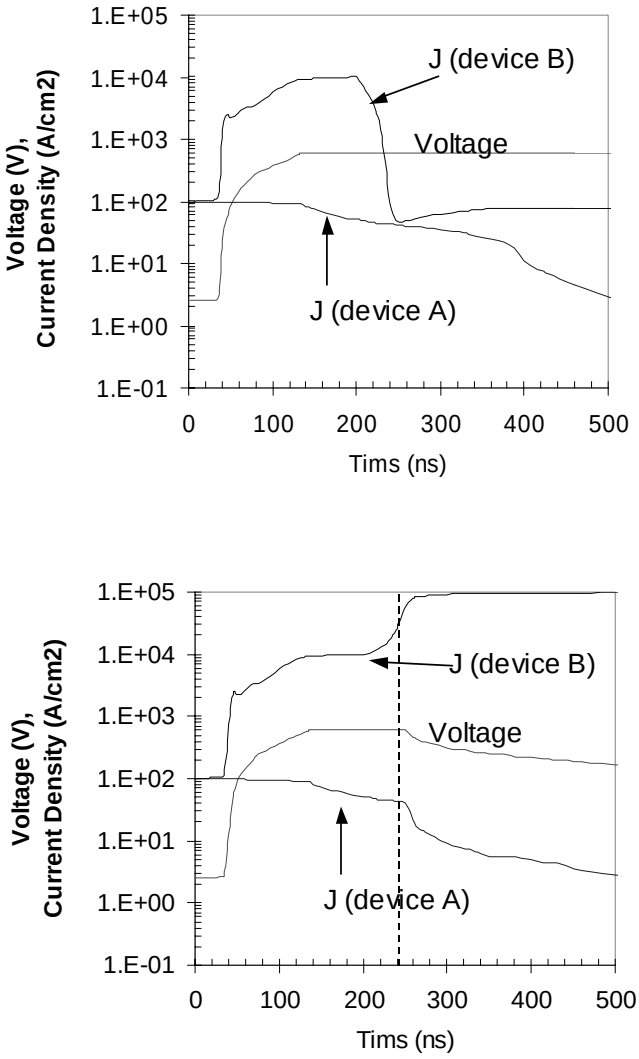


Fig. 3.15 Simulated current and voltage waveforms of devices A and B during the turn-off of a multi-cell IGBT: (a) gate delay t_d=200 ns and (b) t_d=300 ns.

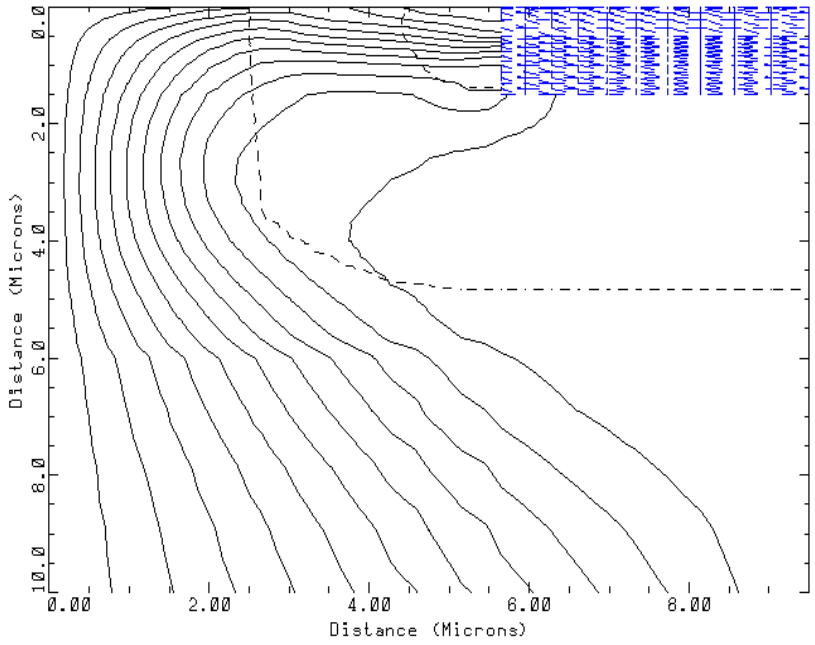


Fig. 3.16 Current flow lines of device B at t=240 ns during the turn-off of a multi-cell IGBT with a gate delay t_d=300 ns.

3.4 Conclusion

In this chapter, some fundamental device characteristics of the MCT are investigated with the help of numerical simulation, and compared to those of the IGBT. The apple-to-apple comparison studies have been undertaken at two different levels: unit-cell and multi-cell.

The comparison at the unit-cell level focused on the design tradeoff between the on-state voltage drop (V_F), turn-off loss (E_{off}), and the RBSOA characteristics. The multi-cell level comparison emphasized the fundamental difference between the MCT and the IGBT in handling the non-uniform turn-off due to the internal propagation gate delay of a large-area unit-cell device, which is used to scale up the current handling capability as needed in application.

The results contained in this chapter suggest the following.

1) A MCT structure has a better V_F vs. E_{off} tradeoff than an IGBT structure because the MCT has a more optimized on-state carrier profile as a result of its double-side carrier injection. The superiority of the MCT in terms of the V_F vs. E_{off} tradeoff is more pronounced in the P-type devices than in the N-type devices.
2) While the J_{mcc} capability of the MCT is lower than the IGBT, the dynamic avalanche limited RBSOA characteristics of the MCT are similar to those of the IGBT. Under the same V_F condition, the MCT can be "irradiated" harder or can use a higher buffer charge to achieve better dynamic avalanche limited RBSOA characteristics than the IGBT.
3) Due to the lack of current saturation capability, the turn-off capability of a multi-cell MCT is intrinsically vulnerable to the formation of current filament in the regions with the longest gate delays during turn-off. Increasing the J_{mcc} capability of the unit-cell is not an effective solution to this problem. Reducing the internal propagation gate delay is critical in the large-area MCT technology.
4) Compared to a MCT, a multi-cell IGBT is less sensitive to gate delays, and more likely to survive a non-uniform turn-off because of its unique current saturation characteristic.

However, the research work presented in this chapter only qualitatively illustrates the fundamental difference between the turn-off capabilities of a multi-cell MCT and a multi-cell IGBT, using a simplified two-lumped-device model to represent the multi-cell device. A distributed device model provides more accurate representation of the multi-cell device. More investigation is needed in order to quantify the non-uniform turn-off capability of a large-area multi-cell MCT.

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Chapter 4 Demonstration of the Dual Operation Mode MCT

4.1 Introduction

Current saturation or current limiting capability is one of the most important features for a power switch. It provides short-circuit protection for the switch, and is also used to achieve controlled turn-on which regulates the reverse recovery of the associated diode. However, in an Insulated Gate Bipolar Transistor (IGBT), enhancement in current saturation capability can only be achieved by decreasing the channel density, and comes at the cost of a higher on-state voltage drop [1]. On the other hand, the MCT has a much lower on-state voltage drop compared to the IGBT, but lacks the current saturation capability, which makes it difficult to protect the MCT against a short-circuit failure. Unlike an IGBT, the turn-on speed of a MCT is not controllable by the gate. The turn-on of a MCT is usually too fast, which results in a snappy reverse recovery in the associated diode.

The difference between the turn-on process of the IGBT and the MCT is illustrated in Fig. 4.1, which shows the static output characteristics of the devices and the dynamic current-voltage locus during the turn-on transient with an inductive load. For the IGBT, the locus is within the saturation region of the device, and its gate-controlled turn-on capability can be characterized by the transconductance (g_m). The transconductance of the IGBT in the saturation region of operation is given by

$$g_m = \frac{dI_D}{dV_G} = \frac{1}{1-\alpha_{PNP}} \frac{\mu_{ns} C_{ox} W_{CH}}{L_{CH}} (V_G - V_T) \qquad (4.1)$$

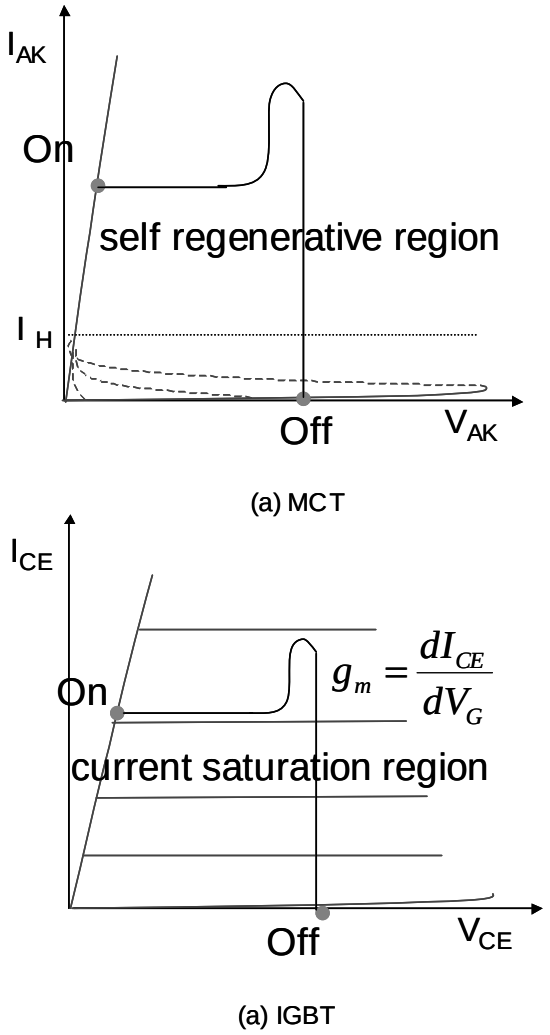

Fig. 4.1 Static output characteristics and the dynamic switching locus during an inductive turn-on: (a) MCT and (b) IGBT.

It can be seen from Eq. 4.1 that, for a given channel length (L_{CH}), the g_m of the IGBT is in proportion to the channel density, which is defined as the total channel width (W_{CH}) within a unit area. Reducing the g_m via decreasing the channel density can enhance the current limiting capability of the IGBT. However, this results in a higher on-state voltage drop.

Unlike an IGBT, which requires a continuous channel current to drive the lower transistor in the forward conducting state, the MCT can maintain itself in the forward conducting state by the regenerative action between the two coupled transistors within the structure when the forward current is above its holding current level (I_H). Since the holding current level is typical well below the on-state operating current densities of the MCT, the anode current level of the MCT is not determined by the gate bias during the turn-on transient. To provide controlled turn-on capability to thyristor-based power devices, devices with current saturation capability (also called forward-biased safe operating area) should be developed to obtain lower saturation current level to enhance the short-circuit capability and greater di/dt control (low g_m).

It has been reported that the current saturation feature and gate-controlled turn-on capability can be realized in MOS Gated Thyristor (MGT) devices, including the MCT by using structures with two gates [1-9]. Without exception, these reported double gate or dual gate devices achieve the current saturation feature and gate-controlled turn-on capability by providing an extra IGBT-like operation mode for the devices. However, the reported devices either have a high on-state voltage drop due to the introduction of a MOSFET in series with the thyristor structure [1, 2], or have a low maximum controllable current density (J_{mcc}) in the IGBT mode operation [3-9]. These two drawbacks limit the performance of these devices. As a result, most of the above work only provides some wafer-level static testing results, and none of these devices has been characteristized in a real switching circuit. How the dual operation mode feature of the device is going to affect the switching performance of the circuit has not yet been explored.

This chapter will investigate the switching performance of a dual operation mode MCT with superior current saturation capability in a hard-switching circuit. The following sections will first discuss the device design and the operation principle of the experimental dual operation mode MCT, and then demonstrate for the first time how a dual operation mode MCT can be beneficial in switching circuit applications.

4.2 Device Design and Operation

An advanced N-MCT process capable of a MOS channel density as high as 30 m/cm^2 has recently been developed by Harris Semiconductor with the support from Virginia Tech [10]. The developed N-MCT has already successfully turned off 1100A/cm^2 at room temperature and 500A/cm^2 at 150 ^{o}C. This performance is about twice better than that of the conventional MCT. With this advanced process, it is also practical to manufacture devices with more than one electrically separate MOS gate. This enables the fabrication of dual operation mode MCTs that behave either as conventional MCTs or as IGBTs [11].

Fig. 4.2 shows the schematic diagram of the unit cell of a dual operation mode MCT based on the high-channel-density MCT process. Fig. 4.2(a) is the top view of the structure and Fig. 4.2(b) is the cross-section view of the structure along the line A-A'. The unit cell of the fabricated device has a cell pitch (L_p) of 9.5 μm, less than half of that of the previously reported dual gate devices [1-9]. Furthermore, the cell structure changes from the conventional cellular structure to a structure that looks like long closely packed snakes. It is easy to have two electrically separate gate electrodes in this linear-type structure. This dual operation mode MCT was built by alternately stacking gates G1 and G2.

If G1 and G2 are tied to the same bias, the device is essentially a conventional MCT. Because the thyristor structure is latched in the on state, the on-state voltage drop of the device in this operational mode (referred to as the thyristor mode) is independent of the channel density of the turn-on N-MOSFET under G1. To operate the device in an IGBT mode, a positive bias is applied to G1 while a negative bias is applied to G2. In this case, electron current flows through the N-MOSFET under G1, while the hole current entering into the p-base is shunted to the cathode via the P-MOSFET under G2. The current flow lines of the device in these two operation modes are shown in Fig. 4.3. The channel density of the N-MOSFET determines the forward voltage drop as well as the current saturation level of the dual operation mode MCT in the IGBT operation mode. In the dual operation mode MCT, the channel density of the N-MOSFET can

therefore be optimized. On the other hand, in a conventional IGBT, reducing the channel density to enhance the current saturation capability is a two-edge sword, since its on-state voltage drop and the conduction loss increase with the decrease of the channel density.

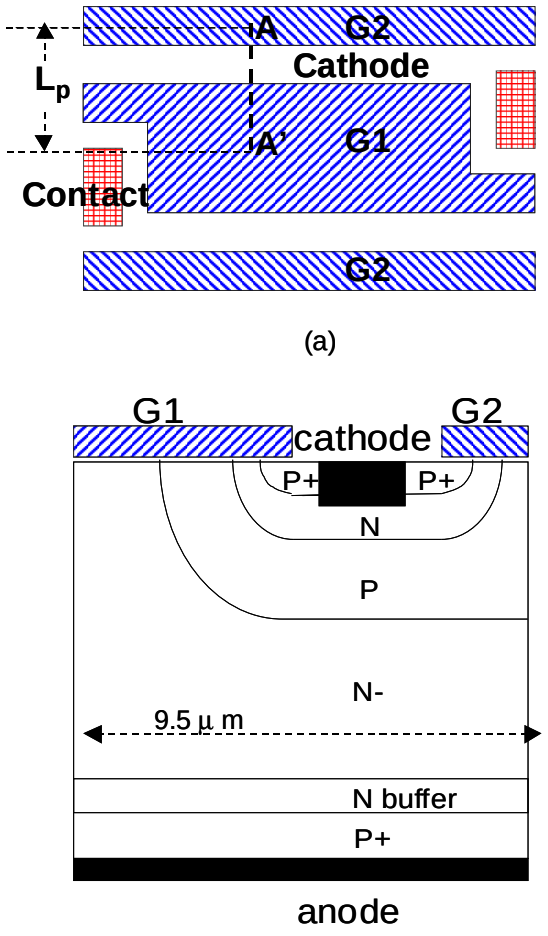

Fig. 4.2 Schematic diagram of the unit cell of the dual operation mode MCT: (a) top view and (b) cross section along line A-A'.

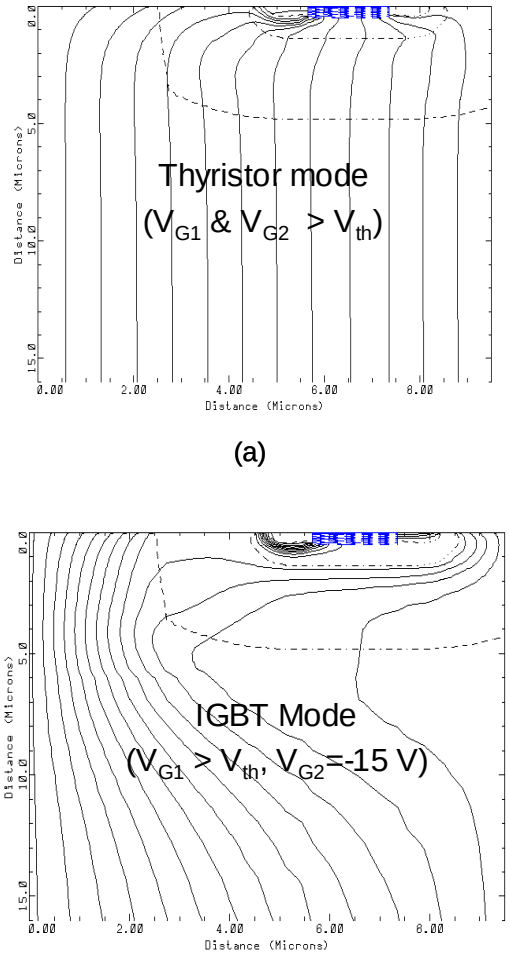

Fig. 4.3 Current flow lines of the dual operation mode MCT in the forward-conducting state: (a) thyristor mode operation, and (b) IGBT mode operation.

The dual operation mode MCT overcomes the tradeoff between the on-state voltage drop and the current saturation capability of the conventional IGBT by working in a thyristor mode in the on state and in an IGBT mode during the switching transient. The control scheme of the device is shown in Fig. 4.4. In the time t_{d_off} before the turn-off signal arrives at G1, G2 changes

the device operation from thyristor mode to IGBT mode. In the time t_{d_on} after the turn-on signal arrives at G1, G2 changes the device operation from IGBT mode to thyristor mode. Since the IGBT mode operation only accounts for a small percentage of the forward conduction time (T_{on}), the conduction loss of the dual operation model MCT is still significantly lower than that of the conventional IGBT. Therefore, in a dual operation mode MCT, the current saturation capability of the device in its IGBT mode operation can be optimized by reducing the channel density of G1 without affecting the overall on-state conducting loss.

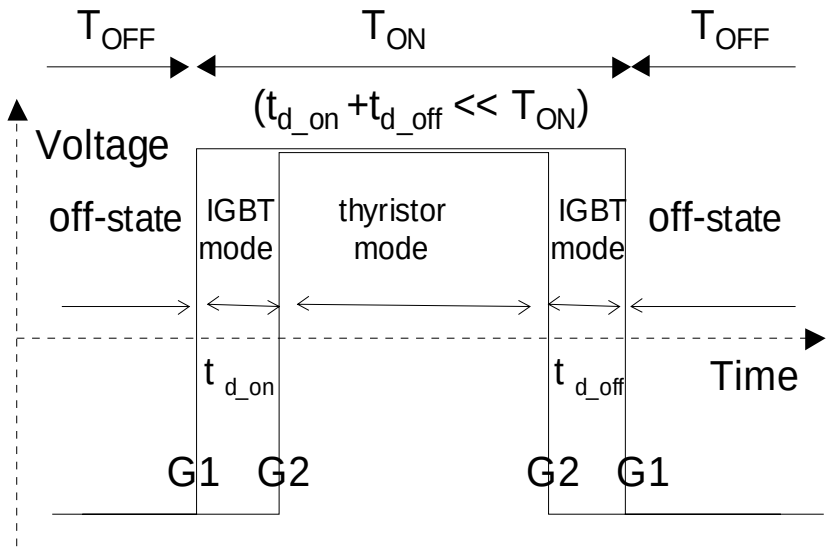

Fig. 4.4 Control scheme of the dual operation mode MCT.

4.3 Experimental Results

The experimental 1200-V N-type dual operation mode MCT was fabricated using the advanced N-MCT process described in the previous section [11]. The devices are TO-218 packaged, with an active area of approximately 2.2 mm^2.

Fig. 4.5 shows the measured output I-V characteristics of this device. The on-state voltage drop of this device is about 1.3 V at 1 A (45 A/cm^2) and 1.6 V at 2.2 A (100 A/cm^2) in the thyristor mode. This compares favorably with the state-of-the-art 1200-V IGBT whose forward drop is typically above 2 V at the same current density. This device also possess an excellent current saturation capability in the IGBT mode over a wide range of gate G1 voltages, from the threshold voltage up to 15 V. As clearly shown in Fig. 4.5, this device even saturates at normal operating current densities, making it attractive for many applications that require the current limiting feature at a normal operating current density instead of at excessive faulty load current [12]. On the other hand, a high g_m IGBT has a very small range of gate voltages that can limit current at normal current densities, and saturates only at a very high current density at its full gate bias. A low g_m IGBT fabricated with the same N-MOSFET channel density, therefore having similar current saturation feature and controlled turn-on characteristics as the dual operation mode MCT, has an on-state voltage drop of 4 V at 1 A and 17 V at 2.2 A.

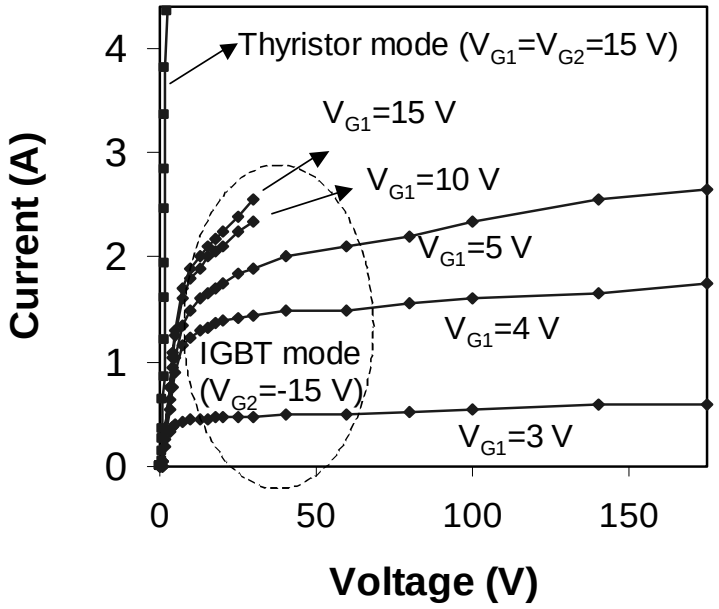

Fig. 4.5 Experimental output I-V characteristics of the dual operation mode MCT.

Fig. 4.6 shows the schematic of the hard-switching circuit used to test the dual operation mode MCT. The test circuit is a typical half-bridge circuit with an inductive load of 1 A and a DC bus voltage of 110 V. The control circuit generates two channels of gate signals to drive two identical gate drivers, whose timing is as shown in Fig. 4.4.

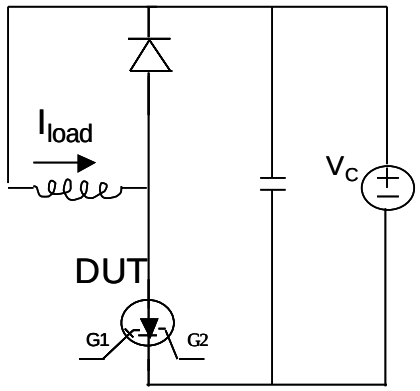

Fig. 4.6 Schematic of the circuit used to test the dual operation mode MCT.

4.3.1 Turn-on Characteristics

The investigation of the turn-on characteristics of the dual operation mode MCT focused on its ability to control di/dt and its impact on the reverse recovery of the freewheeling diode. Two different diodes were used in the testing: one was a slow body diode of a power MOSFET; the other was a state-of-the-art fast recovery diode with a reverse recovery time of 35 ns.

Fig. 4.7 shows the turn-on current waveforms of the dual operation mode MCT when the fast recovery diode was used as the freewheeling diode. It should be noted that the current overshoot came from the diode reverse recovery. When the device was operated as a conventional MCT, which is the case of t_{d_on}=0 μs in the figure, the peak turn-on current was about 3.4 A (2.4 A of overshot). The ringing of the current indicated that a snappy reverse recovery happened on the diode. By turning on the device in the IGBT mode with t_{d_on}= 0.2 μs,

the peak turn-on current was reduced to 1.7 A (0.7 A of overshot). In terms of the peak reverse recovery current of the diode, a 70% reduction was achieved. In addition to the reduction of the peak reverse recovery current, a much softer reverse recovery was also realized.

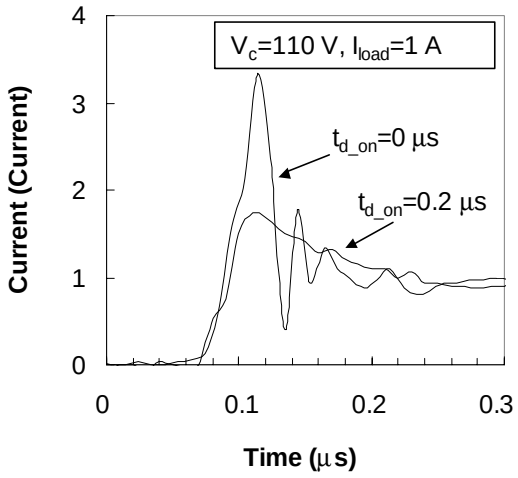

Fig. 4.7 Turn-on current waveforms of the dual operation model MCT when the freewheeling diode is a fast recovery diode.

The turn-on current waveforms of the dual operation mode MCT with the slow body diode as the freewheeling diode are shown in Fig. 4.8. Not surprisingly, the current overshoot was as high as 17 A when the device was operated as a conventional MCT. However, by turning on the device in the IGBT mode with t_{d_on}= 1 μs, the current overshoot was dramatically reduced to 3 A, results similar to those produced when the fast recovery diode was turned on by a conventional MCT. Fig. 4.9 shows the voltage-current locus of the freewheeling diode during the turn-on transient. Compared with the conventional MCT, the dual operation mode MCT succeeded in confining the voltage-current locus of the freewheeling diode within a relatively smaller area, which translates to a less demanding safe operating area (SOA) requirement for the diode.

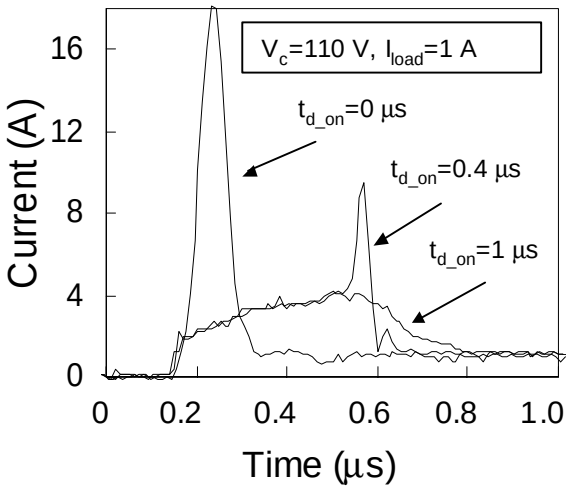

Fig. 4.8 Turn-on current waveforms of the dual operation model MCT when the freewheeling diode is a slow body diode.

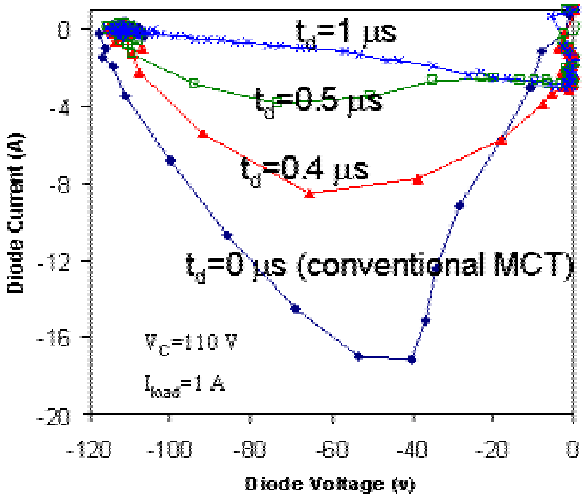

Fig. 4.9 V-I locus of the freewheeling diode during the turn-on transient of the dual operation mode MCT.

The peak current, the turn-on di/dt, and the loss of the dual operation mode MCT, as well as the reverse recovery loss of the freewheeling diode (the slow body diode), with different t_{d_on} are tabulated in Table 4.1. The measured data shows that t_{d_on} =1.0 μs is sufficient to control the turn-on di/dt and regulate the diode reverse recovery current. The data shows that, although the controlled turn-on feature of the device greatly reduces the reverse recovery loss of the diode, this reduction is achieved at the cost of increased turn-on loss on the dual operation mode MCT. Nevertheless, the greatly reduced turn-on di/dt achieved by the dual operation mode MCT greatly solves the diode reverse recovery problem and makes the diode selection easier.

Table 4.1 Measured turn-on performance of the dual operation mode MCT.

t_{d_on} (μs)	0	0.2	0.5	1.0	2.0
Peak current (A)	18.1	16.9	4.8	4.2	4.1
Turn-on di/dt (A/μs)	278	96	8.9	11	8.7
Turn-on loss* (μJ)	50	71	163	171	174
Diode loss* (μJ)	74	65	20	17	16

* Loss per switching cycle

4.3.2 Turn-off Characteristics

The turn-off characteristics of the dual operation mode MCT were also tested in the same hard-switching circuit with the same load. Table 4.2 summaries the relationships between the turn-off loss (the extra conduction loss caused by the rise of the forward voltage drop in the IGBT mode, with respect to that in the thyristor mode, is counted as part of the turn-off loss), the turn-off dv/dt and time t_{d_off}. It can be seen that the turn-off dv/dt increases with the increase of t_{d_off}, and stops increasing when t_{d_off} is longer than 1 μs. The turn-off dv/dt increases because the space charge region expands faster as a result of the reduced level of charge storage in the IGBT mode. 1 μs is also the time needed to extract extra carriers and establish an IGBT-like carrier profile. The higher turn-off dv/dt helps reduce the turn-off loss. However, a prolonged t_{d_off} will

generate excessive conduction loss due to a higher forward voltage drop in the IGBT mode operation. A schematic view of the voltage and current waveforms of the dual operation mode MCT during the turn-off transient is illustrated in Fig. 4.10. The dual operation mode MCT has the lowest overall turn-off loss when t_{d_off} is about 0.5 μs; however, the turn-off loss savings are not very pronounced compared with the conventional MCT, demonstrated in the case of t_{d_off}=0 μs in Table 4.2.

Table 4.2 Measured turn-off performance of the dual operation mode MCT.

t_{d_off} (μs)	0	0.2	0.5	1.0	2.0
Turn-off dv/dt (V/μs)	1406	1797	2070	2148	2094
Turn-off loss* (μJ)	26	25	24	26	28

* Loss per switching cycle

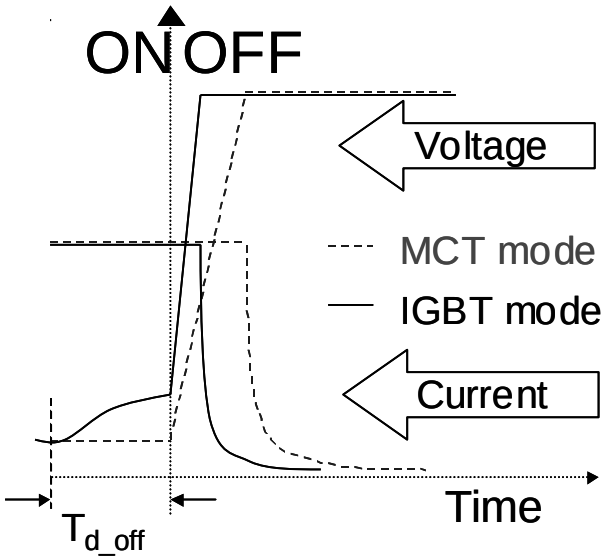

Fig. 4.10 Schematic view of the voltage and current waveforms of the dual operation mode MCT during the turn-off transient.

4.4 Conclusion

While dual operation mode MOS-gated thyristor devices have been previously reported, this is the first time the switching performance of a dual operation mode MCT in a hard-switching circuit is investigated. The experimental dual operation mode MCT was fabricated by using an advanced high-channel-density MCT process, which features a linear-type cell structure.

The dual operation mode MCT overcomes the tradeoff between the on-state voltage drop and the current saturation capability of the conventional IGBT by working in a thyristor mode in the on state and in an IGBT mode during the switching transient. The dual operation mode MCT is experimentally shown to have a lower on-state voltage drop and superior current saturation capability compared to the IGBT.

It is demonstrated that the dual operation mode MCT can greatly lower the stress on the associated freewheeling diode in the hard-switching application. However, it is found that the reduction of reverse recovery loss on the diode is achieved at the cost of increased turn-on loss on the dual operation mode MCT.

It is also found that the dual operation mode MCT does not have any significant impact on the overall turn-off loss of the device compared with the conventional MCT. The dual operation mode MCT therefore has a similar tradeoff between the on-state voltage drop and the turn-off loss as the conventional MCT, which has been proves superior to that of the IGBT [10].

The gate-controlled current saturation feature of the dual operation mode MCT in the IGBT mode operation can be used in the typical PWM phase leg to moderate turn-on di/dt and significantly lower the reverse recovery stress on the freewheeling diode. If the current saturation region (i.e. FBSOA) is large enough, the dual operation mode MCT will be able to operate in existing systems to replace the IGBT for higher efficiency.

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Chapter 5 Dual Operation Mode MGT Structures Compatible with the IGBT Process

5.1 Introduction

In the previous chapter, the dual operation mode MCT with superior current saturation capability was shown to be very effective in regulating the turn-on di/dt in hard-switching applications. As stated, the concept of the dual operation mode is not new. A dual operation mode device, called the Dual Gate MCT [1], with a similar device structure as the dual operation MCT investigated in the previous chapter, has been reported before. However, the previously reported Dual Gate MCT has a low maximum controllable current density (J_{mcc}) due to its large cell pitch, which limits its high current application.

The maximum controllable current density (J_{mcc}) in the IGBT mode operation is the most important parameter of the dual operation mode devices. The J_{mcc} determines the boundary of the operating area within which the device possesses the current saturation capability. Beyond this operating area, the inherent thyristor structure will latch and the device will lose its short circuit withstanding and gate-controlled current saturation capabilities. Since the device is operated in the forward conducting state, this characteristic is sometimes referred as the Forward-Biased Safe Operating Area (FBSOA).

The reason that the dual operation mode MCT possesses superior characteristics over the previously reported devices is because it was fabricated by an advanced N-MCT process capable of a very high MOS channel density, as pointed out in the previous chapter. As a result, the dual operation mode MCT has a high J_{mcc}, which makes it suitable for high current applications.

Compared with the IGBT, the fabrication process of the dual operation mode MCT, as well as that of the conventional MCT, is inherently more complex since the MCT structure requires a triple diffusion to accommodate the formation of both the turn-on and turn-off channels under the same gate (for the dual operation mode MCT, there are both turn-on and turn-off channels under the gate G1). The optimization of the turn-on and turn-off channel doping of the MCT is much more complicated than that of the IGBT.

Dual operation mode MOS Gated Thyristor (MGT) devices that can be fabricated by a less complex IGBT-like process have also been previously reported [2-8]. For the sake of consistency and simplicity, this category of devices is generally called the Dual MOS Gated Thyristor (DMGT) in this chapter. Similar to what happened to the previously reported dual gate MCT, low J_{mcc} problems also limited the performances of the reported DMGT devices.

In the dual operation mode MCT, improvement in the J_{mcc} is mainly achieved by increasing the channel density through the shrinkage of the cell pitch. In the DMGT, the separation of the turn-on and turn-off channels, as required by the double diffusion IGBT process, creates many variations in term of device structures. Optimizing device structure is therefore critical in improving the J_{mcc} of the DMGT.

This chapter analyzes the J_{mcc} of two typical DMGT device structures with the aid of two-dimensional numerical simulation and a first-order analytic J_{mcc} model. A new DMGT structure with improved J_{mcc} is then proposed based on the analysis. DMGT devices are fabricated by an IGBT-like process to experimentally verify the analysis.

5.2 Device Structures and Operation

As mentioned in the previous section, there are many variations in terms of the device structure of DMGTs. A straightforward DMGT structure that can be fabricated by an IGBT-like process is the DMGT structure A shown in Fig. 5.1 [2]. The DMGT structure A consists of a four-layer thyristor structure to which a floating ohmic contact (FOC) and a lateral N-channel

MOSFET have been added to the right hand side to provide the current saturation capability. The ability to turn off a MOS-thyristor structure using a FOC metalization has been previously reported [9], showing that holes are effectively removed during the turn-off process from the P-body region to the FOC, where they recombine with electrons coming from the cathode through a lateral N-channel MOS transistor.

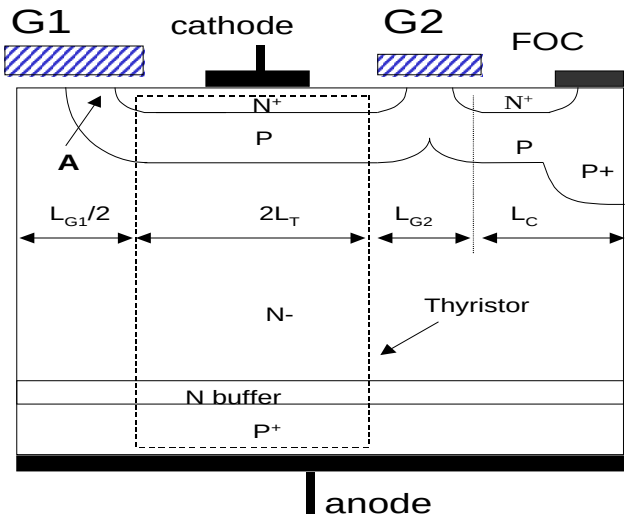

Fig. 5.1 Cross-section view of the DMGT structure A.

When a positive voltage is applied to the gate electrode of MOSFET1 while a zero or a negative bias is applied to the MOSFET2 gate, electrons are supplied to the base region of the PNP transistor from the N+ emitter via the channel of the MOSFET1. This results in the injection of holes from the anode P+ into the N- drift region. These holes diffuse across the N- drift region and are collected at the reverse biased N- drift/P base junction, where they are then swept into the P base region. If the injection of the holes is strong enough, the holes collected by the P base will forward bias the P base/N+ emitter junction to start the injection of electrons from the N+ emitter into the P base region. This triggers the regenerative feedback mechanism between the two

coupled transistors within the thyristor structure. The device is turned on to the thyristor mode. Fig. 5.2 shows the current flow lines of the DMGT structure A in the thyristor mode operation.

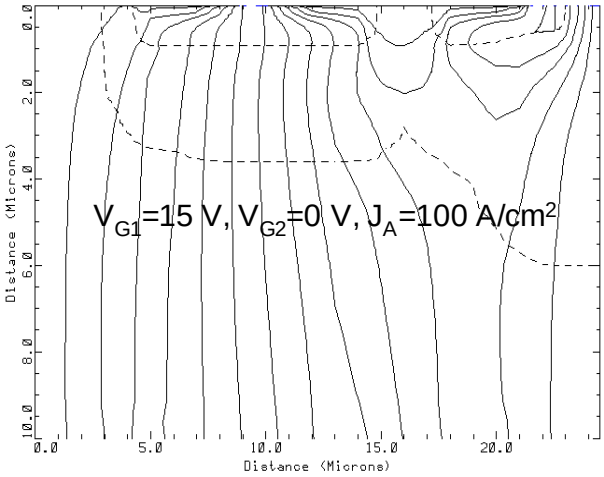

Fig. 5.2 Current flow lines of the DMGT structure A in the thyristor mode.

When the gate electrodes of both the MOSFET1 and MOSFET2 are positively biased, holes entering the P base region are diverted to the FOC and recombine with electrons coming from the cathode through the lateral N-channel MOSFET2. Since the FOC acts as a cathode short in this operation mode, the device functions as an IGBT with the MOSFET1 conducting the electron current. The current flow lines of the DMGT structure A in the IGBT mode operation are shown in Fig. 5.3.

In the DMGT structure A, the same P base region is involved with both the thyristor and IGBT mode operations. This makes the base optimization more difficult due to the conflicting requirements on the P base parameters by the two operation modes: the high J_{mcc} in the IGBT mode requires a short P base with low sheet resistance, while the low forward voltage drop in the thyristor mode prefers a long P base with a high sheet resistance. The DMGT structure B [3], whose cross-section view is shown in Fig. 5.4, separates the IGBT region from the main thyristor

region. The operation principle of the DMGT structure B is similar to that of the DMGT structure A.

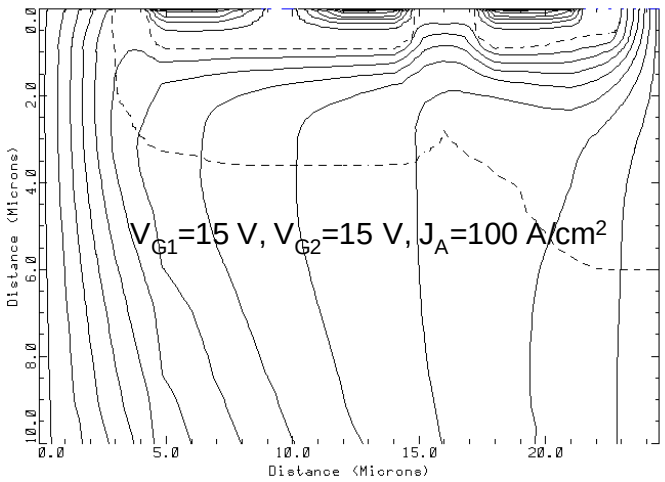

Fig. 5.3 Current flow lines of the DMGT structure A in the IGBT mode.

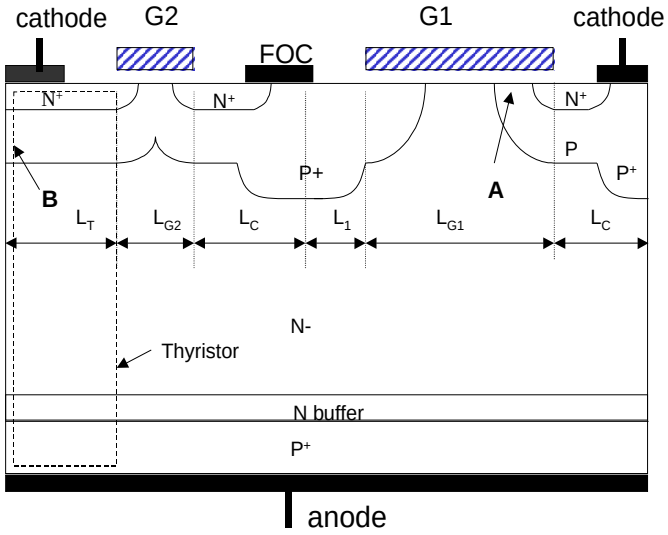

Fig. 5.4 Cross-section view of the DMGT structure B.

The DMGT structures A and B are the two basic structures for the DMGT devices. A detailed review of the literature will find that most of the others reported DMGT structures were built by using either one or a combination of these two structures as the building block. Therefore, these two basic structures set the fundamental limitation on the J_{mcc} of the reported DMGT structures. For the sake of simplicity, only these two basic DMGT structures will be analyzed.

DMGT structure C is the proposed DMGT structure with a higher J_{mcc} capability than the DMGT structures A and B. Similar to structure B, the DMGT structure C also has a separated IGBT region. What distinguishes it from DMGT structure B is that the main thyristor region of the DMGT structure C is also isolated from the parasitic thyristor region. Fig. 5.5 shows the cross-section view of the DMGT structure C. The operation principle of the DMGT structure is also similar to those of the DMGT structures A and B.

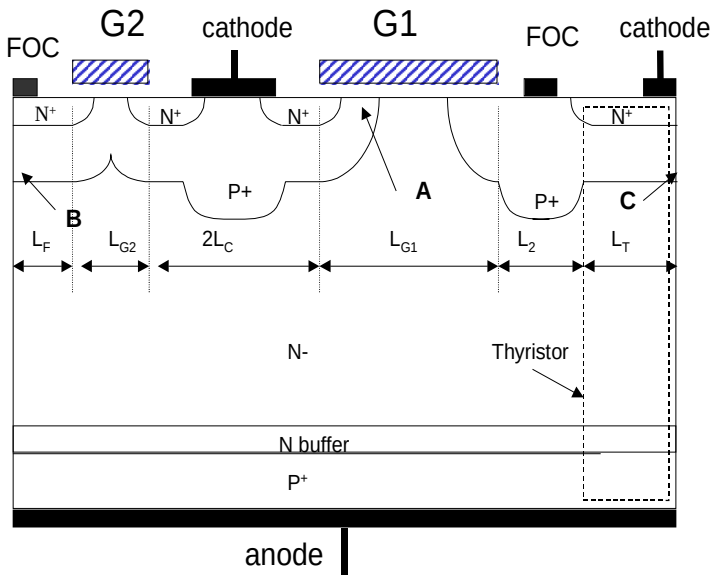

Fig. 5.5 Cross-section view of the proposed DMGT structure C.

5.3 Simulation Results

The drift region of the simulated DMGTs have a doping concentration of 1×10^{14} cm^{-3} and a thickness of 50 μm. The N buffer layer has a doping of 1×10^{17} cm^{-3} and a thickness of 10 μm. These values were chosen to achieve a forward blocking capability of 600 V. The P base diffusion has a junction depth of 3.6 μm and a surface concentration of 4×10^{17} cm^{-3}. The N+ emitter has a junction depth of 1 μm and a surface concentration of 1×10^{20} cm^{-3}. The gate oxide is 500 Å thick. Another deep P+ diffusion is used for implementing the P base contact. The doping profile and the geometrical dimensions of the DMGT structures are listed in Table 5.1. In this section, two-dimensional numerical simulation results using MEDICI [10] are used to verify the operation of the DMGT in the two operation modes, and to compare them to the IGBT with the same process parameters and critical dimensions. A high injection level carrier lifetime of 8 μs is assumed in the simulations.

When a positive 15 V is applied to the gate electrode of MOSFET1 while the MOSFET2 gate is grounded, the DMGTs are operated in the thyristor mode. The simulated on-state characteristics of the DMGTs in the thyristor mode and their comparison with those of the IGBT are shown in Fig. 5.6. As expected, the on-state voltage drops of the DMGTs are much lower than those of the IGBT. The on-state voltage drop of the DMGT structure A is slightly lower than those of DMGT structures B and C due to its smaller cell pitch. The on-state voltage drops of DMGT structures A, B, and C, and of the IGBT at a forward current density of 100 A/cm^2 are 0.87 V, 0.91 V, 0.91 V, and 1.07 V, respectively.

Table 5.1 Doping profile and geometrical dimensions used in the simulation of the DMGT.

N- epitaxy thickness	50 μm
N- epitaxy doping	1×10^{14} cm^{-3}
N buffer thickness	10 μm
N buffer doping	1×10^{17} cm^{-3}
P+ substrate thickness	3 μm
P+ substrate doping	5×10^{19} cm^{-3}
P base junction depth	3.6 μm
P base doping	4×10^{17} cm^{-3}
P+ junction depth	6 μm
P+ doping	1×10^{19} cm^{-3}
N+ emitter junction depth	1 μm
N+ emitter doping	1×10^{20} cm^{-3}
MOSFET1 gate width L_{G1}	10 μm
MOSFET2 gate width L_{G2}	4 μm
L_C	6.5 μm
L_1	2.5 μm
L_2	13.5 μm
L_F	4.5 μm
L_T	4.5 um

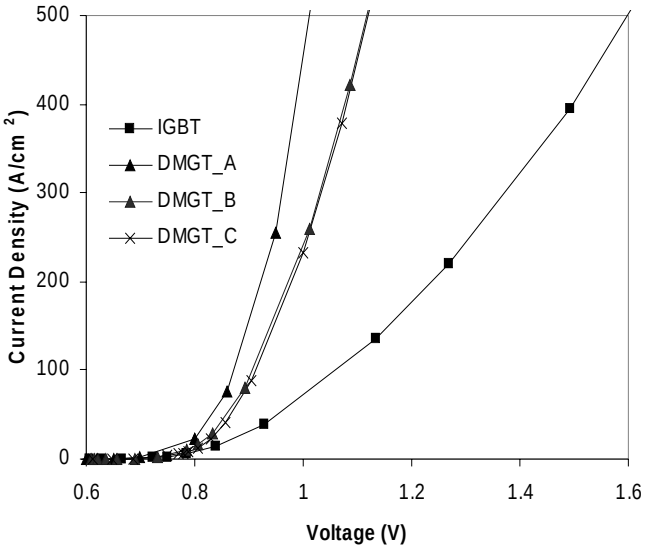

Fig. 5.6 Simulated on-state characteristics of the DMGTs in the thyristor mode

When the gate electrodes of both the MOSFET1 and MOSFET2 are positively biased to 15 V, the DMGTs are operated in the IGBT mode. The output characteristics of the DMGT in the IGBT mode are shown in Fig. 5.7. The maximum controllable current densities (J_{mcc}) of the DMGT structures A, B and C in the IGBT mode are 140 A/cm^2, 680 A/cm^2, and 800 A/cm^2, respectively. The DMGT structure C has the highest J_{mcc}, while the J_{mcc} of the DMGT structure A is significantly lower than those of the other two.

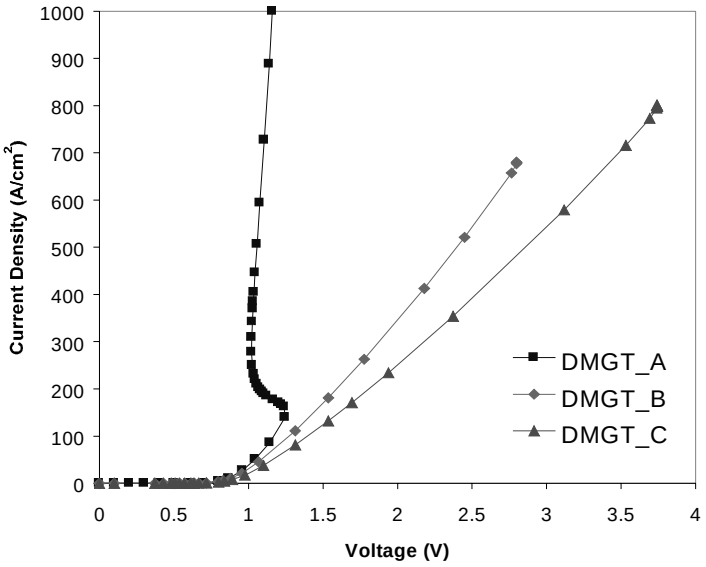

Fig. 5.7 Simulated output characteristics of the DMGTs in the IGBT mode.

In the next section, a first-order analytic model is developed to characterize the J_{mcc} of the DMGT structures in the IGBT operation mode.

5.4 The J_{mcc} Model

One assumption of the J_{mcc} model is that the hole current flowing upward is uniform at the N- drift/P base junctions of the DMGT devices. This assumption is justified by examining Fig. 5.8, which shows the hole current vector of the DMGT structure A in the IGBT mode operation. The hole current density (J_H) at the N- drift/P base junctions is

$$J_H = \alpha_{PNP} J_A \tag{5.1}$$

where J_A is the anode current density and α_{PNP} is the gain of the lower PNP transistor of the DMGT devices.

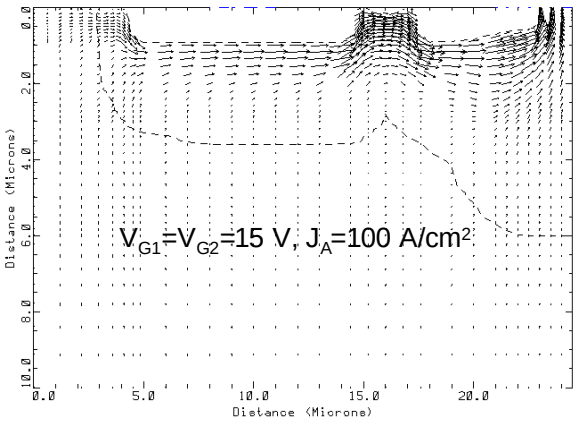

Fig. 5.8 Hole current vectors in the IGBT mode of the DMGT structure A.

The DMGT structure A is subdivided into the regions shown in Fig. 5.1. The main thyristor may be assumed to start to latch when a potential difference of 0.7 V is established at the P base/N+ emitter junction at point A, which has the highest voltage drop across the junction. The potential drop at point A with respect to the FOC due to the hole current flow is given by

$$v_A = \alpha_{PNP} J_A \left(\int_0^{\frac{L_{G1}}{2}} \rho_{SP}\, x\,dx + \int_{\frac{L_{G1}}{2}}^{\frac{L_{G1}}{2}+2L_T} \rho_B\, x\,dx \right.$$

$$\left. + \int_{\frac{L_{G1}}{2}+2L_T}^{\frac{L_{G1}}{2}+2L_T+L_{G2}} \rho_{G2}\, x\,dx + \int_{\frac{L_{G1}}{2}+2L_T+L_{G2}}^{\frac{L_{G1}}{2}+2L_T+L_{G2}+L_C} \rho_W\, x\,dx \right) \qquad (5.2)$$

where ρ_{SP}, ρ_B, ρ_{G2}, and ρ_W are the sheet resistance of the P base spreading resistance region, the sheet resistance of the P base, the sheet resistance of the merged P base region beneath the lateral polysilicon gate G_2, and the sheet resistance of the P base near the deep P+ region, respectively.

Since the use of the deep P+ diffusion makes the ρ_W relatively small compared with the other terms, and the dimension L_C is always designed as small as possible, the last term in Eq. 5.2 can be dropped in the approximation. Upon integration, Eq. 5.2 yields

$$v_A = \frac{\alpha_{PNP} J_A}{2}\left[\frac{\rho_{SP}}{4} L_{G1}^{\ 2} + \rho_B (4L_T^{\ 2} + 2L_T L_{G1}) + \rho_{G2}(L_{G2}^{\ 2} + L_{G1}L_{G2} + 4L_T L_{G2})\right] \tag{5.3}$$

Since the resistivity of the N+ emitter is small, the horizontal resistive drop in the N+ emitter can be ignored. The electron current flowing through the MOSFET2 is equal to the hole current collected at the FOC. Assuming the MOSFET2 is operated in the linear region, the potential at the FOC is given by

$$v_{FOC} = \frac{\alpha_{PNP} J_A \left(\frac{L_{G1}}{2} + 2L_T + L_{G2} + L_C\right) L_{ch2}}{\mu_{inv2} C_{ox} (V_{G2} - V_{th2})} \tag{5.4}$$

where μ_{inv2} is the electron inversion layer mobility at the lateral MOSFET2, C_{ox} is the gate oxide capacitance per unit area, and V_{th2} is the threshold voltage of the lateral MOSFET2. The maximum controllable current density of the DMGT structure A in the IGBT mode is the latching current density at which $V_A + V_{FOC} = 0.7$ V. From this condition, it follows that

$$J_{mcc} = \frac{0.7}{\alpha_{PNP}\left[\frac{\rho_{SP}}{8} L_{G1}^{\ 2} + \rho_B (2L_T^{\ 2} + L_T L_{G1}) + \frac{\rho_{G2}}{2}(L_{G2}^{\ 2} + L_{G1}L_{G2} + 4L_T L_{G2}) + \frac{\left(\frac{L_{G1}}{2} + 2L_T + L_{G2} + L_C\right) L_{ch2}}{\mu_{inv2} C_{ox} (V_{G2} - V_{th2})}\right]} \tag{5.5}$$

The J_{mcc} of the simulated DMGT structure A in the IGBT mode operation is only 140 A/cm^2. According to Eq. 5.5, there are two factors that account for the low J_L in this structure. One factor is the high ρ_{SP} for the spreading resistance region right under the channel of MOSFET1 where the electrons flow into the N- drift region. A considerable amount of hole current is collected in this region to meet the charge neutrality requirement. The other factor is the fact that holes collected at point A on the left edge of the device cell have to travel across the long P base ($2L_T$) to the cathode contact on the right edge of the device. The current flow lines in the DMGT structure A when the device starts to latch in the IGBT mode are shown in Fig. 5.9. It is clearly shown that the latching initializes at point A in the DMGT structure A.

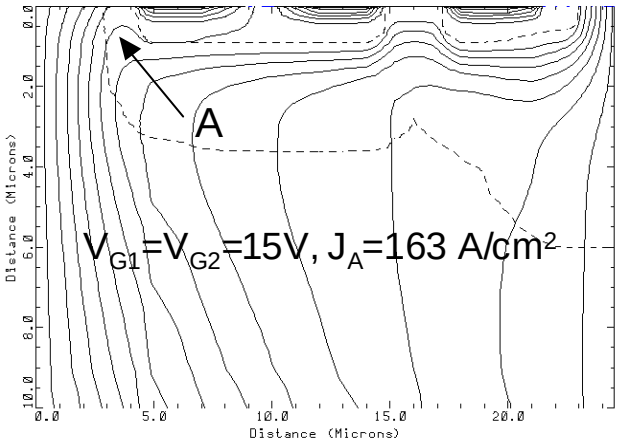

Fig. 5.9 Current flow lines of the DMGT structure A when the device starts to latch in the IGBT mode.

For the DMGT structure B shown in Fig. 5.2, the thyristor may latch at either point A or point B. The potential at point A due to the hole current flow is given by

$$v_A = \alpha_{PNP} J_A \left(\int_0^{\frac{L_{G1}}{2}} \rho_{SP} x dx + \int_{\frac{L_{G1}}{2}}^{\frac{L_{G1}}{2}+L_C} \rho_w x dx \right) \tag{5.6}$$

Therefore, the current density under which the device latches at point A is given by

$$J_L = \frac{0.7}{\alpha_{PNP} \left[\frac{\rho_{SP}}{8} L_{G1}^2 + \frac{\rho_W}{2} \left(L_C^2 + L_C L_{G1} \right) \right]} \tag{5.7}$$

On the other hand, the potential drop at point B with respect to the FOC due to the hole current flow is given by

$$v_B = \alpha_{PNP} J_A \left(\int_0^{L_T} \rho_B x dx + \int_{L_T}^{L_T+L_{G2}} \rho_{G2} x dx + \right.$$
$$\left. + \int_{L_T+L_{G2}}^{L_T+L_{G2}+L_C} \rho_W x dx \right) \tag{5.8}$$

Assuming the MOSFET2 is operated in the linear region, the potential at the FOC of the DMGT structure B is given by

$$v_{FOC} = \frac{\alpha_{PNP} J_A \left(L_T + L_{G2} + L_C + L_1 + \frac{L_{G1}}{2} \right) L_{ch2}}{\mu_{inv2} C_{ox} \left(V_{G2} - V_{th2} \right)} \tag{5.9}$$

Neglecting the last term in Eq. 5.8, the latching current density J_L at which $V_B + V_{FOC} = 0.7$ V at point B in the DMGT structure B is

$$J_L = \frac{0.7}{\alpha_{PNP}[\frac{\rho_B}{2} L_T{}^2 + \frac{\rho_{G2}}{2}(L_{G2}{}^2 + 2L_T L_{G2}) + \frac{(L_T + L_{G2} + L_C + L_1 + \frac{L_{G1}}{2})L_{ch2}}{\mu_{inv} C_{ox}(V_{G2} - V_{th2})}]} \qquad (5.10)$$

The maximum controllable current density of the DMGT structure B in the IGBT mode is determined by the lower J_L value in Eq. 5.7 and Eq. 5.10. Compared with Eq. 5.5, the denominator in Eq. 5.7 does not have the ρ_B term from the long P base, the ρ_{G2} term from the merged region under the MOSFET 2 gate, or the FOC voltage term, while the denominator in Eq. 5.10 does not have the ρ_{SP} term from the spreading resistance region. Therefore, the maximum controllable current density of the DMGT structure B in the IGBT mode is higher than that of the DMGT structure A. In the simulated DMGT structure B, the latching initializes at point B in the IGBT mode as indicated by the current flow lines shown in Fig. 5.10. It should be pointed out that the J_L given in Eq. 5.7 is essentially the latching current density for the IGBT with the same process parameters and critical dimensions.

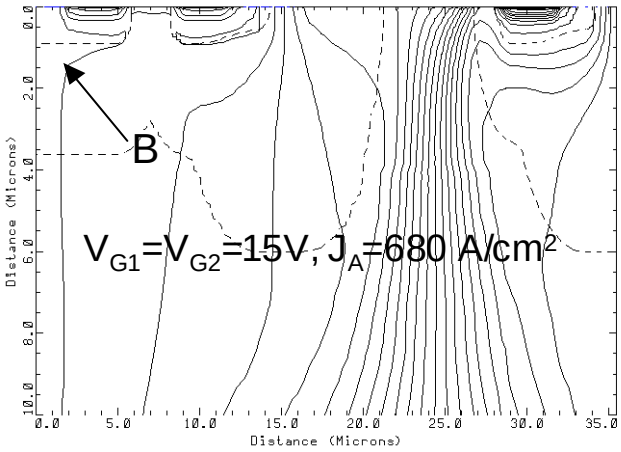

Fig. 5.10 Current flow lines of the DMGT structure B when the device starts to latch in the IGBT mode.

The case is a little more complicated in the DMGT structure C. In this structure, whose cross-section is shown in Fig. 5.3, there are three possible positions where the device may start to latch. Those three positions are labeled as point A, point B and point C in the figure.

The current density and process at which the device starts to latch at point A is identical to those at point A in the DMGT structure B. As previously pointed out, it is essentially the latching current density for the IGBT with the same process parameters and critical dimensions. The J_L has been given in Eq. 5.7.

Again, assuming the MOSFET2 is operated in the linear region, the potential at the FOC of the DMGT structure C is

$$v_{FOC} = \frac{\alpha_{PNP} J_A (L_T + L_2 + \frac{L_{G1}}{2}) L_{ch2}}{\mu_{inv2} C_{ox} (V_{G2} - V_{th2})} \tag{5.11}$$

The potential at point B due to the hole current flow can be obtained as

$$v_B = \alpha_{PNP} J_A (\int_0^{L_F} \rho_B x dx + \int_{L_F}^{L_F+L_{G2}} \rho_{G2} x dx + \int_{L_F+L_{G2}}^{L_F+L_{G2}+L_C} \rho_W x dx) \tag{5.12}$$

The latching current density J_L at point B is the anode current density at which V_B-V_{FOC}=0.7 V. From this condition, and ignoring the last term in Eq. 5.12, we get

$$J_L = \frac{0.7}{\alpha_{PNP}[\frac{\rho_B}{2} L_F^2 + \frac{\rho_{G2}}{2}(L_{G2}^2 + 2L_F L_{G2}) - \frac{(L_T + L_2 + \frac{L_{G1}}{2}) L_{ch2}}{\mu_{inv} C_{ox} (V_{G2} - V_{th2})}]} \tag{5.13}$$

The potential drop at point C with respect to the FOC due to the hole current flow is given by

$$v_C = \alpha_{PNP} J_A \left(\int_0^{L_T} \rho_B x \, dx \right. \tag{5.14}$$

The latching current density J_L at point C is the anode current density at which $V_C+V_{FOC}=0.7$ V, and is given by

$$J_L = \frac{0.7}{\alpha_{PNP}\left[\frac{\rho_B}{2} L_T^{\,2} + \frac{(L_T + L_2 + \frac{L_{G1}}{2}) L_{ch2}}{\mu_{inv} C_{ox} (V_{G2} - V_{th2})}\right]} \tag{5.15}$$

The maximum controllable current density of the DMGT structure C in the IGBT mode is determined by the lowest J_L value in Eq. 5.7, Eq. 5.13 and Eq. 5.15. Compared with Eq. 5.10, the FOC voltage in Eq. 5.13 is subtracted from instead of being added to the sum of the voltage drops across different P regions. This is a unique feature of the DMGT structure C. The FOC potential built up in shunting the holes current actually prevents the latch-up happening at point B. As far as the J_L value in Eq. 5.15 is concerned, it is obvious that it is much higher than that given in Eq. 5.10. In conclusion, the maximum controllable current density of the DMGT structure C in the IGBT mode is by no means lower than that for the DMGT structure B. In the simulated DMGT structure C, the J_L given by Eq. 5.7 has the lowest value among those in Eq. 5.7, Eq. 5.13 and Eq. 5.15; therefore, the thyristor latching initializes at point A in the IGBT mode as indicated by the current flow lines shown in Fig. 5.11.

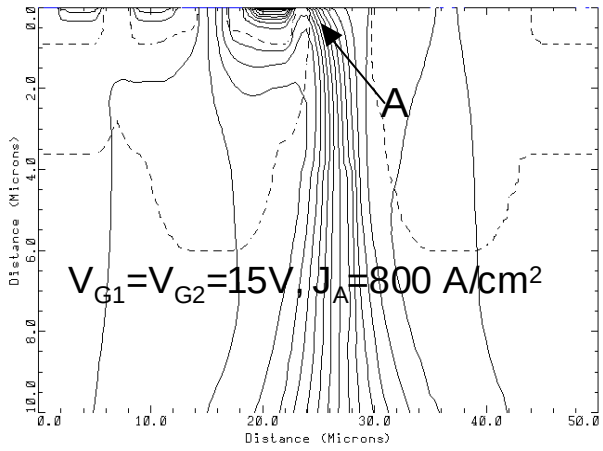

Fig. 5.11 Current flow lines of the DMGT structure C when the device starts to latch in the IGBT mode.

5.5 Experimental Results

DMGT devices with 600 V forward blocking capability were fabricated using <100> oriented P+ substrate wafers with a 60 μm thick, 45 ohm-cm N- epitaxial layers as the starting material. An IGBT-like process with eight masking levels was used for the fabrication of the DMGT devices. The key process steps and the highlights of the integrated DMOS process flow is as follows [11].

(1) Field oxidation
(2) Active area patterning and etch (Mask 1)
(3) JFET implantation (Mask 2)
(4) Gate oxidation
(5) Poly-silicon deposition, doping and patterning (Mask 3)
(6) P+ implantation and diffusion (Mask 4)

(7) P base implantation and diffusion (Mask 5)

(8) N+ implantation and diffusion (Mask 6)

(9) Inter-level oxide deposition

(10) Contact hole patterning (Mask 7)

(11) Metal deposition and patterning (Mask 8)

A stripe layout approach was adopted for convenience in placing the two separated gates. Each device consisted of several unit cells operating in parallel. The device cells were laid out within a 500 μm × 500 μm area, surrounded by the device termination region consisting of floating rings with field plates. The pads, which were about 100 μm × 100 μm in size, were placed in the centers of the devices. The active area of the devices was about 0.13 mm^2. Fig. 5.12 shows a photomicrograph of the DMGT structure C device fabricated.

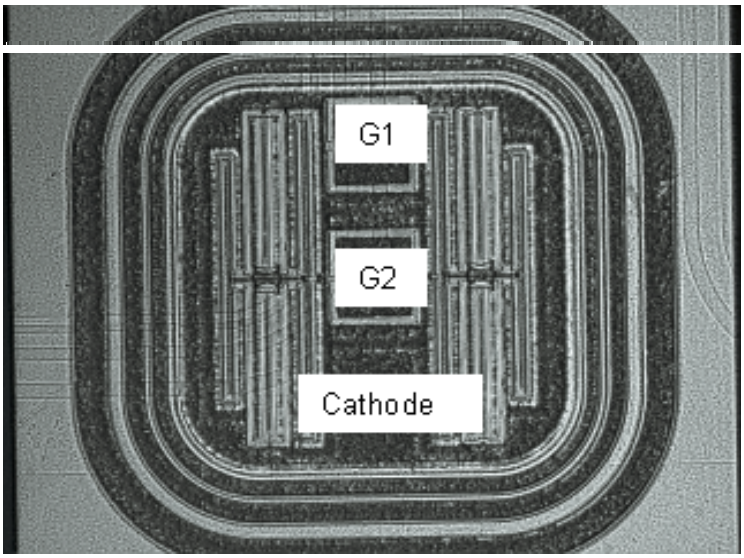

Fig. 5.12 Photomicrograph of the fabricated DMGT structure C.

The typical measured output characteristics of the DMGT structure A in the IGBT mode operation with varied gate bias for the MOSFET1 are shown in Fig. 5.13. The J_{mcc} of the DMGT structure A in the IGBT mode operation (under $V_{G1}=V_{G2}=15$ V) was about 160 mA (123 A/cm^2). The main reason that the device showed a very high forward voltage drop in the IGBT mode operation was due to the high JFET resistance. The junction depth of the P base of the fabricated devices was found to be 4.6 μm instead of the designed 3.6 μm. The over drive-in of the P base generated a very strong JFET effect, when considering that the MOSFET1 had a gate length (L_{G1}) of only 10 μm. Besides the JFET effect, the ill-controlled high threshold voltage (V_{th}= 7 V) and extremely low measured carrier lifetime also contributed to the abnormal high forward voltage drop [11].

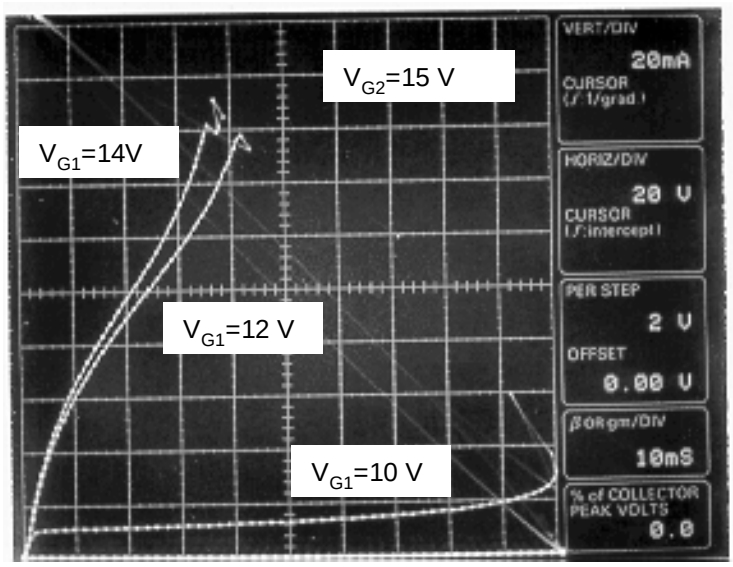

Fig. 5.13 Experimental output characteristics of the DMGT structure A in the IGBT mode.

The measured J_{mcc} of the DMGT structures B and were 250 mA (192 A/cm^2) and 300 mA (231 A/cm^2), respectively. The DMGT structure C not only had the highest J_{mcc}, but also had the widest FBSOA. Fig. 5.14 shows the output characteristics of the DMGT structures A and C in the IGBT mode operation with the lower gate voltage (V_{G1}=10 V). While the DMGT structure A started to latch at 200 V, the DMGT structure C could sustained a forward voltage of over 400 V. The higher voltage sustaining capability of the DMGT structure C was also attributed to the higher J_{mcc} capability of the device. The J_{mcc} of the DMGT device generally decreases with the increase of the forward blocking voltage for two reasons: one reason was the increase of the hole current due to the higher current gain of the lower PNP transistor at higher voltage; the other reason was the increase of the P base pinch resistance as a result of the depletion expansion.

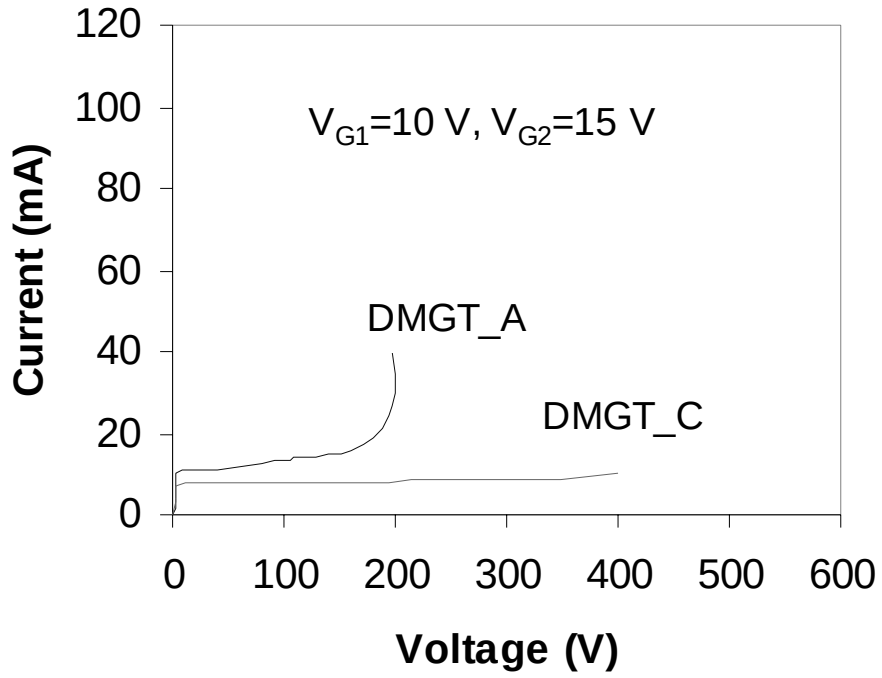

Fig. 5.14 Experimental output characteristics of the DMGT structures A and C in the IGBT mode with lower gate voltage.

It should to be pointed out that the measured J_{mcc} of the base-line IGBT fabricated on the same process run was above 350 mA (270 A/cm^2), higher than that of the DMGT structure C. The reason for this is that the assumption of the uniform hole current distribution was not strictly true, particularly in the JFET region of the MOSFET1, where enhanced hole concentration was observed due to the existence of a high concentration of electron current. This tended to reduce the normalized anode latching current density for the DMGT structures with large cell pitches, such as the DMGT structures B and C.

5.6 Conclusion

In this chapter, the dual operation mode MOS-gated thyristor (DMGT) devices that are compatible with the IGBT process were analyzed with the aid of two-dimensional numerical simulations and first-order analytic models developed to characterize the maximum controllable current density (J_{mcc}) in the IGBT mode operation. A new device structure was proposed and compared with two previously reported basic DMGT structures. It was experimentally demonstrated that the novel DMGT structure has a higher J_{mcc} capability than the previously reported DMGT structures.

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Chapter 6 Background and Analysis of the TBJD

6.1 Introduction

In power electronics applications, there has been a continuous trend toward higher operating frequency, especially in switch mode power supplies. In switch mode power supplies, operation at higher frequencies is attractive because of the reduction in size and power loss in the passive components, which leads to a more efficient, compact system design. To accomplish higher frequency operation in power electronics circuits, it is essential to use power devices with improved switching performance.

Since the introduction of modern power switches, such as the Insulated Gate Bipolar Transistor (IGBT) and MOS-Gated Thyristor (MGT) devices, diodes in many applications are subjected to higher voltage and current levels, and are required to switch at higher speeds and frequencies. Under these conditions, power diodes with low forward voltage drop, low leakage current, low peak reverse recovery current and low reverse recovery charge are needed in order to decrease the overall power loss in the power electronics circuits.

In high-voltage power electronics applications, the P-i-N diodes still dominate due to their low forward voltage drop and reverse leakage current. However, the conventional P-i-N diode suffers from poor dynamic characteristics due to the large amount of charge stored in the lightly doped i-region during forward conduction. On the other hand, the Schottky diode has been limited to low-voltage applications because of its high leakage current and soft breakdown. A high-voltage power diode with improved static and dynamic characteristics to match the

performance of the modern power switches is essential in high-voltage power electronics applications.

In this chapter, the development of high-voltage power diodes is reviewed to set the stage for the introduction of the Trench Bipolar Junction Diode (TBJD), a novel high-voltage power diode concept with superior static and dynamic characteristics.

6.2 Review of Power Diode Development

The P-i-N diode is the structure generally used in the high-voltage power applications. A cross section of the conventional P-i-N diode is shown in Fig. 6.1 [1]. The i-region refers to the lightly doped N- drift region used to support the high voltage. In this device, the i-region is flooded with minority carriers during forward conduction. As a result, the resistance of the i-region is significantly lowered during current flow, allowing this diode to carry a high current density during forward conduction. For this reason, it has been possible to develop P-i-N diodes with long and lightly doped N- drift regions for very high breakdown voltage. However, the injection of a high concentration of carriers into the i-region also creates problems during switching of the P-i-N diodes.

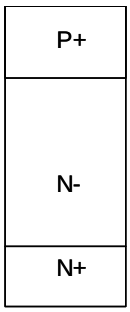
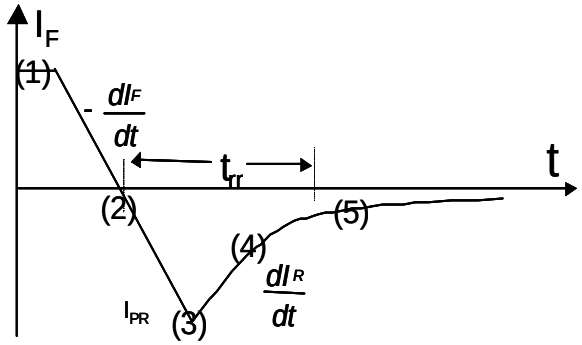


Fig. 6.1 Cross-section view of the P-i-N diode.

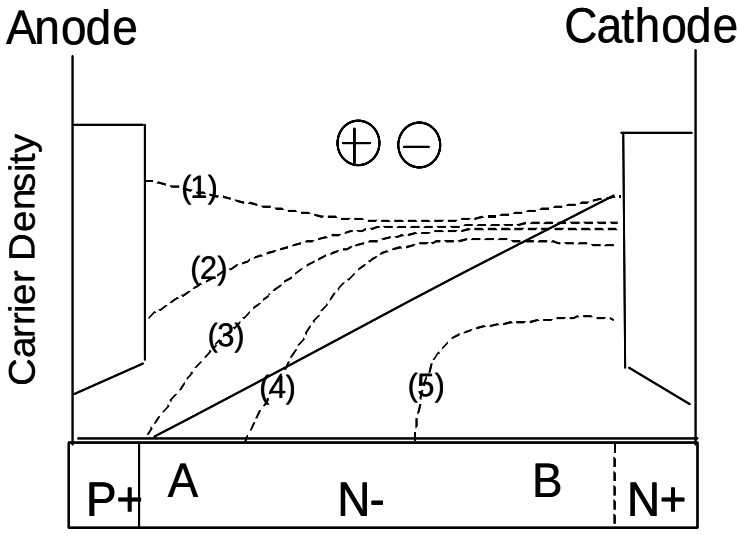
The major drawback of the P-i-N diode is its poor reverse recovery characteristics. Reverse recovery is the process whereby the diode is switched from its forward conduction state to its reverse blocking state. Fig. 6.2 illustrates the reverse recovery current waveform of a P-i-N diode and the instant minority carrier profile in the i-region during the reverse recovery phase. During the forward conducting state, carriers are injected into the N- region from both the P+/N- and N-/N+ junctions, and the carrier concentration is the highest at both junctions, with the minimum concentration closer to the cathode side due to the difference in the mobility of electrons and holes [1]. To undergo the reverse recovery transition, the minority carriers stored in the i-region during the forward conducting state must be removed before the i-region can support the reverse blocking voltage. More specifically, the carriers stored near the anode side need to be removed before the diode can sustain any reverse voltage, since it is the P+/N- junction that blocks the reverse voltage. Considering the fact that carrier concentration is the highest at the anode junction of the P-i-N diode, the P-i-N diode has a long reverse recovery time and high peak reverse recovery current.

6.2.1 Lifetime Controlling Techniques

The most popular approach used to improve the switching characteristics of a P-i-N diode is carried out by introducing recombination centers in the i-region and controlling the minority carrier lifetime value. By reducing the minority carrier lifetime value, the carriers stored in the i-region can be reduced effectively, resulting in a reduced reverse recovery time and charge. However, this has always been accompanied by an increase in both the reverse leakage current and forward voltage drop [2]. The lifetime killing methods include introducing recombination centers by either the diffusion of gold or platinum, or by electron or gamma irradiation. These methods have different influences on the diode characteristics. The lifetime control through gold diffusion has a better outcome for the static and dynamic characteristics but introduces high levels of leakage current, while irradiation techniques have shown snappy recovery behavior.



(a)



(b)

Fig. 6.2 Reverse recovery of the P-i-N diode: (a) current waveform, and (b) instant minority carrier profile during the reverse recovery phase.

The snappy recovery of the diode causes stress elsewhere within the system. Protective snubber circuits are used to allow a softer recovery for the diode by providing an additional current path to limit the slop of the reverse recovery. However, these circuits are costly and bulky. Finding a practical solution to this problem through diode structure design is an important and necessary objective.

The reduction of the stored charge can also be achieved by controlling the anode P+ or the cathode N+ emitter injection. Porst et al. [3] studied how the amount of charge and the shape of the carrier distribution in the i-region influence the static and dynamic behaviors of a P-i-N diode, and experimentally demonstrated that reducing either the P+ or the N+ emitter injection helps reduce the reverse recovery charge; however, while the former achieves an overall improved performance, the latter results in a snappy reverse recovery. This study is consistent with the dynamics of diode reverse recovery. In a P-i-N diode, it is the P+/N- junction that sustains the reverse voltage; therefore, reducing the amount of charge stored in this region facilitates the junction recovery process and helps reduce the peak reverse recovery current. Just as a lower P+ emitter injection does, reducing the N+ injection reduces the reverse recovery charge by decreasing the total amount of charge stored in the i-region during the forward conducting state. However, when the depletion region reaches the N-/N+ junction, the sudden disappearance of the stored charge near the N+ emitter causes the reverse current chop-off (extremely high di/dt) and results in a snappy reverse recovery.

6.2.2 Cathode Engineering Techniques

Some diode structures, such as the N-buffer layer diode [4], the hybrid diode [5], and the Emitter-Controlled-Punch-Through (ECPT) diode [6], have been reported to prevent the diode reverse recovery current from snapping because of the sudden disappearance of the minority carriers stored in the i-region. Fig. 6.3 shows the cross-section views of these diodes as well as the above mentioned P-i-N diode structure. The main difference between these three diodes is in the cathode portions of the device structures. The common feature of these diode structures is

that each softens the reverse recovery by providing some extra residue charge in the i-region near the N+ emitter when the depletion region reaches the N-/N+ junction.

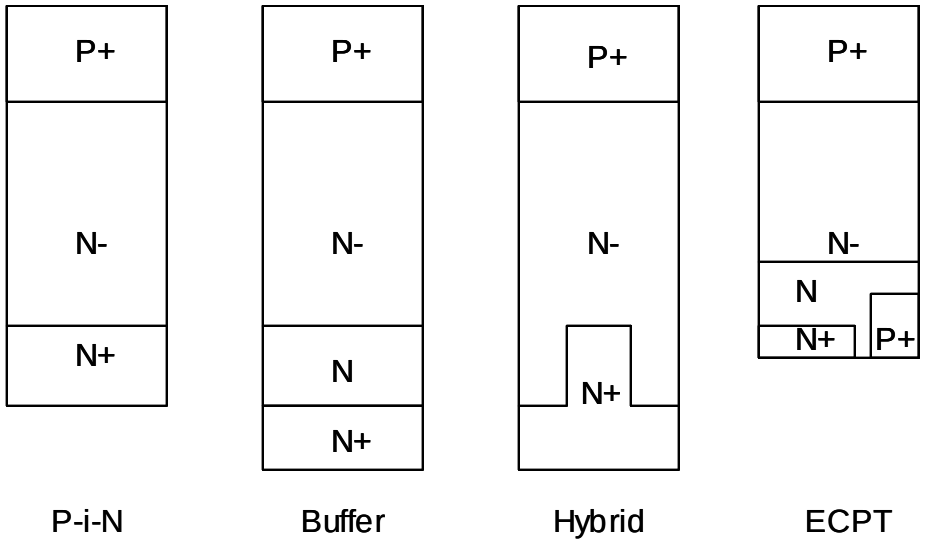


Fig. 6.3 Cross-section views of the diode structures using cathode engineering techniques.

In the N-buffer layer diode, this is accomplished by introducing an N buffer layer between the i-region and the N+ emitter. The doping level of the N buffer layer must be high enough to prevent the depletion layer from reaching the N/N+ junction, yet low enough to allow conductivity modulation to provide some extra residue charge. Since the buffer layer increases the total thickness of the drift region, the forward voltage drop of the buffer layer diode is higher than that of the conventional P-i-N diode.

The hybrid diode concept is based on splitting the diode into two sections, which have different drift region thicknesses. The section with the shorter drift region is designed to be just sufficient for the desired voltage capability, while the section with longer drift region provides an extra residue charge to soften the reverse recovery. In the hybrid diode, the main portion of

forward current flows through the section with shorter drift region; therefore only a slightly increase of the forward voltage drop has been observed.

Unlike the previous two approaches, which provide an additional reservoir of stored charge to avoid a sudden interruption of current, the ECPT diode uses an alternative method. In the ECPT, in addition to the N+ emitter being diffused into the N buffer layer, a small and deeper P+ region is also diffused into the N buffer layer. Since the P+ emitter is shorted to the N buffer layer through the cathode contact, the cathode P+/N junction stays inactive until the N buffer layer under the cathode P+ emitter region is depleted during the reverse recovery. After that happens, the P+ emitter will inject some holes into the i-region to provide the extra charge needed for a soft reverse recovery.

Although all three of these diode structures soften the reverse recovery, they accomplish this by introducing some extra carriers into the i-region. Therefore, the total amount of charge stored in the i-region increases. As a consequence, the peak reverse recovery current and reverse recovery charge of these diodes will be even higher than those of the conventional P-i-N diode, and an overall improvement in the switching performances has not yet been realized by any of these diode structures.

6.2.3 Anode Engineering Techniques

Most diode developments have been focused on improving the overall performance by controlling the anode P+ emitter injection. The cross-section views of those different diode structures are shown in Fig. 6.4. Compared with the conventional P-i-N diode structure, those diodes differ in the anode portion of the device structure. The common goal of these diode structures is to reduce the carrier concentration near the anode side of the i-region during the forward conducting state.

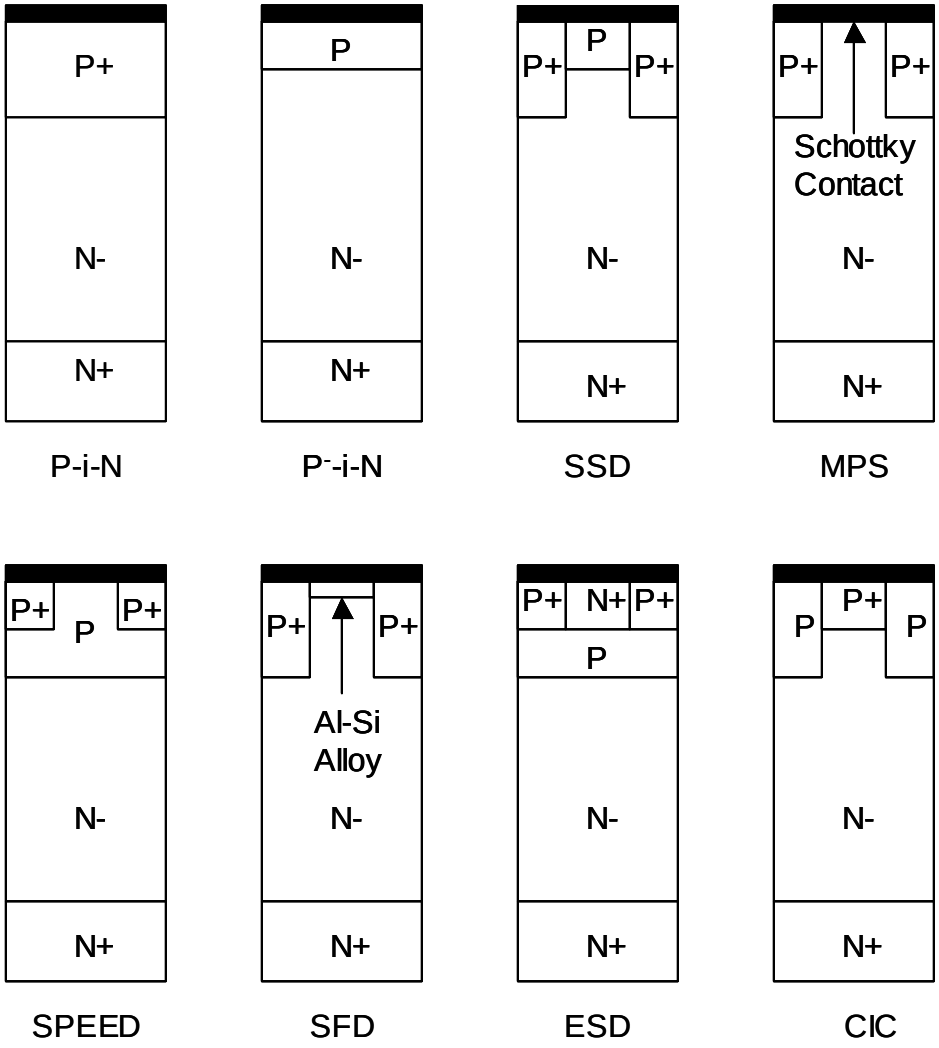


Fig. 6.4 Cross-section views of the diode structures using anode engineering techniques.

Reducing the P+ emitter injection decreases the carrier concentration in the i-region near the P+ emitter. It not only results in a reduced stored charge, but also produces a softer reverse recovery because the P+/N- junction becomes reverse biased earlier during the reverse recovery process. The reverse recovery process of the power diodes involves sweeping out the carriers from both the anode P+/N- and cathode N-/N+ junction. Because of the unequal electron and hole mobility, the carriers at the anode side are swept out more slowly than those in the cathode

side [7]. Since a lower carrier concentration near the P+ emitter promotes an earlier recovery of the P+/N- junction, more stored charge is removed by the recombination process, which results in a softer reverse recovery.

The P^--i-N diode reported in 1976 used a shallow P emitter with low doping to reduce the anode injection [8]. Although it was reported that this diode has a low forward voltage drop, this is only true at very low current densities and high lifetime value [2]. Due to the very poor conductivity modulation in the drift region, the forward voltage drop of this diode is considerable higher than that of the conventional P-i-N diode at and beyond normal operating current densities. In addition, the punch-through effect on the shallow P emitter limits the reverse voltage blocking capability of the P^--i-N diode.

The Static Shielding Diode (SSD) reported in 1984 aimed to solve the low blocking voltage problem of the P^--i-N diode by surrounding the shallow and lightly doped P emitter (called a channel) with a deep and heavily doped P+ layer [9]. When reverse voltage is applied to a SSD, the N- region between the deep P+ regions will be pinched off by the depletion region and will serve as a potential barrier to prevent the shallow P emitter from punching through.

The Merged P-i-N Schottky Diode (MPS) reported in 1987 replaced the shallow and lightly doped P emitter of the SSD with a Schottky contact formed between the anode electrode and the N- region [10]. The deep and heavily doped P+ emitter of the MPS keeps the forward voltage drop low by injecting some minority carriers into the i-region, while the Schottky contact of the MPS controls the minority injection and helps it to achieve a faster switching speed [11]. As in the SSD, the P+ emitter also serves to lower the electric field applied at the Schottky, which improves the reverse blocking characteristics of the MPS. Nevertheless, the major drawback of the MPS diode is still its large leakage current at elevated temperature, which is intrinsic in a Schottky junction. This limits the high-temperature performance of the MPS diode.

The Self Adjusting P-Emitter Efficiency Diode (SPEED) reported in 1989 consists of a deep and lightly doped P emitter with low injection efficiency, and a shallow and highly doped P+ region, which provides high injection efficiency at high current densities to reduce the forward voltage drop [12]. However, not much improvement has been observed in this diode [7].

The Soft and Fast Diode (SFD) reported in 1991 has a similar structure to the SSD except that the thin P layer is formed by an aluminum alloy [13]. The performance of the SFD is similar to that of the SSD.

The Emitter Short Diode (ESD) was reported in 1992 [14]. The N+ and P+ regions are formed at the surface of a P emitter to reduce the anode injection efficiency. However, the doping of the thin P layer under the N+ short region is limited by the punch-through effect, which limits the structure's reverse blocking capability. Furthermore, the ESD is subject to a parasitic transistor effect.

The Charge Injection Control (CIC) concept for fast recovery was reported in 1993 [15]. In the CIC diode, the shallow and highly doped P+ region and the deep and lightly doped P region are arranged in an inter-digitized fashion. Reduction of the anode injection efficiency is achieved by designing the highly doped P+ portion of the emitter to have a very shallow junction.

Although the diode structures that use anode engineering techniques have shown better reverse recovery characteristics than the conventional P-i-N diode, they also have either a much higher forward voltage drop, a lower reverse blocking voltage or a higher leakage current [2,7].

6.3 TBJD Structure and Operation

In this section, a new high-voltage power diode structure, called the Trench Bipolar Junction Diode (TBJD), is proposed and analyzed with the aid of two-dimensional numerical simulations [16,17]. For the first time, the feasibility of controlling the anode injection efficiency while maintaining a low on-state voltage drop of a P-i-N diode by the action of an integrated reverse active transistor (RAT) is demonstrated. With the base of the RAT effectively shielded by a pair of deep P+ poly-Si trenches, the TBJD achieves superior dynamic characteristics over the conventional P-i-N diode. The dynamic parasitic transistor effect, which generally limits the performance of the diode structures involving an N+ region integrated in the anode side of the device such as the ESD, is shown to be suppressed effectively in the TBJD.

6.3.1 Device Structure

The cross-section view of the proposed TBJD structure and its equivalent circuit is shown in Fig. 6.5. The new concept is to control the anode injection efficiency of the TBJD by a RAT. In the TBJD, RAT refers to the action of the transistor structure consisting of the anode N+ (emitter), P (base) and N- (collector) regions, which operates in its reverse active region with a forward biased base collector junction and a reverse biased base emitter junction in the forward conducting state of the TBJD. The P base of the RAT is shielded by a deep P+ region formed by a trench-refilled P+ poly-Si, which consumes much less area than a deep P+ region formed by extensive diffusion.

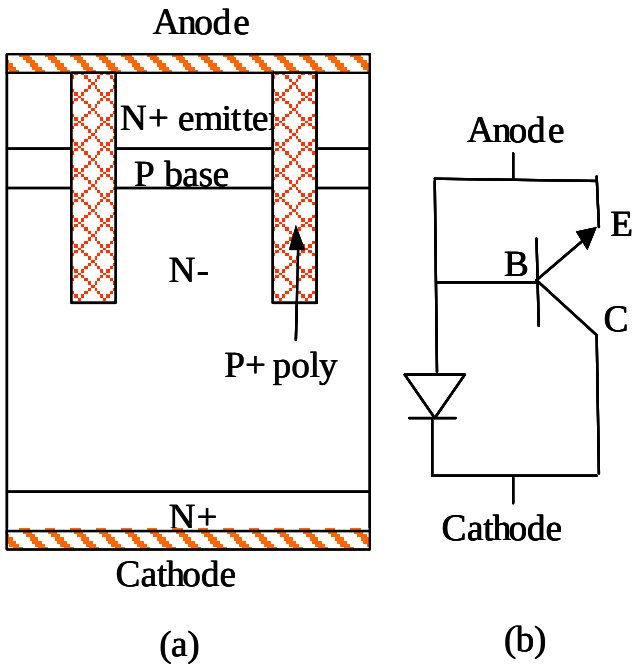


Fig. 6.5 TBJD: (a) cross-section view, and (b) equivalent circuit.

Unlike the ESD [14], which uses a mosaic of P+ and N+ contact to control the doping of the P emitter to reduce the anode injection (Fig. 6.4), the TBJD structure controls its anode injection efficiency through the action of a RAT. To capitalize the effect of the RAT, the sheet resistance of the P base of a TBJD is much higher than that of the P emitter of an ESD, which is made possible through a dynamic shielding effect provided by the deep P+ region. In an ESD, the sheet resistance of the P emitter is limited not only by the punch-through effect in the static reverse blocking state but also by a dynamic parasitic transistor effect during the reverse recovery transient period. The dynamic shielding effect of the deep P+ region in the TBJD is analyzed and demonstrated to be very effective in suppressing the parasitic transistor effect.

Numerical simulation will be used to illustrate this novel power diode structure in the following sections.

6.3.2 Numerical Simulation

TBJD structures with a trench width of 1 μm, varied trench depths (X_t) and trench spacing (W_s) will be analyzed through two-dimensional simulator ATLAS [18]. The simulated 600-V TBJD has a 60-μm-thick N- region with a doping concentration of 1×10^{14} cm^{-3}. The P base diffusion has a surface concentration of 5×10^{18} cm^{-3} and a junction depth of 3 μm, and the anode N+ emitter diffusion has a surface concentration of 7×10^{20} cm^{-3} and varied junction depths to achieve different sheet resistance in the P base. The comparative P-i-N diode structure has the same doping profiles as the TBJD. The carrier lifetime is 2 μs in the study unless otherwise indicated. The physics models used in the simulations include the Dorkel and Leturq mobility model [19], which describes the carrier-carrier scattering effect.

6.3.2.1 Forward-Conducting Characteristics

In the forward-conducting state of the TBJD, electrons are injected from the cathode N-/N+ junction. In a conventional P-i-N diode structure, all of those electrons will recombine with the holes injected from the anode P+/N- junction. Since the TBJD is designed with a P base with

high sheet resistance, the RAT has a reverse active current gain (β_r) greater than unit, even when it operates in a reverse active region. Fig. 6.6 shows the on-state current flow lines of a TBJD. The RAT has an β_r of 5 with a base sheet resistance of 33 kΩ/square. Due to the action of the RAT, parts of the injected electrons will flow directly through the P base and are collected by the anode N+ emitter. The on-state electron current vectors in the TBJD are shown in Fig. 6.7.

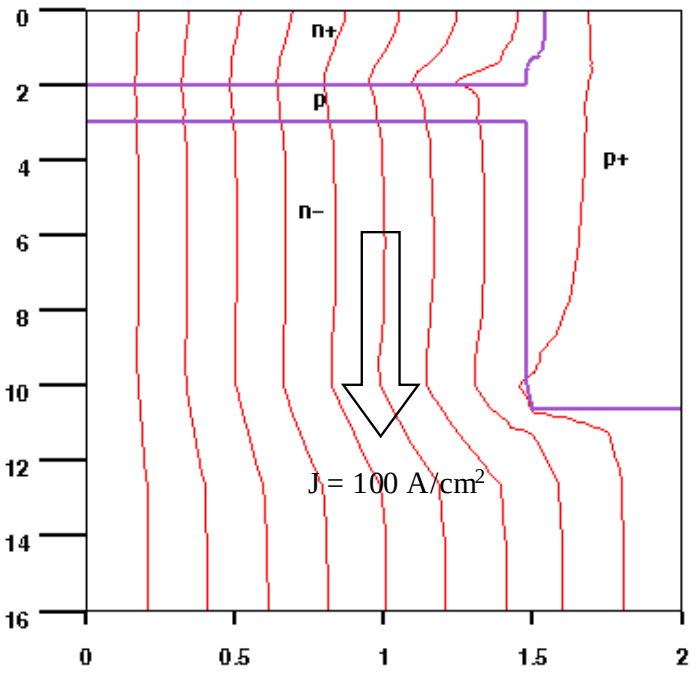


Fig. 6.6 Simulated on-state current flow lines of a TBJD.

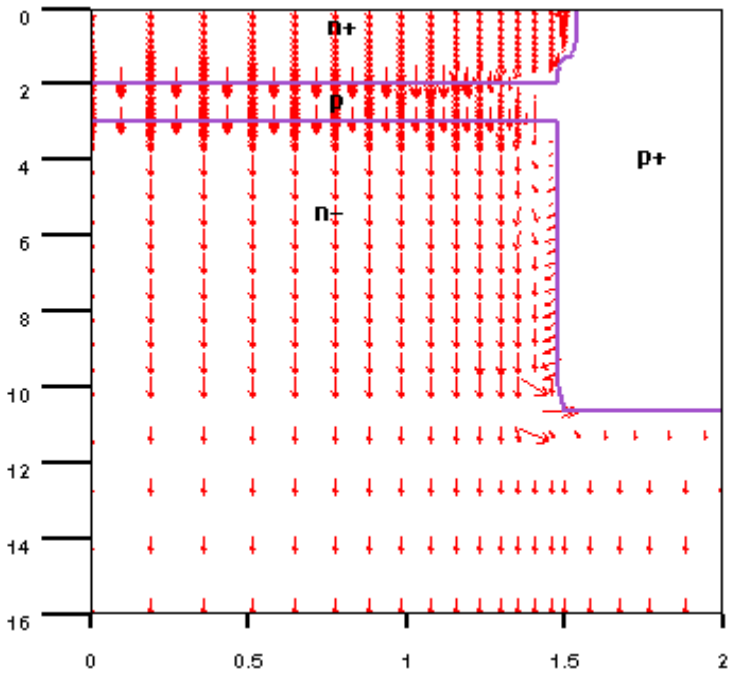


Fig. 6.7 On-state electron current vectors in the TBJD.

Assuming the electron current injected from the cathode is I_E and the common base current gain of the RAT is α_r, the electron current collected by the anode N+ emitter (I_C) can be expressed as $I_C = \alpha_r I_E$. For this portion of electrons collected by the anode N+ emitter, no holes are injected into the N- region to recombine with them. The remaining portion of electron current (I_B) will cause the injection of holes, and

$$I_B = I_E(1-\alpha_r) \tag{6.1}$$

Assuming the anode injection efficiency (defined as the ratio of the injecting hole current to the sum of hole and electron current) of the P+/N- junction structure is γ_p, the injecting hole current due to the electron current I_B can be expressed by

$$I_H = I_B \frac{\gamma_p}{1-\gamma_P} = I_E (1-\alpha_r) \frac{\gamma_p}{1-\gamma_p} \tag{6.2}$$

The effective anode injection efficiency (γ_e) of the TBJD is defined as

$$\gamma_e = \frac{I_H}{I_E + I_H} \tag{6.3}$$

Substituting Eq. 6.2 into Eq. 6.3 will generate

$$\gamma_e = \frac{(1-\alpha_r)\frac{\gamma_p}{1-\gamma_p}}{1+(1-\alpha_r)\frac{\gamma_p}{1-\gamma_p}} \tag{6.4}$$

The common base current gain (α_r) of the RAT can be rewritten as

$$\alpha_r = \frac{\beta_r}{1+\beta_r} \tag{6.5}$$

where β_r is the current gain of the RAT. Substituting Eq. 6.5 into Eq. 6.4 will give rise to

$$\gamma_e = \frac{\gamma_p}{(1+\beta_r)(1-\gamma_p)+\gamma_p} \tag{6.6}$$

It is clear from Eq. 6.6 that increasing the β_r will reduce the effective anode injection efficiency of the TBJD, and this results in less charge stored in the N- region. Fig. 6.8 shows the

on-state carrier profiles in the N- region of a TBJD structure, which have varied β_r while carrying a fixed forward current of 100A/cm^2. The simulated TBJD has the same cell pitch as the TBJD shown in Fig. 6.6. The amount of charge stored in the N- region is labeled in the figure. It is shown that the TBJD with an β_r=5 (labeled as TBJD3 in the figure) has an on-state charge of 26 μC/cm^2, about one third of that in the P-i-N diode. Another distinctive feature is that the reduction in carrier concentration happens near the anode side, which is significantly different from the symmetric carrier profile in the P-i-N diode. It has been known that the excess carrier stored near the anode side is responsible for the high peak reverse recovery current (I_{pr}) and long reverse recovery time (T_{rr}) of a P-i-N diode; therefore, the tailored carrier profile achieved in the TBJD will reduce the I_{pr} and T_{rr}. Another set of simulations confirms that although the ESD can also reduce the carriers stored in the N- region; a carrier profile like that of the TBJD3 shown in Fig. 6.8 is beyond the capability of the ESD.

The on-state voltage drop of the TBJD can be viewed as consisting of two portions: One is the potential barrier for the electron to across the RAT, the other is the voltage drop across the entire N- drift region. Compared with the P+/N- junction of a P-i-N diode structure, TBJD has a lower potential barrier for the electron due to the action of the RAT. On the other hand, the less modulated N- region near the anode junction of the TBJD contributes to a higher voltage drop across the N- drift region.

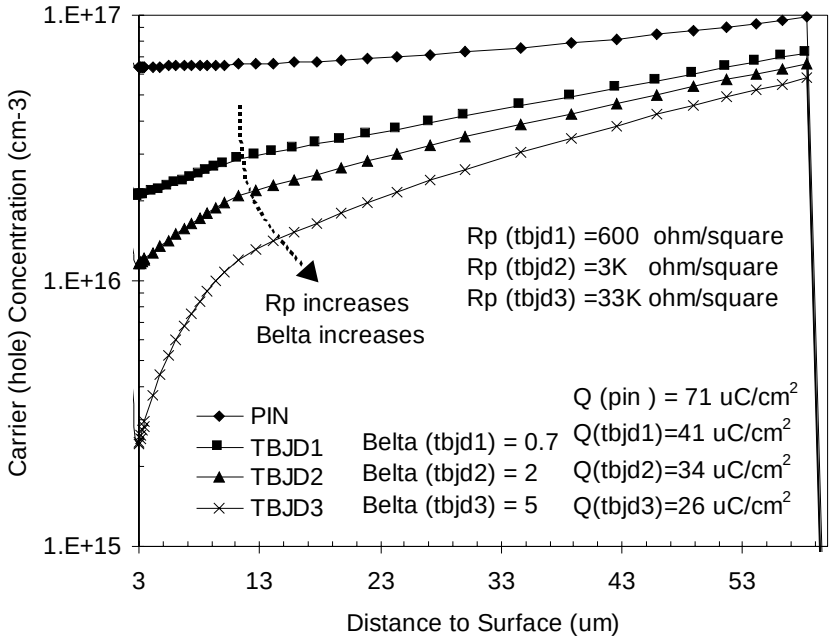


Fig. 6.8 On-state carrier distribution profiles in the N- region of a TBJD with varied current gain βr while carrying a forward current of 100A/cm^2.

The simulated forward I-V curves of the TBJD (β_r=5) and the comparative P-i-N diode are shown in Fig. 6.9. It is noted that there is a crossover point at a current density of about 500 A/cm^2 between these two I-V curves. The forward voltage of the TBJD is slightly higher than that of the P-i-N diode at current densities above the crossover point due to the less modulated N-region. However, if the TBJD is operated at a current level below that point, it exhibits an even lower forward voltage drop than the P-i-N diode. Since the current density at which these two curves cross over is a slightly higher than the typical on-state current level for the power diode, the TBJD achieves an optimized on-state carrier profile without compromising its on-state voltage drop.

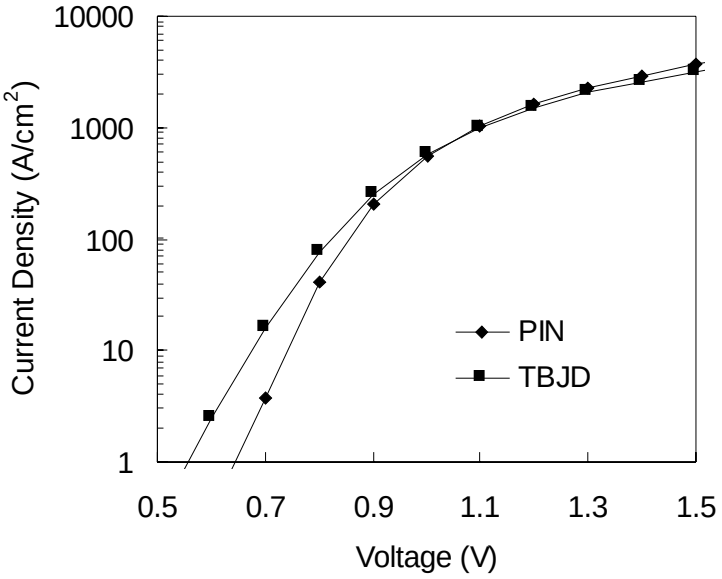


Fig. 6.9 Forward I-V curves for the TBJD (β_r=5) and the comparative P-i-N diode.

6.3.2.2 Reverse Blocking Characteristics

When a reverse voltage is applied to a TBJD, the depletion region between the deep P+ regions will expand both vertically and laterally. With the increase of the reverse voltage, the N- region between the two deep P+ regions eventually will be pinched off and will serve as a potential barrier to prevent the shallow P base from punch-through breakdown. The equal-potential contour and the leakage current flow lines in the TBJD (β_r=5) while withstanding a 600-V reverse voltage are shown in Fig. 6.10. The pinch-off effect is clearly shown by its equal-potential contour. Simulations also show that the TBJD, with a P base sheet resistance as high as 33 kΩ/square, can block the same reverse voltage as the P-i-N diode with no observed increase of leakage current. An ESD with the same sheet resistance in the P emitter can only sustain 80 V of reverse voltage due to punch-through breakdown. The static electric field shielding effect of the TBJD can be strengthened by decreasing the trench spacing or increasing the trench depth.

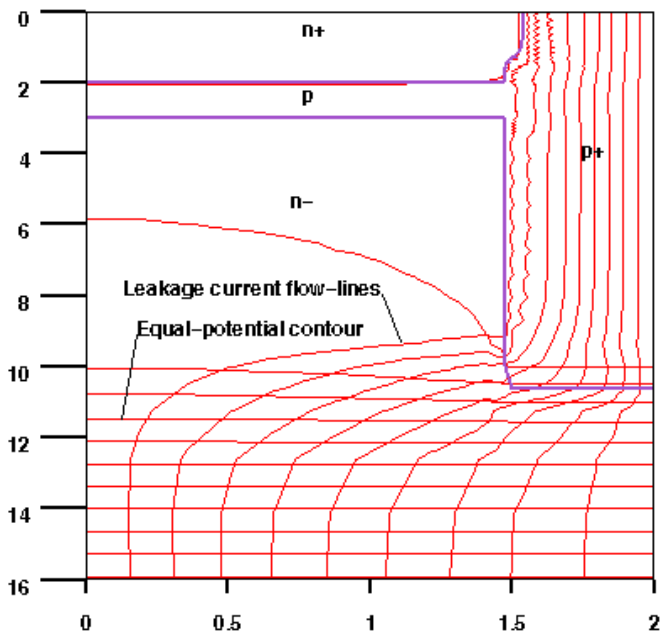


Fig. 6.10 Equal-potential contour and the leakage current flow lines of the TBJD under an 800-V reverse voltage.

6.3.2.3 Reverse Recovery Characteristics

The switching performance of the TBJD was studied by simulation. The diodes shown in Fig. 6.8 were switched from an on-state operation with a forward current density of 100 A/cm^2 to an off-state condition with a 100-V reverse blocking voltage. The rate of the fall of the current (di_F/dt) was set to be 2000 A/(cm^2.μs). The simulated peak reverse current (I_{pr}) and the calculated loss per cycle (E_{rr}) are given in Fig. 6.11. It is clear that increasing the β_r reduces the peak reverse current and the switching loss. Compared with the P-i-N diode, the TBJD with β_r =5 reduces the I_{pr} by 55% and E_{rr} by 65%, which is beyond the reach of the ESD according to the simulation study. All these improvements are attributed to the optimized on-state carrier profile tailored in the N- region of the TBJD.

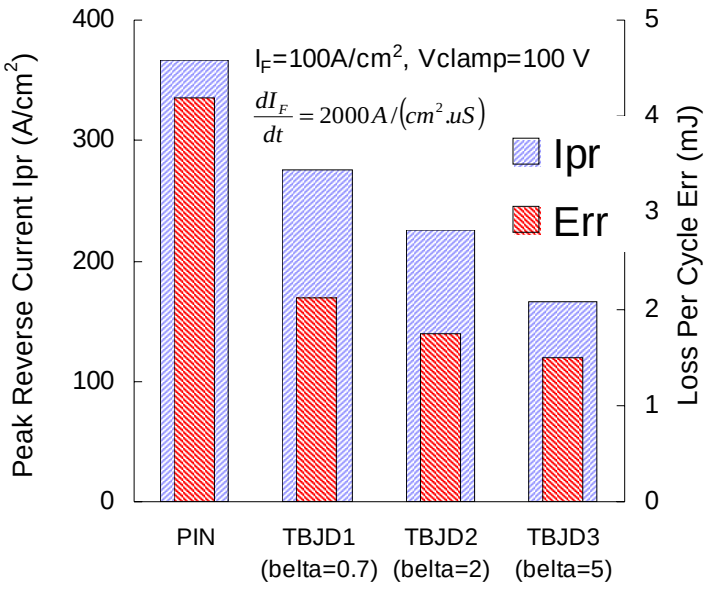


Fig. 6.11 Peak reverse current (I_{pr}) and the loss per cycle (E_{off}) during the reverse recovery of the diodes with varied β_r.

6.3.2.4 Dynamic Transistor Effect

In the ESD structure, the maximum sheet resistance value of the P emitter actually is not limited by the static punch-through effect in its reverse blocking state; instead, it is limited by a dynamic parasitic transistor effect that occurs during the reverse recovery transient period. If, for any reason, the P/N+ junction of either TBJD or ESD is turned on by the reverse hole current flowing laterally in the thin P base or P emitter region, the transistor consisting of the N+/P/N- regions will operate in its forward active region, and the devices then will suffer from the reverse-biased second breakdown characteristics of this forward active transistor. This dynamic parasitic transistor effect limits the maximum value of the sheet resistance of the P emitter region of the ESD. However, this parasitic transistor effect is suppressed effectively by the deep P+ region in the TBJD. In the TBJD, the holes are dragged out of the N- region by the deep P+

region during the reverse recovery transient period. Little, if any, hole current will flow through the P base, which is essentially free of the parasitic transistor effect limitation.

Fig. 6.12 shows the simulated reverse recovery current waveforms of a TBJD and an ESD with the same doping profile. TBJD has a 6-μm deep P+ trench shield. The sheet resistance of the P region in both devices is 7 kΩ/square, and both the TBJD and ESD can sustain a static 600-V reverse voltage with this P region design. The current flow lines of the TBJD and the ESD at four different time points are illustrated in Fig. 6.13 and Fig. 6.14, respectively. It is shown clearly that, in the TBJD, although the RAT carries most of the forward conducting current, the deep P+ shield region will immediately divert the reverse recovery current once the TBJD starts to recover. The base of the TBJD then is protected fully by the deep P+ shield. Unlike the TBJD, the reverse current in the ESD flows through the P emitter. At time t=400 ns, the reverse current flowing laterally in the P emitter triggers the turn-on of the forward active transistor.

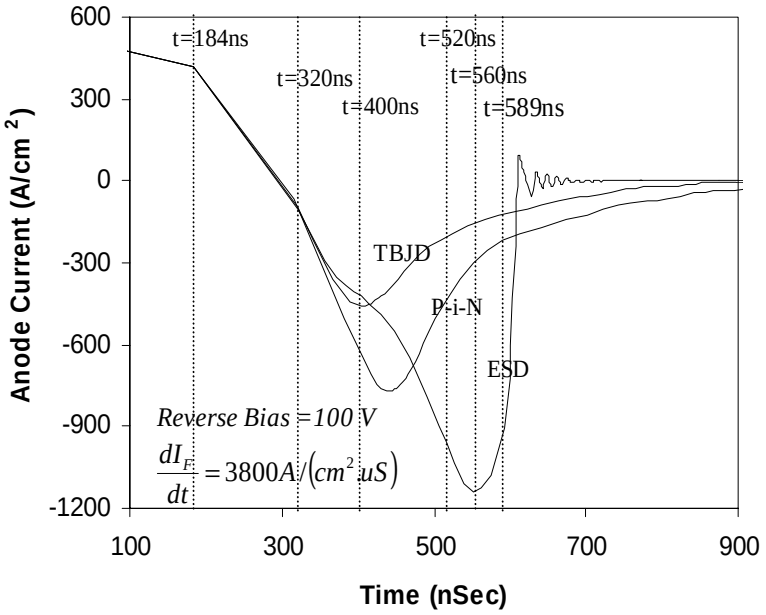
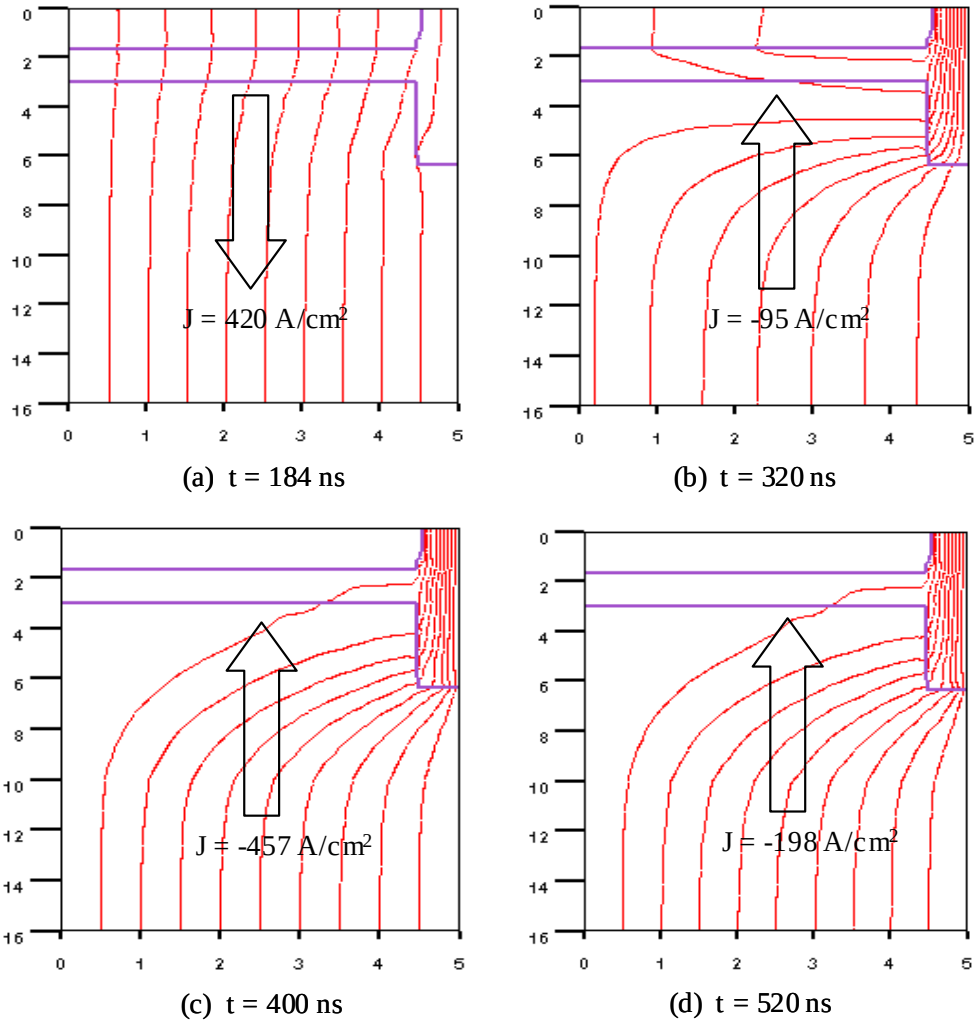


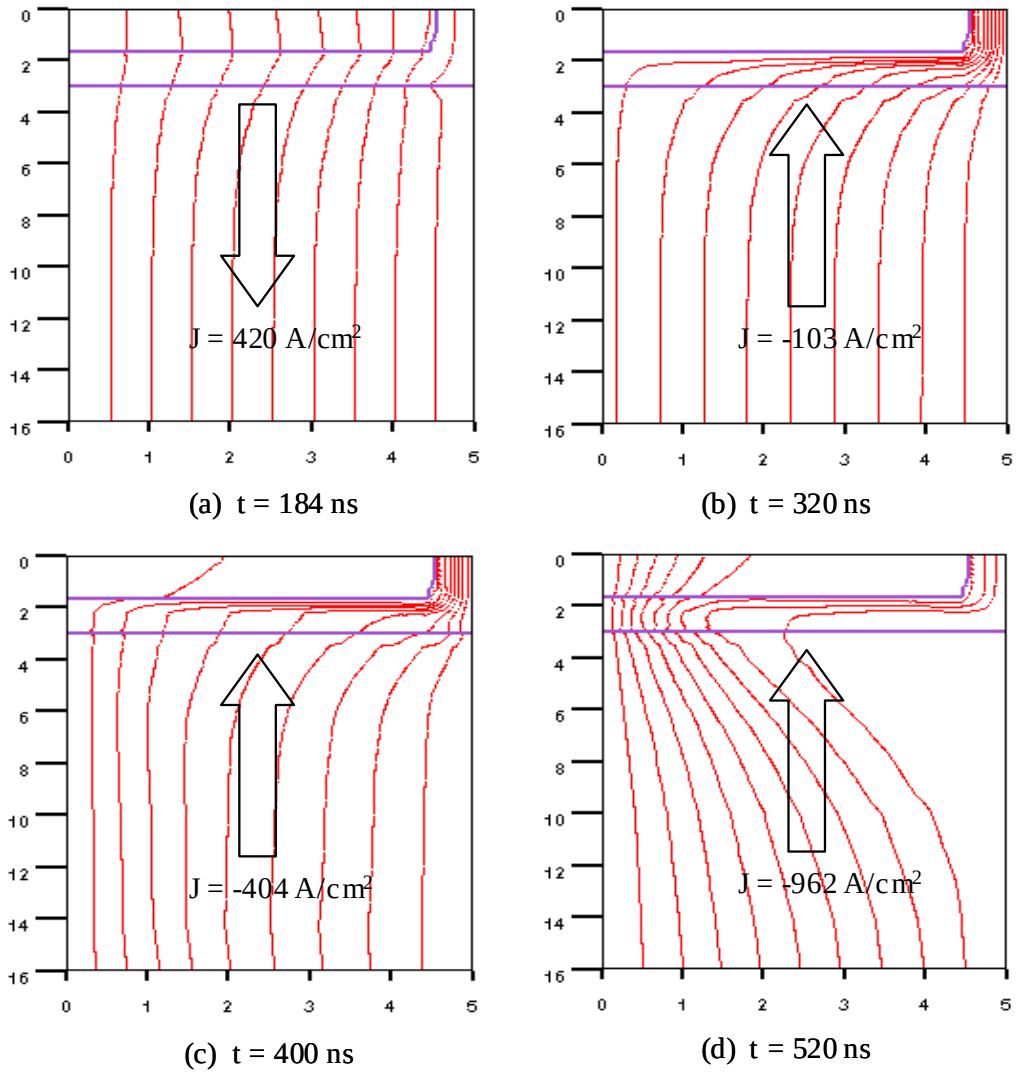
Fig. 6.12 Reverse recovery current waveforms of a TBJD and an ESD.



(a) t = 184 ns (b) t = 320 ns

(c) t = 400 ns (d) t = 520 ns

Fig. 6.13 Current flow lines of the TBJD during the reverse recovery transient period.



(a) t = 184 ns (b) t = 320 ns

(c) t = 400 ns (d) t = 520 ns

Fig. 6.14 Current flow lines of the ESD during the reverse recovery transient period.

What happens after time t=400 ns in the ESD is a typical reverse-biased second breakdown phenomenon due to the current crowding of a bipolar transistor. The current crowding of the transistor is shown clearly by the current flow lines at t= 520 ns in Fig. 6.14. The instant electron profile and the electric field distribution in the N- region of the ESD right under the center of the P/N+ junction at five different time points are given in Fig. 6.15 and Fig. 6.16, respectively. Initially, carriers are swept out of the N- region by the reverse current and a space charge region developed near the anode P/N- junction; after the parasitic transistor is triggered to turn on, the space charge region spots a sudden increase of the electrons injected from the N+ emitter. As a consequence, the space charge region collapses, and the diode reverse blocking voltage snaps back instantly as indicated in the insert of Fig. 6.16. The sudden increase of the electrons in the drift region dramatically increases the reverse current. The presence of the large electron current alters the electric field distribution. If the electron current is large enough, as it is in this case, it will change the polarity of the net charge in the drift region from positive to negative, which in turn reverses the slope of the electric field profile and shifts the peak electric field from the P/N- junction to the N-/N+ junction. The shift of the peak electric field can be seen in Fig. 6.16.

It needs to be noted that the parasitic transistor cannot sustain its operation without the base-driving hole current. The hole current is supported by the drift of the holes stored in the N- region out of the space charge region. Initially, that happens in the N- region near the anode side. With the shift of the electric field and the space charge region from anode P/N- junction to the cathode N-/N+ junction, the carrier stored in the N- region near the cathode side will be swept out immediately. This is an unfavorable characteristic because the carrier stored in this region provides the necessary softness for the reverse recovery of the diode. Without this portion of the carrier, reverse recovery will be extremely snappy. In the simulated ESD scenario, the reverse recovery current snaps off drastically and generates a very high voltage spike on the serial stray inductance. The ringing of the ESD current is due to the avalanche breakdown caused by the voltage spike.

The TBJD mainly reduces the on-state carriers stored near the anode junction as shown in Fig. 6.8. Compared with the P-i-N diode, the TBJD will have a shorter time T_A to reach its peak reverse current, while it needs a similar time T_B for the reverse current to snap off; the TBJD therefore has a softer reverse recovery as shown in Fig. 6.12.

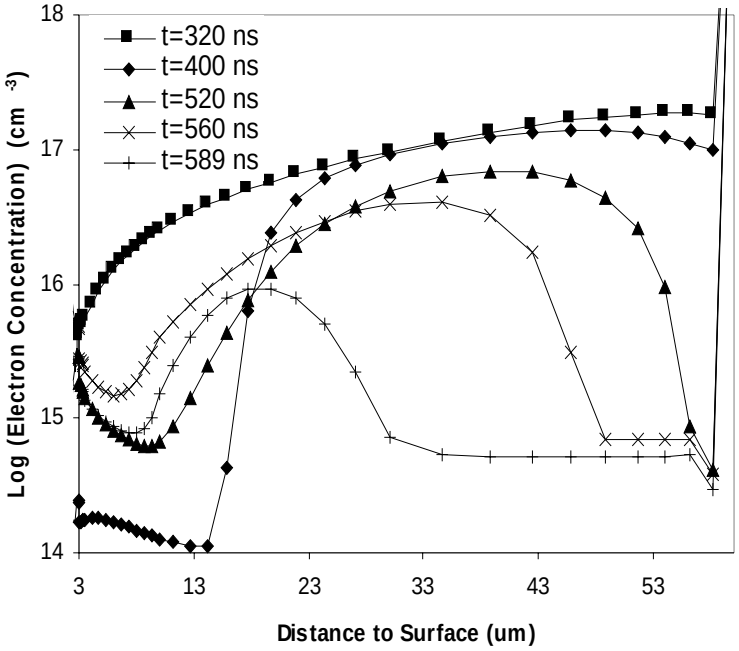


Fig. 6.15 Instant electron profile in the N- region of the ESD during the reverse recovery transient period.

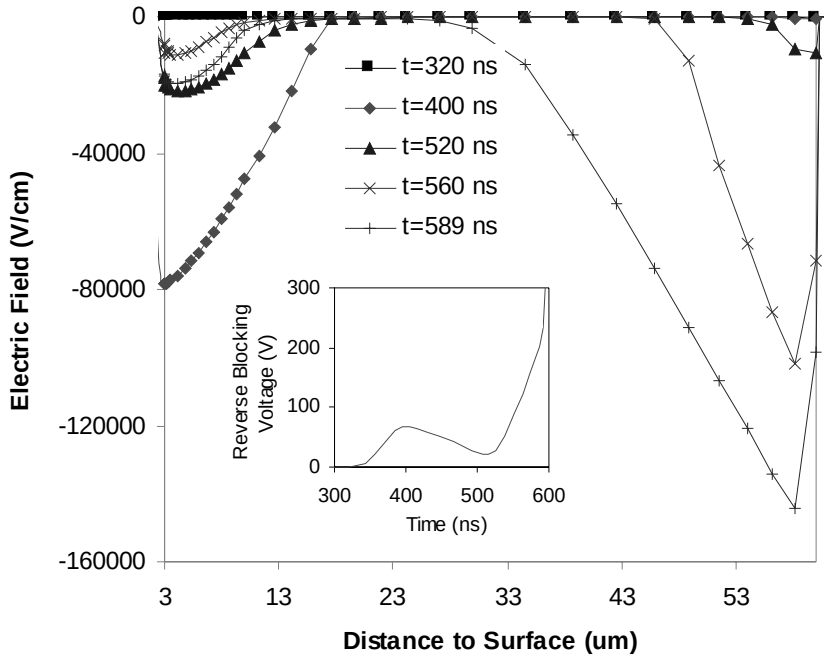


Fig. 6.16 Instant electric field distribution in the N- region of the ESD during the reverse recovery period. The figure insert shows the waveform of the reverse blocking voltage.

Additional simulations have shown that increasing the trench depth or decreasing the trench spacing can further enhance the dynamic shielding capability of the P+ region, making the TBJD eventually immune to this parasitic transistor effect.

6.4 Conclusion

In this chapter, a comprehensive review of the power diode techniques was conducted by classifying the reported diode techniques into three categories: lifetime controlling, anode engineering and cathode engineering. Although most of the reported diode techniques previously achieved better reverse recovery characteristics than the conventional P-i-N diode, none had been

realized without sacrificing other characteristics such as the on-state voltage drop and the reverse leakage current.

A new high-voltage TBJD was proposed and demonstrated to have superior characteristics over the conventional P-i-N diode structure with the aid of two-dimensional numerical simulation. The TBJD controls the anode injection efficiency by the action of a reverse active transistor structure integrated on its anode junction. The reverse active transistor helps tailor an optimized on-state carrier profile to improve the diode switching characteristics without compromising the on-state voltage drop.

The P base of the reverse active transistor of the TBJD is shielded by a deep P+ region formed by refilling P+ poly-Si into a deep trench. The deep P+ region not only prevents the thin P base from being punched through in the reverse blocking state, but also effectively suppresses the dynamic parasitic transistor effect. The electric field shielding effect helps the TBJD maintain the same leakage current level as the conventional P-i-N diode. These unique features make TBJD suitable for high-voltage applications.

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Chapter 7 Design and Fabrication of the TBJD

7.1 Device Design

After verifying the concept of the TBJD through two-dimensional numerical simulations, devices were designed and fabricated to experimentally demonstrate their operation. A TBJD process with seven masking levels was developed to fabricate the devices.

The mask set in this work was designed using the Cadence layout tool. Fig. 7.1 shows a photomicrograph of a typical fabrication of multi-cell TBJD die. The multi-cell dies were laid out in a 2200 μm × 2200 μm area surrounded by the device termination region, which translates into an active area of approximately 4.8 mm^2. The cross-section view of the edge termination region designed with five P+ floating rings with field plates is shown in Fig. 7.2. The radius of the inner ring (about 160 μm) was used to achieve cylindrical breakdown for a P+ junction depth of 4.5 μm. The same edge termination region was used for each of the devices to achieve a reverse blocking voltage of 600 V.

Fig. 7.3 shows a photomicrography of a typical unit-cell of a TBJD. The unit-cell is square and surround by trenches. While the trench width was fixed, the center-to-center spacing (W_s) between two trenches varied from 10 to 30 μm in the design. The multi-cell device consists of thousands to tens of thousand of unit-cells.

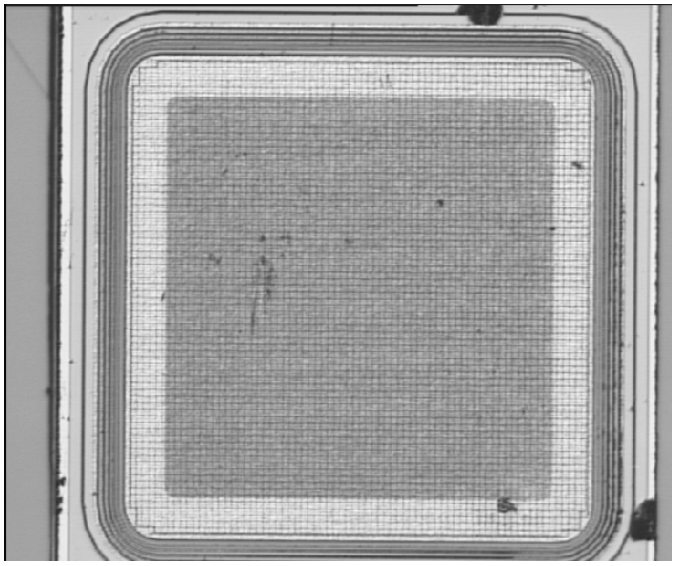


Fig. 7.1 Top view of a TBJD die.

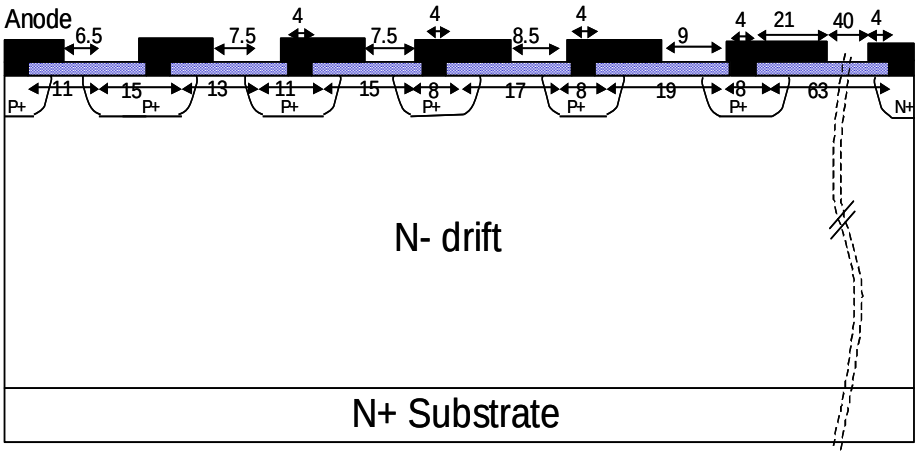


Fig. 7.2 Cross-section view of the TBJD edge termination region.

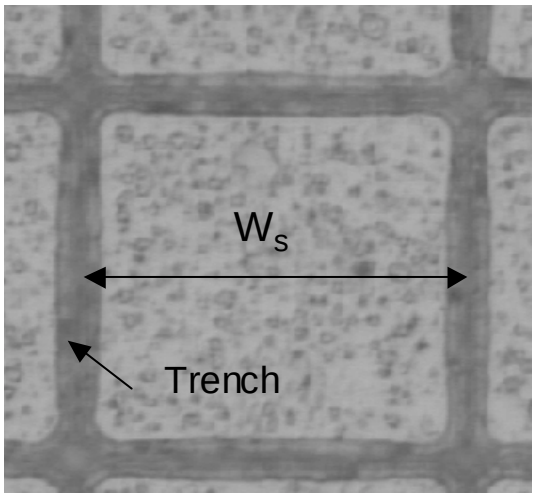


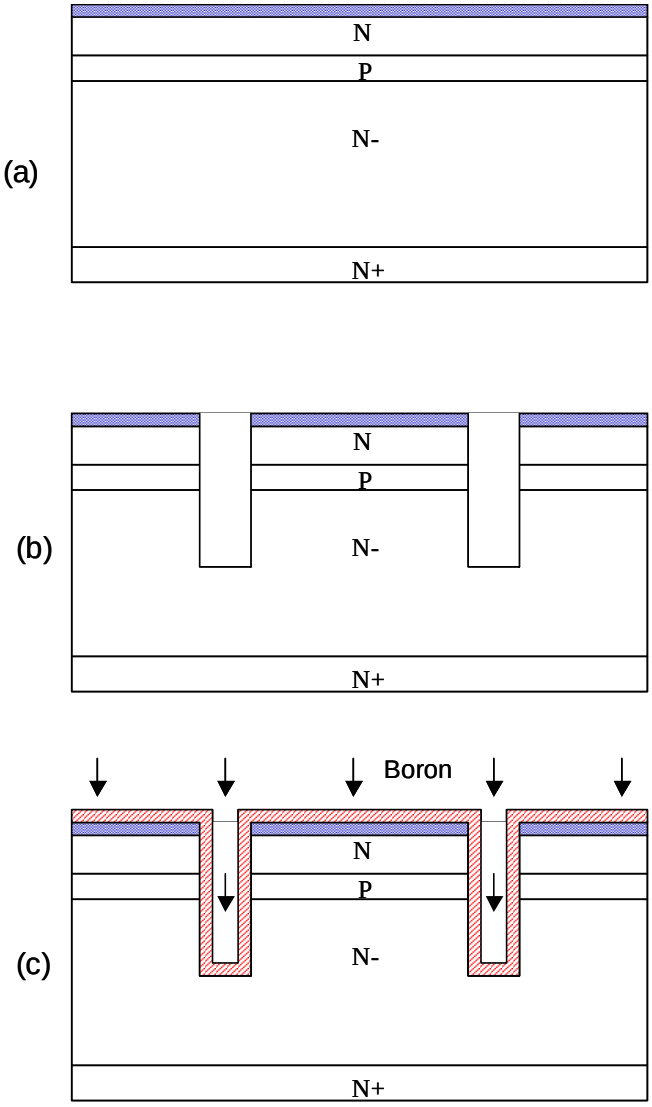
Fig. 7.3 Photomicrography of a unit-cell of the TBJD.

7.2 Process Flow

The TBJD devices were fabricated using <100> oriented N+ substrate (~ 20 mils) wafers with a 60 μm thick, 45 ohm-cm (doping concentration is about 1×10^{14} cm^{-3}) N- epitaxial layers as the starting material. A complete process flow list is given in Appendix. Fig. 7.4 illustrates the major steps of the self-aligned TBJD process.

The wafers were initially grown with 1-μm thick field oxide. The first mask (TER) was used for the P+ boron diffusion to form the edge termination. The field oxide was then patterned to delineate the active and termination areas on the wafer surface. This was achieved by a two-step active area definition using BAS and SNE masks.

Next, a sacrificial oxide was grown, and a photoresist mask (BAS) was used to pattern the wafers for the P base boron implantation. After the implantation, the photoresist was stripped and P base was driven in. The wafers were similarly patterned for the N+ emitter phosphorus implantation. After that, a 6000-A protection oxide was grown (Fig. 7.4a).



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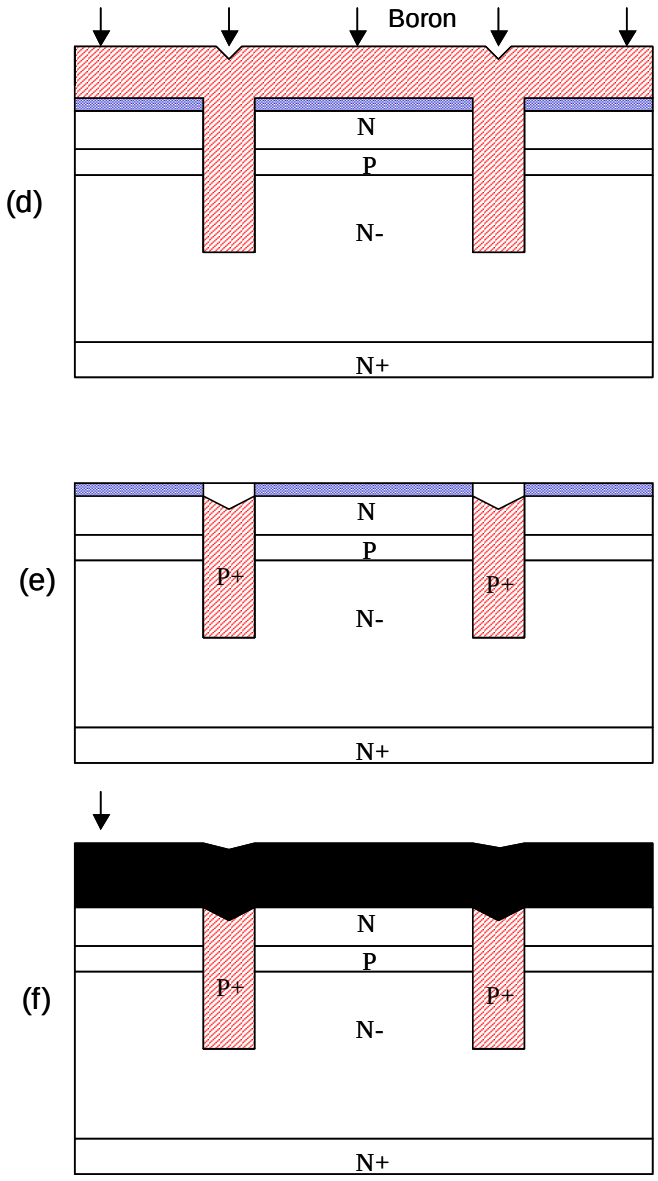


Fig. 7.4 Major steps of the TBJD fabrication process.

The fourth photoresist mask (PPT) was then used to pattern the trenches by dry etching oxide, which was immediately followed by a reactive ion etching to form the deep trenches (Fig. 7.4b). After that, the photoresist was stripped and the wafers were cleaned. The trenches were refilled with poly-Si through a two-step process: a 6000-A thick poly-Si layer was first deposited and doped with boron through diffusion (Fig. 7.4c); then, a 2-μm thick poly-Si was deposited and likewise doped with boron (Fig. 7.4d). Since the actual trench is wider than 1.2 μm (line width is 1 μm in the mask) due to the lateral etching, this two-step process guarantees that the boron can get into the deep trench region. A SEM image of the cross-section view of the TBJD's cross section the poly-Si refilling is shown in Fig. 7.5. The poly-Si was planarized through a plasma etch-back process (Fig. 7.4e).

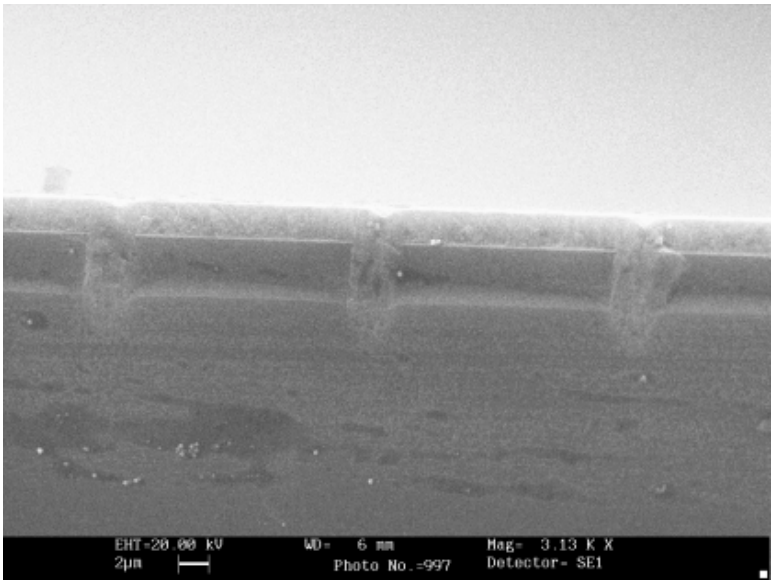


Fig. 7.5 A SEM cross-section view of the TBJD after the poly-Si refilling.

The fifth, sixth and seventh masks were for contact, metalization and bond pad definitions, respectively. The contact holes were patterned by wet etching using a photoresist mask. This was followed by the sputter depositing of 3 μm of aluminum (Fig. 7.4f). The

aluminum then undergoes wet etching, again using a photoresist mask. A layer of silicon nitride was then used to passivate the top surface of the wafers, and then patterned to open windows at the anode pads.

The substrates of the wafers were then lapped until the remaining thickness was about 270 um. A multi-layer metal was deposited to provide good ohmic contact, good adhesion to the substrate and solderability. In this work, the wafers were diced to separate the dies and have them TO-220 packaged.

Unlike the Trench Base Shielded Bipolar Transistor (TBSBT) process [1], which formed the trench P+ poly-Si regions before the formation of the P base and N+ emitter, the TBJD process did the self-aligned trench etching after the formation of the P base and N+ emitter. Therefore, the TBJD process has better control of two critical design parameters: trench spacing (W_s) and base charge (Q_p).

It needs to be pointed out that since the P+ poly-Si trench of the TBJD was formed through a two-step refilling process, the lateral diffusion of the boron from the P+ poly-Si trench into the N- region will generate a P-Si layer surrounding the P+ poly-Si trench. The width of the P-Si layer is about 1 μm. Therefore, the effective base shield region consisting of the P-Si layer and the P+ poly-Si trench is about 1 μm wider per side and 1 μm deeper than the original P+ poly-Si trench.

7.3 Spreading Resistance Profile

In order to study the effect of the P base charge on the device characteristics, several process splits were introduced to obtain different charges by varying the junction depth of the N+ emitter junction while keeping the same junction depth for the P base. This was achieved by adjusting the drive-in time of the P base and N+ emitter implant as shown by some process split steps which are shaded in the process flow given in Appendix. The conditions for these splits

were obtained through processing simulations using the TSUPREM-4 [2]. The simulated doping profile for one of the splits, taken after the entire process sequence, is shown in Fig. 7.6. It represents the doping profile of the reverse active transistor from the surface of the semiconductor. The doping profile shows the N+ emitter implant, P base implant and the N- epi regions.

Fig. 7.6 also shows the measured spreading resistance profile (SRP) and compares it with the TSUPREM-4 simulation result. It is noted that the N+ emitter region was diffused deeper than it was originally designed to be. The total charge of the P base (Q_P) is found to be 1.2e12. In this work, TBJDs with three different values of Q_p were investigated. The measured SRP data show that they were 1e13, 1.2e12 and 2.9e11.

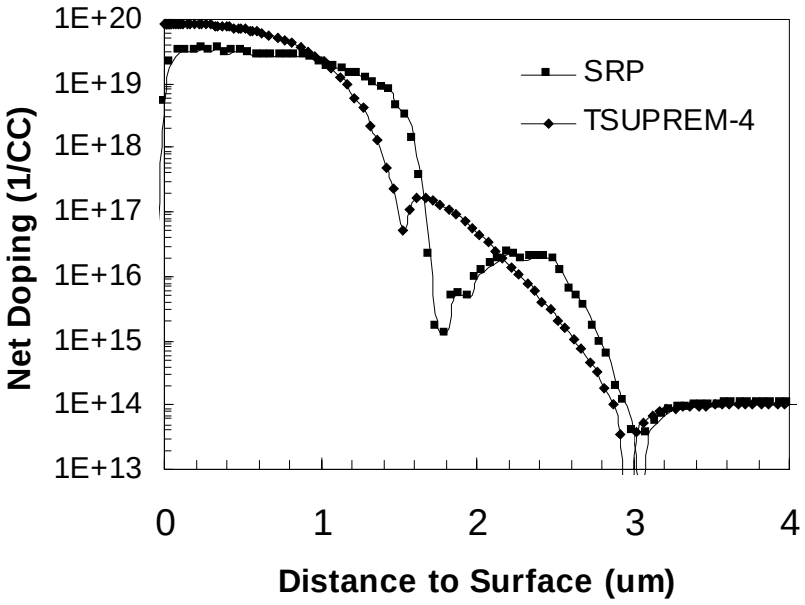


Fig. 7.6 Simulated and experimental SRP doping profiles of a TBJD.

The main reason for the observed discrepancy between the measured SRP data and the simulated doping profile is the lack of complete characterization of the furnace operation. The process could not be extensively characterized prior to fabrication due to the time constraints. However, this discrepancy will not affect the study of the TBJD as long as all the comparative devices are fabricated on the same process run.

References

[1] Q. F. Chen, J. K. O. Sin and Q. X Chen, “A new trench base-shielded bipolar transistor,” *Proceedings of ISPSD*, pp. 169-172, 1998.

[2] TSUPREM-4 User's Manual, Version 6.3," Technology Modeling Associates, Inc., 1995.

Chapter 8 Experimental Characterization of the TBJD

8.1 Introduction

After the devices designed in the previous chapter were fabricated and packaged, the static and dynamic characteristics of the devices were investigated at both room and elevated temperatures. It was found that their characteristics correspond well with the simulation results. The unique feature of the TBJD, which controls the anode injection efficiency by the action of an integrated RAT, was experimentally confirmed to meet design goals.

A comparative P-i-N diode was also fabricated on the same process run with the same edge termination design. The P+ emitter of the P-i-N diode was formed by the P base implant of the TBJD. Compared with the P-i-N diode, the TBJDs were shown to have not only superior reverse recovery characteristics, but also lower on-state voltage drop and the same leakage current level.

8.2 Experimental Results and Discussion

8.2.1 Reverse Active Transistor

Demonstration of the action of the reverse active transistor needs a TBJD designed with three terminals. The novel self-aligned process described in the previous chapter cannot fabricate such a TBJD. The I-V characteristics of the RAT of a TBJD fabricated by a trench bipolar

transistor process is shown in Fig. 8.1 [1, 2]. The transfer curves of the RAT clearly show the action of the reverse active transistor with a β_r of 2.

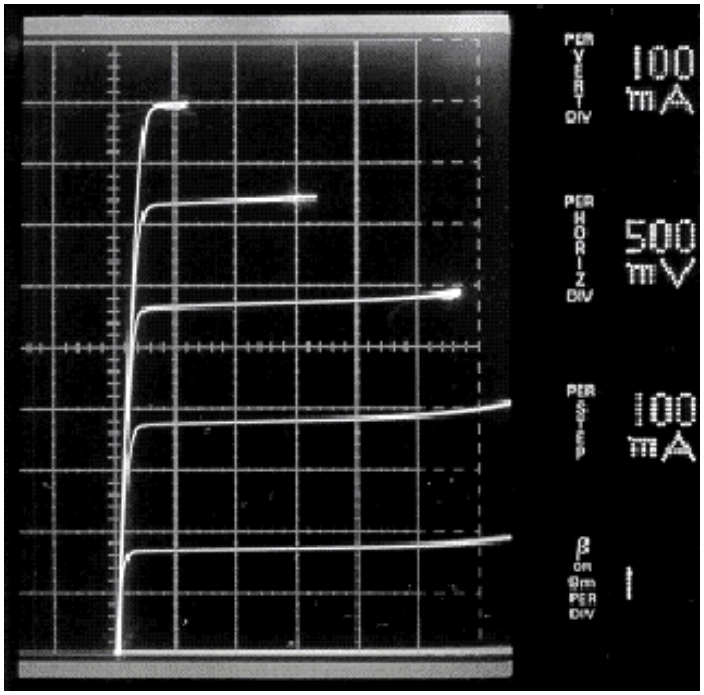


Fig. 8.1 Experimental I-V characteristics of the RAT.

8.2.2 Forward Characteristics

Typical forward I-V characteristics of a TBJD measured at room temperature are shown in Fig. 8.2. The TBJD (TBJD3) shown in Fig. 8.2 has a Q_p of 1.2e12 and a W_s of 15 μm. Fig. 8.3 shows the comparison between the forward I-V characteristics of the TBJD and that of the P-i-N diode. It is shown that the on-state voltage drop of the TBJD is lower than that of the P-i-N diode up to 20 A (416 A/cm^2). The measured I-V characteristics of the diodes agree with the simulation results shown in Fig. 6.9. Since the normal operating current of the device is 10 A (208 A/cm^2), the TBJD has a lower on-state voltage drop than the P-i-N diode. It was also

observed that the forward I-V curve of the TBJD would move in the direction shown by the arrows with the increase of W_s or decrease of Q_p. The reason for this trend is the effect of the RAT in the TBJD as discussed in the previous chapters. Nevertheless, the measured crossover points between the I-V curves of the TBJDs and that of the P-i-N diode stay above the normal operating current.

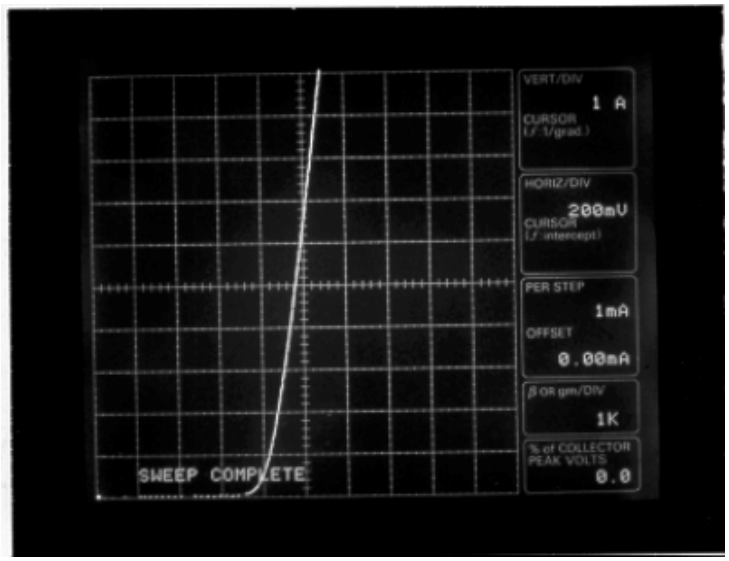


Fig. 8.2 Measured forward I-V characteristics of a TBJD.

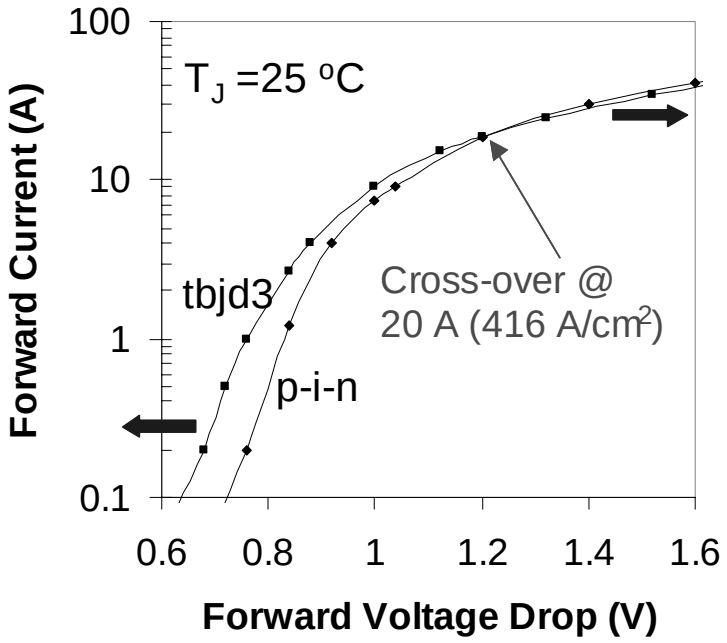
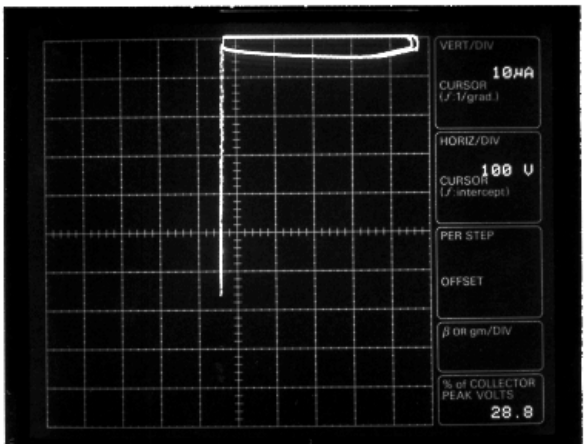


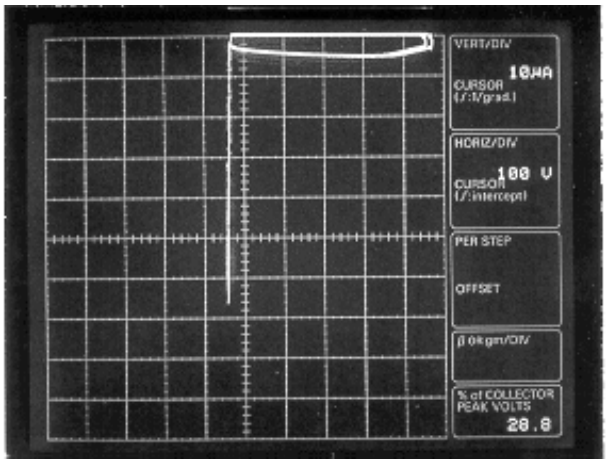
Fig. 8.3 Measured forward I-V characteristics of the TBJD and P-i-N diode.

8.2.3 Reverse Blocking Characteristics

The reverse blocking I-V characteristic of the TBJD (TBJD3) measured at room temperature is shown in Fig. 8.4 and compared with that of the P-i-N diode. The breakdown voltage of the TBJD is about 550 V, lower than the designed 600 V. However, considering the fact that the breakdown characteristic of the TBJD is almost identical to that of the P-i-N diode, this premature breakdown is by no means due to the TBJD structure itself. Since both diodes share the same edge termination design, it was concluded that the termination region accounts for this premature breakdown problem. The main reason for this is that the junction depth of the deep P+ diffusion for termination was found to be 6 μm instead of the expected 4.5 μm. Therefore, the termination design shown in Fig. 7.2 is no longer an optimized design. Fortunately, the 550 V reverse breakdown voltage was still adequate for the purpose of characterization.



(a) TBJD (TBJD3)



(b) P-i-N

Fig. 8.4 Measured reverse blocking characteristics at room temperature: (a) TBJD , and (b) P-i-N diode.

The important design parameters that decide the reverse blocking voltage of the TBJD are the base charge (Q_p), trench spacing (W_s) and trench depth (X_t). The reverse blocking voltage of the TBJD as a function of these three design parameters is given in Fig. 8.5. As seen from the figure, the reverse blocking voltage tends to decrease with the increase of W_s, decrease of Q_p and decrease of X_t. These observations can be easily explained, since decreasing Q_p makes the base prone to the punch-through effect, while lowering the trench depth or increasing the trench spacing weakens the electric field shielding effect of the P+ poly-Si trench, as discussed in the previous chapters. For the TBJD with a Q_p of 2.9e11, the electric field shielding effect provided by the 7-μm deep trenches is sufficient when the trench spacing is no wider than 30 μm. The electric field shielding effect of the deep trench is best shown in the TBJD with a Q_p of 1.1e10. Even with that extremely low Q_p, a pair of very closely placed trenches (W_s=10 μm) helps the device sustain a reverse voltage up to 90% of the BV of the comparative P-i-N diode. It should be noted that, without the deep trench, a TBJD with a Q_p=2.9e11 is not able to sustain the 550 V of reverse voltage due to the punch through.

Another important characteristic of a high-voltage power diode is the reverse blocking leakage current level at elevated temperature. To measure the reverse leakage current characteristics, the substrates of the TBJDs were mounted on a large piece of heat sink, and heated up to 150 ^{o}C. The reverse blocking characteristics of the TBJDs measured at 150 ^{o}C are shown in Fig. 8.6. For the TBJD (TBJD3) shown in Fig. 8.3, no increase of the leakage current has been observed compared with the P-i-N diode. It is also found that increasing W_s (like TBJD5) or decreasing Q_p (like TBJD9) beyond certain level results in the increase of the leakage current, since they tend to weaken the electric field shielding effect provided by the P+ poly-Si regions.

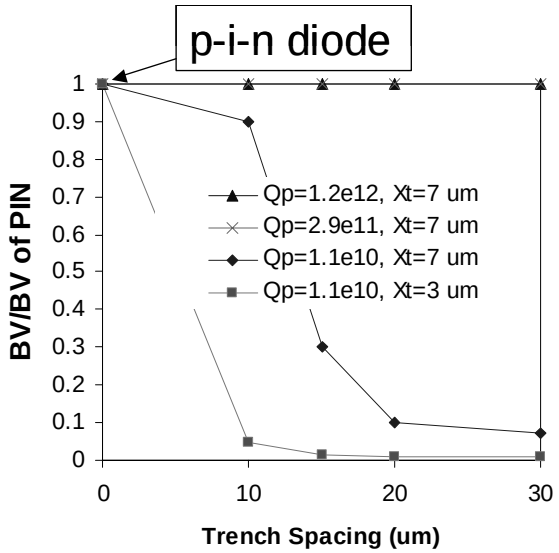


Fig. 8.5 Reverse blocking capability of the TBJD as a function of the trench spacing, trench depth and P base charge.

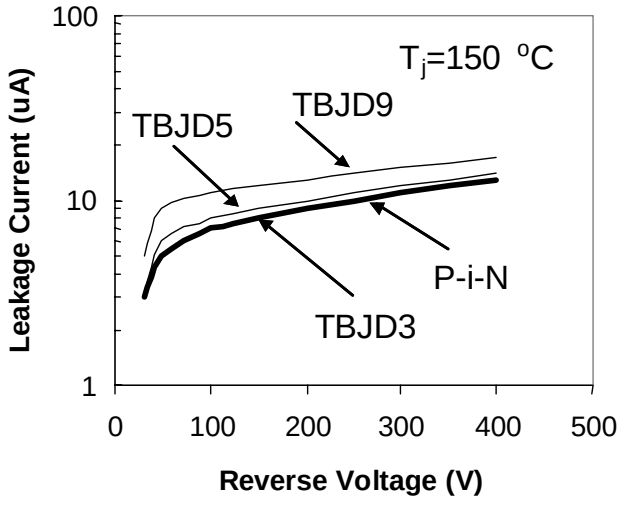


Fig. 8.6 Leakage current measured at elevated temperature.

As stated in the previous chapter, there is a 1-μm wide P-Si layer surrounding the P+ poly-Si trench in the TBJD due to the lateral diffusion of boron from the P+ poly-Si into the N- region. This P-Si layer has a sufficient amount of charge to not be fully depleted at the reverse blocking state of a TBSBT. The existence of a Si junction (instead of a P+ poly-Si/N- Si junction) prevents the TBJD suffering from the higher generation recombination rate of a carrier at the interface of a P+ poly-Si/N- Si junction. Compared with the P-i-N diode, no increase of the leakage current due to the existence of the P+ poly-Si has been observed in the TBJD at either room or elevated temperatures.

8.2.4 Reverse Recovery Characteristics

The reverse recovery performances of the diodes were compared by subjecting the diodes to a reverse di_F/dt of 150 A/μs. The diodes were switched from initially conducting a forward current of 10 A to sustaining a reverse blocking voltage of 300 V. The measured reverse recovery waveform of the TBJD (TBJD3) is shown in Fig. 8.7. The reverse recovery waveform of the P-i-N diode is included for comparison. The measurement data confirm the superior reverse recovery characteristics of the TBJD.

Table 8.1 summarizes the measured reverse recovery performances of the TBJD as a function of W_s and Q_p. All the devices listed in the table have a static breakdown voltage of about 550 V. The base charge Q_p affects the current gain of the RAT, while the trench spacing W_s determines its relative active area. The lower the Q_p or the wider the W_s, the stronger the RAT. The peak reverse recovery current (I_{pr}) and the reverse recovery charge (Q_{rr}) extracted from the measured reverse recovery waveforms decrease with the increase of W_s or decrease of Q_p. The effect of the W_s and Q_p on the reverse recovery characteristics of the TBJD confirms that a stronger RAT in the TBJD will further reduce the anode injection efficiency and result in fewer carriers stored in the drift region. For the TBJD with W_s=15 μm and Q_p=2.9e11, the reverse recovery charge is less than one quarter of that of the P-i-N diode.

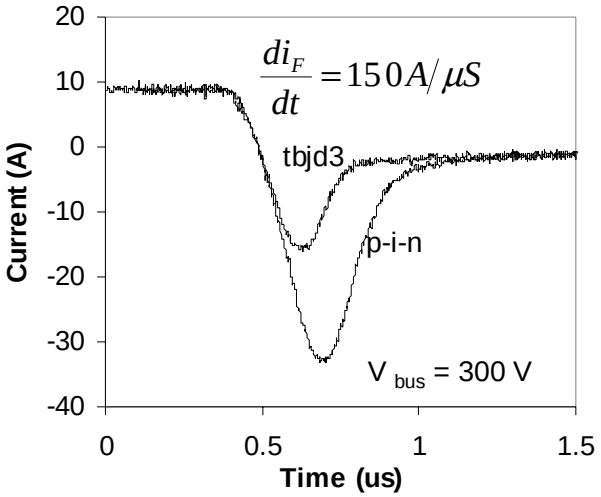


Fig. 8.7 Measured reverse recovery current waveforms of the TBJD and the P-i-N diode.

Table 8.1 Measured reverse recovery performance of the diodes.

Device types	p-i-n	tbjd20	tbjd3	tbjd9
Design parameters		W_s =15 μm, X_t=7 μm		
Test conditions	I_F=10A, V_{bus}=300 V, di_F/dt=150 A/μs			
Q_p(1/cm^2)	5e14	1e13	1.2e12	2.9e11
I_{pr} (A)	33.1	22.2	15.9	13.4
Q_{rr} (μC)	8.39	4.78	3.25	2.02

Device types	p-i-n	tbjd2	tbjd3	tbjd5
Design parameters		Q_p = 1.2e12, X_t=7 μm		
Test conditions	I_F=10A, V_{bus}=300 V, di_F/dt=150 A/μs			
Ws (μm)		10	15	30
I_{pr} (A)	33.1	20.6	15.9	12.2
Q_{rr} (μC)	8.39	4.65	3.25	1.85

The design limitation of the W_s and Q_p is determined by the degree of electric field shielding effect as needed by the reverse blocking characteristics. The optimized TBJD should be designed to have a proper Q_p and W_s so that the device has the stronger RAT effect without affecting the reverse voltage blocking capability or increasing the leakage current. The most distinctive feature of the TBJD therefore is that, compared with a P-i-N diode, a properly designed TBJD (such as TBJD3) achieves superior reverse recovery characteristics without trading off either the on-state voltage drop or the reverse leakage current.

8.3 Conclusion

TBJDs have been successfully fabricated and their operation has been demonstrated for the first time. The measured on-state voltage of the TBJD is lower than the P-i-N diode fabricated on the same wafer. The TBJD has reverse blocking characteristics similar to the P-i-N diode at both room and elevated temperatures. A dynamic switching test of the TBJD shows improvement in the reverse recovery charge of four times that of the P-i-N diode. It was experimentally confirmed that a properly designed TBJD could achieve superior dynamic characteristics without trading off either the on-state voltage drop or the leakage current, which makes the TBJD stand apart from other power diodes.

References

[1] B. You, A. Q. Huang and J. K. O. Sin, “A new trench bipolar junction diode,” *Proc. ISPSD*, pp. 133-136, 1999.

[2] B. You, A. Q. Huang and J. K. O. Sin, “Analysis of high-voltage trench bipolar junction diode,” *Solid-State Electronics*, vol. 43, no. 9, pp. 1777-1783, 1999.

Chapter 9 Conclusions and Future Work

The research work reported in the dissertation is composed of three portions: investigation of the MOS-controlled thyristor (MCT), exploration of operation mode MOS-gated thyristors (MGT), and development of the Trench Bipolar Junction Diode (TBJD). In the first portion of the work, a comprehensive investigation of the fundamental device characteristics that distinguish the MCT from the IGBT has been undertaken. The second portion of the work explored the dual operation mode MGT with improved performance compared to the conventional MCT. In the third portion of the work, a new power diode called the Trench Bipolar Junction Diode (TBJD) has been developed from a conceptual stage to a fully operational device. The following sections highlight the findings and the conclusions of this research work, and propose possible future work.

9.1 Investigation of the MCT

This aspect of the work was carried out by conducting an extensive comparative study between the MCT and the IGBT through numerical simulation. The apple-to-apple comparison studies have been undertaken at two different levels: unit-cell and multi-cell.

9.1.1 Unit-cell Level

The comparison at the unit-cell level focused on RBSOA characteristics and design tradeoff between the on-state voltage drop (V_F), turn-off loss (E_{off}), and RBSOA of the MCT.

The research work performed a comprehensive theoretical investigation of the turn-off failure mechanisms of the MCT, and identified the voltage versus current locus of the lower open-base transistor in its high-current forward blocking state as the dynamic avalanche limited RBSOA boundary of the MCT. Since the MCT, the IGBT, and other MGT devices all behave as open-base transistors in the turn-off transient, the RBSOA limitations due to the dynamic avalanche are essentially the same for all these devices.

A first-order analytical model, based on the concept of dynamic current gain, was developed to characterize the high-current forward blocking characteristics of the lower open-base transistor of the MCT. A characteristic equation for the dynamic avalanche limited RBSOA boundary of the MCT was developed. It was found that the difference between the dynamic current gain value and the constant critic gain value determines the dynamic avalanche limited RBSOA boundary.

It is the dynamic current gain characteristic of the lower open-base transistor that accounts for the discrepancy between the dynamic avalanche limited RBSOA characteristics of the P-MCT and the N-MCT. It was concluded that the strong voltage-dependent RBSOA characteristics of the P-MCT eventually diminish the benefit of its high maximum controllable current density (J_{mcc}) capability, and the N-MCT is preferred not only from the application point of view, but also from the RBSOA point of view because a relatively square RBSOA can be achieved in the N-MCT, as in the N-IGBT. It was also found that a high upper-base charge is necessary in order to achieve a square RBSOA in the N-MCT due to the modulation effect of the upper base resistance.

While the J_{mcc} of the MCT is always lower than that of the IGBT, the dynamic avalanche limited RBSOA characteristics of the MCT are similar to those of the IGBT. It was found that, under the same V_F condition, the MCT can be irradiated harder or can use a higher buffer charge to achieve an even better dynamic avalanche limited RBSOA characteristic than the IGBT.

The comparative study also confirmed that a MCT structure has a better V_F vs. E_{off} tradeoff than an IGBT structure because the former has a more optimized on-state carrier profile

as a result of its double-side carrier injection. The superiority of the MCT in terms of the V_F vs. E_{off} tradeoff is found more pronounced in the P-type devices than in the N-type devices.

9.1.2 Multi-cell Level

The multi-cell level comparison emphasized the fundamental difference between the MCT and the IGBT in handling the non-uniform turn-off due to the internal propagation gate delay existing within a large-area multi-cell device, which is used to scale up the current handling capability as needed in application.

Compared to the IGBT, the turn-off capability of a multi-cell MCT was found intrinsically more vulnerable to the formation of current filament in the region with the longest gate delay during turn-off due to its lack of current saturation capability. A multi-cell IGBT is less sensitive to gate delays, and more likely to survive a non-uniform turn-off because of its unique current saturation characteristic.

It was also found that increasing the J_{mcc} capability of the unit-cell of the MCT is not an effective solution to this problem. Reducing the internal propagation gate delay is therefore particularly important in the realization of a large-area MCT.

However, the research work only qualitatively illustrated the difference between the turn-off capabilities of a multi-cell MCT and a multi-cell IGBT, using a simplified two-lumped-device model to represent the multi-cell device. A distributed device model provides more accurate representation of the multi-cell device. Further investigation is needed in order to quantify the non-uniform turn-off capability of a large-area multi-cell MCT.

9.2 Exploration of Dual Operation Mode MGTs

Dual operation mode MGT devices possess current saturation or current-limiting capability, a feature not available in the conventional MCT. A dual operation mode MCT also

overcomes the tradeoff between the on-state conduction loss and the current saturation capability of the conventional IGBT by working in a thyristor mode in the on state and in an IGBT mode during the switching transient period.

While dual operation mode MGT devices have been previously reported, this is the first time the switching performance of a dual operation mode MCT with superior current saturation capability in a hard-switching application has been investigated. The experimental dual operation mode MCT was fabricated by using an advanced high-channel-density MCT process. The dual operation mode MCT was experimentally shown to have a lower on-state voltage drop and superior current saturation capability compared to the IGBT.

It has been demonstrated that the dual operation mode MCT could greatly lower the stress on the associated freewheeling diode in the hard-switching application to make the diode selection easier. However, it was found that the reduction of reverse recovery loss on the diode is achieved at the cost of increased turn-on loss on the dual operation mode MCT. It was also found that the dual operation mode MCT does not have any significant impact on the overall turn-off loss of the device compared with the conventional MCT.

The gate-controlled current saturation feature of the dual operation mode MCT in the IGBT mode operation can be used in the typical PWM phase leg to moderate turn-on di/dt and significantly lower the reverse recovery stress on the freewheeling diode. If the current saturation region (i.e. FBSOA) is large enough, the dual operation mode MCT will be able to operate in existing systems to replace the IGBT for higher efficiency.

The dual operation mode MGT devices that are compatible with the IGBT process were analyzed with the aid of two-dimensional numerical simulations and first-order analytic models developed to characterize their maximum controllable current densities (J_{mcc}) in the IGBT mode operation. A novel device structure was proposed and fabricated. It was experimentally demonstrated that the novel device structure has a higher J_{mcc} capability than the previously reported dual operation mode MGT structures that are compatible with the IGBT process.

The major limitation of the dual operation mode devices is the difficulty in laying out a large-area device, since they all have two electrically separate gates. In this work, a stripe layout

approach was used in the design of the dual operation mode devices. The gates of the cells located at the center of the device rely on a long horizontally run polysilicon to make connection with the gate electrode located at the perimeter. The large RC time constant as seen by the center cells limits the maximum area of the device. How to scale up the current handling capability of the dual operation mode device needs further exploration.

9.3 Development of the TBJD

A new high-voltage Trench Bipolar Junction Diode (TBJD) has been proposed and demonstrated to have superior characteristics over the conventional P-i-N diode.

The TBJD controls the anode injection efficiency by the action of a reverse active transistor (RAT) structure integrated on its anode junction. The RAT helps tailor an optimized on-state carrier profile to improve the diode switching characteristics without compromising the on-state voltage drop. The thin P base of the RAT is shielded by a deep P+ region formed by refilling P+ polysilicon into a deep trench. The deep P+ region not only prevents the thin P base of the RAT from being punched through in the reverse blocking state, but also effectively suppresses the dynamic parasitic transistor effect. The electric field shielding effect helps the TBJD maintain the same leakage current level as the conventional P-i-N diode. These unique features make TBJD suitable for high-voltage applications.

The TBJDs have been successfully fabricated with a novel self-aligned trench process. The measured on-state voltage of the TBJD is lower than that of the P-i-N diode fabricated on the same wafer. The TBJD has reverse blocking characteristics similar to the P-i-N diode at both room and elevated temperatures. A dynamic switching test of the TBJD shows improvement in the reverse recovery charge of four times that of the P-i-N diode. It was experimentally confirmed that an optimized TBJD could achieve superior dynamic characteristics without

trading off either the on-state voltage drop or the leakage current level, which makes the TBJD stand apart from other power diodes.

Appendix: Process Flow of the TBJD

Step	Operation	Process Description
1	Field oxidation (1 μm) #13,14,15,18,c1,c2,c3,c4 #13,14,15,18	 1.1 RCA cleaning 1.2 Thermal oxidation: temp: 1100 ^{o}C t =5'DO_2+150'WO_2+5'DO_2+20'N_2
2	P+ edge termination #13,14,14,18 #13,14,14,18,c4	Mask 1 (TER: clear field) 2.1 HMDS, PR coating, soft bake, expose (Mask 1), hard bake, develop, descum 2.2 BOE etching: remove ~ 1μm SiO_2 2.3 Remove resist 2.4 Piranha cleaning 2.5 Boron pre-deposition temp: 1050 ^{o}C, t=60' boron (B_2O_3) 2.6 Drive-in Temp: 1050 ^{o}C t=30' DO_2+180' WO_2+10' DO_2+240' N_2
3	Active area definition #13,14,14,18	Mask 2 (BAS: clear field) Mask 3 (SNE: clear field) 3.1 HMDS, PR coating, soft Bake, expose (Mask 1), hard bake, develop, descum

		3.2 BOE etching: remove ~ 1.5 μm SiO_2 3.3 Remove resist 3.4 Piranha cleaning 3.5 HMDS, PR coating, soft bake, expose (Mask 2), hard bake, develop, descum 3.6 BOE etching: remove ~ 1.5 μm SiO_2 3.7 Remove resist
4	Base implant & drive #13,14,14,18,c1,c2,c3,c4 #13,14,14,18, #13,14,14,18,c1,c2,c3 #13,14,14,18,c1,c2,c3,c4 #13,14,14,18,c1,c2,c3,c4 #13,14,c1,c2 #13,c1	Mask 2 (BAS: clear field) 4.1 Piranha cleaning 4.2 Grow screen oxide 200 A temp: 950 ^{o}C, t=30' DO_2 4.3 HMDS, PR coating, soft bake, expose (Mask 2), hard bake, develop, descum Boron implantation 8e14, 40 keV Strip resist (plasma) Piranha cleaning 4.7 Drive-in: temp=1050 ^{o}C, 360' N_2 4.8 Drive-in: temp=1050 ^{o}C, 60' N_2 4.9 Drive-in: temp=1050 ^{o}C, 60' N_2
5	Emitter implant & drive #13,14,15,18 #13,14,15,18,c1,c2,c3 #13,14,15,18,c1,c2,c3	Mask 3 (SNE: clear field) 5.1 Piranha cleaning 5.2 HMDS, PR coating, soft bake, expose (Mask 3), hard bake, develop, descum 5.3 Phosphorus implantation 8e15, 100 keV Strip resist (plasma)

	#13,14,15,18,c1,c2,c3,c4	Piranha cleaning
	#14,15,18,c2,c3,c4	5.6 Drive-in: temp=1050 ^{o}C, 60' N_2
	#15,18,c3,c4	5.7 Drive-in: temp=1050 ^{o}C, 60' N_2
7	Oxidation (0.6μm)	
	#13,14,15,18,c1,c2,c3,c4	7.1 Piranha cleaning
		7.2 Oxidation
		temp: 1050 ^{o}C,
		t=5' DO_2+60' WO_2+5' DO_2+5' N_2
8	Trench etching	Mask 4 (PPT: clear field)
	#13,14,15,18,c1,c2,c3	8.1 HMDS, PR coating, soft bake, expose (Mask 4), hard bake, develop, descum
		8.2 Dry etching: remove ~ 0.6 um SiO_2
	#13,14,15,c1,c2,c3	8.3 RIE etching trench (target 3 μm)
		SF_6:F115=120:120, 8'
	#18	8.4 RIE etching trench (target 7 μm)
		SF_6:F115=120:120, 18'
	#13,14,15,18,c1,c2,c3	8.5 Remove resist
9	Poly refilled and doped	
	#13,14,15,18,c1,c2,c3	9.1 Piranha cleaning
		9.2 First LPCVD poly-Si
		temp: 620 ^{o}C
		target: 6000 A
		9.3 Boron diffusion
		temp: 1050 ^{o}C, t=30'
		9.4 Second LPCVD poly-Si
		temp: 620 ^{o}C
		target: 2 um

		9.3 Boron diffusion temp: 1050 ^{o}C, t=30’
10	Poly planarization #13,14,15,18,c1,c2,c3	10.1 Plasma etching poly-Si: SF_6, F115, 150mTorr, 500W target: remove 2.6 um poly-Si
11	Contact formation #13,14,15,18	Mask 5 (CNT: clear field) 11.1 Piranha cleaning 11.2 HMDS, PR coating, soft bake, expose (Mask 5), hard bake, develop, descum 11.3 BOE etching: remove ~ 1.8 um SiO_2 11.4 Remove resist
12	Metalization	Mask 6 (MTL: dark field) 12.1 Piranha cleaning 12.2 Sputtering 3 um Al 12.3 HMDS, PR coating, soft bake, expose (Mask 6), hard bake, develop, descum 12.3 Wet etching: remove 3 um Al Remove resist 12.5 Annealing temp: 400 ^{o}C, t=30 ' H_2:N_2=1:8
13	Passivation	Mask 7 (PSS: clear field) 13.1 PECVD SiN 13.2 HMDS, PR coating, soft Bake, expose (Mask 7), hard bake, develop, descum 13.3 Wet etching: remove 3 um Al Remove resist

14	Lapping and polishing	
15	Backside metalization	

Vita

The author, Budong You, was born in Yongding, Fujian, China, in October 1971. He received the B.S. degree in Electronic Engineering from Zhejiang University, Hangzhou, China, in 1992, and the M.S. degree in Electrical Engineering from Virginia Polytechnic Institute and State University (Virginia Tech), Blacksburg, Virginia, in 1997. Since 1995, he has been with the Virginia Power Electronics Center, now Center for Power Electronics Systems, in Virginia Tech, as a graduate research assistant. His research interests include power semiconductor devices and integrated circuit technology.

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