IPC-J-STD-001 Rev G, Amendment 1, Section 8 Cleanliness Section SIR Test Method for Developing Objective Evidence for the Production Assembly

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Abstract
Since the 1970s, ROSE testing was used to determine "clean enough." In 2015, the J-STD-001 committee assigned a team to develop the next generation of "cleanliness" requirements. Section 8 defines the key concepts that drove the need for developing new cleanliness requirements.

- ROSE testing for product acceptance (pass-fail) is an ***obsolete*** practice for determining ***acceptably*** clean
- ROSE testing for process control is perfectly acceptable, but the numbers have to MEAN something. And those values need to be scientifically/statistically determined
- No one set value defines the line between acceptably clean and unacceptably dirty
- No one ***method*** determines acceptably clean and unacceptably dirty

A qualified manufacturing process should be determined using some form of temperature-humidity-bias sort of testing (such as SIR). Qualifying a manufacturing process through chemical analysis alone (e.g., ion chromatography) does not tell you the effects of the residue under humid conditions, which is where electrochemical failures occur. Companies that have come up with ionic standards by IC also use temperature-humidity-bias (THB) testing somewhere in their qualification process.

The purpose of this paper is two-fold: 1. Research on the development of temperature-humidity-bias instrumentation and test board designs forproduct acceptance. 2. Follow on DOE to better understand the impact of cleanliness at the bottom termination of the QFN/BTC component.

Introduction
The electronics manufacturing process has many variables that impact the quality and reliability of the manufactured assemblies in the end use environment[1]. Two of the critical variables for consideration are the ionic nature of the residues, which are present on the electronic assembly post soldering and the effects these residues have on reliability. While there are several ways to measure residues and their impact on electrical performance, the two most common approaches are ionic cleanliness testing and surface insulation resistance (SIR) testing.

Electronic devices have evolved into highly complex architectures and larger form factors. Increased density and miniaturizationincreases the sensitivity of the assemblies to ionic residues and may impact device reliability. A large number of surface mount components are leadless such as BTCs and LGAs (Bottom Terminated Components and Land Grid Arrays). The bottom termination can comprise a high number of interconnects and thermal paddles. The gap from the surface of the board to the bottom of the assembly is increasingly narrow. Residues trapped under the bottom termination may not reach proper activation temperatures due to blocked outgassing channels. Even when using a no-clean solder paste, flux residues may be active due to these complexities and challenges.

The J-STD-001 standard document is designed to regulate the production of printed circuit boards[2]. A committee made up of knowledge experts formed a working group to determine the "next generation" cleanliness guidelines and standards requirements[3]. Objective Evidence requires an assembler to have documented evidence that the methods used in the design, process development and process control comprise documented proof that the assembly process produces an acceptable product.

Research Grant

Realizing that many of the present methods of ionic assessment or SIR evaluations were beyond the reach of small-to-medium sized assemblers, a research grant was issued by a government entity to research cleanliness test methods that can be implemented at the assembly site to test the effects of residues present on production assemblies. The purpose of the grant was to develop tools which would allow a small to the mediumuser to generate objective data to meet the requirements of acceptably clean and unacceptably dirty. Section 8.1 defines a Qualified Manufacturing Process – "Unless otherwise specified by the User, the Manufacturer shall [N1D2D3] qualify solderingand cleaning processes that result in acceptable cleanliness levels of flux and other residues. Objective evidence shall [N1D2D3] be available for review[4]."

Methodology

Surface Insulation Resistance (SIR) is a quantitative test method that has been with the electronics industry since the advent of the transistor and the printed board[5]. Electrochemical reactions at or below the surface of electronic circuits will affect surface insulation resistance values. The test is conducted on specifically designed test boards that are representative of production hardware. The test requires the presence of humidity and electrical bias to evaluate the mobility of ionic contamination left on the PCB during the assembly process.

SIR test methods can be used to test electrochemical reactions on incoming bare boards; residues left behind from soldering materials; reflow process conditions; No-Clean processing; cleaning processes; and effects from handling. SIR is commonly performed by reliability laboratories and at some larger original equipment manufacturers (OEMs) and contract manufacturers (CMs). SIR is a highly sensitive method. IPC approved test boards populated with components that match up to production hardwarecontain sensor traces in areas where flux residue and other contaminants are present.Temperature-humidity-bias(THB) test methods quantitatively detect the activity of those residuesat the test location and can be used to predict the reliability of electronics placed in service.

Even though SIR is considered the best method for detecting the impact of ionic residues left on the assembly, the lack of availability at the production site limits the use of this test method for process control. The research grant focused on addressing these limitations with the objective being to design SIR instrumentation for use in system design, process development, process control and quality assurance at the production site.

System design focused on the following attributes:

1. Test Board Designs
2. Test Instrumentation
3. Common Data Structure
4. Real-Time Data Analytics
5. Reporting
6. Trend Analysis
7. System Diagnostics

IPC-B-52 Test Board Design

Test vehicles representative of the electronic circuits used in production allows the process engineer to assess whether or not their assemblies have electrochemical risks. The test used for *Process Qualificationand Process Control* demonstrates that a proposed manufacturing process or process change can produce hardware with acceptable end-item performance related to cleanliness[6]. Changes may involve any assembly process step, or a change in the printed board supplier, solder mask, plating,metallization, soldering material supplier, conformal coating, etc. The test vehicle construction will vary dependent on the component sets used on production hardware. Focusing the investigation on the most problematic components enables the process engineer to select test boards designed with specific component configurations for determining acceptable cleanliness and objective evidence that the process is meeting acceptable cleanliness levels.

The IPC-B-52 test board, designed with a range of components, and tested to IPC-9202 protocols, has been successfully used by many to examine the electrochemical risk in their assembly processes. This test board represents some of the more challenging to clean components used on production hardware. The test board in Figure 1 shows only the SIR portion. The board contains 14 SIR test patterns[6] (Figure 1). The test board also allows up to two SIR test patterns to be added to the test vehicle, such as the QFN bottom terminated component.

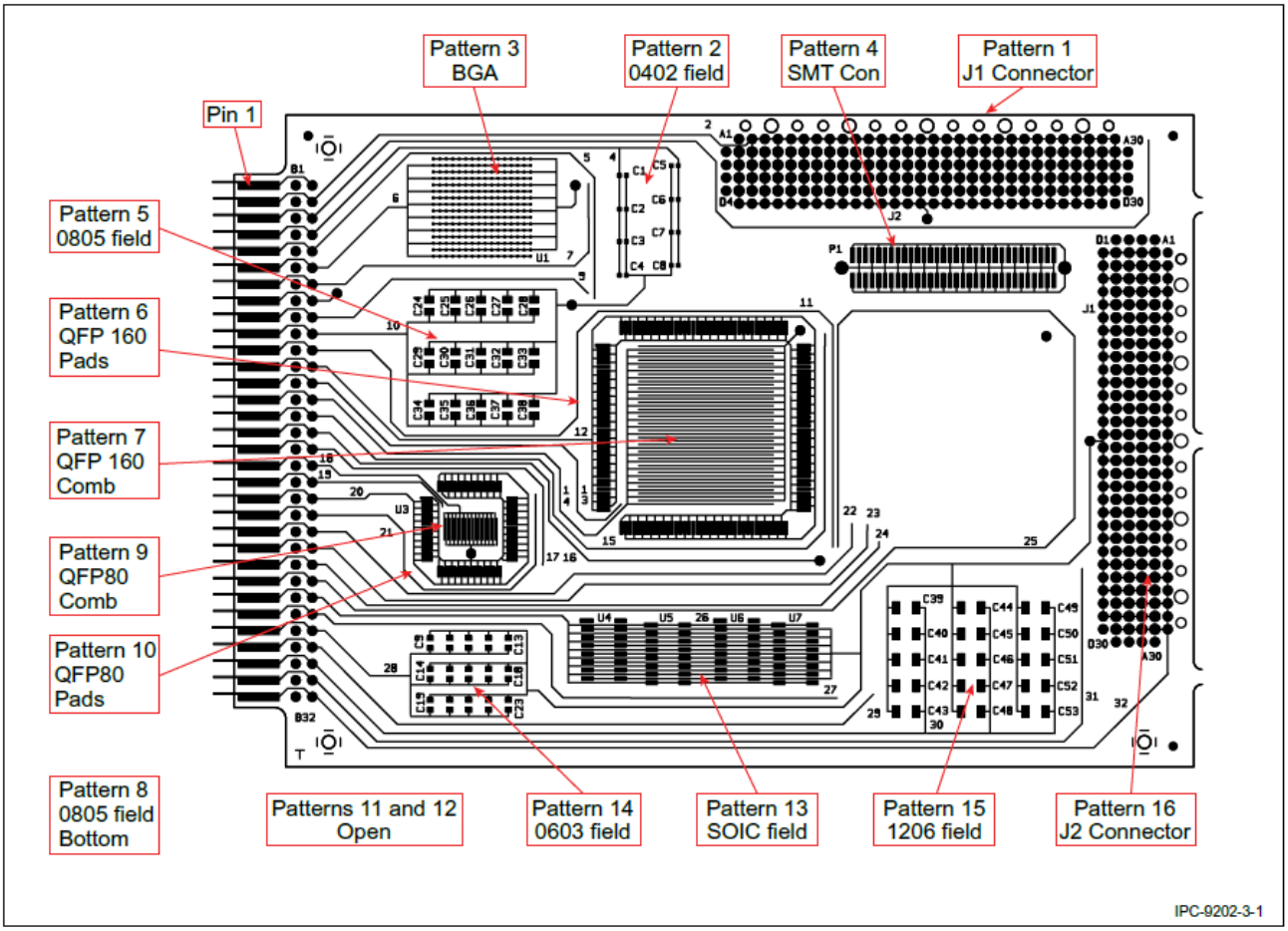


Figure 1: IPC-B-52 SIR Test Board

While the B-52 board, designed in the early 2000s, has proved to be a good test vehicle for characterizing the impact of assembly residues, it does not have some of the more challenging component geometries (e.g., BTCs) or solder mask configurations under such challenging components. In the development of the SIR test system, it was desired to take assembly testing to the next level and address such challenging components. The goal was to build correlations back to the existing process knowledge base on the IPC-B-52 test board. The first alternative SIR test vehicle is shown in Figure 2. The results of the testing of this prototype card and associated SIR system have been widely published[7, 8, ...29]. New test board designs will be presented in the follow-on research portion of thispapertodevelop correlations to IPC-B-52 test patterns on some of the more challenging to clean components.

QFN Test Board with Parallel Nets on the Front and Back Side

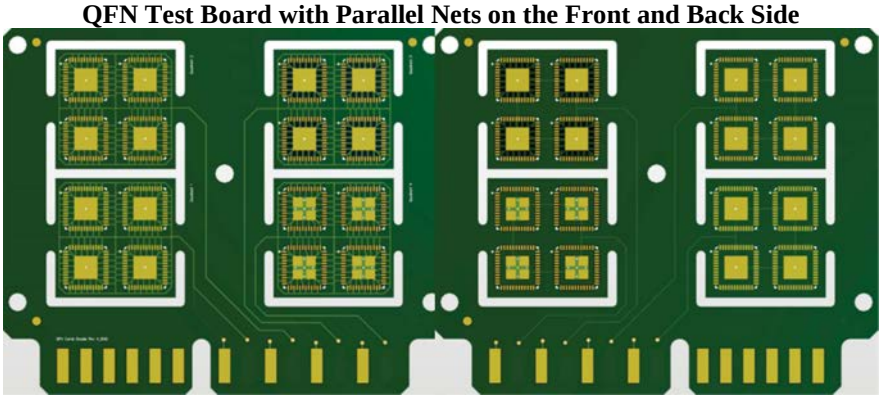


Figure 2: BTC Test Board populated with the QFN Component

The question many ask is "What constitutes Good SIR Data?" Pauls (2018) built a chart showing LogOhm resistivity values on the Y-axis and measurement time on the X-axis[28].As illustrated in Figure 3, LogOhm resistance values less than 7 Logohms (10 megohm resistance) indicates current leakage or dendritic growth formation, values in the range of 7-8

Logohms (10-100 megohms resistance) suggests an area for concern, while values above 8 Logohms (above 100 megohm resistance) indicates the circuit is typically reliable. It should be noted that the "zones" in Figure 3 represent experience with the IPC-B-52 test assembly and its SIR patterns, which may not translate exactly for other SIR patterns, or pattern geometries. However, these guidelines were used for this experiment in assessing the data.

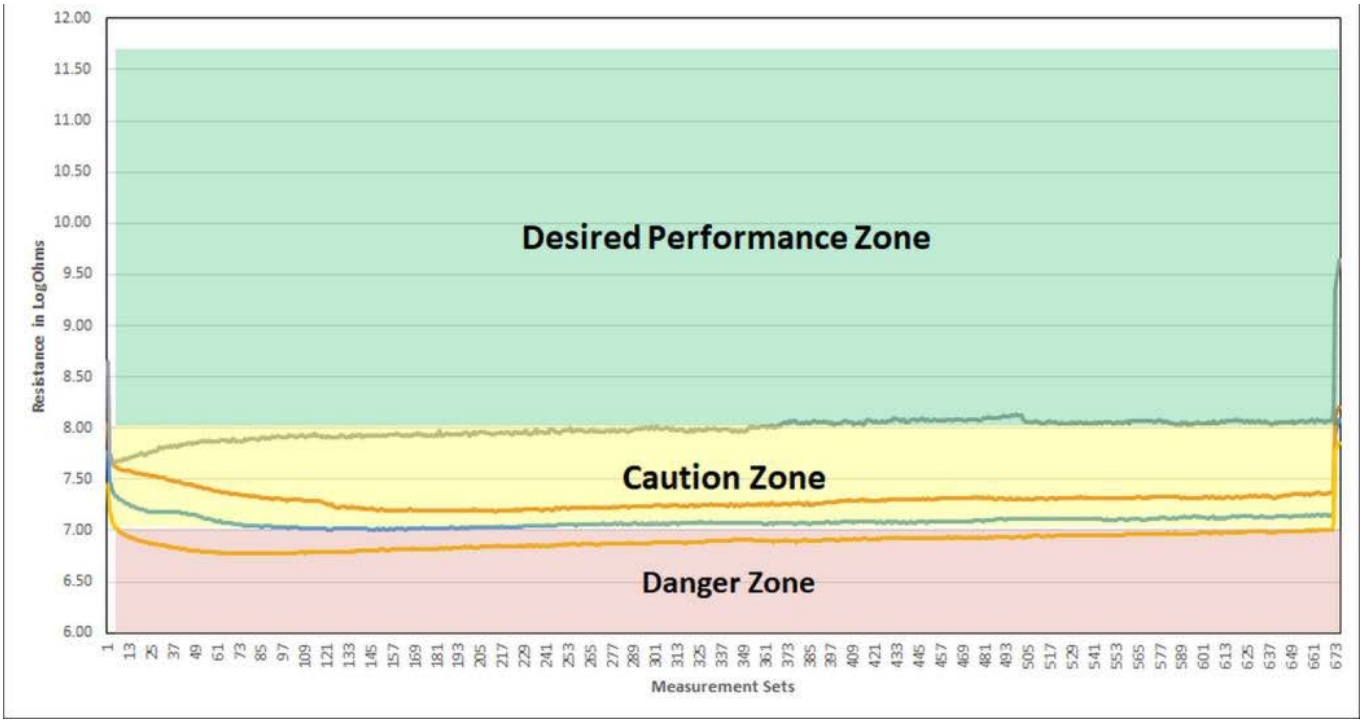


Figure 3: Desired Good / Cautious / Danger SIR Zones

Experimental

Surface Insulation Resistance (SIR), as defined by IPC[2], is the electrical resistance of insulating material between a series of positive and negative conductors. SIR testing discriminates the impacts of contamination between components, solder masks, solder pastes, reflow conditions, cleaning agents and cleaning machines. SIR testing can also be used to define the electrical performance of residual contamination such as when using a no-clean process, rework, and touch-up processing.

The QFN test board shown in Figure 2 was used for this research study. SIR traces, routed under the bottom terminations, on a net of QFN components, were tested under specified environmental and electrical conditions. The DOE study was done to evaluate the cleanliness of the QFN component and its ability to resist "failure" in the form of current leakage or an electrical short (i.e., dendritic growth). The environmental conditions were performed under elevated temperature and humidity conditions (40°C/90% RH). Insulation resistance (IR) measurements were taken every 20 minutes over the life of the test with a bias voltage of 8 volts DC used for both resistance measurements and for biasing the patterns between measurement sets.

The test boards were soldered with two different No-Clean solder pastes. A prior study using the QFN test board and the two No-Clean solder pastes resulted in SIR values that were in either the Caution or Danger zones (see Figure 3). The QFN test boards were processed at standard and fast inline cleaning belt speeds. At these throughput rates, the wash time ranged from 2.5 minutes at the standard time and 1.5minutes for the fast time.

The SIR versus Time for the SnPb (tin-lead) solder paste processed at the slow condition, which equates to roughly 2.5 minutes of wash chemistry exposure resulted in low SIR Values (Figure 4). The SIR versus Time for the SnPb solder paste processed at the fast condition, which equates to roughly 1.5minutes of wash chemistry exposure also resulted in low SIR values (Figure 6). The data findings indicate that active residue was still present under the QFN bottom termination at both the slow and fast wash exposure times.

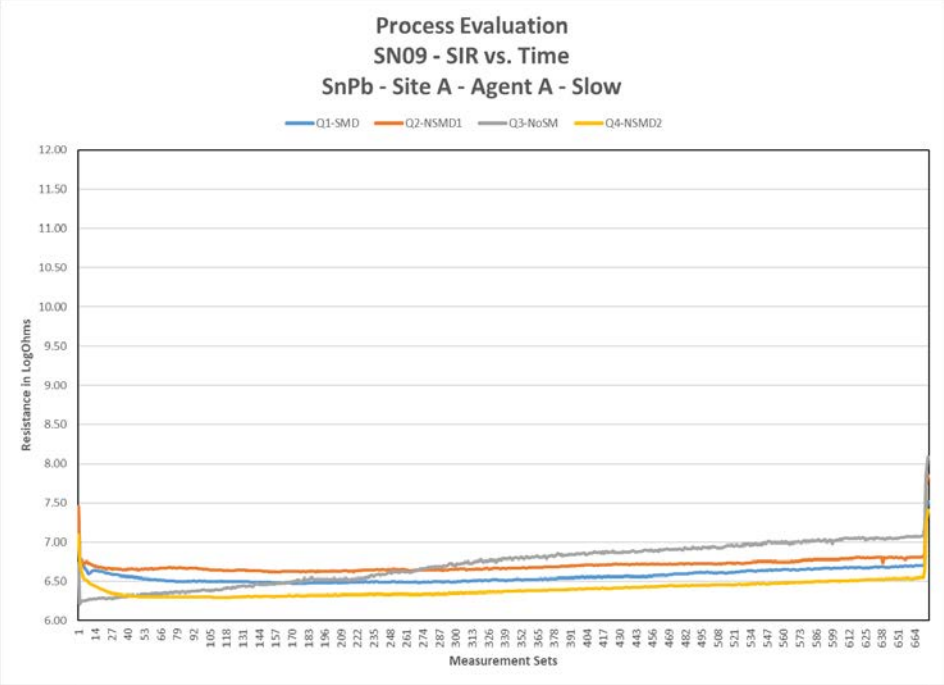


Figure 4: SnPb 2.5 Minute Wash Exposure

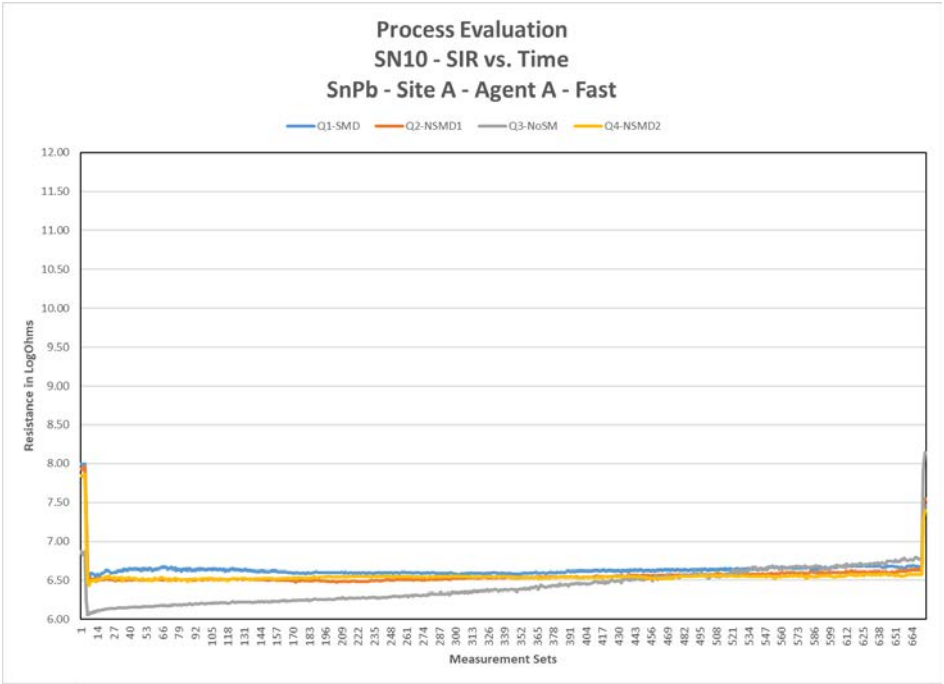


Figure 5: SnPb 1.5 Minute Wash Exposure

The SIR versus Time for the Pb-Free (Lead-Free) solder paste processed at the slow condition, which equates to roughly 2.5 minutes of wash chemistry exposure resulted in cautionary SIR Values (Figure 6). The SIR versus Time for the Pb-Free solder paste processed at the fast condition, which equates to roughly 1.5minutesof wash chemistry exposure showed slightly better SIR values (Figure 7). The data finds that Pb-Free SIR values were better than the SnPb SIR. This indicates that either the Pb-Free flux component is not as active or cleaned better than the SnPb flux component. Even so, the SIR values were still in the Caution or Danger zones.

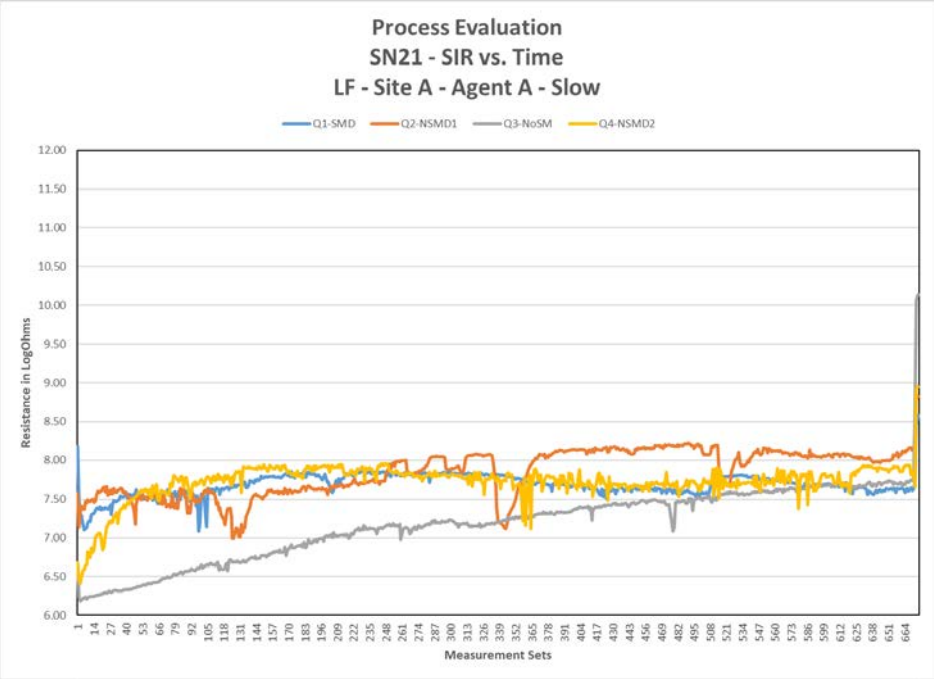


Figure 6: Pb-Free 2.5 Minute Wash Exposure

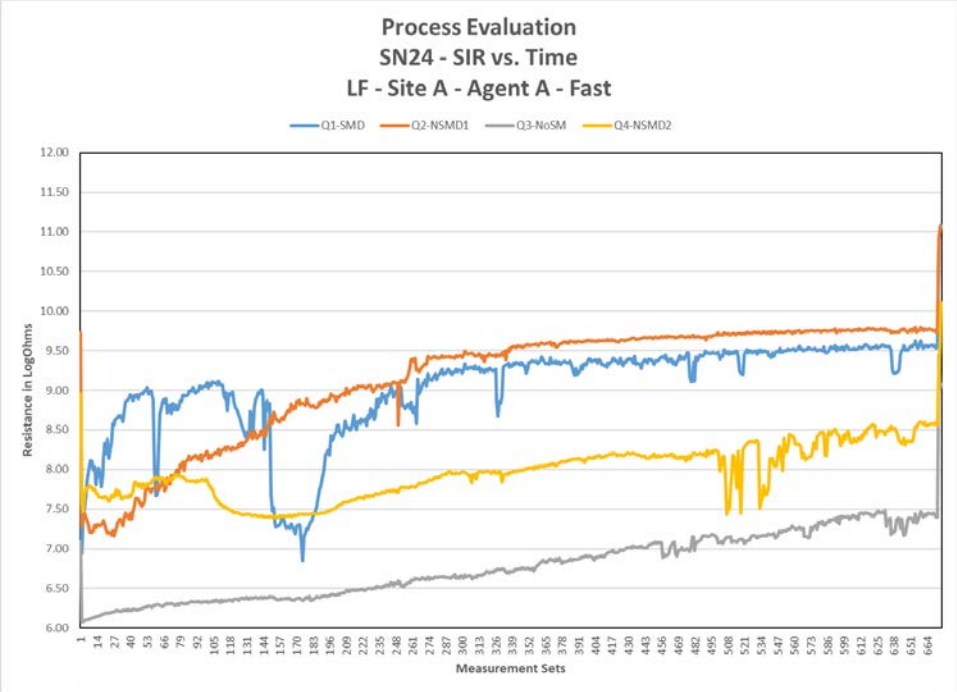


Figure 7: Pb-Free 1.5 Minute Wash Exposure

Second DOE Test Parameters – Longer Wash Cycle Study

The DOE run for this study exposed the QFN test board to longer wash times to determine if the SIR values improved. Three cleanliness conditions were evaluated: 1. Not Cleaned; 2. Wash Chemistry Time = 10 minutes; and 3. Wash Chemistry Time = 5 minutes. Table 1 lists the DOE matrix. Eight test boards were used for this study. Table 1 lists factors and levels. The Bias, Temperature, Environment and Time used for this DOE are listed below.

- Bias: 8 volts – Note, bias can be set between 1 and 40 volts,but 8 volts was chosen for this series of tests because of the defense agencies preference was advised in the previous testing.
- Temperature: 40°C
- Environment: 90% RH
- 336 Hours

The SIR instrument developed from the research grant was used for this study. The system contains a high impedance meter, power supply, matrix cards, shielded cabling, environmental chamber, and 8-slot edge-card test fixture. The 32 channel design takes a reading every 20 minutes. The user interfaceis designed to processthe card stats and exponential / Logohm charts as the test is being run. A solid-state temperature-humidity sensor is embedded in the edge-card test fixture with the values displayed as the test is being run.

Figure 8: Test Instrument (Left) and Fixture (Right) Located in the Environmental Chamber

Table 1: DOE 2 Matrix

Card #	Solder Paste	Cleaning Agent	Cleaning Tool	Wash Time	Wash Conc.	Wash Temp.
1	Tin-Lead NC	N/A	N/A	Not Cleaned	N/A	N/A
2	Tin-Lead NC	Engineered Aqueous	Inline Spray-in-Air	10 minutes	15%	140-150F
3	Tin-Lead NC	Engineered Aqueous	Inline Spray-in-Air	3.5 minutes	15%	140-150F
4	Lead-Free NC	N/A	N/A	Not Cleaned	N/A	N/A
5	Lead-Free NC	Engineered Aqueous	Inline Spray-in-Air	10 minutes	15%	140-150F
6	Lead-Free NC	Engineered Aqueous	Inline Spray-in-Air	3.5 minutes	15%	140-150F
7	Bare QFN Board	N/A	N/A	N/A	N/A	N/A
8	Known Resistor Card 6-7-8-9 (Figure 8)	N/A	N/A	N/A	N/A	N/A

Data Findings:
A bare QFN board was placed into Slot 7. The unprocessed control boardwas used to verify that the board surface is free of harmful residues. The controlboards' exponential resistance values ranged in the 11-12 Logohms, which indicates that the bare board is clean (Figure 19).

Card 7: Bare Board Control

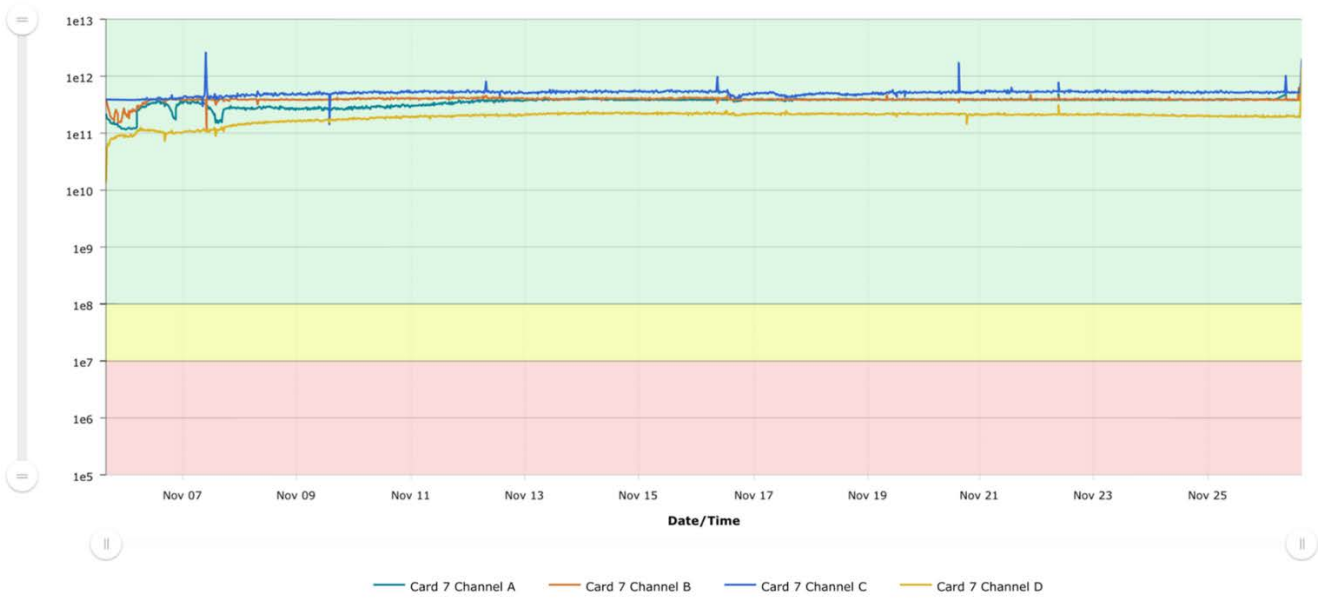
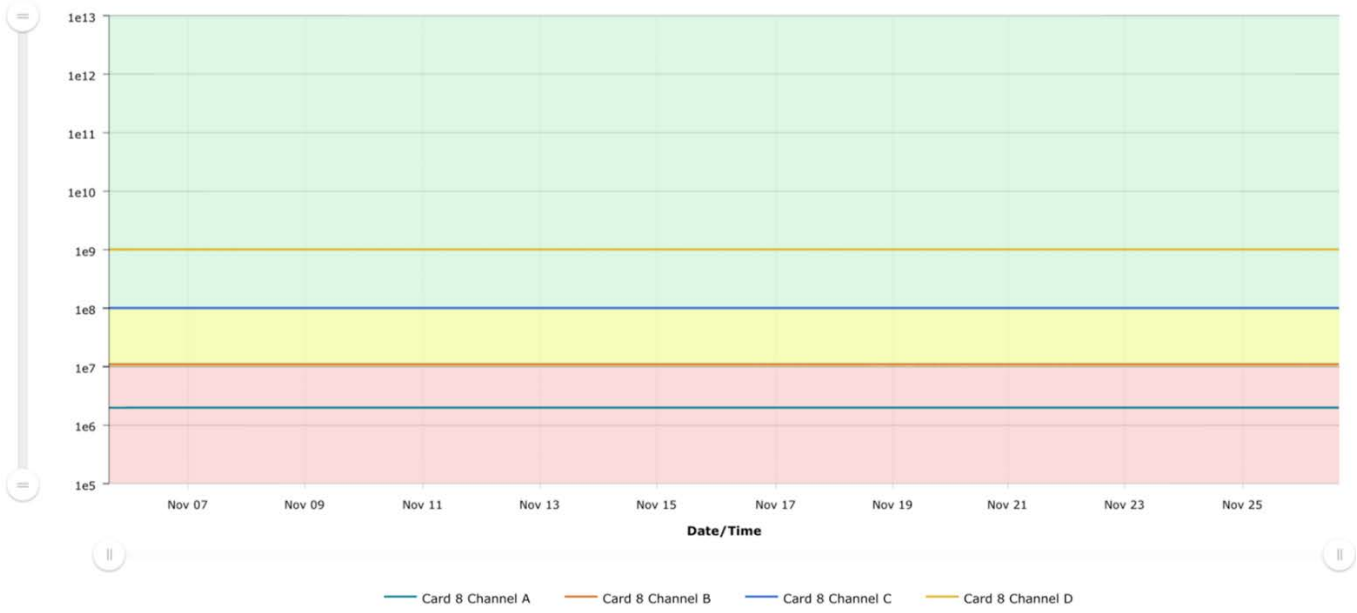


Figure 19: Unprocessed Control Board Card Stats and Chart

A validation resistor board was placed into Slot 8. The validation resistor board contains a 6-megohmresistorin Quadrant 1, 7-megohmresistorin Quadrant 2, 8-megohmresistor in Quadrant 3 and 9-megohmresistor into Quadrant 4. Figure 10 chart and card stats find that the system readings for the validation test card were in line with each of these known resistors, which confirms that the system measurements are accurate. Note, the red color was placed in the chart to highlight the range of the resistor values.

Card 8: Validation Resistor Board



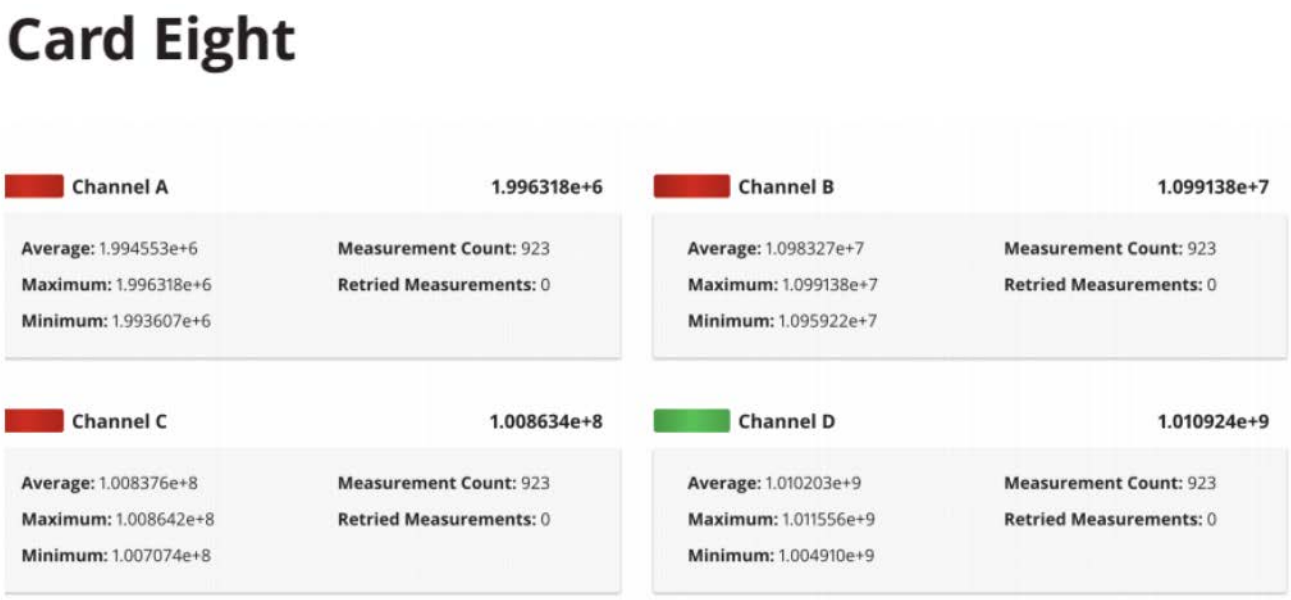


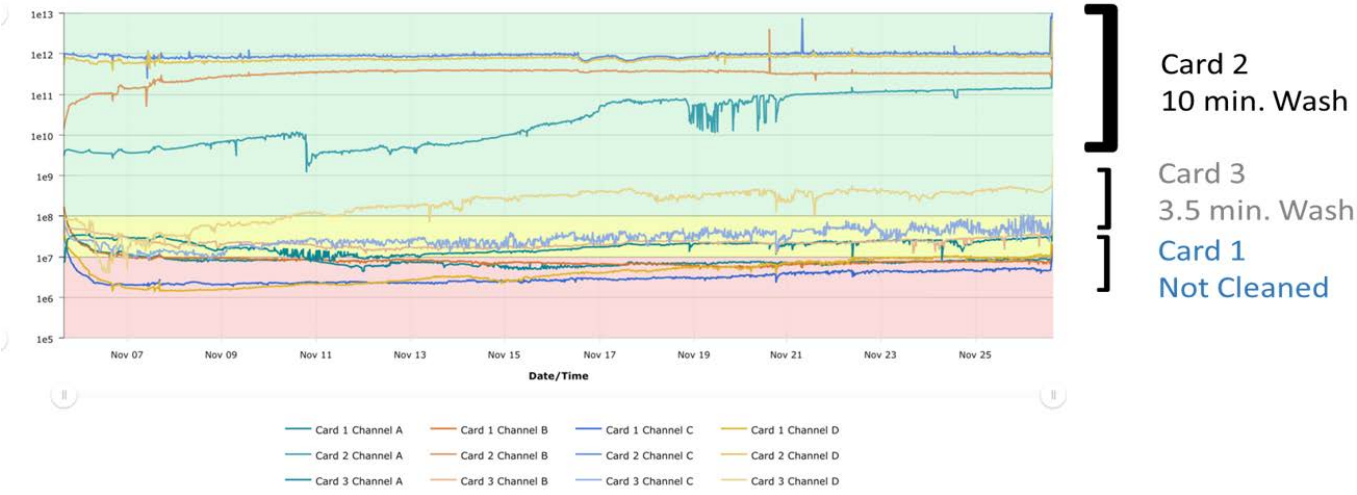
Figure 20: Validation Resistor Test Board Chart and Card Stats

The SIR values for SnPb Solder Paste #1 find significant differences in the test results based on the cleanliness levels of the board tested.

- Card 1: SnPb SP #1 was not cleaned post soldering
- Card 2: SnPb SP #1 was cleaned. The board was exposed to 10 minutes in the wash zone.
- Card 3: SnPb SP #1 was cleaned. The board was exposed to 3.5 minutes in the wash zone

The SIR values charted over the life of the test for the three test boards is shown in Figure 21. Card 2, exposed to 10 minutes wash time finds good SIR values over the four channels. Card1, not cleaned board SIR values were in the CautionandDanger zones. Card 3, exposed to 3.5 minutes of wash time SIR values were in the caution and danger zones.

Cards 1, 2 and 3: Tin-Lead (SnPb) SIR Values



Card One: Tin-Lead (SnPb Not Cleaned)

Channel A 7.158324e+6

Average: 7.234255e+6
Maximum: 1.604681e+8
Minimum: 4.365588e+6
Measurement Count: 807
Retried Measurements: 0

Channel B 5.324849e+6

Average: 5.720149e+6
Maximum: 1.737011e+8
Minimum: 5.001810e+6
Measurement Count: 807
Retried Measurements: 0

Channel C 3.530271e+6

Average: 3.526365e+6
Maximum: 5.472017e+7
Minimum: 1.599001e+6
Measurement Count: 807
Retried Measurements: 0

Channel D 6.327697e+6

Average: 6.426918e+6
Maximum: 5.248775e+7
Minimum: 1.398506e+6
Measurement Count: 807
Retried Measurements: 0

Card Two: Tin-Lead (SnPb 10min. wash)

Channel A 8.836389e+10

Average: 7.862999e+10
Maximum: 9.682068e+10
Minimum: 1.241915e+9
Measurement Count: 807
Retried Measurements: 0

Channel B 3.331603e+11

Average: 5.539426e+11
Maximum: 3.965322e+12
Minimum: 3.256841e+11
Measurement Count: 807
Retried Measurements: 0

Channel C 1.020173e+12

Average: 9.816762e+11
Maximum: 1.224774e+12
Minimum: 2.498291e+11
Measurement Count: 807
Retried Measurements: 0

Channel D 8.435301e+11

Average: 8.625728e+11
Maximum: 1.102724e+12
Minimum: 3.837136e+11
Measurement Count: 807
Retried Measurements: 0

Card Three: Tin-Lead (SnPb 3.5min. wash)

Channel A	2.175685e+7	Channel B	2.112554e+7
Average: 2.071692e+7	Measurement Count: 807	Average: 2.141720e+7	Measurement Count: 807
Maximum: 3.674613e+7	Retried Measurements: 0	Maximum: 5.031377e+7	Retried Measurements: 0
Minimum: 7.180296e+6		Minimum: 1.214261e+7	

Channel C	3.541044e+7	Channel D	4.036020e+8
Average: 3.849942e+7	Measurement Count: 807	Average: 4.053892e+8	Measurement Count: 807
Maximum: 8.538978e+7	Retried Measurements: 0	Maximum: 4.841867e+8	Retried Measurements: 0
Minimum: 7.428092e+6		Minimum: 3.890054e+6	

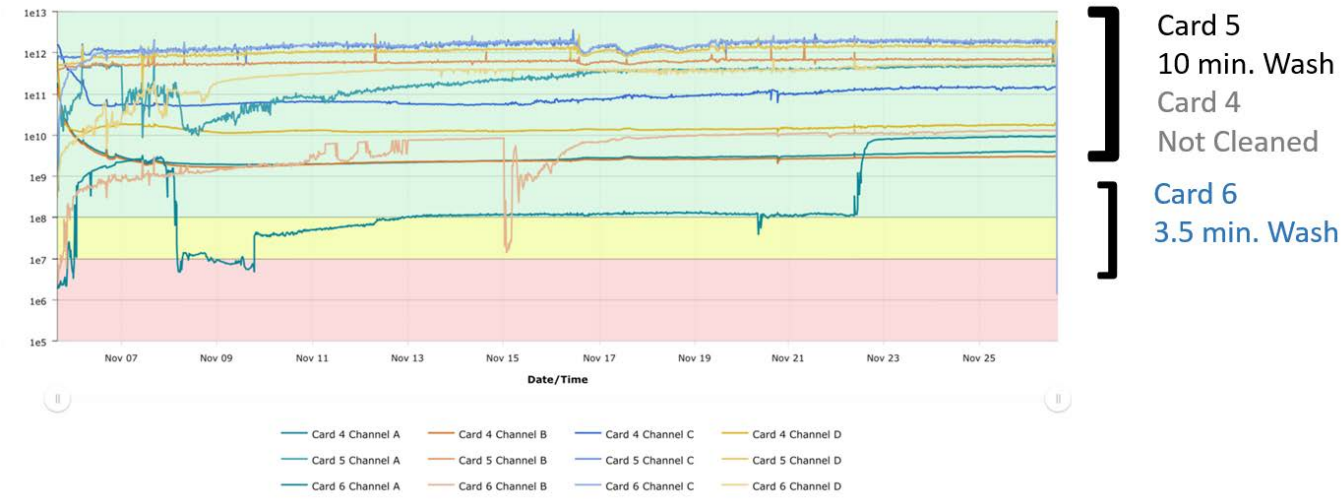
Figure 21: SnPb Solder Paste #1 Chart and Card Stats

The SIR values for Pb-Free Solder Paste #2 find that Card 4 and Card 5 were significantly better than Card 6.

- Card 4: Pb-Free SP #2 was not cleaned post soldering.
- Card 5: Pb-Free SP #2 was cleaned. The board was exposed to 10 minutes in the wash zone.
- Card 6: Pb-Free SP #2 was cleaned. The board was exposed to 3.5 minutes in the wash zone.

The SIR values charted over the life of the test for the three test boards is shown in Figure 22. Card 5, exposed to 10 minutes wash time find good SIR values over the four channels. Card 4, the not cleaned board find good SIR values. Card 6, the board with 3.5 minutes of wash time exhibited caution zone SIR values. The residue condition for the Pb-Free solder paste was less active than was the residue condition for the SnPb solder paste. For both solder pastes, longer wash exposure times resulted in good SIR values.

Cards 4, 5 and 6: Lead-Free (Pb-Free) SIR Values



Card Four: Lead Free (Pb-Free - Not Cleaned)

Channel A 3.071751e+9

Average: 3.037644e+9
Maximum: 1.849810e+11
Minimum: 1.888919e+9
Measurement Count: 807
Retried Measurements: 0

Channel B 2.707167e+9

Average: 2.708172e+9
Maximum: 1.423027e+11
Minimum: 1.651089e+9
Measurement Count: 807
Retried Measurements: 0

Channel C 1.239351e+11

Average: 1.133712e+11
Maximum: 1.583471e+12
Minimum: 3.856163e+10
Measurement Count: 807
Retried Measurements: 0

Channel D 1.453835e+10

Average: 1.422784e+10
Maximum: 6.884983e+11
Minimum: 1.101882e+10
Measurement Count: 807
Retried Measurements: 0

Card Five: Lead Free (Pb-Free - 10min. Cleaned)

Channel A 3.960723e+11

Average: 3.975760e+11
Maximum: 1.196661e+12
Minimum: 3.809871e+11
Measurement Count: 807
Retried Measurements: 0

Channel B 6.497286e+11

Average: 7.469355e+11
Maximum: 2.890685e+12
Minimum: 3.292765e+11
Measurement Count: 807
Retried Measurements: 0

Channel C 1.853922e+12

Average: 1.800121e+12
Maximum: 3.574763e+12
Minimum: 5.812313e+11
Measurement Count: 807
Retried Measurements: 0

Channel D 1.340847e+12

Average: 1.383770e+12
Maximum: 2.766489e+12
Minimum: 1.259597e+11
Measurement Count: 807
Retried Measurements: 0

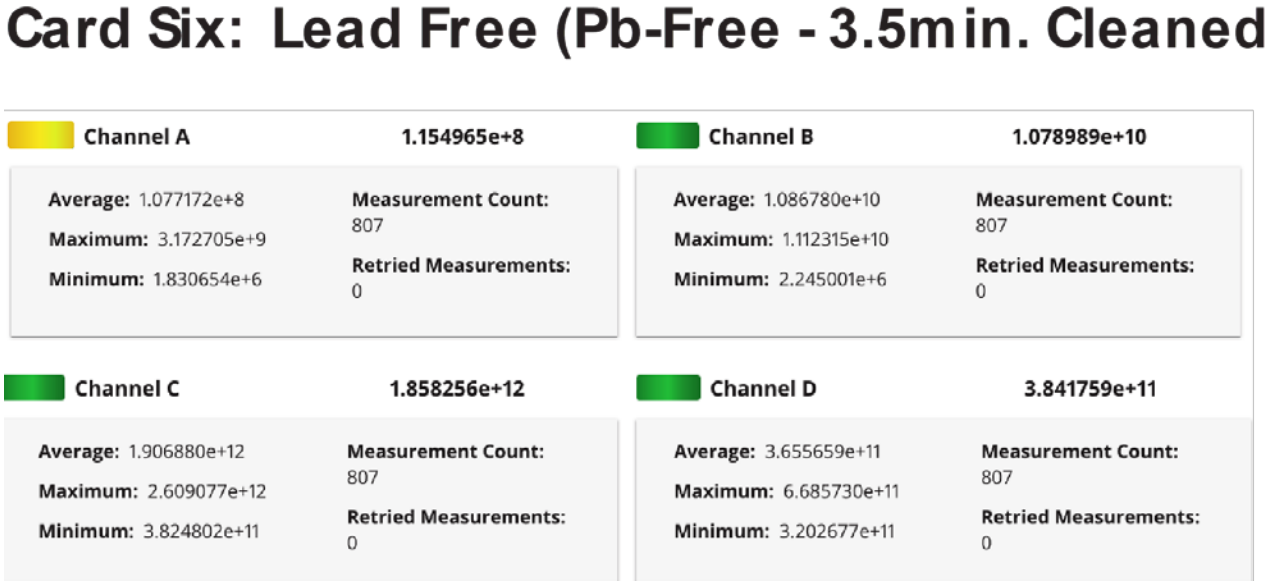


Figure 22: Pb-Free Solder Paste #2 Chart and Card Stats

The chart in Figure 23 compares Card 1 (SP#1) SnPb not cleaned to Card 4 (SP#2) Pb-free not cleaned SIR values. The data suggest that Card 4 Pb-Free solder paste has a more benign residue than does the Card 1 SnPb solder paste.

Cards 1 and 4: SnPb and Pb-Free Not Cleaned Board Comparison

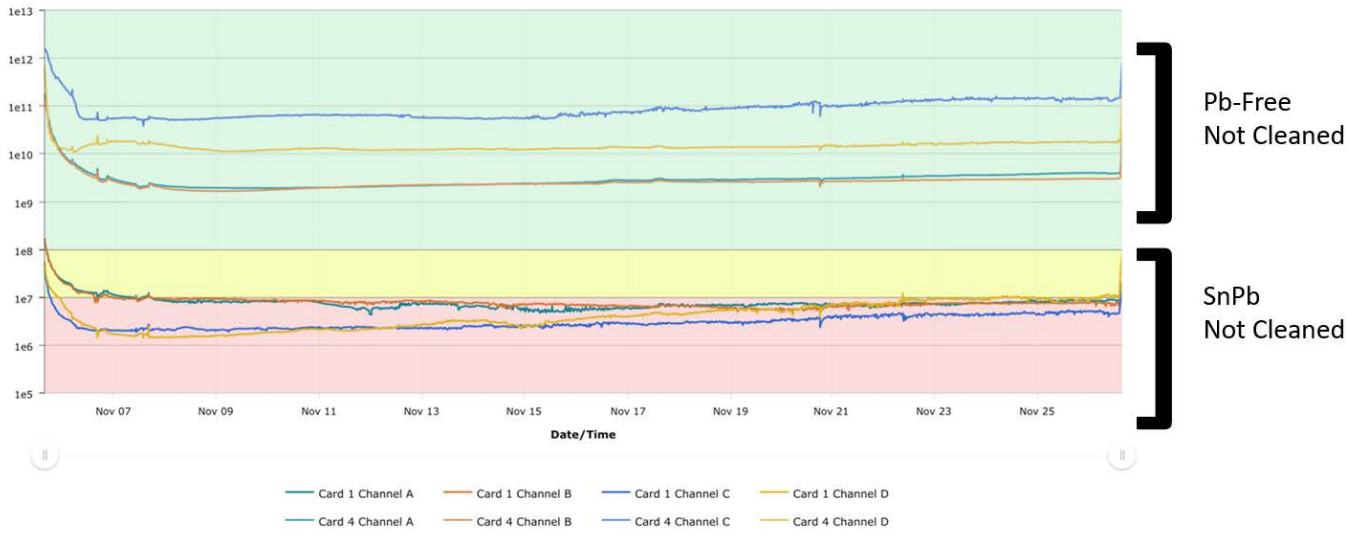


Figure 23: Not Cleaned Pb-Free (Top) compared to Tin-Lead (bottom)

The SIR values for Card 2 SnPb (SP #1) and Card 5 (SP #2), boards exposed to 10 minutes of wash time, exhibited good SIR values. It is worth noting that Quadrant 3, the No-Solder Mask condition was less stable than the other solder mask conditions on the test board.

Cards 2 & 5: SnPb and Pb-Free Comparison at 10 minutes Wash Time

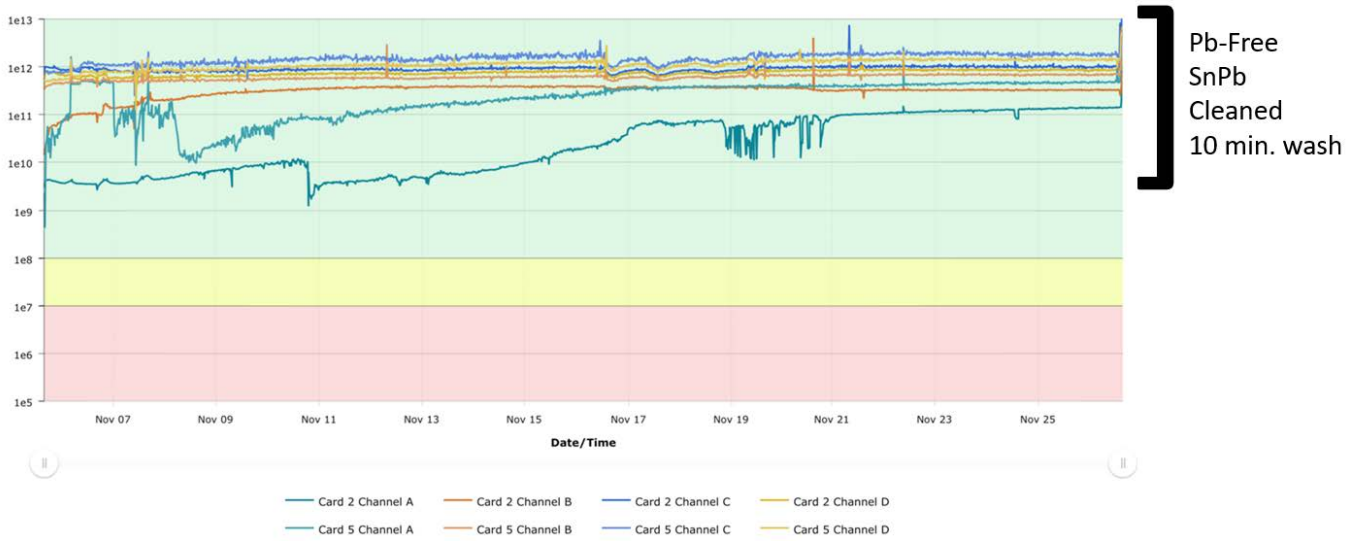


Figure 24: Comparison of the Tin-Lead and Pb-Free Cleaned Boards

The SIR values for Card 3 SnPb (SP #1) and Card 6 (SP #2) Pb-Free, boards exposed to 3.5 minutes were significantly different for the two solder pastes. The data suggest that the Pb-Free solder paste was less active and easier to clean. The movement in the readings indicates that some residue remains under the component. This partially cleaned condition indicates that longer wash time exposure is needed.

Cards 3 and 6: SnPb and Pb-Free Comparison at 3.5 minutes Wash Time

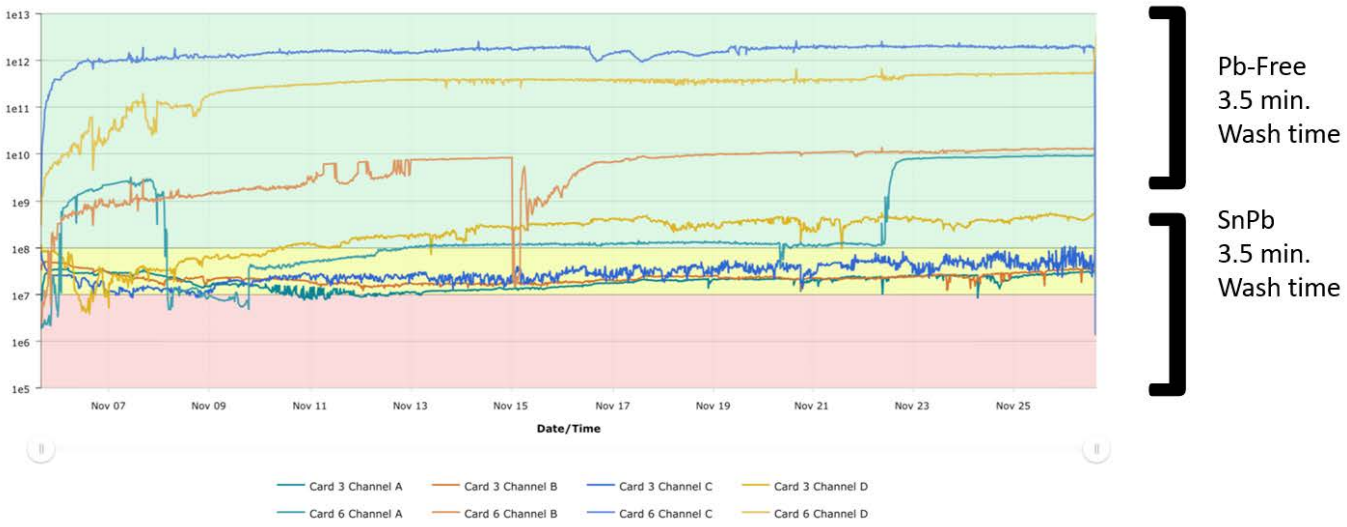


Figure 25: Comparison of the Tin-Lead (bottom) and Pb-Free (top) Partially Cleaned Boards

Inferences from the Data Findings

SIR testing is useful at discerning cleanliness levels under bottom terminated components. The test method can be applied to more challenging component geometries (e.g., BTCs) to understand better the impact of residues left under the bottom termination and the effects of cleaning. The SIR method is also effective at comparing solder pastes, reflow conditions, cleaning agents, and cleaning machines. As found in this study, longer wash exposure times were needed to remove active residues.

The value of SIR testing has been used for years to help understand cleanliness issues as they relate to material choices and process parameters. The tool is commonly used for process development, verification and validation of assembly processes. The changes in the IPC-J-STD-001G, Amendment 1 cleanliness requirements, increased the need for better cleanliness test

methods at the assembly site to capture objective evidence that one understands their material choices and process parameters as they interrelate to the final assemblies overall cleanliness. The ability to test inside the production facility allow for process engineers to gain direct feedback of their choices in materials as well as seeing how their process parameters impact their final cleanliness state. SIR testing at the facility allows for the hands-on engineers to see how their decision impacts the product they build directly as it relates to cleanliness. The SIR instrument design from the research grant along with test board developments with the more challenging components used on today's production hardware is a step in the right direction.

Follow On Research

Follow on research is underway to evaluate a series of test boards designed to build on this data and to take assembly testing to the next level and address such challenging components. The goal of these test additional test boards is to establish correlations back to the existing process knowledge base on the IPC-B-52 test board. One of the goals of the subsequent testing is to develop pass-fail criteria suitable for these test boards, related to the pass-fail criteria of the B-52 test board and IPC-9202.

The B-52 Legacy I and II test cards, shown in Figure 26, contains the NSMD Quad Flat Pack No Lead (QFN44) patterns and components from the Phase 1 testing to maintain the data linkage from the developmental work. Quadrant 2 (upper left) contains a variation on the IPC-B-52 ball grid array (BGA) test pattern. The Legacy I Quadrant 3 (top right) includes the IPC-B-52 QFP80 test pattern, tying together the lead-to-lead test pattern and the underlying comb pattern into a single SIR test pattern. The Legacy II Quadrant 3 (upper right) contains the IPC-B-52 QFP 80 test pattern, separating the lead-to-lead test pattern and underlying comb pattern into a dual-net SIR test patterns. The Legacy I Quadrant 4 (lower right) contains the IPC-B-52 QFP160 test pattern, tying together the lead-to-lead test pattern and the underlying comb pattern into a single SIR test pattern. The Legacy II Quadrant 4 (lower right) contains the IPC-B-52 QFP 160 test pattern, separating the lead-to-lead test pattern and underlying comb pattern into a dual-net SIR test patterns. Each quadrant has routed grooves to facilitate removal for supplemental testing, such as ion chromatography (IC) analysis. Of these test patterns, the QFNs are considered the most challenging component and the overall assumption was that if you could reliably clean under a QFN, you could clean under less challenging components as well.

B-52 Legacy I **B-52 Legacy II**

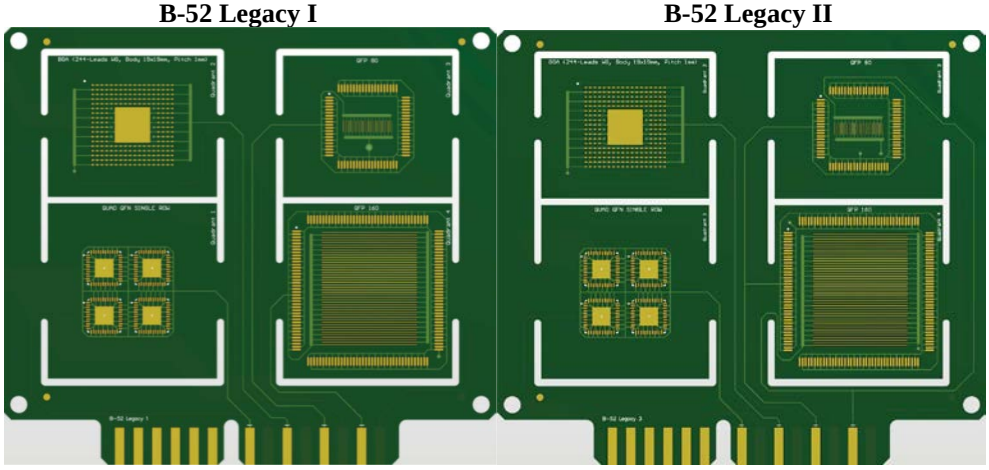


Figure26: B-52 Legacy I and II Test Board Design

The B-52 Legacy III card, shown in Figure 27, is the same as the Legacy I card, with the exception that a capacitor network, designed similarly to the B-52 capacitor networks, replaces the QFP80 test pattern. The QFP160 patternis located on the top right quadrant.

B-52 Legacy III

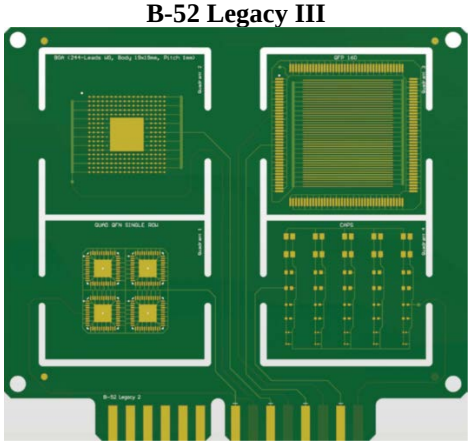


Figure 27: B-52 Legacy III Test Board Design

The B-52 Legacy IV test board has both the single row and dual row QFNs. The board has jumper pins to tie ground lugs to each other and signal pins around the parameter. The ground lugs are negative,andsignal pins are positive. If there is a short during testing, the board has a jumper system that allows you to discern whether the problem is coming from the single row or dual row. The capacitor nets are designed for the 0805, 0603, 0402 or 0201 components. The jumpers are designed to tell you whether or not you have a problem with any grouping. If there is a failure, you can jumper one group at a time to find the short. The SMD and Thru-hole allow for measuring in the X or Y position. This allows a user to determine whether the problem occurs vertically across components or horizontal side to side.

B-52 Legacy IV

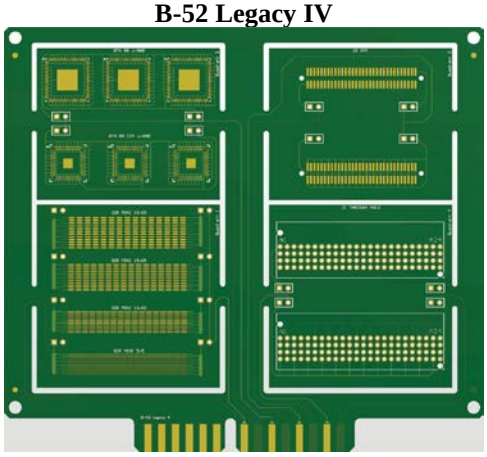


Figure 28: B-52 Legacy IV Test Board Design

The B-52 Legacy V test board is designed for testing BGA and LGA components. Quadrant 1 (lower left) BGA contains 256 IO, 17x17 mm, and 1 mm pitch. Quadrant 2 (upper left) BGA contains 572 IO, 25x25 mm, and 1 mm pitch. Quadrant 3 (top right) BGA contains 1020 IO, 33x33 mm, and 1 mm pitch. Quadrant 4 (lower right) contains 1832 IO, 46x46 mm, and 1 mm pitch.

B-52 Legacy V

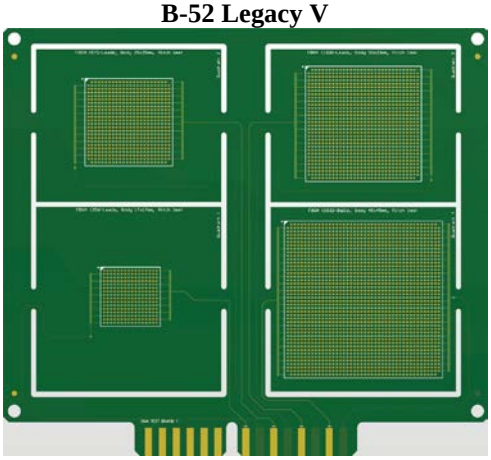


Figure 29: B-52 Legacy V BGA Test Board Design

The B-52 Legacy VItest boardis designed to evaluate the reliability of a mixed technology PCB process. This test board design focuses on rework and selective soldering. The test board contains a connector soldered with SMT on the top side and Thru-hole pins on the back side. Chip caps are placed exterior to the connector. The board has four quadrants. Quadrants 1 and 3 SIR electrical traces are patterned to measure resistance at the SMT and through-hole sites on the connector body. Quadrants 2 and 4 SIR traces are patterned to measure surface resistance at the SMT capacitive components.

B-52 Legacy VI

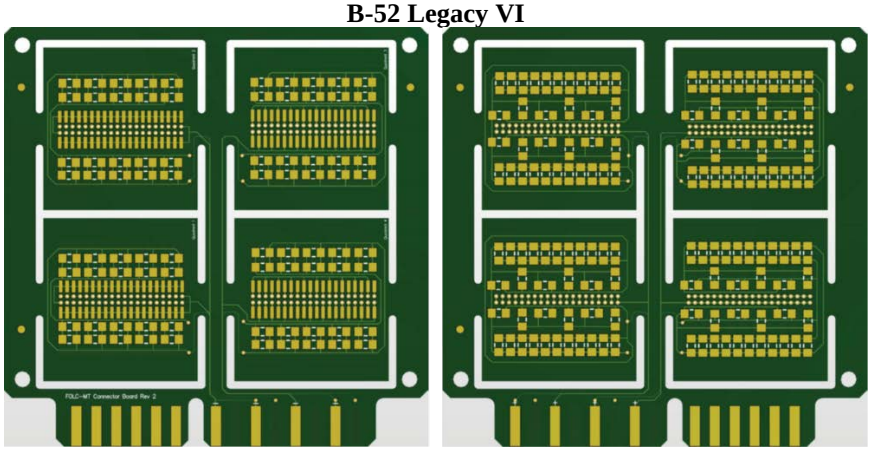


Figure 30: B-52 Legacy VI Connector Board Design

The B-52 Legacy VII test board is designed with known resistors. This test board is used to validate that the instrument readings are accurate. Quadrant 1 (lower left) uses the 1e9 Log Ohm resistor. Quadrant 2 (upper left) uses the 1e8 Log Ohm resistor. Quadrant 3 (top right) uses the 1e7 Log Ohm resistor. Quadrant 4 (lower right) uses the 1e6 Log Ohm resistor.

B-52 Legacy VII

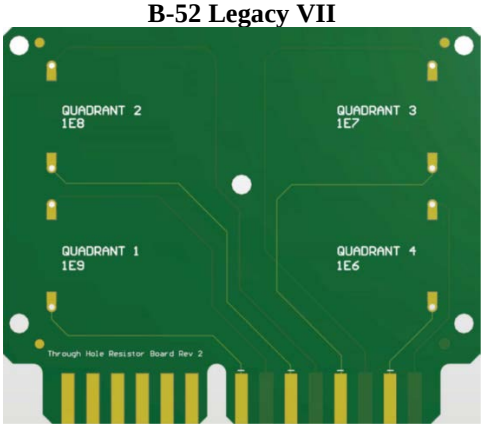


Figure 31: B-52 Legacy VIII Test Board Design

Conclusions

A qualified manufacturing process requires assemblers to qualify solderingand cleaning processes that result in acceptable levels of flux and other residues. This paper reported research on both test boards and instrumentation for use at the assembly site. The instrument and test board combinations are tools that process engineers and line personnel can use to develop objective evidence as it relates to the cleanliness of production hardware.

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